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Soft Error Rate Estimations of the Kintex-7 FPGA within the ATAS Liquid Argon Calorimeter

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There is great interest in using Field Programmable Gate Arrays (FPGAs) within high-energy physics experiments due to their reconfigurability, ease of use, and support for high-speed serial I/O. SRAM-based FPGAs, however, are susceptible to radiation induced single event upsets. This paper estimates the soft-error upset rate of the Kintex-7 FPGA within the ATLAS Liquid Argon Calorimeter environment. Radiation experiments were performed on this device at the Los Alamos Neutron Science Center and the H4 beam line at CERN. Results from these experiments suggest that while single event upsets are present, they can be addressed with appropriate SEU mitigation techniques.

Summary

Field Programmable Gate Arrays (FPGAs) are an attractive alternative to application specific integrated circuits (ASICs) because of their in-field reprogrammability, low non-recurring engineering costs (NRE), and relatively short design cycle. They provide high logic density, access to the latest I/O standards, and can be designed with a variety of low-cost tools. FPGAs are increasingly used in non-traditional applications such as harsh environments and in safety critical systems. In particular, FPGAs are increasingly being used within high radiation environments such as spacecraft and high-energy physics experiments.

There is interest in exploiting the use of reprogrammable FPGAs within the ATLAS Liquid Argon Calorimeter (LAr). FPGAs are considered for data collection, simple processing, and communication functions. This environment, however, contains significant high energy hadrons that will upset the configuration memory, user memory, and block memory of the FPGA. This work evaluates the suitability of using the Xilinx Kintex-7 family of FPGAs within this environment by first, measuring its sensitivity to high energy hadrons with two radiation tests, and second, estimating the configuration upset rate within the ATLAS LAr environment.

The FPGA chosen for this work was the Xilinx Kintex-7 FFG900. This device was tested in a neutron beam at the Los Alamos Neutron Science Center in Los Alamos, New Mexico, USA, as well as in the H4 beam line within the North area of CERN in France. The purpose of these tests was to estimate the static upset cross section of the FPGA configuration memory and the internal block memory. To accomplish this, a simple design was created that uses all of the available block memory (BRAM) in the FPGA and limited control logic. The contents of the configuration memory and BRAM memory were periodically read and compared with the golden copy to identify upsets. After reading this memory, the contents are scrubbed and the procedure is repeated. The sensitive cross section was be calculated by dividing the total upsets for each region by the total particle count that struck the FPGA per configuration bit. The same design and procedure were followed at LANSCE and H4.

The results from the LANSCE test suggest sensitive cross section of 7.49E-15 n/cmˆ2 for the configuration memory and 6.69E-15 for the BRAM memory. The results from the H4 test suggest a sensitive cross section of 1.51E-14 HEH/cmˆ2 for configuration memory and 1.45E-14 HEH/cmˆ2 for the BRAM memory.

The radiation environment of the ATLAS LAr environment has been modeled and simulations suggest that this environment will receive 3.1E10 high energy hadrons per year. Multiplying the total particles by our cross section results and the number of configuration bits gives 41924 upsets per year. This suggests a mean time between upsets of 12.5 minutes per device. Although the upset will occur relatively frequently, this upset rate is much larger than the scrubbing rate of these devices (less than a second). This result suggests that with

appropriate mitigation and scrubbing, the Kintex-7 could be deployed within this environment. Future work will investigate configuration scrubbing architectures.

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