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Simulation of the ATLAS sTGC trigger for the Phase-I new small wheel detector upgrade

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A Verilog Behavioral simulation of sTGC trigger will be presented based on the current baseline concept with particular focus on the Level 1 latency obtained. Data for this trigger is taken from detector simulations with Garfield and PSpice, current measurements made in the existing small wheel, and FLUGG simulation of the arrival times of hits at high luminosities. These simulations will become the HDL that is used to compile the ASIC in the 130nm IBM CMOS process. The CERN designed GBT serializer is to be included in the ASIC for transmission of the resulting trigger information to the rim of the nSW.

Summary

The primary trigger of the ATLAS New Small Wheel (NSW) is based on the sTGC detector. A behavioral Verilog simulation of the detector and on-chamber electronics has been developed and the results will be presented. The detector has been characterized with Garfield and Spice with detailed comparison to test beam data. This characterization of the detector has been coded in Verilog and extended to include the front-end ASD chip of the NSW, the VMM. This software is used as a test bench for stimulating the trigger processing circuitry, the trigger data serializer (TDS) chip. Both the VMM and the TDS chips are radiation tolerant ASICs. The TDS accepts both pad and strip data from the sTGC. Pad data is immediately sent to circuits on the rim of the NSW where track roads are formed. Strip data is captured by the TDS chip and stored awaiting confirmation from the track roads. Once confirmed, the strip data is serialized and send off-chamber. Data rates and particle arrival times are provided by a combination of existing muon data and FLUGG simulation. The algorithms and data flow through the TDS chip will be exhibited as well as the measured latency. The TDS output includes a Verilog simulation of the GBT serializer provided by the CERN microelectronics group

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