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Ultra-thin packaging technologies for CMOS pixel sensors: embedding in kapton foils

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Monolithic CMOS Pixels (MAPS) integrate on the same silicon substrate the radiation sensor element with the processing electronics.
Their thickness can be very small: typically less than 50 μm. This allows for very small material budget, if not spoiled by other mechanics elements. In order to demonstrate feasibility of large area, ultra-light sensor ladders (< 0.1% radiation length) based on MAPS, we develop novel packaging method. Thinned sensors are embedded in polymer (kapton) film, electrical connection to pads are implemented by aluminum deposition following by lithography steps (no wire bonding). Details of ladder design and electrical tests results are presented.

Summary

Monolithic CMOS Pixels (MAPS) integrate on the same silicon substrate the radiation sensor element with the processing electronics.
Their thickness can be very small: typically 20 μm for active silicon (sensor plus electronics) and less than 10 μm for interconnections (several metal-insulator layers). Therefor MAPS can be thinned down to less than 50 μm, without losing their tracking performance. This allows very small material budget and construction of non-planar (cylindrical) detector layers: thin silicon is quite flexible. In order to demonstrate feasibility of large area, ultra-light (< 0.1% radiation length) sensor ladders we develop novel packaging method. Thinned sensors (<50 microns) are embedded in polymer (kapton) film, electrical connection to pads are implemented by metal deposition (sputtering) and lithography steps (no wire bonding). The fabrication is based on slightly modified process (existing at CERN) for flexible multi-layer PCB fabrication, in which aluminum is used for all metal interconnections. For the demonstration of this new packaging method, medium size CMOS sensor (Mimosa 26, approximately 2x1 cm sq.) has been chosen. In the first iteration, a single-chip flex module has been fabricated and electrically tested. Two metal layers are used to provide connection down from the bonding pads on Mimosa 26 up to the micro-connector and few capacitors (standard SMD components) on top of the stack. Production of module with two chips and four metal layers (two reserved for power supply planes) is in progress and should be finished within few weeks. The final demonstrator module with six Mimosa 26 chips is planned soon after. The dimensions and the material budget of that demonstrator (12x1 cm sq.) are similar to that required by the inner layer of Vertex Detector for the International Linear Collider. We present details of ladder design adapted for large area coverage, followed by electrical tests results, thermal study consideration and minimum ionizing particle tracking performance. Possible improvements of the process will be also proposed.

Primary author: DULINSKI, Wojciech (Institut Pluridisciplinaire Hubert Curien (FR))

Co-authors: WINTER, Marc (Institut Pluridisciplinaire Hubert Curien (FR)); DE OLIVEIRA, Rui (CERN); FERRY, Serge (CERN); GOFFE, mathieu (IPHC CNRS)

Presenter: DULINSKI, Wojciech (Institut Pluridisciplinaire Hubert Curien (FR))

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