# QIE10
# A New Front-End Custom Integrated Circuit For High-Rate Experiments

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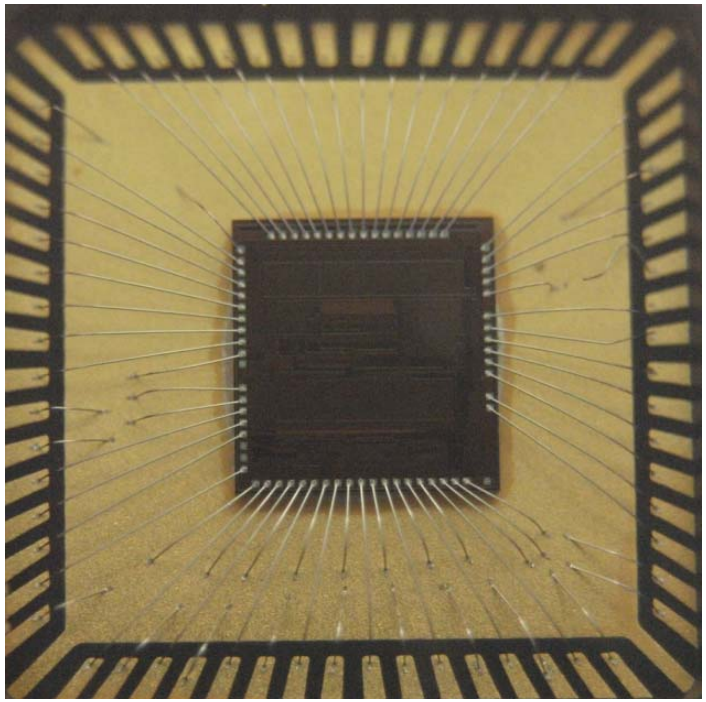
# Outline

- Overview of the QIE10
- Bench Measurements at Fermilab and Argonne
- Radiation Tolerance Measurements
- Outlook and Plans

# Overview of the QIE

- The QIE [Charge (Q) Integrator and Encoder] is a custom ASIC designed to digitize charge signals from photo-detectors
- The newest design (QIE10) features:
  - Dead-timeless operation @ 40 MHz, using 4-phase operation
  - High dynamic range (17 bits), with 6 bits of mantissa, 4 Ranges → 256 codes
  - Logarithmic response - ~1% measurement across dynamic range
  - 6 bit TDC (0.5 nS)
  - On-board Q-Inj
  - Low power: 320 mW
    - +5V @ 40 mA analog
    - +3.3V @ 35 mA digital
  - 350 nm SiGe (rad-hard)

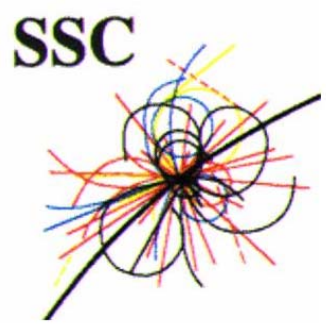


QIE10

# Overview of the QIE (Cont.)

- A short history of development:
  - 1989: Originally conceived by Bill Foster for **SDC @ SSC**
  - 1995: 1st fully-functional chip designed by Tom Zimmerman for the **KTeV experiment @ FNAL**
    - 2 μm Orbit "Bi-CMOS", 3000 ch.
  - 1996: Front-end for calorimeters of **CDF @ FNAL**
    - 2 μm Orbit "Bi-CMOS", 10,000 ch.
  - 2002: Front-end for **MINOS Near Detector @ FNAL**
    - 2 μm Orbit "Bi-CMOS", 10,000 ch.
  - 2003: Front-end for **CMS HCAL @ CERN**
    - 0.8 μm AMS BiCMOS, 10,000 ch.
  - 2013: Front-end for **CMS HCAL** upgrade, and a ***candidate*** for **ATLAS TileCAL** upgrade
    - 0.35 μm AMS SiGe, 17,000 ch. → 27,000 ch.

***Joint Development***



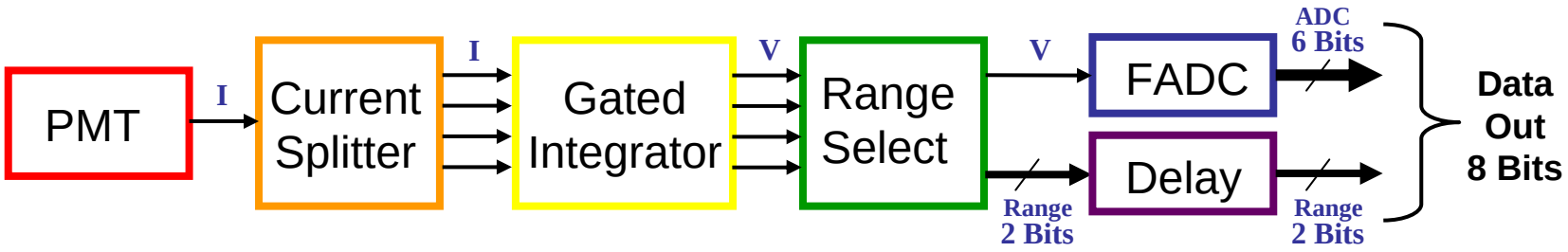





# Overview of the QIE (Cont.)

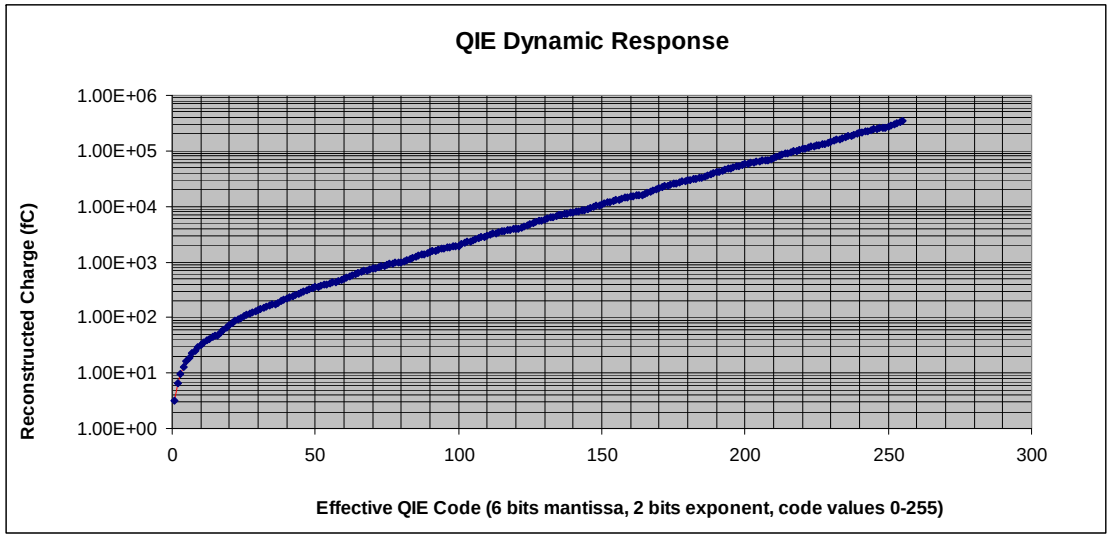
- How the chip works:
  - ✶ Receives charge (current) from PMT Anode
  - ✶ "Splits" current into four logarithmically-weighted ***Ranges***
  - ✶ Integrates current fractions onto separate capacitors using gated integrators
  - ✶ Selects (somehow…) one of the four Ranges to be digitized
  - ✶ Digitizes the analog voltage from the selected Range
    - 6-bit FADC with *exponential* response → *"Mantissa"*
  - ✶ Outputs 2-bit code for the Range digitized (0 - 3) → *"Exponent"*

⇨ ***Produces floating-point output codes***
⇨ ***Response is approximately logarithmic…***



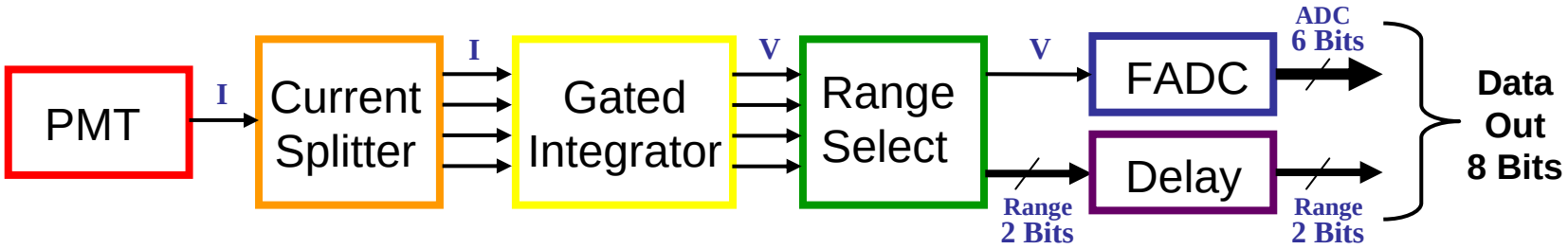
# Overview of the QIE (Cont.)

- How the chip works (Cont.):
  - Result of Logarithmic Current Splitting & Exponential ADC gives the following transfer function:




⇨ ***Dynamic response has 5 orders of magnitude, encoded into 8 bits***

⇨ ***The key to the operation is the "current splitter"…***



# Overview of the QIE (Cont.)

- QIE10 multi-ranging splitter/integrator concept:
  - 24 identical NPN transistors, arranged in 5 groups or ***Ranges***: 16, 4, 2, 1, 1
  - Each Integrator Range has an integrating capacitor, with ratios: 1, 2, 8, 32,

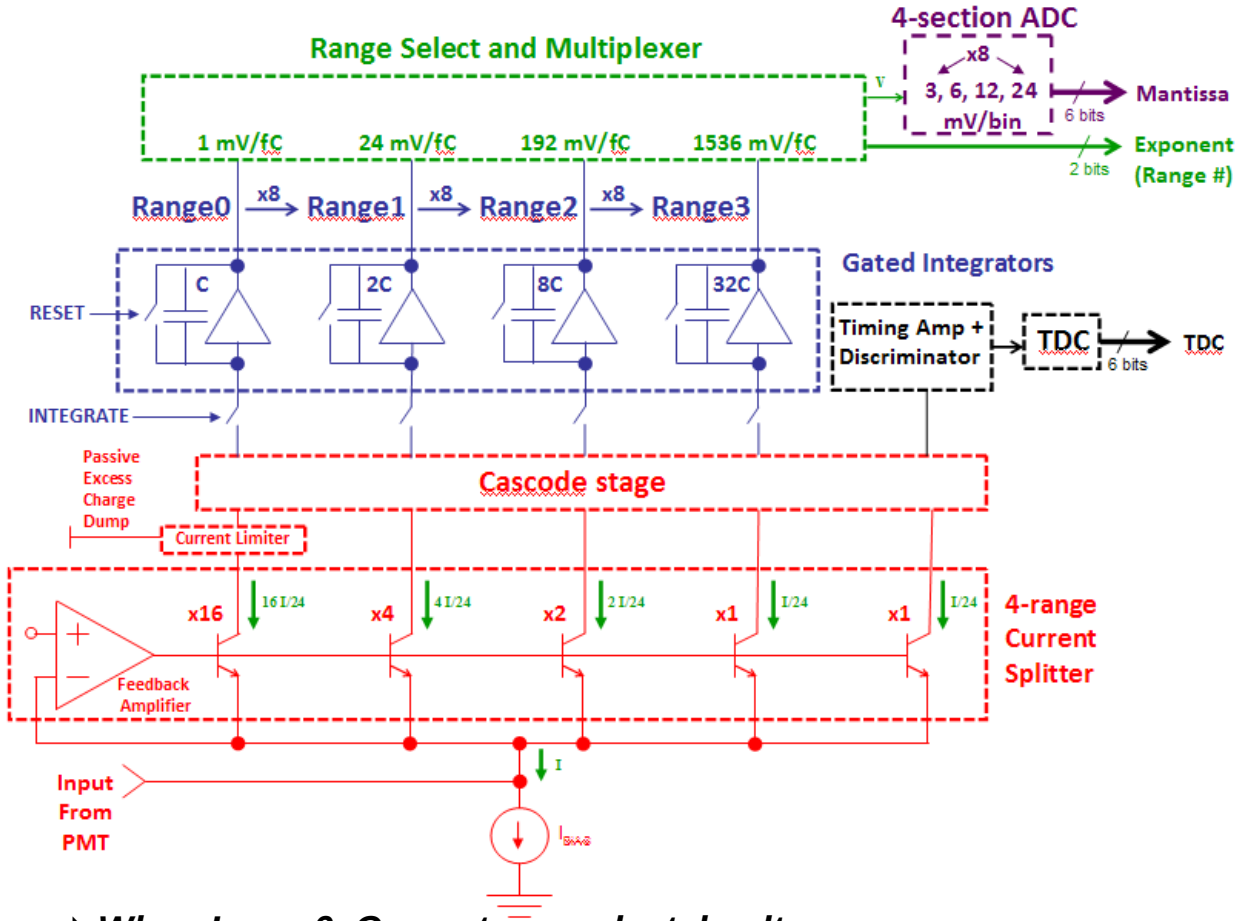
**1 Clock Cycle #1**

- Begin with capacitors **Reset**
- Current I splits onto each Range according to the grouping of the NPN transistors

**1 Clock Cycle #2**

- **Integrate** switches close for 1 clock period
- Split currents integrate on integrating capacitors
- At the end of the period, Integrate switches open
- Resulting voltages:

$$V_{Cap} = \frac{1}{C}\int_{0}^{25ns} I_{Range}\,dt$$




⇨ ***When $I_{PMT}$ = 0, Caps store pedestal voltages***

⇨ ***When $I_{PMT} \neq 0$, Caps store + fractions of $I_{PMT}$ charge***

# Overview of the QIE (Cont.)

- How the chip works (Cont.):
  - After Integration period, capacitor voltages sent to **Range Select** circuit

1 Clock Cycle #3

    - One and only one voltage will be within the valid input range of the ADC
  - Selected capacitor then **Digitized** by the Flash ADC

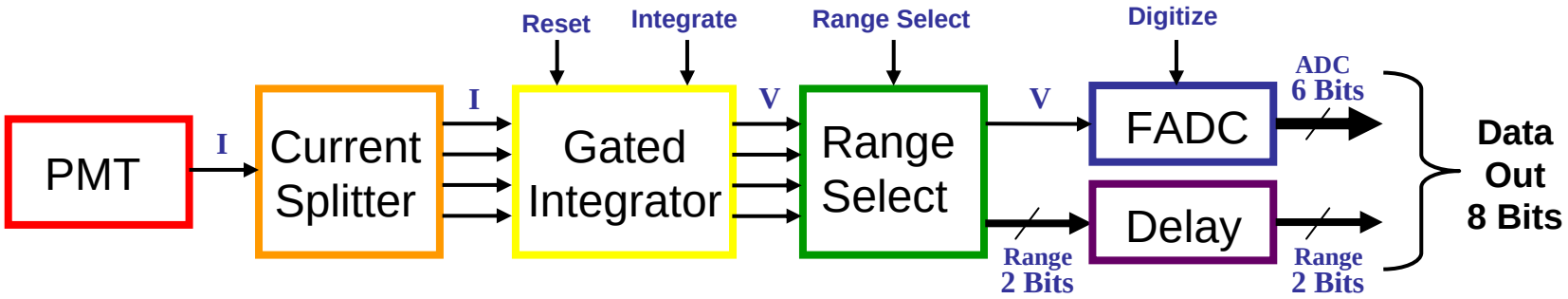
1 Clock Cycle #4

    - ADC codes are another aspect to the logarithmic response…
- 4 Phases of operation:

  1. Reset 2. Integrate 3. Range Select 4. Digitize

  - It takes 4 clock cycles to process a measurement from 1 integration period

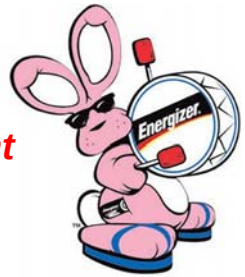
    ⇨ ***Why is the chip not dead 75% of the time?...***



# Overview of the QIE (Cont.)

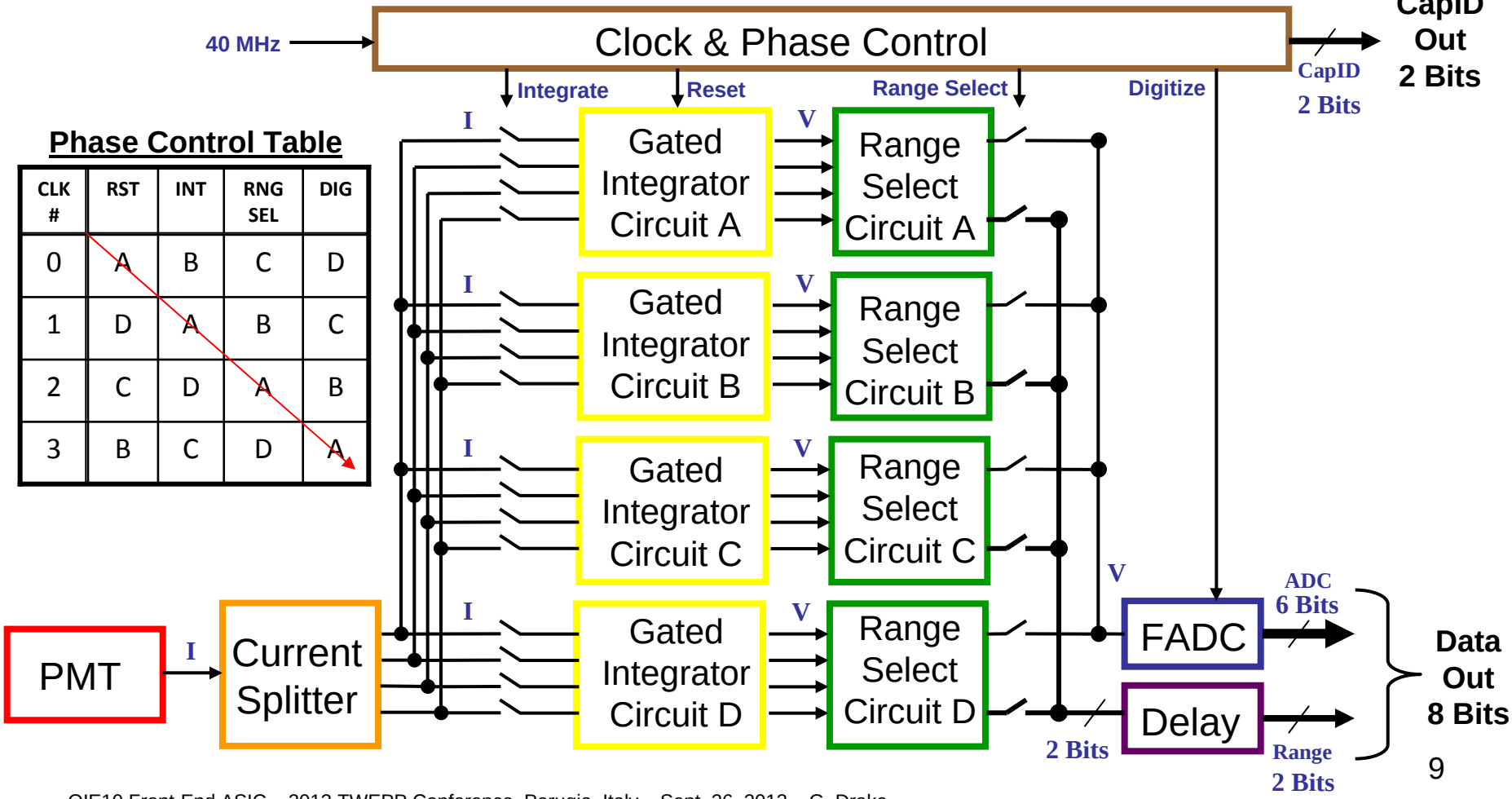
- How "Dead-timeless" is achieved:
  - Operates at 40 MHz
  - Operations are pipelined using 4-phase circuits
  - Data includes 2-bit ***CapID*** to indicate phase

⇨ ***Produces a code representing the current integrated in each and every 25 ns period and never stops***




**Phase Control Table**

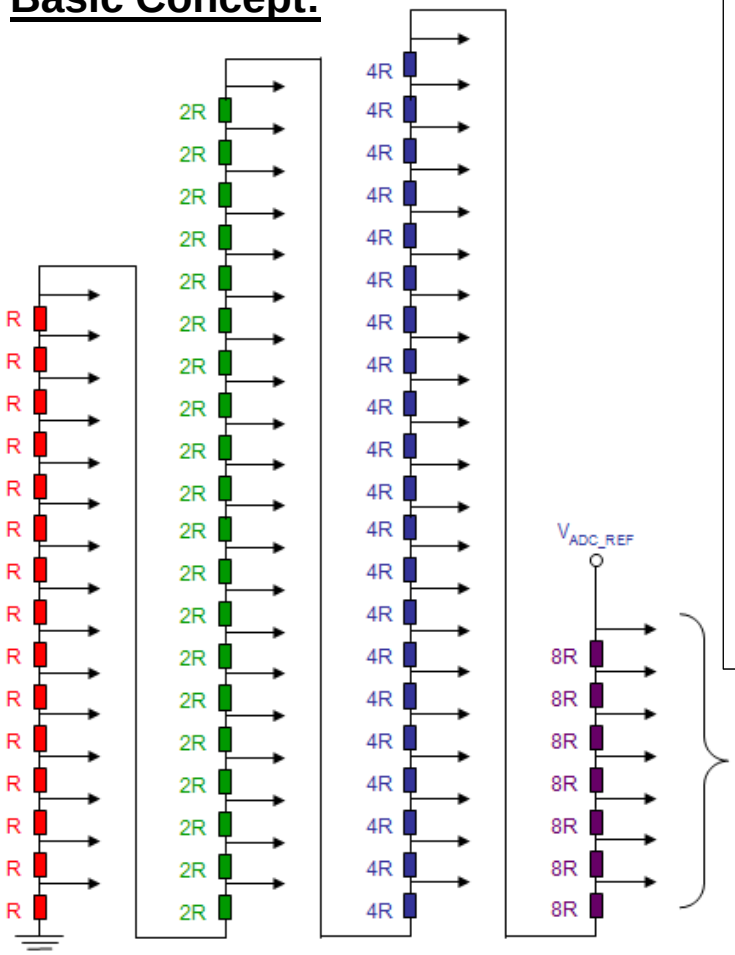
| CLK # | RST | INT | RNG SEL | DIG |
|---|---|---|---|---|
| 0 | A | B | C | D |
| 1 | D | A | B | C |
| 2 | C | D | A | B |
| 3 | B | C | D | A |



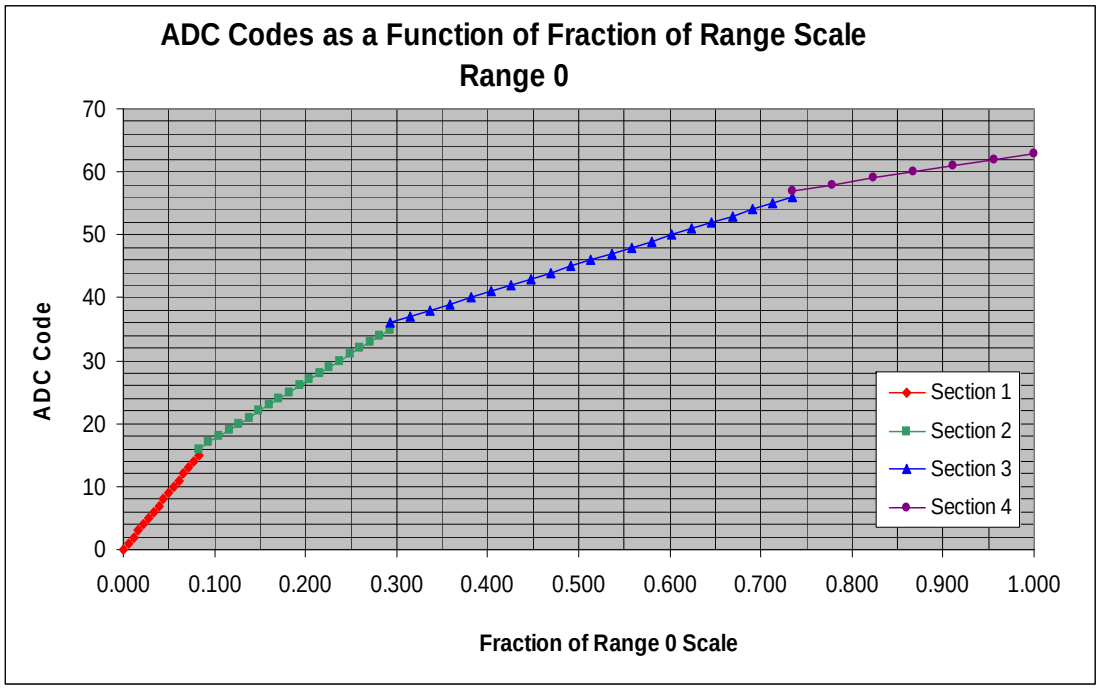
# Overview of the QIE (Cont.)

- Flash ADC Codes
  - Uses “non-linear” arrangement in the resistor divider chain
  - Resistor taps arranged to give approximate exponential response

**Basic Concept:**




Taps to FADC Comparators

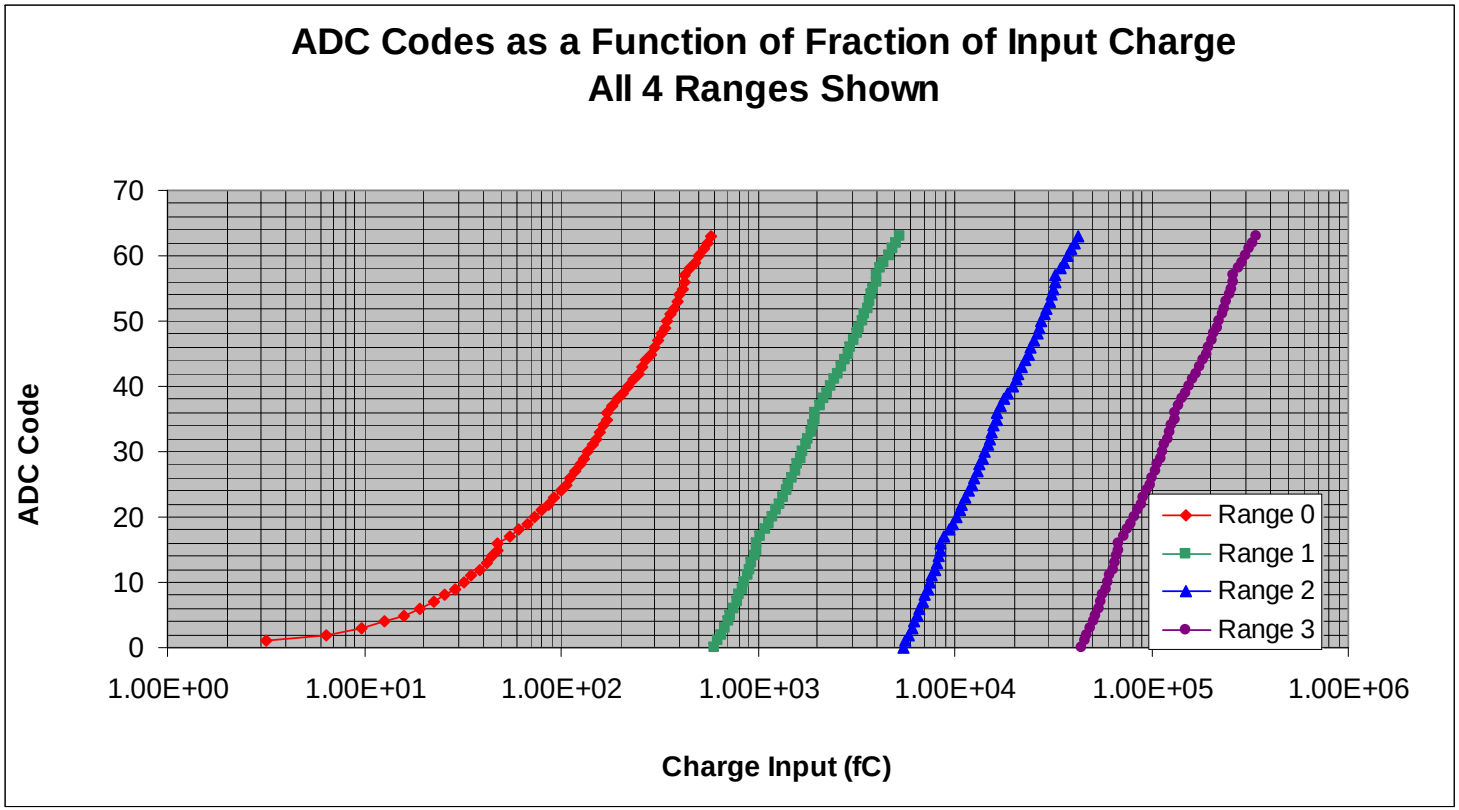



Ideal Response

***Note: Actual implementation is different…***
***See T. Zimmerman talk at 2013 IEEE-NSS for details***

# Overview of the QIE (Cont.)

- Full Response – Raw Data
  - Combination of current split weighting and FADC codes gives the following Transfer Function – Multi-range, floating point



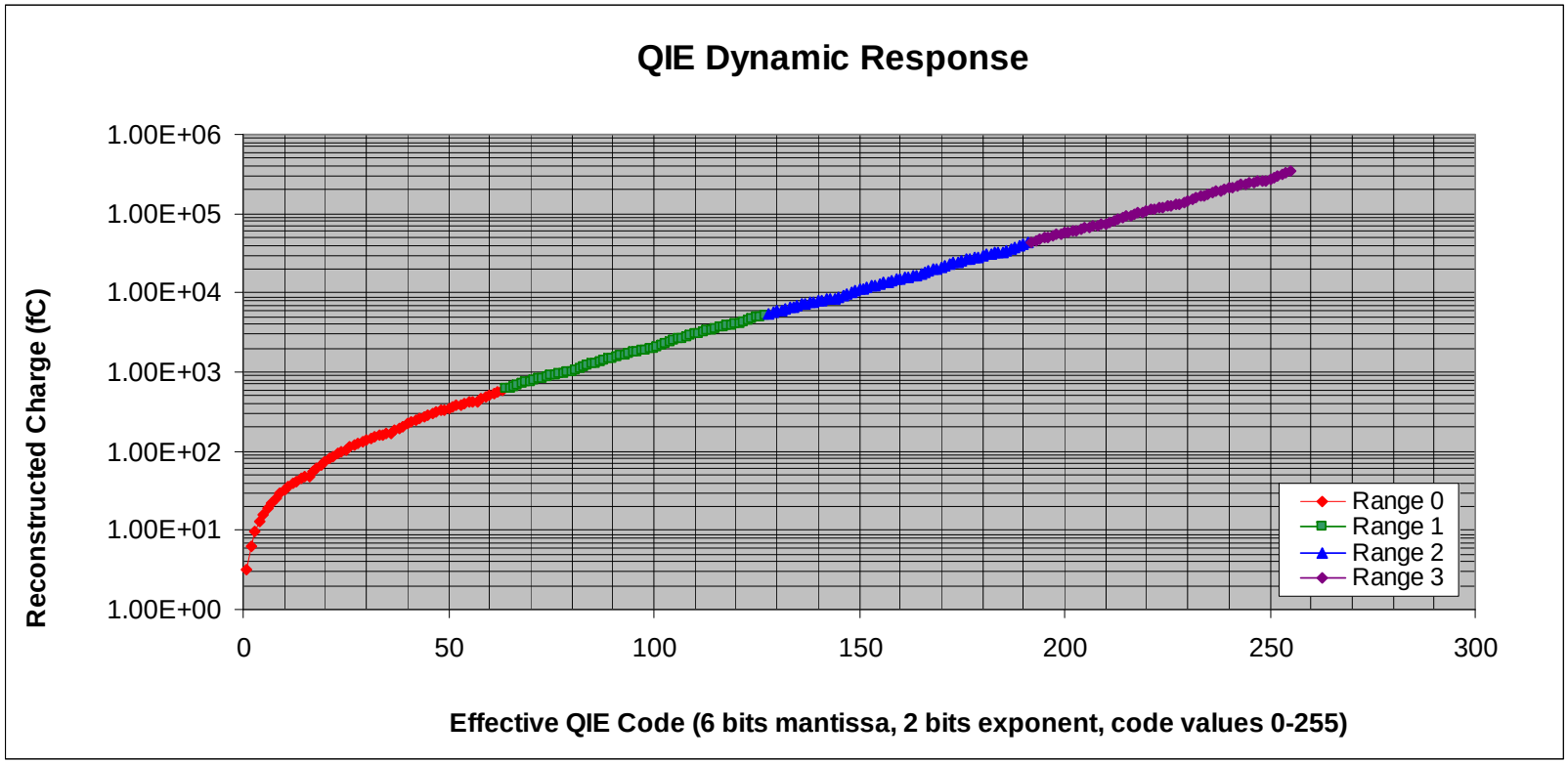

Raw Data:
6-bits ADC
2-bits Range
2-bits CapID
6-bits TDC
⇨***16 bits total***

Ideal Response – One set of CapIDs shown

# Overview of the QIE (Cont.)

- Reconstructed Response
  - Use Look-Up Tables in DAQ to “Linearize” QIE Data
  - Each code (ADC, Range, CapID) has an assigned charge value (or MeV)
    - CMS: Carry calibration constants from checkout to the experiment
    - ATLAS: Use in-situ calibration techniques

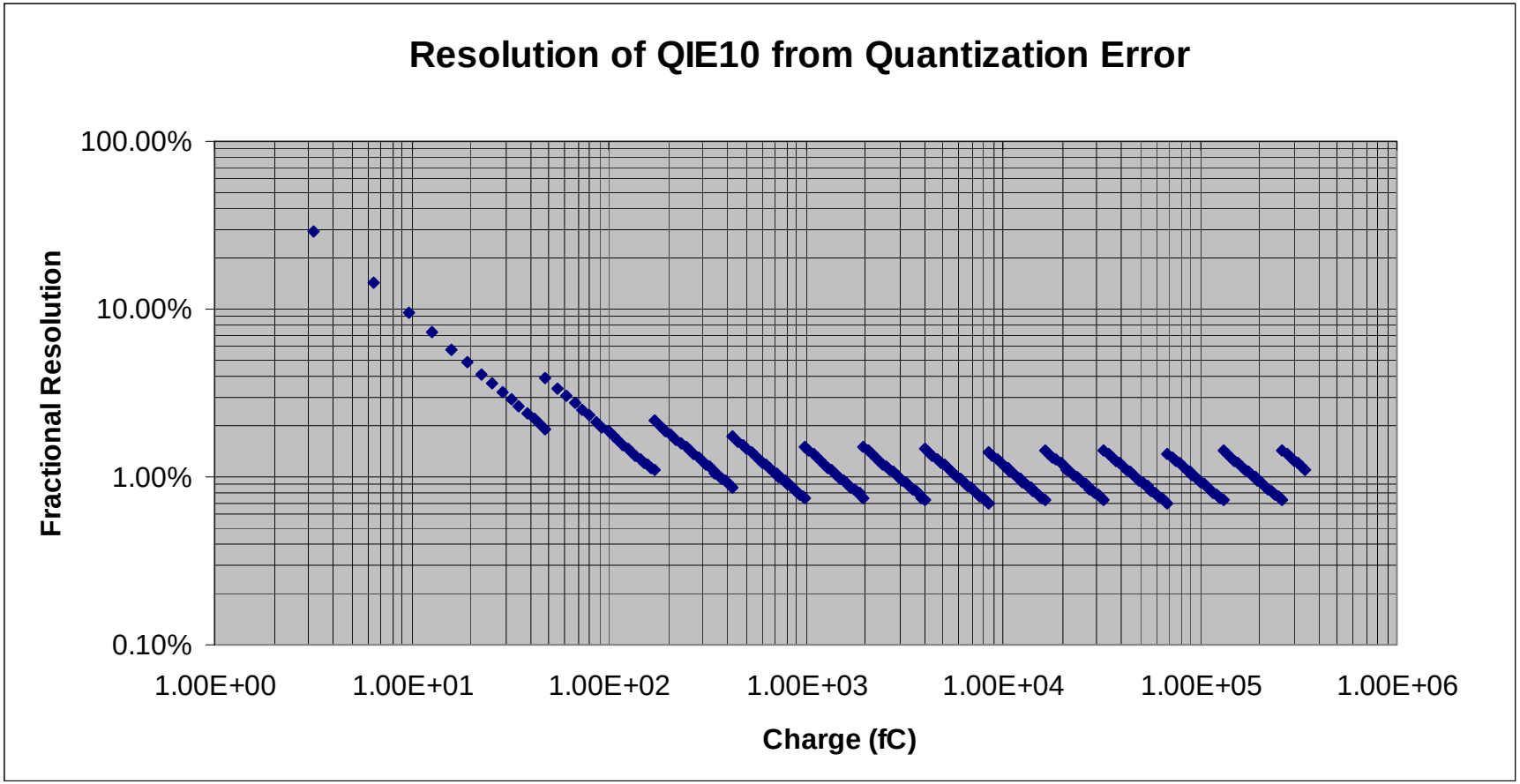
***1024 constants per chip***




Ideal Response – One set of CapIDs shown

# Overview of the QIE (Cont.)

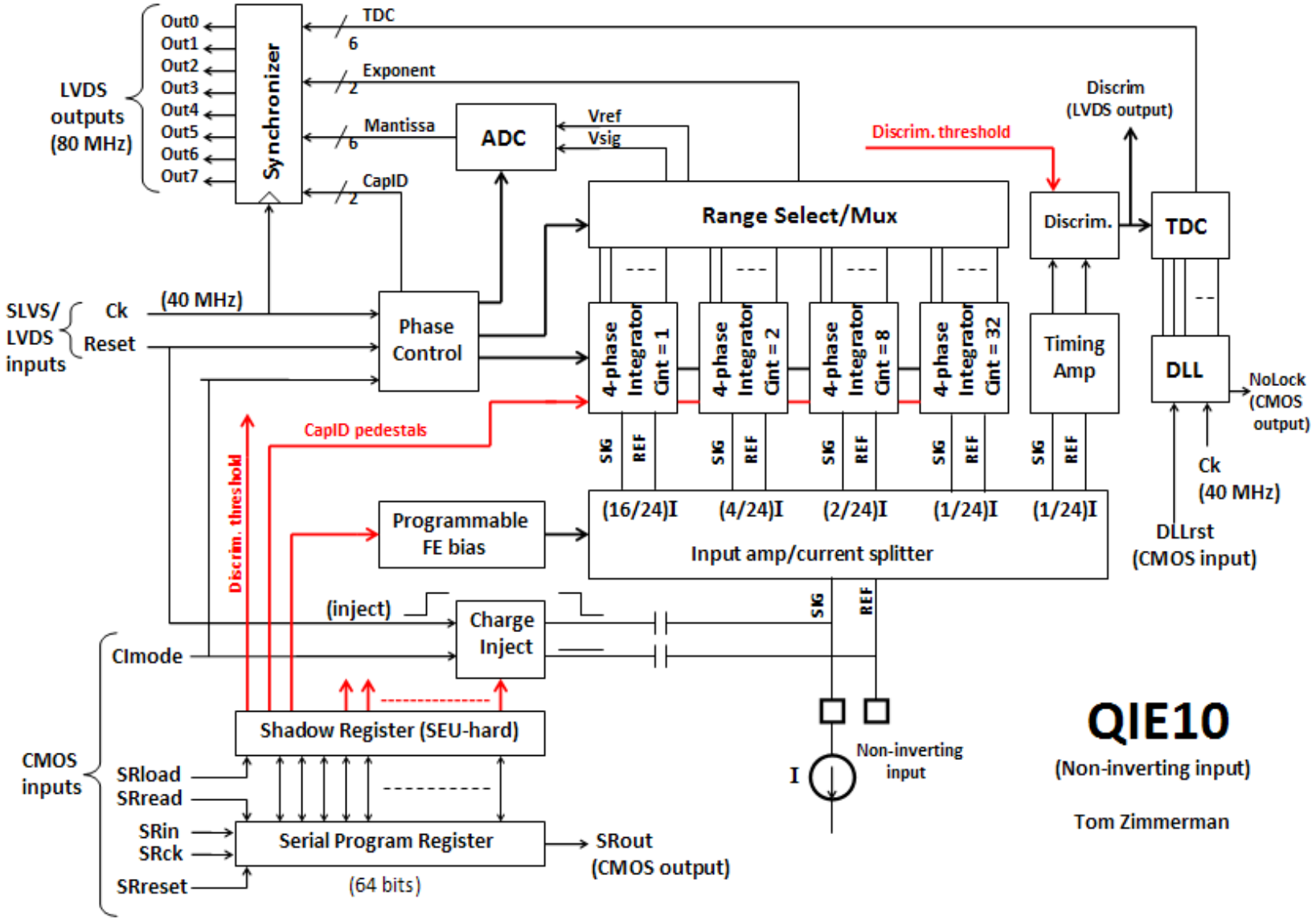
- Quantization Error & Resolution




Ideal Response

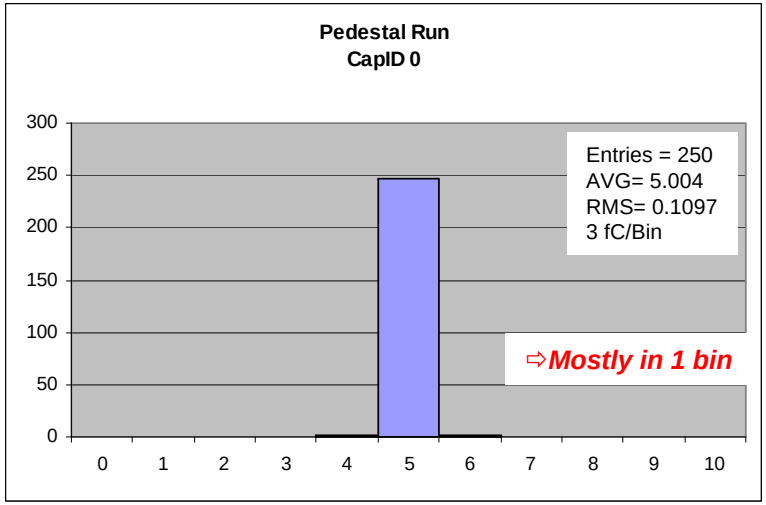
# Overview of the QIE (Cont.)

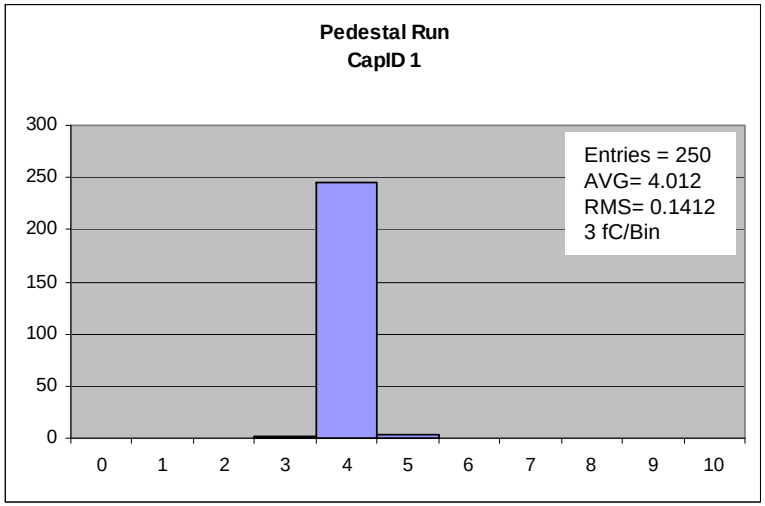
- Block diagram of the entire chip:

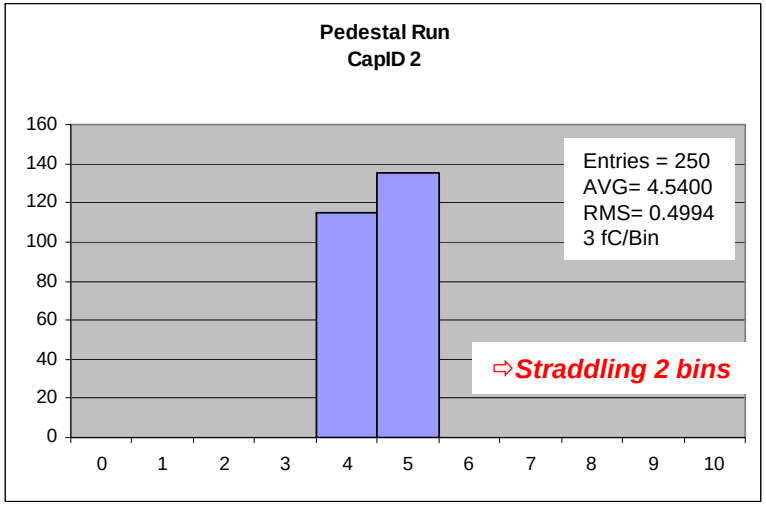


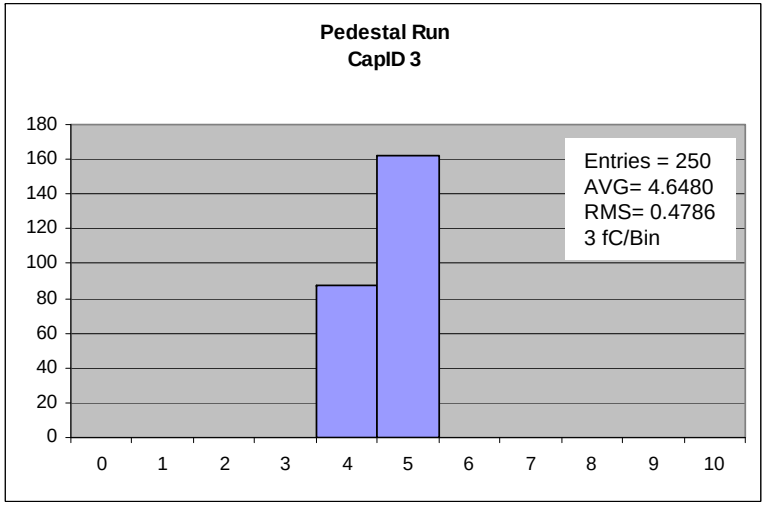
# Performance Studies

- Pedestal Measurement – 1000 Consecutive Clock Cycles, No Source Capacitance



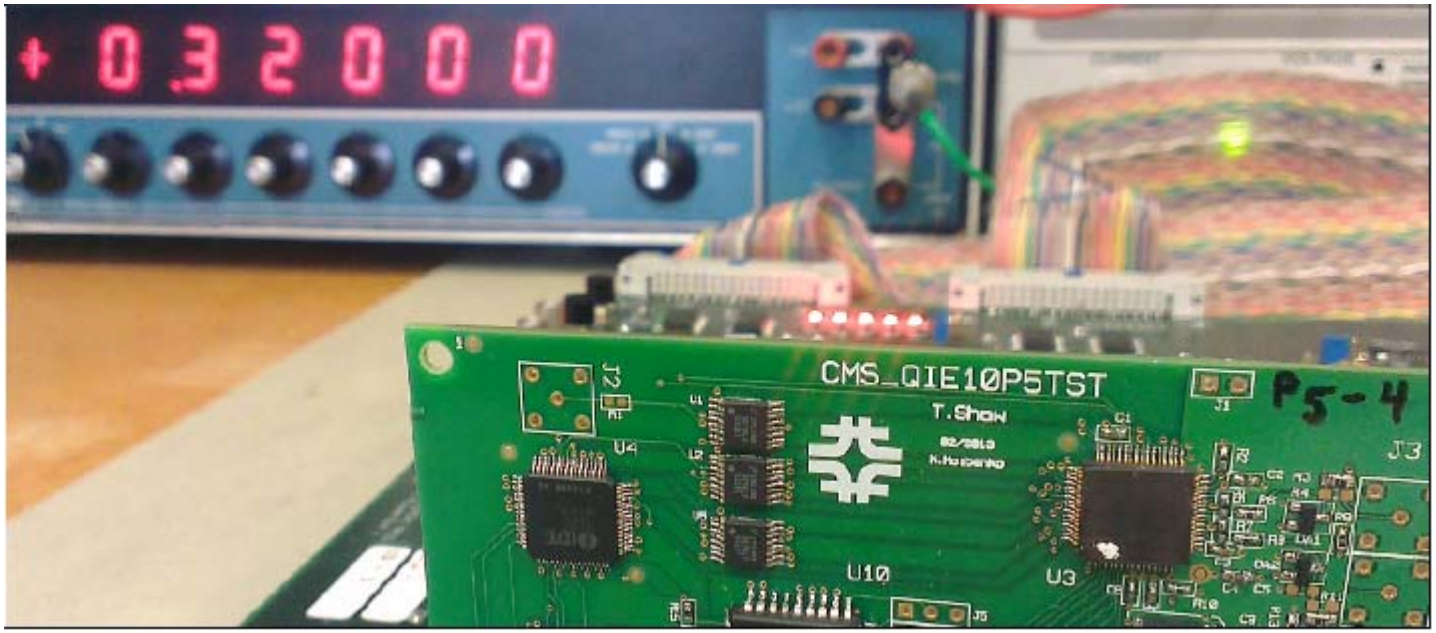




⇨ ***Exceptional noise performance - ~1.5 fC RMS!***

# Performance Studies (Cont.)

- DC Current Injection
  - Use a precision DC current injector to inject current into chip
  - Allows the study of:
    - Range gains
    - Bin widths
    - Range overlap

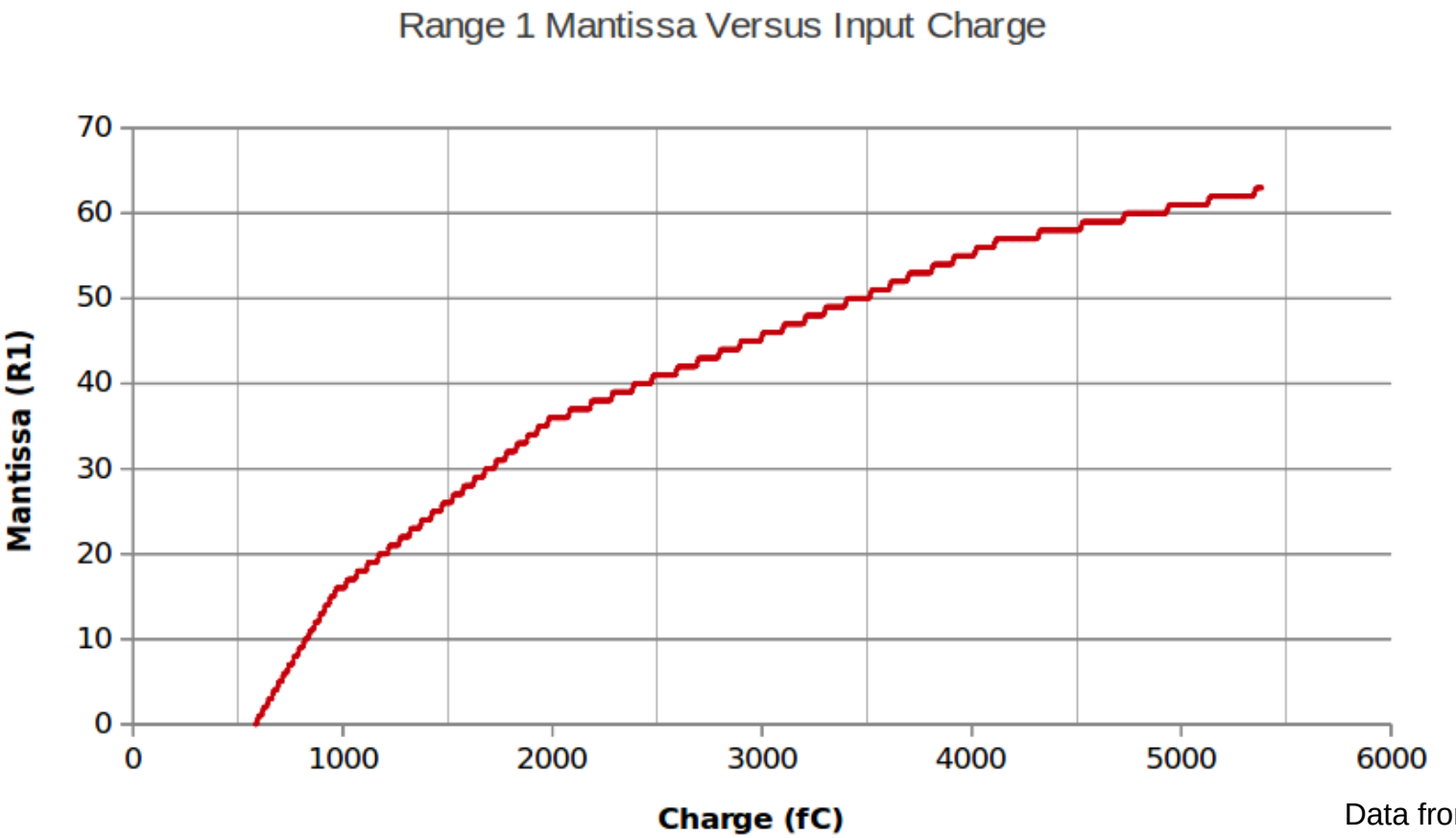
⇨ ***Use results to load Look-Up Tables to reconstruct charge from QIE codes***




Setup At Fermilab

# Performance Studies (Cont.)

- DC Current Injection (Cont.)
  - Response on a single range → Study ADC response

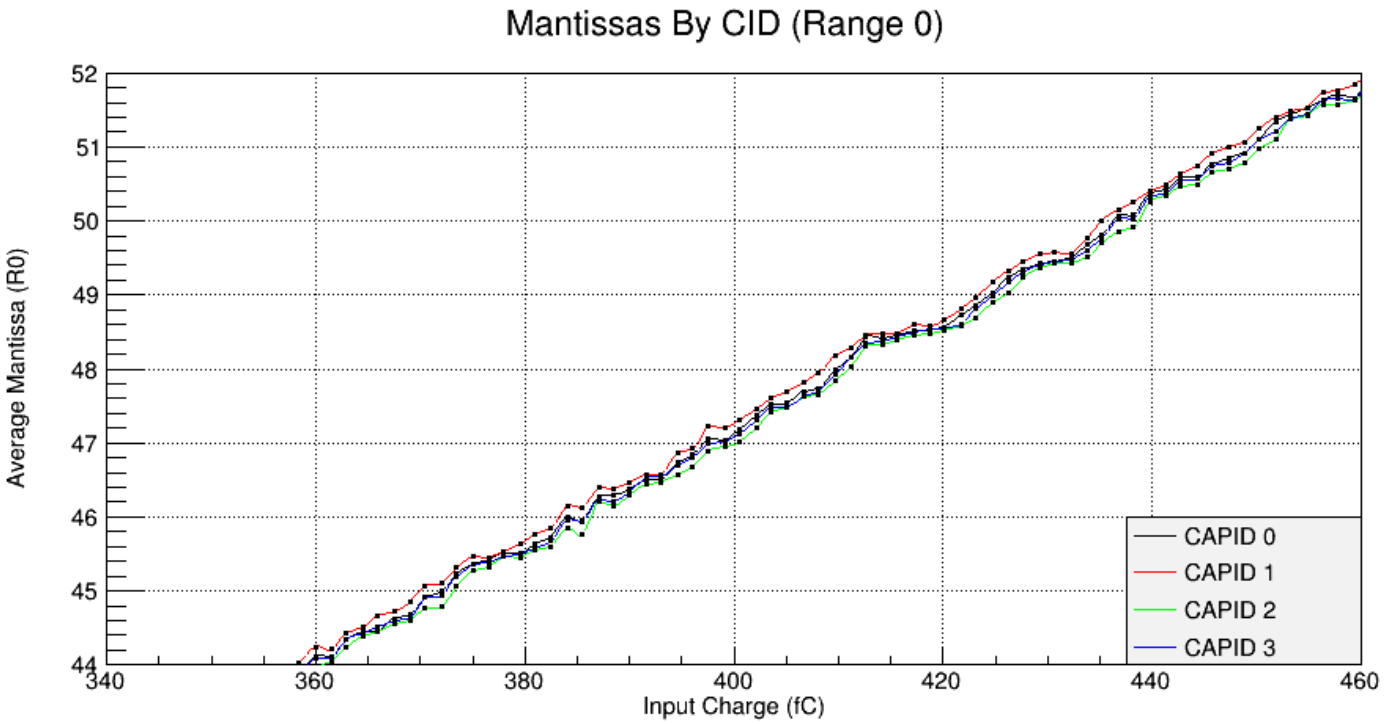



Data from Fermilab

⇨ ***Response as expected – See all 4 ADC sections***

# Performance Studies (Cont.)

- DC Current Injection (Cont.)
  - Look at uniformity across all 4 CapIDs
    - 100 events per point
    - One ADC section shown



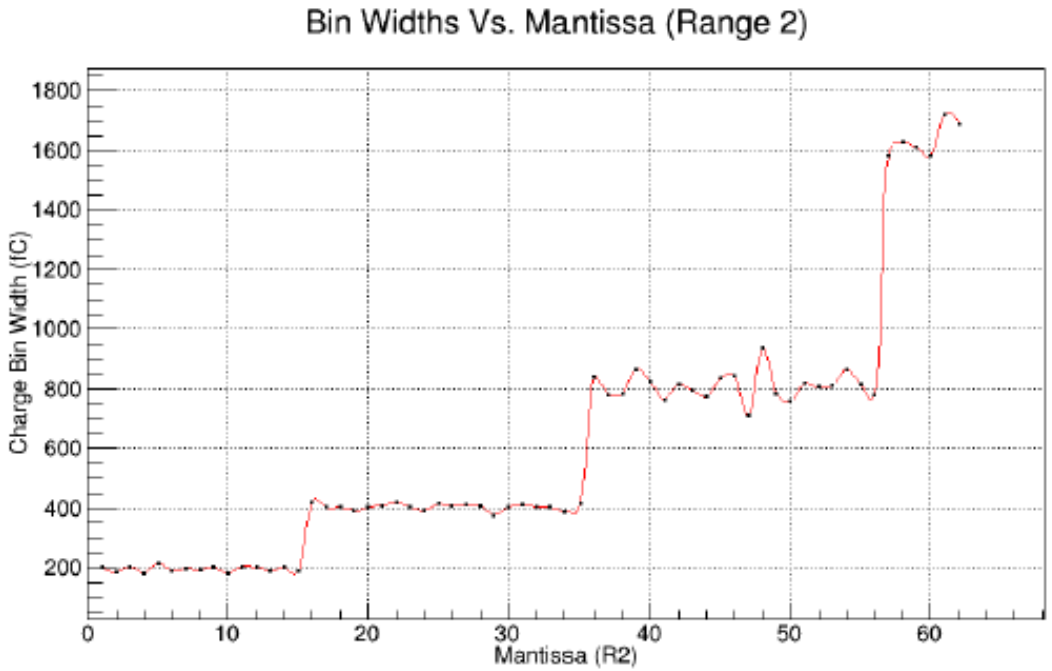

Data from Fermilab

⇨ ***Response as expected***

⇨***Note: Uses pedestal adjust feature to make pedestals uniform***

# Performance Studies (Cont.)

- DC Current Injection (Cont.)
  - Study of ADC bin widths




Data from Fermilab

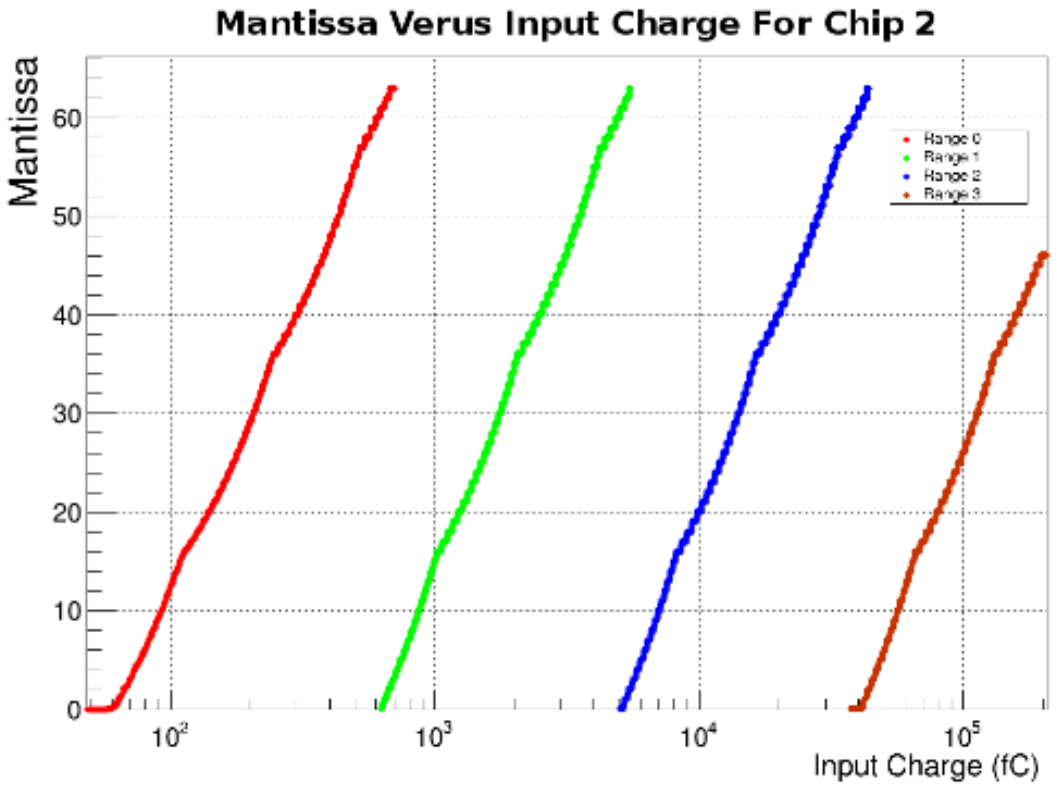
P5 widths, Range 2

⇨ ***See nice uniform bin widths***

⇨ ***Bin width variation minimized in bottom 2 sections by design***

# Performance Studies (Cont.)

- DC Current Injection (Cont.)
  - Raw data for one capacitor bank over full input range

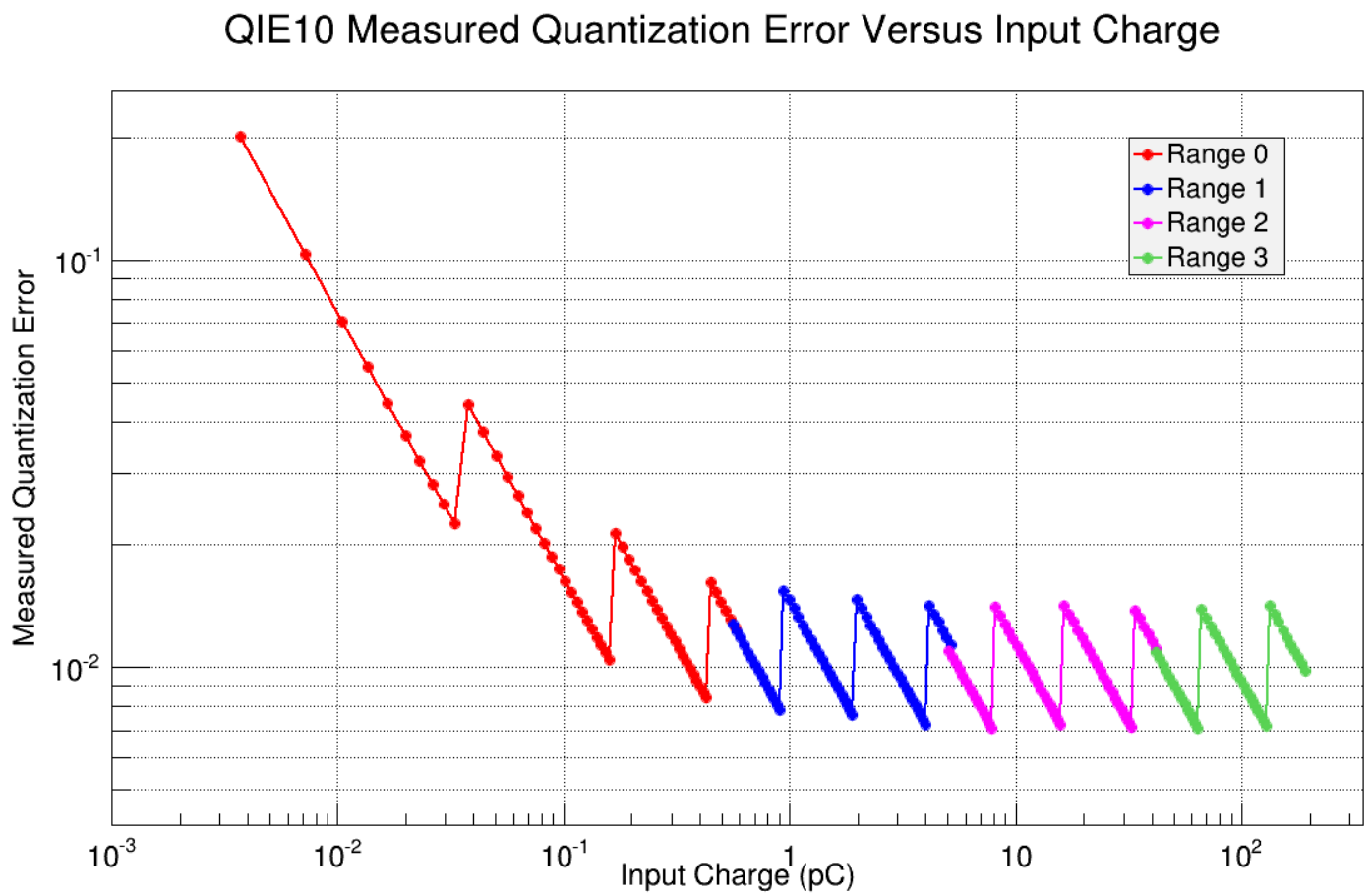



Data from Fermilab

⇨ ***Response as expected***

# Performance Studies (Cont.)

- DC Current Injection (Cont.)
  - Calculate quantization error from measured ADC bin widths

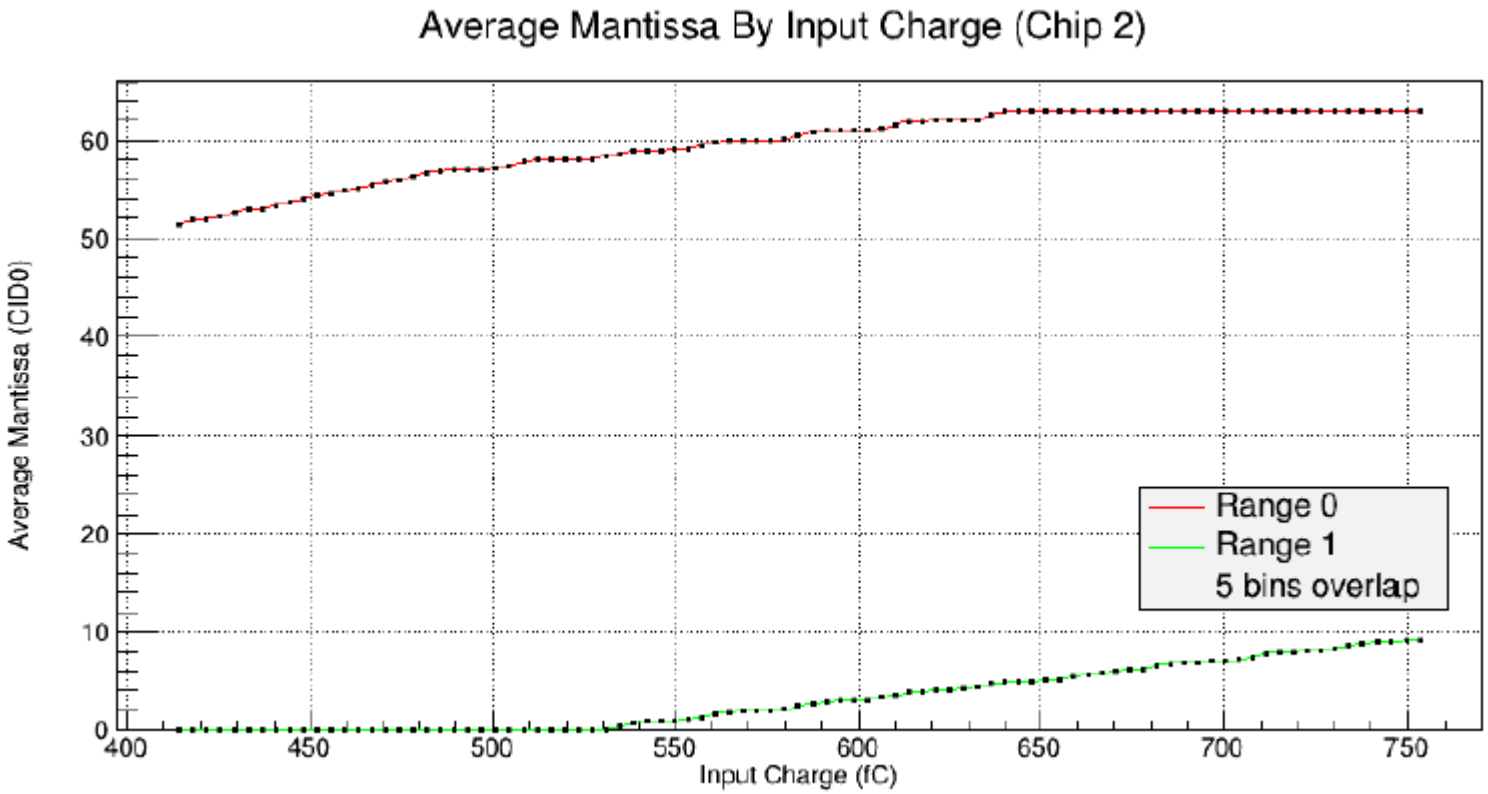



⇨ ***Response as expected***

Data from Fermilab

# Performance Studies (Cont.)

- DC Current Injection (Cont.)
  - Range overlap
    - Can force QIE10 to read out on a specified Range (i.e. turn off auto-ranging)
    - Want to make sure that there are no gaps in coverage

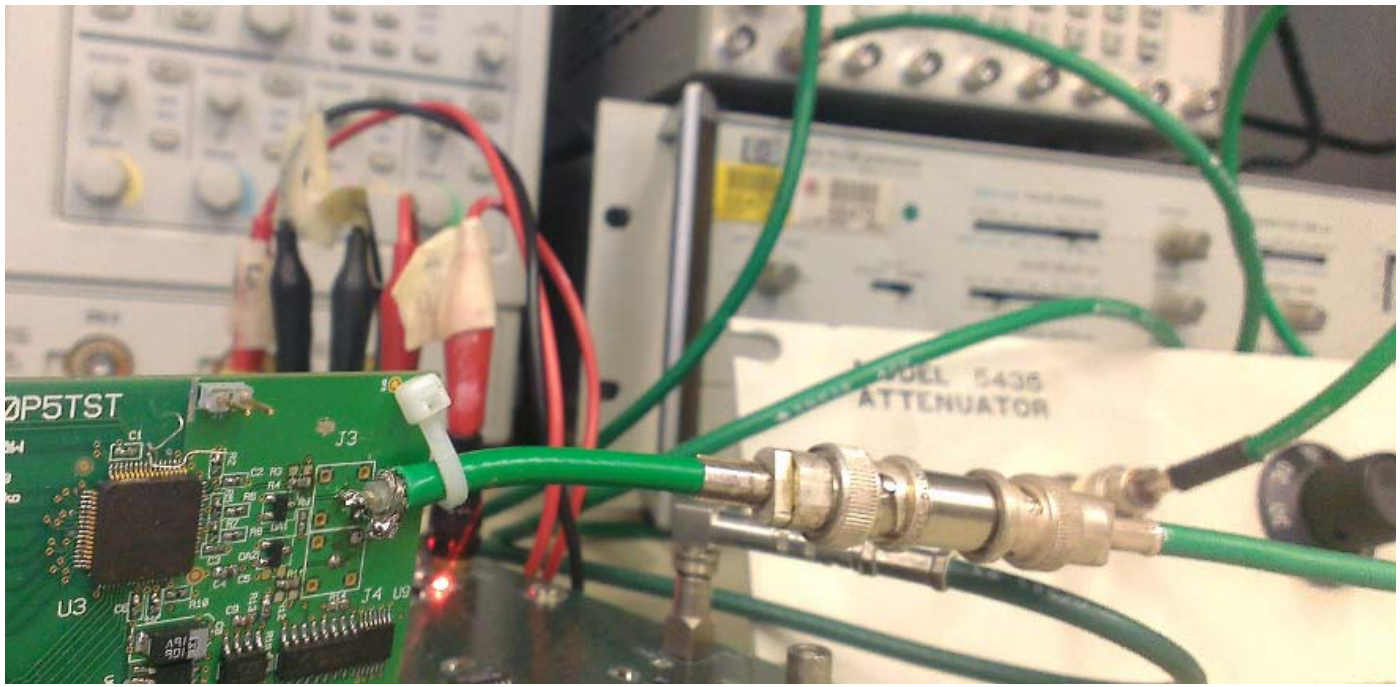



Data from Fermilab

⇨ ***See nice overlap in all Ranges***

# Performance Studies (Cont.)

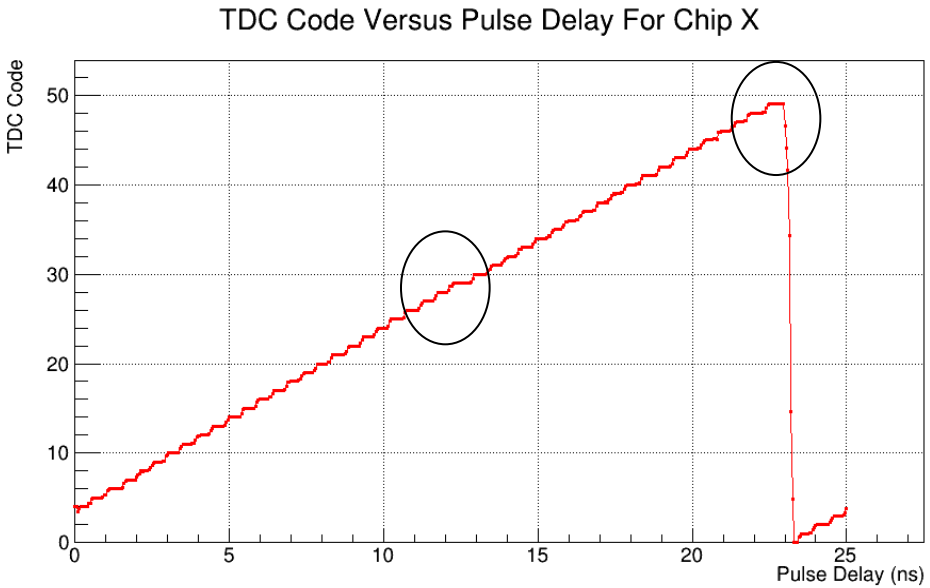
- Timing Studies
  - QIE10 has a 6-bit TDC
    - Marks time of input signal within the 25 nS clock period
    - 49 codes, 0.5 nS time bins

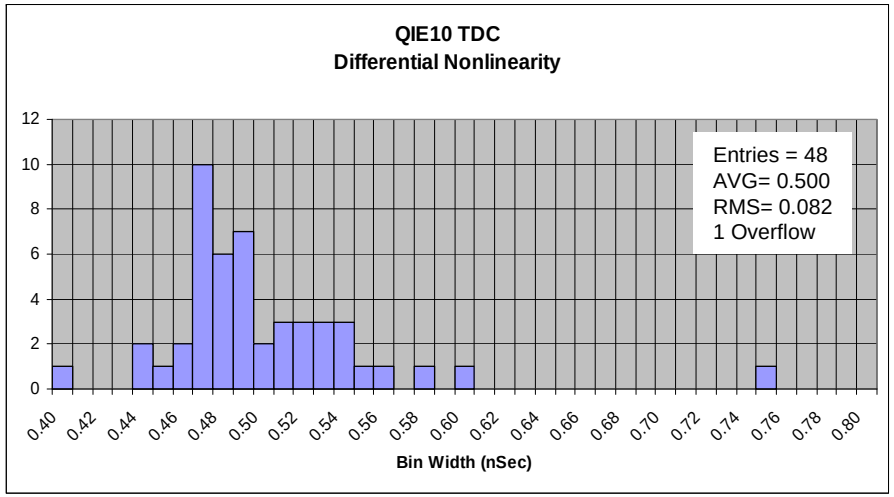



Setup
At
Fermilab

# Performance Studies (Cont.)

- Timing Studies - TDC Response
  - Using programmable delay to generate charge injection
    - 100 points per setting



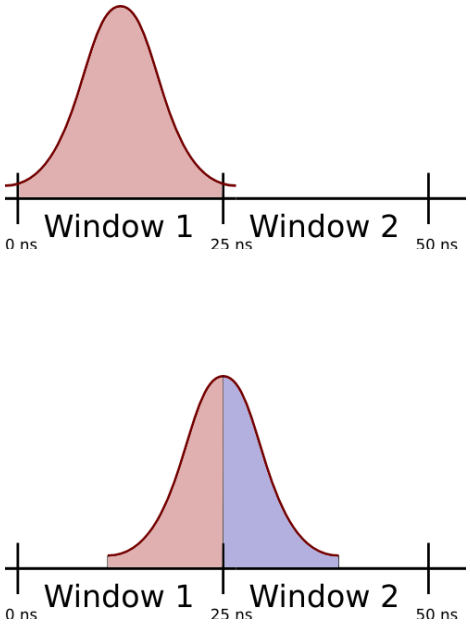

Data from Fermilab

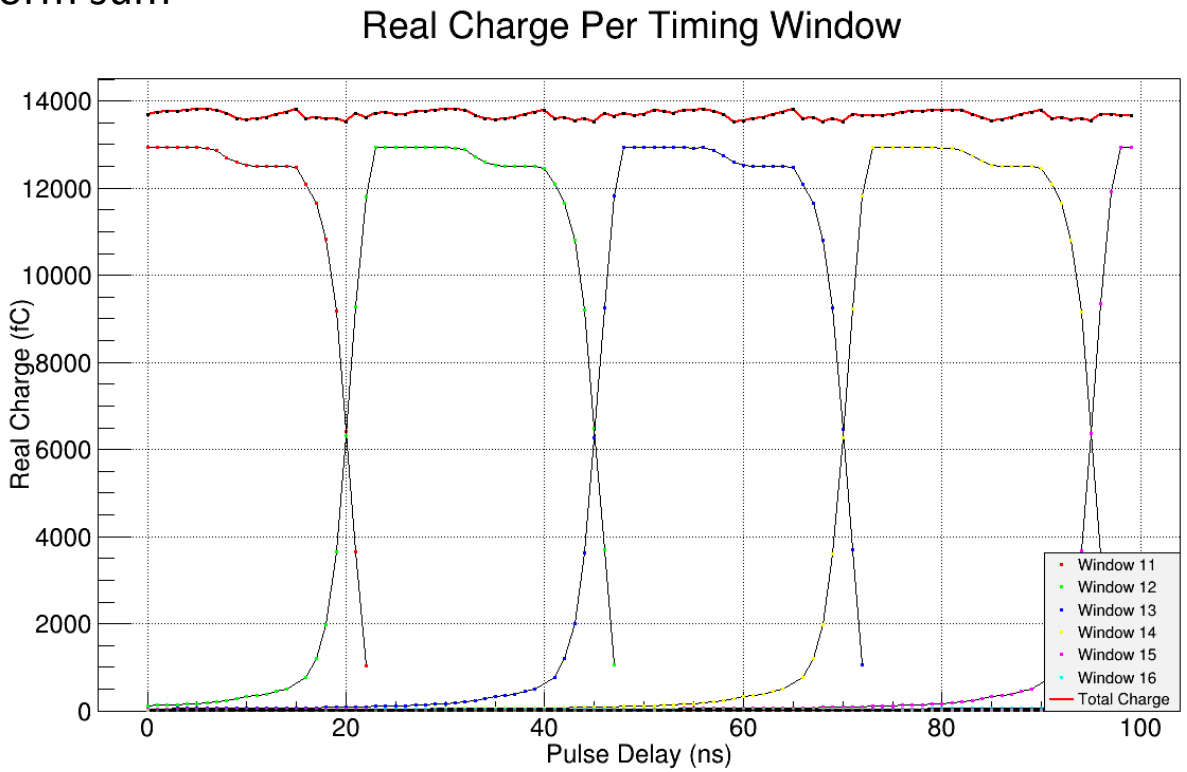
⇨ ***See nice linear response***

⇨ ***Bin width uniformity OK (worst at 12 ns & 25 ns)***
***(Tom Z.: No design reason for 12 ns outlier…)***

# Performance Studies (Cont.)

- Timing Studies – Pulse Integration
  - Walking charge injection pulse through clock periods
    - 1 ns steps
    - At each delay, calculate total charge from all windows
    - Look for uniform sum



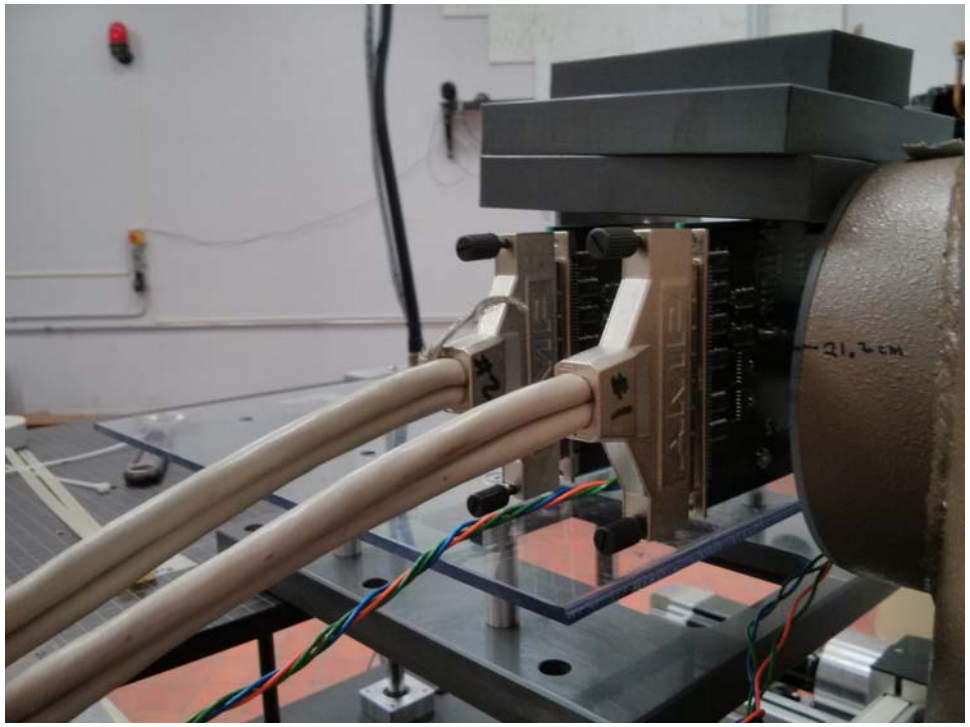




Data from Fermilab

⇨ ***See nice uniform response***

# Performance Studies (Cont.)

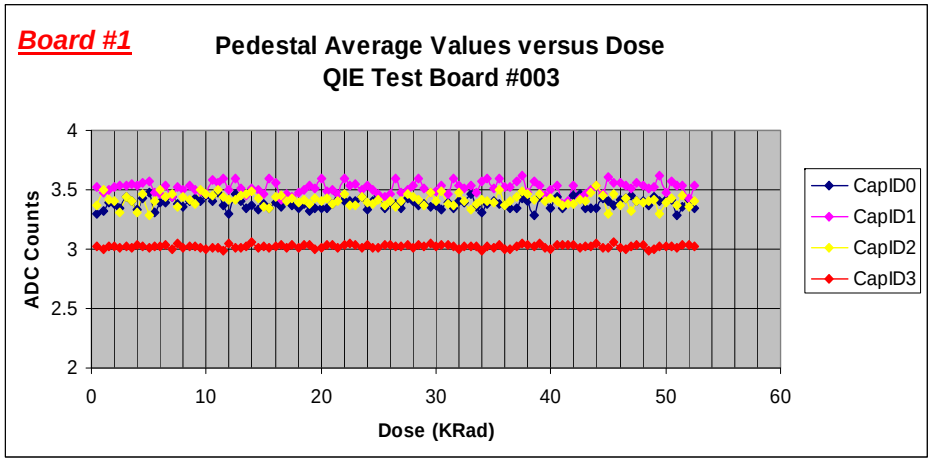
- Radiation Studies
  - Study of tolerance to Ionizing Dose (TID)
    - Use Cs-137 source at Argonne, ~1 KRad/hr.
    - Read pedestals 2X per hour
    - Read digital data (Shadow Reg & Shift Reg) continuously to look for data corruption

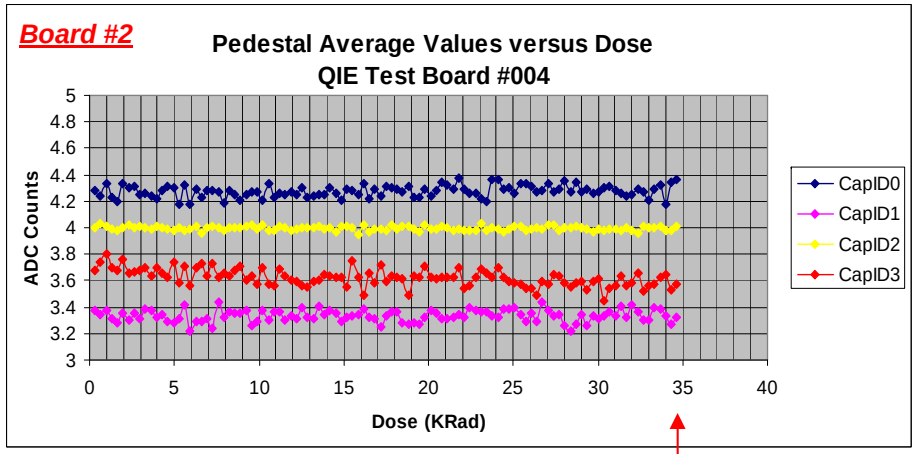


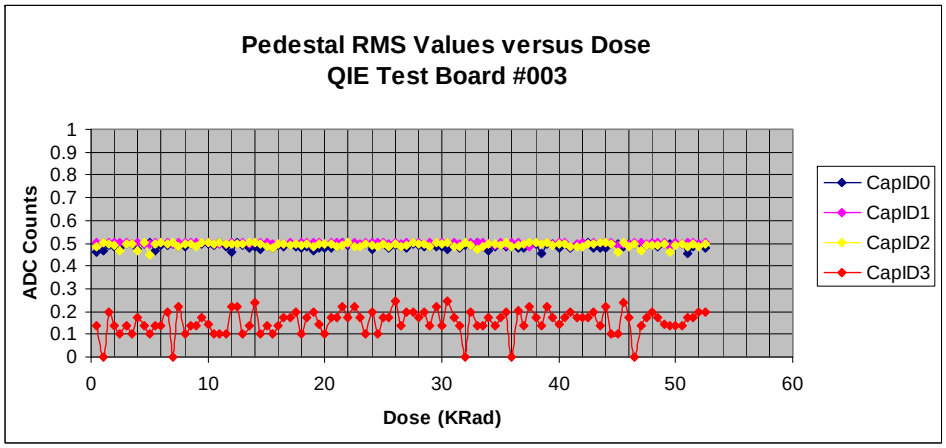
Setup
At
Argonne

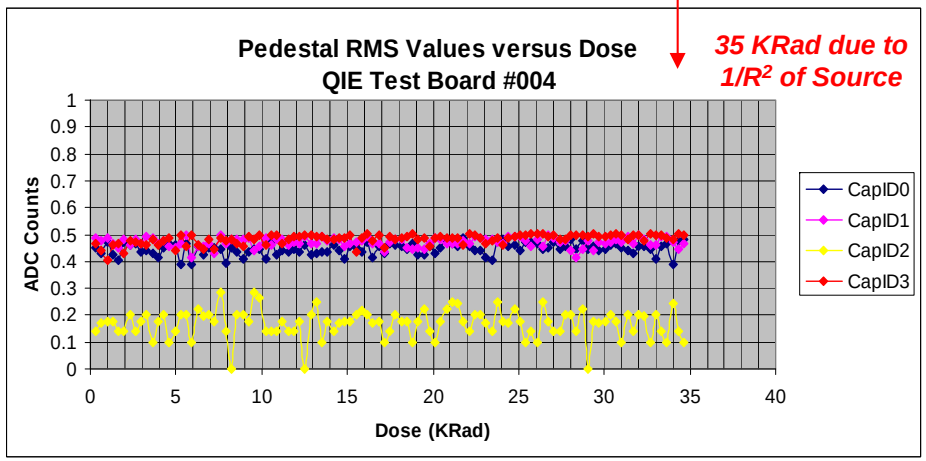
# Performance Studies (Cont.)

- Radiation Studies (Cont.)
  - Study of tolerance to Ionizing Dose (TID) – Results:




***35 KRad due to $1/R^2$ of Source***

⇨ ***No changes in pedestals out to ~50 KRad***

⇨ ***No R/W register errors, No CapID errors***

Data from Argonne

# Performance Studies (Cont.)

- Radiation Studies (Cont.)
  - Study of tolerance to Single Event Upset (SEUs)
    - Use 230 MeV proton beam at Central DuPage Hospital – Warrenville, IL
    - Read digital Shift Register during irradiation – Look for corruption
    - Read Shadow Register periodically – Look for corruption

Setup At CDH

⇨ ***Results after 6E12 p/cm$^2$:***

- 2 SEU errors in Shift Register data
- 0 SEU errors in Shadow Register data
- Pedestal readout was non-functional at the end
  - ADC values were nonsense
  - CapIDs no longer rotated
  - ⇨ ~330 KRad TID from protons…
  - ⇨ Probably the NPN transistors failed (T. Zimmeman)
  - ⇨ Will redo test in the near future

⇨ ***Meets requirements for SEUs***

# Outlook & Plans

- Summary
  - TDC is a nice addition to the QIE family
    - Direct measurement of out-of-time events
  - Least count sensitivity is excellent
  - Noise performance is excellent
  - Dynamic range is excellent
  - Power consumption is low
  - TID & SEU performance meets requirements for HCAL
- Next:
  - "Small production run" of chips
    - Commission FNAL Robot IC Tester
    - Prepare for test beams
  - Additional radiation studies (SEU, displacement damage)
  - Integration studies (both CMS & ATLAS)
- For CMS
  - Performance is significantly improved over previous version
  - Will be going into production for HCAL upgrade
    - 2015-16 shutdown: 3456 ch. for HF
  - A second design is in the works to add programmable shunt for SiPM readout
    - Allows for use with high-gain SiPMs
    - Allows for increased leakage current with radiation damage
    - 2018 shutdown: 13821 ch. for HB & HE
- For ATLAS
  - Candidate for Phase 2 Upgrade
  - Will be designing a front-end board for the Tile Calorimeter
  - Will be testing in a test beam ~2015
    - 1 drawer = 48 channels
    - Technology decision ~ 2016 (3 competing front-end technologies)

⇨ ***CMS HCAL: Full speed ahead for HCAL Upgrade***

⇨ ***Atlas TileCal: A Strong Candidate for the Phase 2 Upgrade…***

⇨ ***Other related talks & presentations:***

⇨***2013 TWEPP Poster:***
***E. Hughes, et al., "System Level and Production Tests of the CMS HCAL QIE10"***

⇨***2013 IEEE NSS Talk:***
***T. Zimmerman, "QIE10: A New Charge-Integrating Floating-Point ADC Chip for High-Rate Experiments"***

# Thank you for your attention!