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QIE10: A New Front-End Custom Integrated Circuit

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We present results on a new version of the QIE (Charge Integrating Encoder), a custom Application Specific Integrated Circuit (ASIC) designed at Fermilab. Developed specifically for the measurement of charge from detectors in high-rate environments, this most recent addition to the QIE family features 3 fC sensitivity, 17-bits of dynamic range with logarithmic response, a Time-to-Digital Converter (TDC) with sub-nanosecond resolution, and internal charge injection. The device is capable of dead-timeless operation at 40 MHz, making it ideal for calorimetry at the Large hadron Collider (LHC). We present bench measurements and integration studies that characterize the performance, radiation tolerance measurements, and plans for deployment in the Atlas and CMS detectors as part of the Phase 1 and Phase 2 upgrades.

Summary

The QIE10 is the newest version in the family of QIE devices designed at Fermilab. It integrates input charge pulses in 25 nS time slices over a large dynamic range and digitizes the result with approximately constant resolution over the entire dynamic range. This is accomplished in a novel way by simultaneously integrating the input charge on four different ranges which are scaled by factors of 8. One of the ranges is selected for digitization based on the signal size. The selected output is digitized using an on-chip, pseudo-logarithmic, 6-bit flash ADC (FADC). The FADC bin size doubles several times over its full range, so that the bin size at the top of the FADC is 8 times the bin size at the bottom of the FADC. Since the 4 integrator ranges are also scaled by a factor of 8, the end result is that the QIE resolution (the FADC bin size divided by the signal magnitude) is held between 0.7% and 1.4% over the entire dynamic range of the QIE, which is approximately 17 bits.

This scheme provides a floating point digitization of the input charge at 40 MHz. The QIE10 digital output consists of 6 bits of mantissa (FADC outputs), 2 bits of exponent (range code), and 6 bits of TDC, which provides digitized pulse arrival time with respect to the 25 ns clock. The QIE operation is pipelined with 4 phases to allow dead-timeless operation, so a 2-bit "CapID"code is also provided to indicate which phase is associated with each result. Ideally, each phase or CapID has identical response, but in practice there can be small differences in the pedestal at the low end. The ability to adjust the pedestal of each phase is provided via the program shift register. The digital output result for a given integrated input pulse has a 4 clock period latency. Since the QIE10 is pipelined with 4 phases, it is integrating the input charge for the CapID0 phase while outputting the digitized result of the previous CapID0 integration. A block diagram of the device is shown in Fig. 1.

The new version of the QIE differs from earlier versions in several ways. QIE10 is the first QIE chip to be designed in the AMS 0.35u SiGe BiCMOS process. This will give greater radiation-hardness performance. The new design also has a factor of ten greater dynamic range than the previous version, from 30 pC up to 300 pC. Also, many different operational parameters can now be programmed via a serial program shift register (optional, since the register is set to default values upon power-up). A delay-locked loop and a timing discriminator with programmable threshold have been added in order to form a pulse-arrival TDC with 0.5ns resolution. The digital outputs provide data on each edge of the clock, for an effective 80 MHz parallel readout rate. The digital outputs can deliver true LVDS, as opposed to the "pseudo-LVDS"outputs of previous QIE chips.
The device is in an advanced stage of prototyping. We have fully-functional devices that we have tested at the bench, and have also begun studies with detectors and integration into read-out systems. We (will) have performed radiation tolerance studies. This is a joint development project. The device will be used in the CMS

Phase-1 upgrade for the hadronic calorimeter, and is a candidate for use in the Atlas Phase-2 upgrade for the Tile Calorimeter. We will present the status of the project, and our plans going forward.

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