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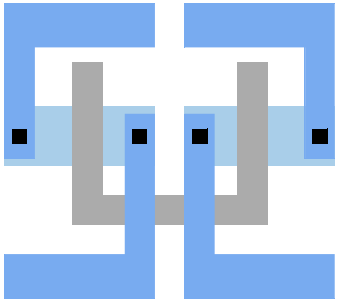
# PETA4 – A Multi Channel TDC/ADC ASIC for SiPM Readout

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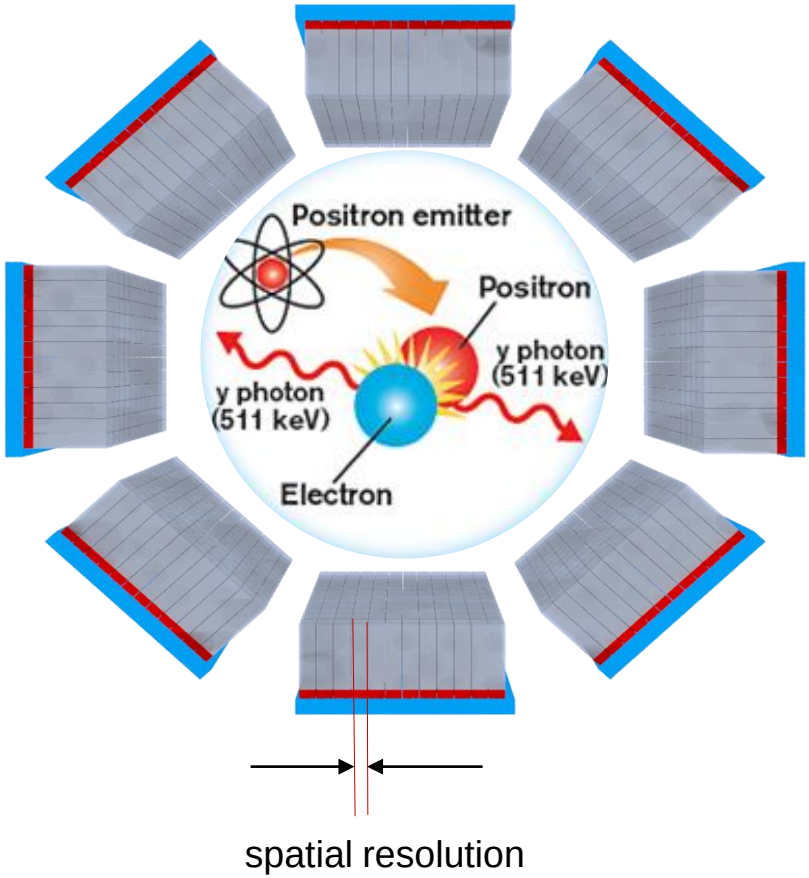
Heidelberg University

TWEPP 2013

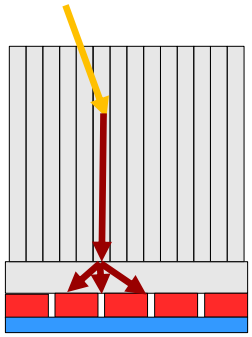
Perugia, 23-27 Sept. 2013

# SUBLIMA: PET/MR whole-body demonstrator



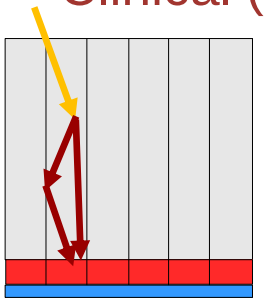

spatial resolution

## Preclinical (small animal) module



- Pixelated LYSO & light spreader + SiPM array
  - Very good spatial resolution → **sub-millimeter array identification**
  - light spreader + mathematical interpolation is mandatory
  - narrow field of view → ns coinc. time resolution is sufficient

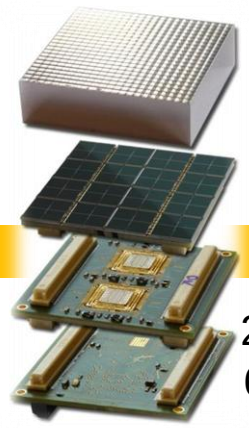
## Clinical (whole-body) module



- Pixelated LYSO in 1:1 coupling with SiPM array
  - Very good time resolution → **less than 300ps coinc FWHM for ToF**
  - reduced data rate
  - spatial resolution < 2mm has **no benefit**
  - **high number of readout channels**

# Position Energy and Timing ASIC Family

2006 PETA

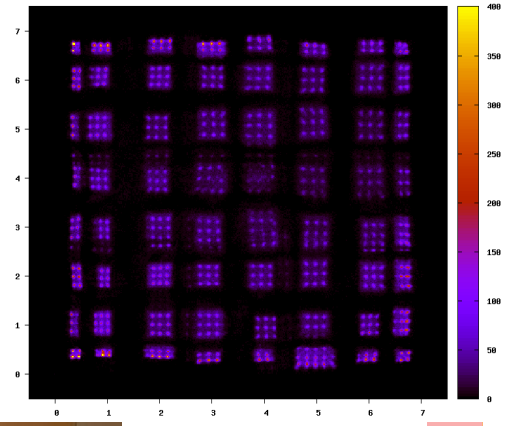


2 PETAs /
64 SiPMs

**HYPERImage**
pre-clinical PET ring in MR

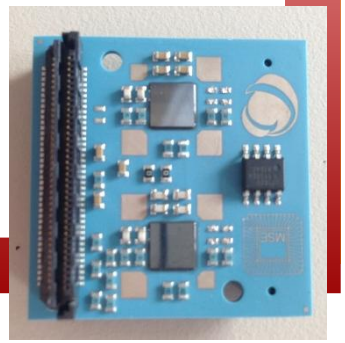
2007 PETA2

2010 PETA3



**in 1:1 configuration**
**dE/E ~ 12.5% FWHM**
**~ 200 ps crt FWHM**

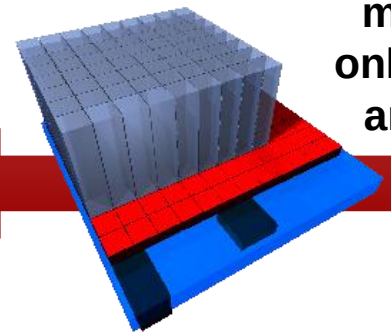
2012 PETA4



**submitted**

2013 PETA5

**very compact module with only one board and 4 ASICs**



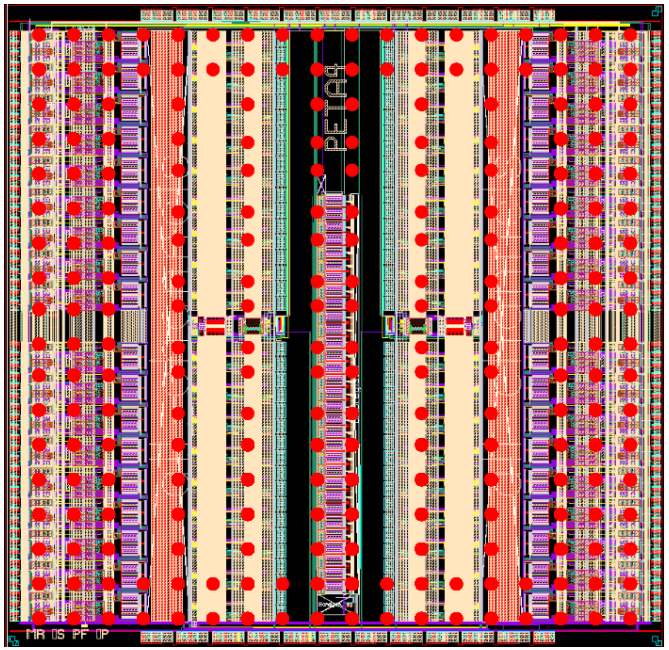
**SUBLIMA**
whole body PET/MR demonstrator

# PETA4 Design

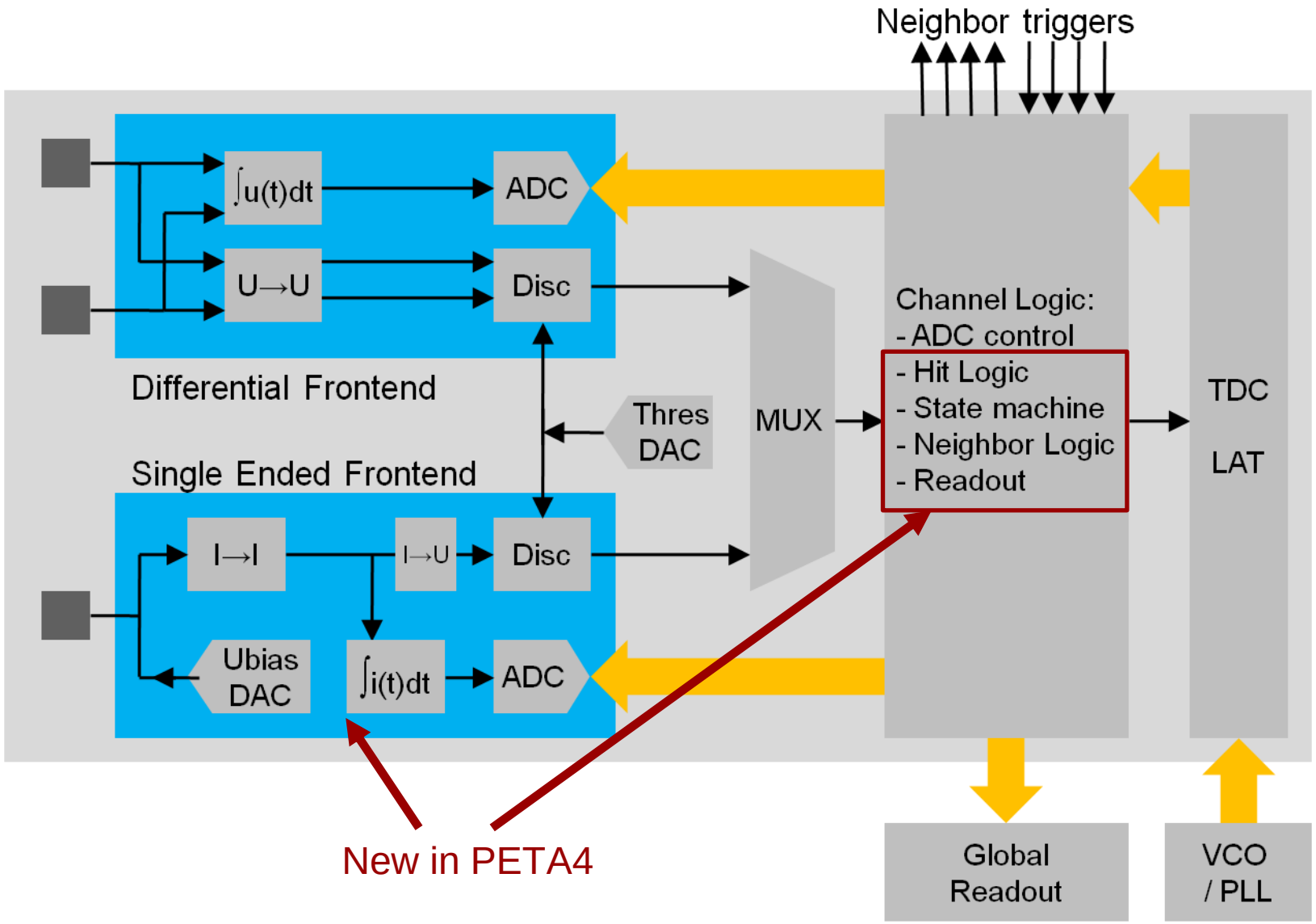
- Aimed to a compact module design
  - 5x5 mm² area, UMC 180nm – six metal layer technology
  - 36 channels
  - **bump-bonded** with pads pitch ~ 270um
  - nearly NO external components: maximal integration on chip
  - configuration and control scheme shared up to **4 chips** with very few wires

- Two **independent frontends** per channel
  - single-ended with low input impedance
  - differential-ended reliable in MR environment

- Low power design
  - 25mW analogue/ 7.5mW digital per channel

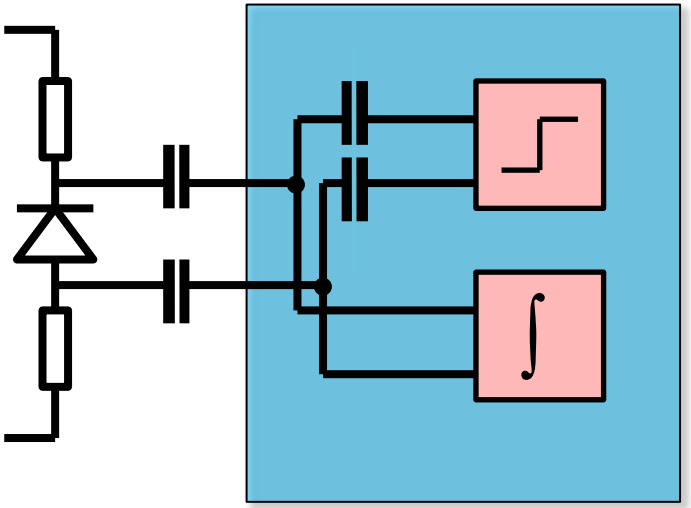


# Single Channel Architecture



# Frontend Design

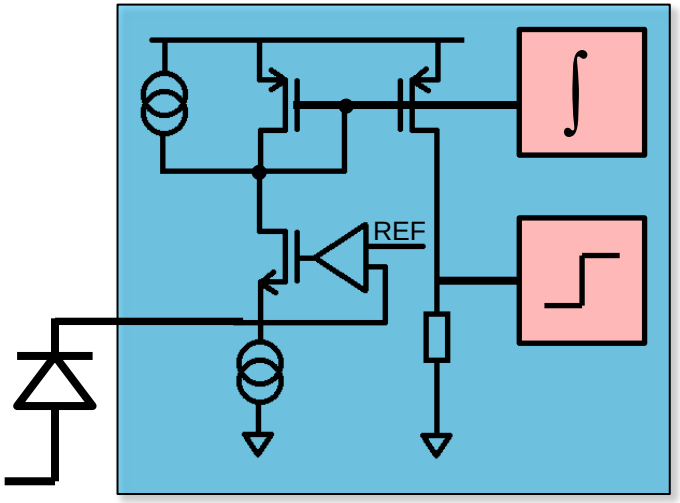
## Fully differential-ended frontend



- Very flexible
- Reliable & tested in MR (previous version)
- External decoupling needed

- ADC: Voltage SAR

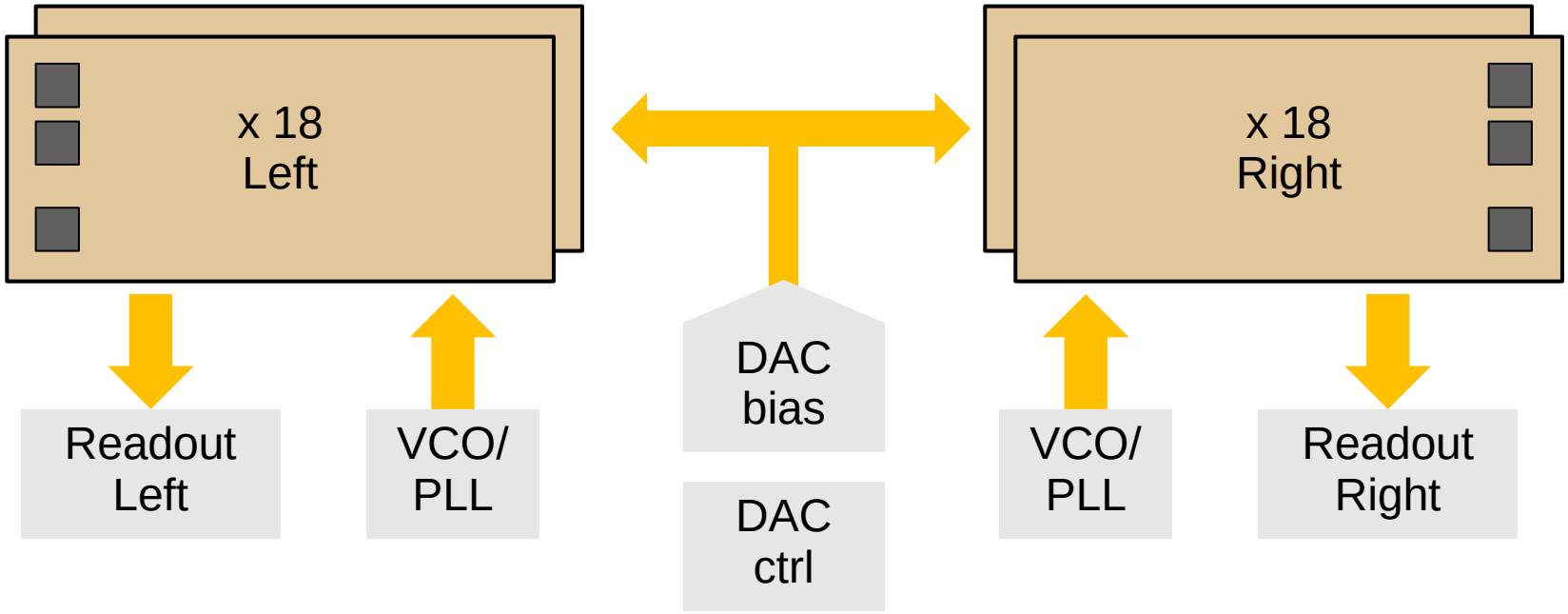
## Single-ended frontend




- Input impedance ~ 7Ω
- Adjustable input DC potential ± 0.4V
- NO external component needed
- Threshold circuit as in differential

- ADC: Integrator discharge + timer

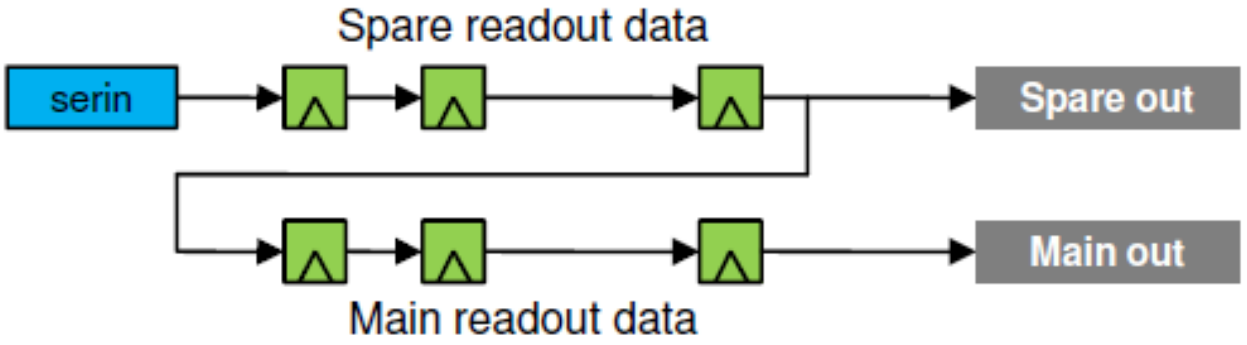
# Overall Architecture




- Fully differential PLL & VCO → fully integrated on chip (new in PETA4)
- Reference clock @ 622.5 MHz
- TDC from 16-stage ring differential oscillator locked to reference → binwidth ~ 50.2 ps

# Serial Readout

- Max readout LVDS clock 160 MHz
- Both chip sides (Left/Right) have two serial LVDS outputs
  - Main readout
  - Monitoring/spare readout

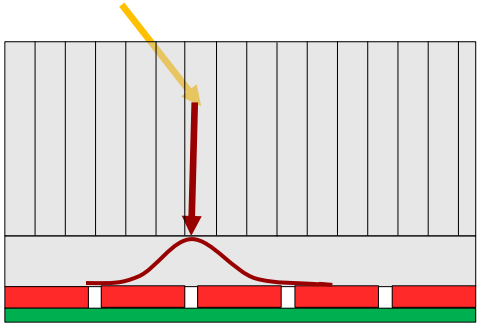



- **Bypass** : empty channels do not send data in shift register (1 flag bit)

- Readout register is 32 bits/channel

# Neighbor logic

- Neighbor logic is necessary in preclinical applications



- All the SiPM with (even small) integrated signals must be readout

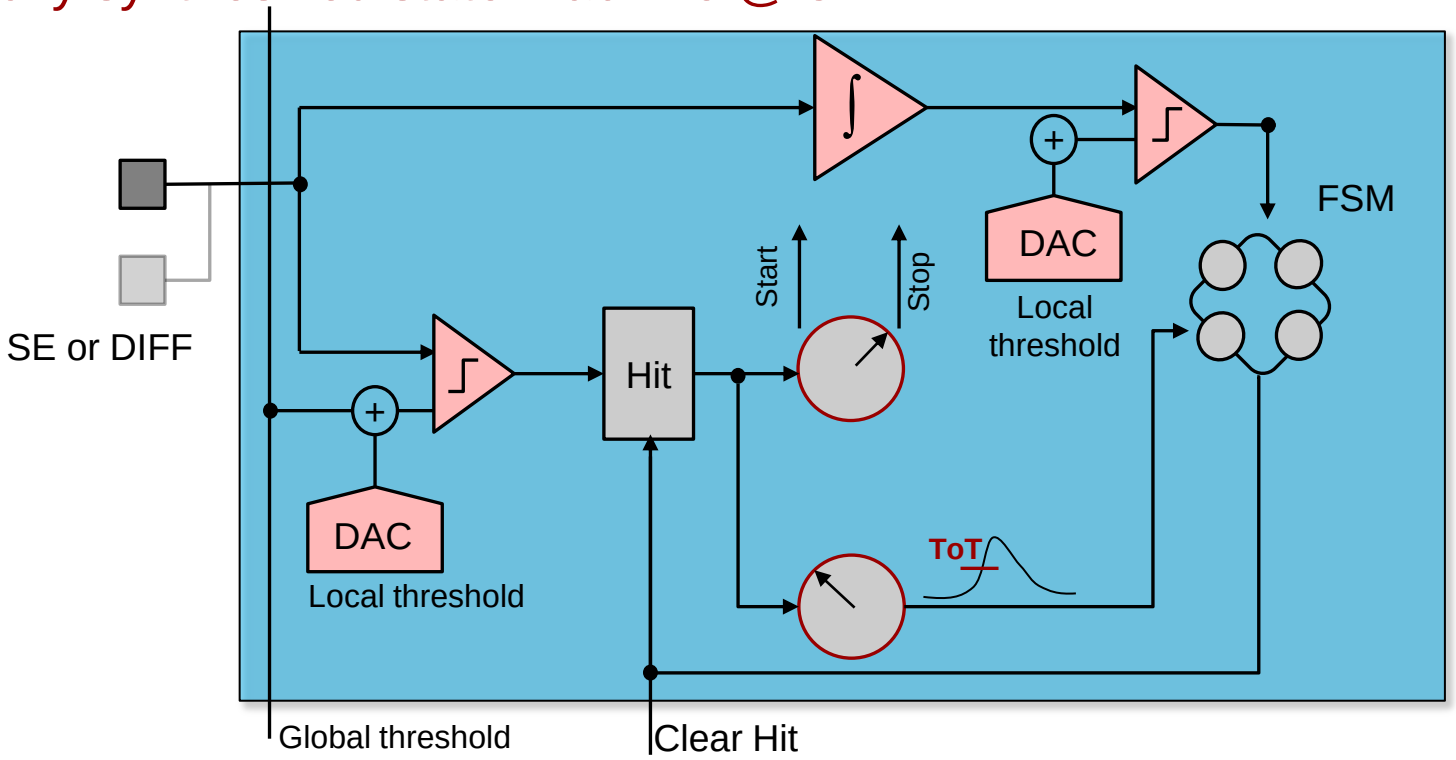
  - low discriminator threshold → noisy hits

  + channel with the **highest energy contribution** triggers its neighbor

- New in PETA4
  - 4 neighbor group per half-chip
  - Membership to each group is programmable
  - Flexible configuration for position-sensitive detector readout

# Hit Validation and Noisy Hit Rejection

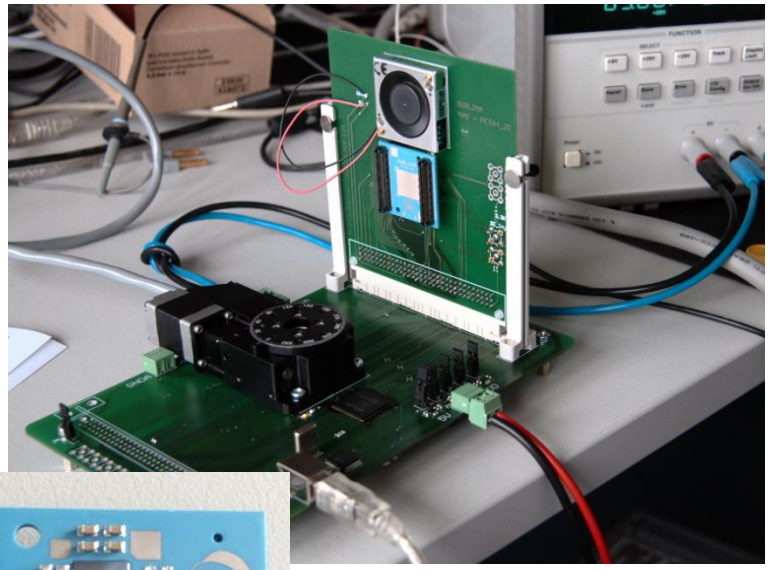
## Fully synthesized state machine @ 312 MHz



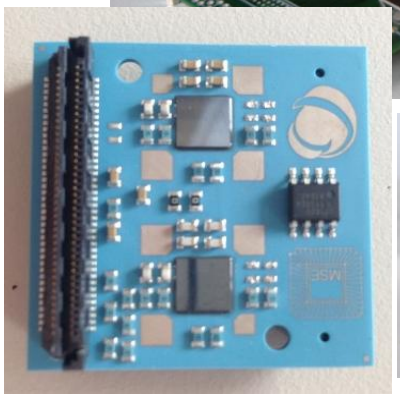

- Early evaluation with Time over Threshold
  - Require a minimum width of the triggering pulse
  - Only in differential FE
- Minimum energy threshold
  - Discard hits with digitized energy lower than a programmable value
  - Both in differential & single ended FE

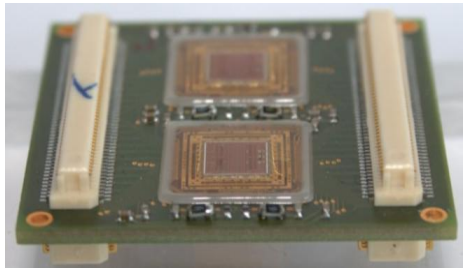
# Test setup

- Only **one** frontend can be connected on the board
  - LTCC with **differential frontend** bump-bonded
  - test injection in single-ended frontend
- Setup with face to face boards for time coincidence measurements with radioactive source
- Rotational stage for 3D reconstruction



- **But**
  - differential FE has a bug → TDC **never** starts the conversion
  - single-ended FE inputs are **not connected on this LTCC**, but TDC works → modifed LTCC for the first validation



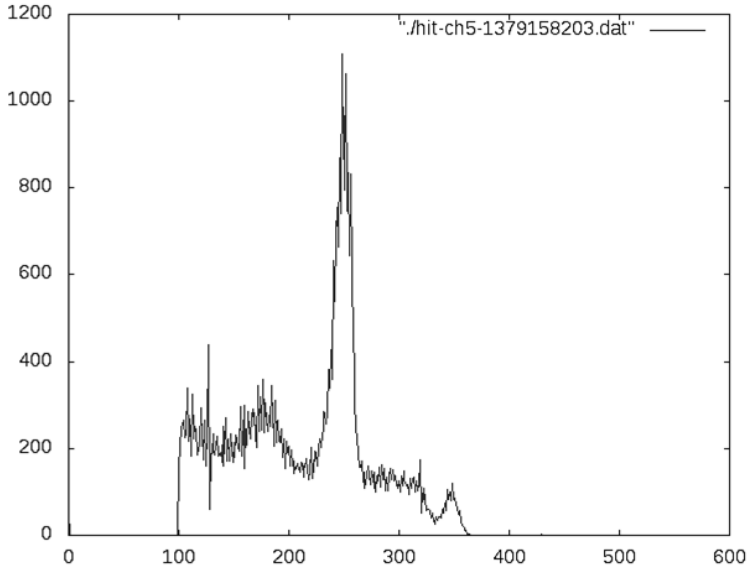


# Energy resolution: differential FE

- SAR-ADC resolution
  - programmable resolution — 5 to 11 bits
  - programmable conversion time — ~ 50 – 100 ns
  - Analogue integration timer — ~ 200 – 300 ns
  - Resolution with analogue pulses (LSB) — $0.35 < \sigma < 0.76$ rms
- Measurements in 1:1 coupling configuration
  - SiPM 4x4mm² with LYSO 4x4x10mm³

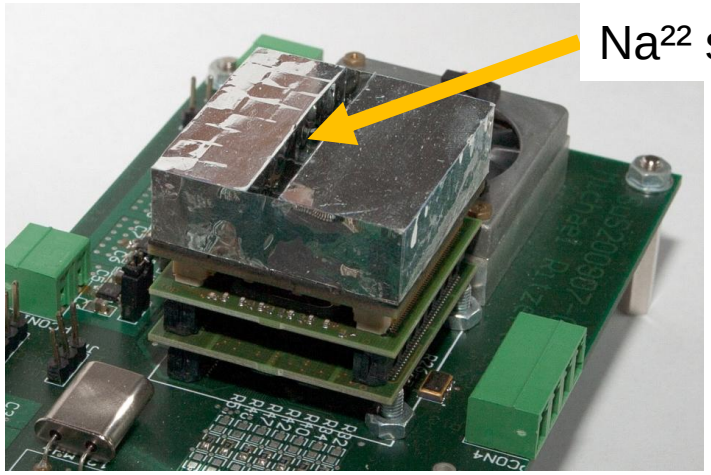
✓ dE/E @ FWHM ~ 12.8 % after linearization

✓ Same as previous PETA, as expected.

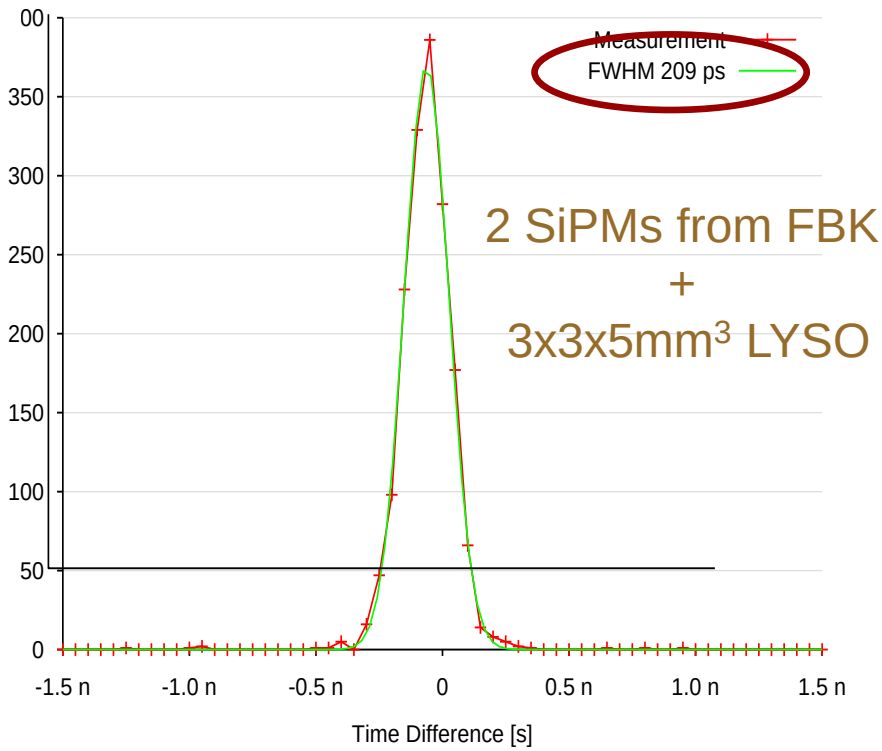


# Time resolution: differential FE

- TDC is not enabled for differential frontend
  - Bug fixed in PETA5 ~ expected for December 2013
- Expected results as PETA3
  - intrinsic time resolution σ~34 ps coinc. rms



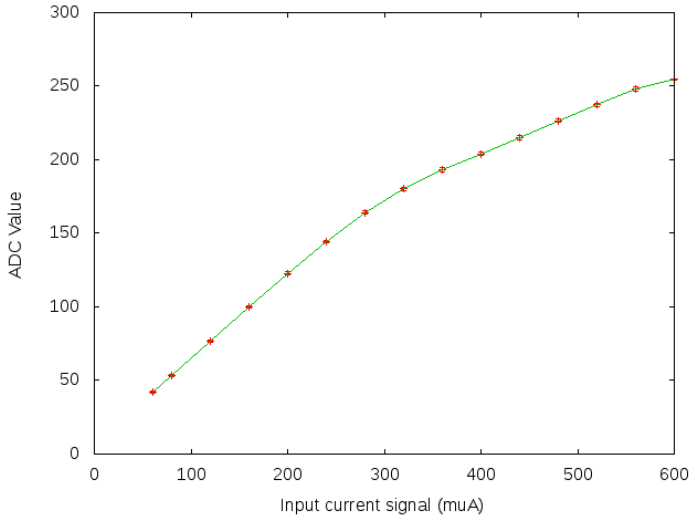
$Na^{22}$ source




Measurements
@ FBK

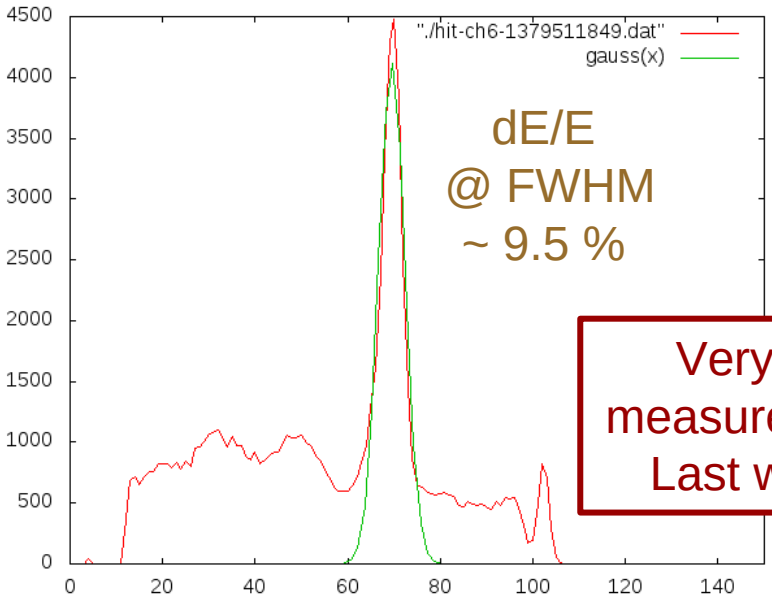
# Energy resolution: single-ended FE

- Signal integration + discharge counter
  - fixed 9 bits resolution
  - Programmable integration time — up to ~200ns
  - Variable discharge time — max 1.5us
  - Resolution with analogue pulses (LSB) — **σ < 0.5 rms**




Almost linear ADC behavior

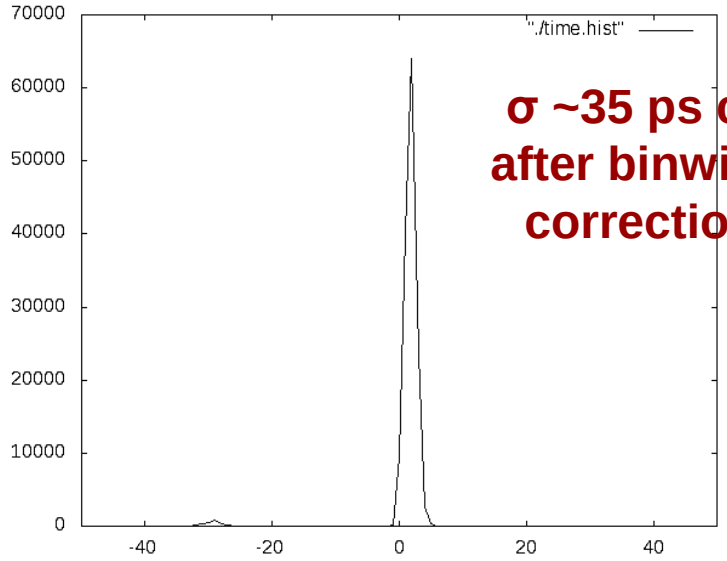
Coupled with 4x4mm² SiPM and 4x4x20mm³ LYSO




Very first measurements! Last week..

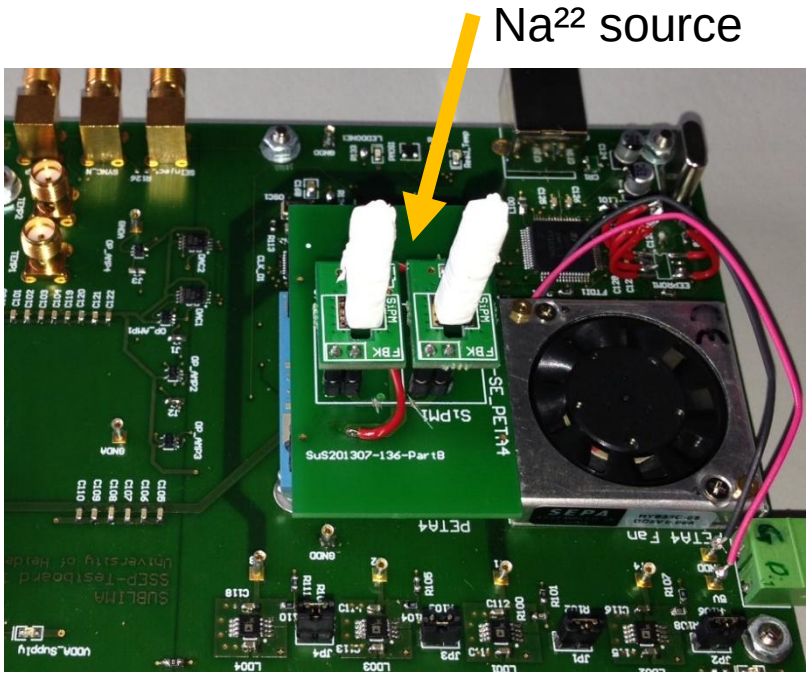
# Time resolution: single-ended FE

- Intrinsic resolution with analogue pulses in test injection path




**σ ~35 ps crt after binwidth correction**

- With SiPM + LYSO **~ 460 ps coinc resolution FWHM**
  Very first measurement!!!

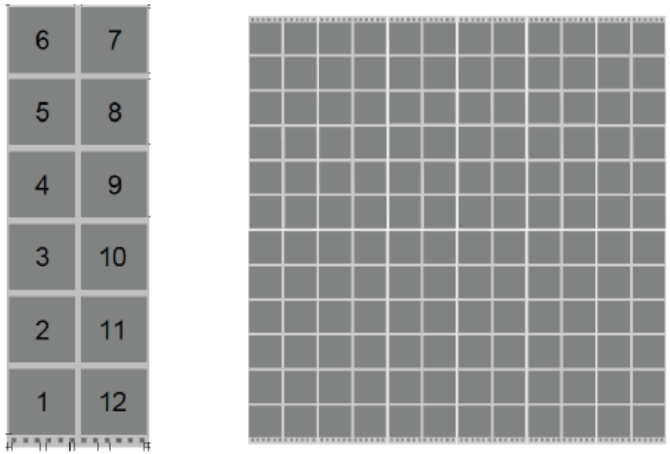


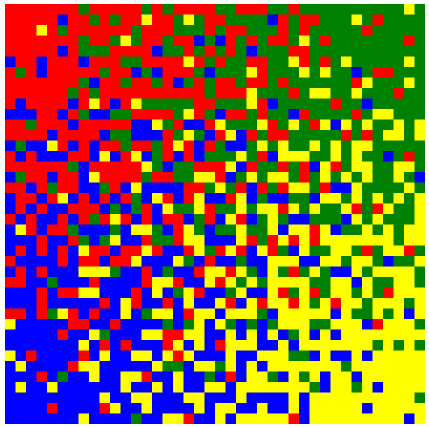
# Differential vs. single-ended FE

| Frontend | Intrinsic resolution | | SiPM + LYSO resolution | | Power/ channel | Advantages |
|---|---|---|---|---|---|---|
| | time | energy | time | energy | | |
| Differential | σ~34ps crt rms exp. | σ <0.7 rms | 200ps exp. | 12.8% @ FWHM 4x4mm$^2$ SiPM 4x4x10mm$^3$ LYSO | 21mW | Low noise<br>No pickup in MR |
| Single-ended | σ~35ps crt rms | σ < 0.5 rms | 460ps crt FWHM 4x4x20 mm$^3$ LYSO | ~9.5% @ FWHM not corrected 4x4mm$^2$ SiPM 4x4x20mm$^3$ LYSO | 25mW | Very low Rin<br>High channel count operation<br>Programmable DC input<br>No external components required |

# Outlook

- Very compact module
  - One **LTCC** with SiPMs & PETAs
  - 4 ASICs per board → max 144 channels



- Clinical demonstrator with **ToF**
  - 144 SiPMs readout with **single-ended FE**
  - LYSO array with **2.6 mm constnat** pitch
  - Nearly NO external components
- Preclinical ring with **position-sensitive SiPM**
  - readout with **single-ended FE**
  - LYSO array with **0.8 mm** pitch
  - Neighbor logic needed
  - Nearly NO external components

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# Thank you!

This work has been supported by the European Union under the 7th framework program Grant Agreement #24171

SUBLIMA