Contribution ID: **145** Type: **Poster**

FEERIC, a very-front-end ASIC for the ALICE Muon Trigger Resistive Plate Chambers

Wednesday 25 September 2013 16:39 (1 minute)

The ALICE Collaboration at the CERN-LHC has started a vast program of upgrades of the detector in the context of the increase of the luminosity of the LHC from 2018 on. The present very front-end electronics (VFE) of the Muon Trigger, whose acronym is ADULT, must be replaced to limit the aging of the Resistive Plate Chambers (RPCs) in the future expected operating conditions. For this purpose, the new VFE, FEERIC, will have to perform an amplification of the analog input signal (this is not the case for ADULT). This will allow to operate the RPCs in avalanche mode with a lower gain at the level detectorgas, in comparison to the current situation.
This VFE represents 21,000 channels, distributed over 2400 electronics cards equipped with one or two FEERIC ASICs. A total of 3000 ASICs of 8 channels each is necessary. The future ASIC has to insure mainly the following functions: amplification, discrimination and LVDS output stage. FEERIC will be capable of handling bipolar signals varying from ±20 fC up to ±5 pC.
A prototype chip has been designed using the 0.35 µm CMOS technology of AMS. The FEERIC ASIC description, technical choices and performance from simulations and tests will be presented.

Summary

The LHC upgrade plan foresees an increase of almost one order of magnitude of the p-p and PbPb collision rates after 2018. In order to reduce the aging speed of the RPC detectors of the ALICE Muon Trigger [1], [2], in such a context, it has been proposed to replace the present VFE ADULT [3] by a new one called FEERIC. Unlike ADULT, FEERIC should perform amplification of the analog input signal from the detector at the VFE level. With such a new feature, the RPCs could be operated in genuine avalanche mode with a reduction by one order of magnitude of the charge per signal produced in the gas. The requirements of the FEERIC ASIC can be listed as follows:
• It must process both positive and negative RPC signals, depending on the readout plane position relative to the electrode polarity;
• The requested dynamic range is from 20 fC to 5 pC, while the expected mean charge at the working point is

rather 50-100 fC;
• The level of noise should be limited to 2 fC rms;
• The time resolution must be better than 1 ns rms in the
whole operating dynamic range;
• The time walk must be less than 1 ns over the whole
operating dynamic range;
• The output signal width must be equal to 23 ± 2 ns;
• After a signal passing the threshold, the electronics must
be blind during 100 ns;
• The output format is Low Voltage Differential Signaling
(LVDS);
• It must present a 50
resistance at the input in order to
match the characteristic impedence of the readout strips;
• The power consumption must be less than 100 mW per
channel;
• It is constituted of 8 channels per ASIC.
The technology used to design this VFE is the low cost AMS
0.35 µm CMOS technology. One channel block diagram is
composed of a transimpedance amplifier, a zero-crossing discriminator,
a one shot and an LVDS output stage. The current
preamplifier amplifies the input signal carried by the strip.
Then a zero-crossing discriminator delivers a signal whose
timing (relative to the input signal) is amplitude independent.
The one shot permits to obtain an output signal width equal to
23 ns and after a signal passing the threshold, the electronics
is blind during 100 ns. Finally, an LVDS output stage allows
to drive an output signal of ±350 mV on a resistive load of
100
.
The results obtained show the time resolution of FEERIC
which depends on the jitter introduced by noise and the
time walk essentially driven by the performance of the zerocrossing.
The obtained time resolution is 300 ps rms for an
input charge of 50 fC, and 100 ps rms for an input charge
of 100 fC. Concerning the time walk, it is less than 600 ps
for the whole charge range above 50 fC. The global power
consumption per channel is estimated to 70 mW, with a 3 V
power supply voltage.
REFERENCES
[1] The ALICE Upgrade, "Letter of intent"CERN-LHCC, 2012-012.
[2] K. Aamodt et al. "The ALICE experiment at the CERN LHC, by ALICE
Collaboration,"JINST, 3:S08002, 2008.
[3] R. Arnaldi et al. "Front-end electronics for the RPCs of the ALICE
Dimuon TRigger, by ALICE Collaboration ,"IEEE Trans. Nucl. Sci.,
52:1176-1181, 2005.
[4] W.M.C. Sansen Analog design essentials. Springer, 2006.
[5] F. Loddo et al. "New developments on front-end electronics for the CMS
Resistive Plate Chambers,"Nuclear Instruments and Methods in Physics
Research, Section A 456, pp. 143–149, 2000.
[6] H. Spieler Semiconductor detector systems. Oxford University, 2005.
[7] P.E. Allen, D.R. Holberg CMOS Analog circuit design. Oxford University,
2002.

Primary author: MANEN, Samuel Pierre (Univ. Blaise Pascal Clermont-Fe. II (FR))

Co-authors: JOLY, Baptiste (Univ. Blaise Pascal Clermont-Fe. II (FR)); Mr BOUTIN, Benjamin (LPC CLermont Ferrand); JOUVE, Frederic (Univ. Blaise Pascal Clermont-Fe. II (FR)); ROYER, Laurent (Univ. Blaise Pascal Cler-

mont-Fe. II (FR)); DUPIEUX, Pascal (Univ. Blaise Pascal Clermont-Fe. II (FR)); Mr VANDAELE, Richard (LPC Clermont Ferrand)

Presenter: MANEN, Samuel Pierre (Univ. Blaise Pascal Clermont-Fe. II (FR))

Session Classification: Poster