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Use of FPGA Embedded Processors for Fast Cluster Reconstruction in the NA62 Liquid Krypton Electromagnetic Calorimeter

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The NA62 experiment at CERN SPS aims to increase the precision in the measure of the Branching Ratio of the K+->pi+nu nubar decay. The required background suppression level due to the decay K+->pi+pi0 can be achieved, among the others, implementing the photon veto in the angular range [1,10] mrad by using a LKr calorimeter. This paper deals with the implementation of the LKr L0 trigger peak reconstruction algorithm on an FPGA by using a mixed architecture based on soft core embedded processors together with custom VHDL modules This solution allows an efficient and flexible reconstruction of the energy-deposition peak.

Summary

The NA62 experiment at CERN SPS aims to study the rare kaon's decays K+ -> pi+ nu nubar. In two years of data taking the experiment goal is to collect about 100 events with 10% of estimated background. The required background suppression level can be achieved by the use of kinematic discrimination and more others specific particles vetoes. The photon veto system design is focused on the suppression of the dominant background originated from the decay K+ -> pi+ pi0. In particular, the role of the Liquid Krypton (LKr) high-performance electromagnetic calorimeter is to veto photons in the angular range [1,10] mrad. The Calorimeter REAdout Module (CREAM) provides 40MHz sampling of the channels and each of them is digitized with a 14-bit resolution. The readout rate is up to 1MHz. The CREAM performs the summation of the selected channel samples, and sends the resulting "Super Cell" (32 tiles) data to the LKr L0 Trigger processor. This trigger system, composed of 36 TEL62 boards, has a three layer structure with consecutive layers connected each other with custom multi Gigabit links. The first layer, the Front End (FE), performs an accurate identification of the energy-deposition peak for a subset of calorimeter cells. The second layer, the first Concentrator stage, merges the peak information collected by the different FE boards and composes them to identify the clusters. The third layer, the second Concentrator stage, receives time ordered data from the previous layer and sends them to the L0 trigger processor.

This paper deals with the implementation of the photons'impact precise time computation algorithm. In particular, it will be presented the performances of such an algorithm on the ALTERA NiosII soft core embedded processors hosted on an FPGA. In order to improve the flexibility on the LKr L0 trigger system, thanks to the high density level of the last generation FPGA devices, we propose an architecture where, on a single device, the embedded processors can coexist together with some proprietary and custom VHDL modules. In this way, the parallel custom circuital module will receive the data samples from the CREAM and it will able to filter them with over threshold, peak in space and peak in time criteria. The "peak in time detection" event will give the start to the algorithm, implemented in C on a proper tailored embedded processor, that will reconstruct the energy-deposition peak on calorimeter. Finally, the occurrence time, the position and the energy will be proper coded to be sent to the custom Gigabit link and then to the first Concentrator. The possibility to fulfil the algorithm, or parts of it, on an embedded processor, that is programmable in high level programming language like C, makes the development and maintenance phases more feasible. Moreover the embedded processors are themselves customizable, which adds further flexibility to the architecture. This mixed architecture, custom VHDL together with Soft Core Embedded processor, allows to develop an efficient and at the same time flexible fast computation.

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