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Test Results of the first 3D-IC Prototype Chip Developed in the Framework of HL-SLHC/ATLAS Hybrid Pixel Upgrade

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To face new challenges brought by the upgrades of the Large Hadron Collider at CERN and of ATLAS pixels detector, for which high spatial resolution, very good signal to noise ratio and high radiation hardness are needed, 3D Integrated Technologies are investigated. Commercial offers of such technologies are only very few and the 3D designer's choice is as a consequence strongly constrained. We present here the test results of the first 3D prototype chip developed in the GlobalFoundries 130 nm chips processed by the Tezzaron Company, submitted within the 3D-IC consortium for which a reliable qualification program was developed. Reliability and influence on the integrated devices behavior of Bond Interface (BI) and Through Silicon Via (TSV) connections, both needed for the 3D integration process, has also been addressed by the tests.

Summary

A major upgrade of the ATLAS pixel detectors in the innermost layers is required for HL-LHC on a 10-year timescale. The detector should operate with luminosity of L= 1035 cm-2 s-1, which is ten times higher than the nominal LHC luminosity. For the pixel B-layer at 3.5 cm radius this will correspond to a major increase in occupancy and to a total fluence of 2 x 1016 cm-2 of 1 MeV neutron equivalent. The improvement in the segmentation of the pixel detectors will then be critical for the success of the upgrade. The ATLAS pixel collaboration has started R&D work to use the latest advances in high density and 3D electronics technology in order to develop a new FE chip (FE-TC4). In addition to IC design, an important part of the work consists in radiation testing.

The basic idea of the FE-TC4 is to split the existing FE-I4 baseline pixel into two tiers (floors): The first tier with analog part and corresponding controls and the second tier with remaining digital part. The aim is to reduce the pixel size in longitudinal direction by a factor of two to reach a pixel size of 50 x 125 microns, while at the same time increasing the digital memory per pixel. The chip size is 19 x 20 mm and will have a rate capability and radiation tolerance appropriate for SLHC pixels.

The 3D FE-TC4_P1 demonstrator chips, which have a small pixel matrix of 61x14 pixels of the size 50 µm x 166 µm and additional 3D test purpose chips were produced in March 2010 in the first multi-project Tezzaron-GlobalFoundries run.
In a first step, we received each individual tier on February 2011 and tested them separately. We have showed that the 3D process did not modify the electrical performances and the radiation hardness of the dies.
In a second step, we received the last batch of 3D assemblies FE-TC4_P1 chips during the summer 2012, and tested them, showing a very good communication between tiers, despite a very bad yield.
The 3D test chips have also been tested to qualify the interconnection technology. These chips have high number of daisy chained interconnections (both BIs and TSVs) and test transistors placed at different distance from the TSV.
The next step should be the test of the chip after bump-bonding to a silicon sensor in order to test the compatibility and yield after bump-bonding. Another important issue to address is the possibility to wire-bond on a very thin tier, up to the sensitive area of the second tier.

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