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A prototype hybrid pixel detector ASIC for the CLIC experiment

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A prototype hybrid pixel detector ASIC whose design is tuned to the requirements of a vertex detector for CLIC is described and first electrical measurements presented. The chip has been designed using a commercial 65 nm CMOS technology and comprises a matrix of 64 x 64 square pixels each measuring 25 um on the side. The main features include simultaneous 4-bit measurement of Time-over-Threshold (ToT) and Time-of-Arrival (ToA) with 10 ns accuracy, on-chip data compression scheme and power pulsing capability.

Summary

CLIC is a high energy linear particle accelerator which is currently under study at CERN. The requirements of its vertex detector concerning material budget, spatial resolution and, in particular, time stamp precision led to the design of a prototype hybrid pixel detector readout chip. A 65 nm low-power CMOS technology was chosen for the design. Preliminary studies were carried out at CERN to evaluate the radiation hardness of the technology [1]. A prototype fully featured chip with a matrix of 64 by 64 pixels was fabricated and tested. The pixel dimensions are 25 x 25 umˆ2 pixels, allowing a subpixel spatial resolution of 3 um. Each pixel contains an analog front-end consisting of a preamplifier with a Krummenacher feedback network [2], a fast comparator and a 4-bit Digital-To-Analog converter for threshold equalization. Each pixel can measure 4-bit Time over Threshold (TOT) and 4-bit Time of Arrival (TOA) simultaneously, with a pulse counting mode available for calibration purposes. The time-stamping accuracy is 10 ns due to a 100 MHz acquisition clock being broadcast to all pixels during the acquisition phase. In order to reduce crosstalk and noise, this clock is sent to each pixel with a different phase, using the delays of the clock buffers to implement this solution. All digital circuits were implemented with standard IP cells from the foundry and high-Vt (low-power) cells were used for low-speed circuits.

The readout is frame based, i.e. the data is read out from the chip after the acquisition and between CLIC pulse trains. To minimize the readout time and the power consumption, a configurable data compression scheme is implemented directly on-chip, allowing to skip the readout of pixels (or groups of pixels) without a valid hit. Simulations show that this solution is optimal for an expected occupancy of between 2% and 5%. The readout uses a single data line with a global 320 MHz clock, which is gated to each pixel column to minimize power consumption.

Due to the low power requirement of the vertex detector (less than 50 mW/cmˆ2), a power pulsing feature has also been implemented. Most of the analog structures in the pixel can be switched to a low power consumption state after the data acquisition has been completed. In order to minimize sudden changes in total power consumption, the power on/off of the array is applied one pixel column at a time, with configurable a delay between columns.

Electrical characterization has been done using a custom PCB connected to an FPGA for automated testing. Test results will be presented.

[1] S. Bonacini, P. Valerio, R. Avramidou, R. Ballabriga, F. Faccio, K. Kloukinas, and A. Marchioro. “Characterization of a commercial 65 nm CMOS technology for SLHC applications”. Journal of Instrumentation, 7(01):P01015–P01015, January 2012.

[2] F. Krummenacher. “Pixel detectors with local intelligence: an ic designer point of view”. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 305(3):527 –532, 1991.

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