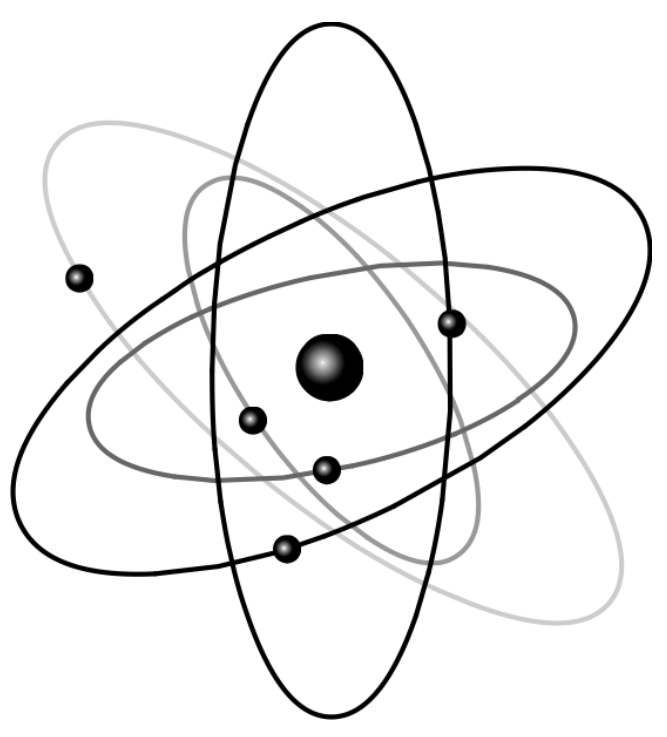


# DEVELOPMENT OF SCALABLE FREQUENCY AND POWER PHASE-LOCKED LOOP (PLL) IN 130NM CMOS TECHNOLOGY



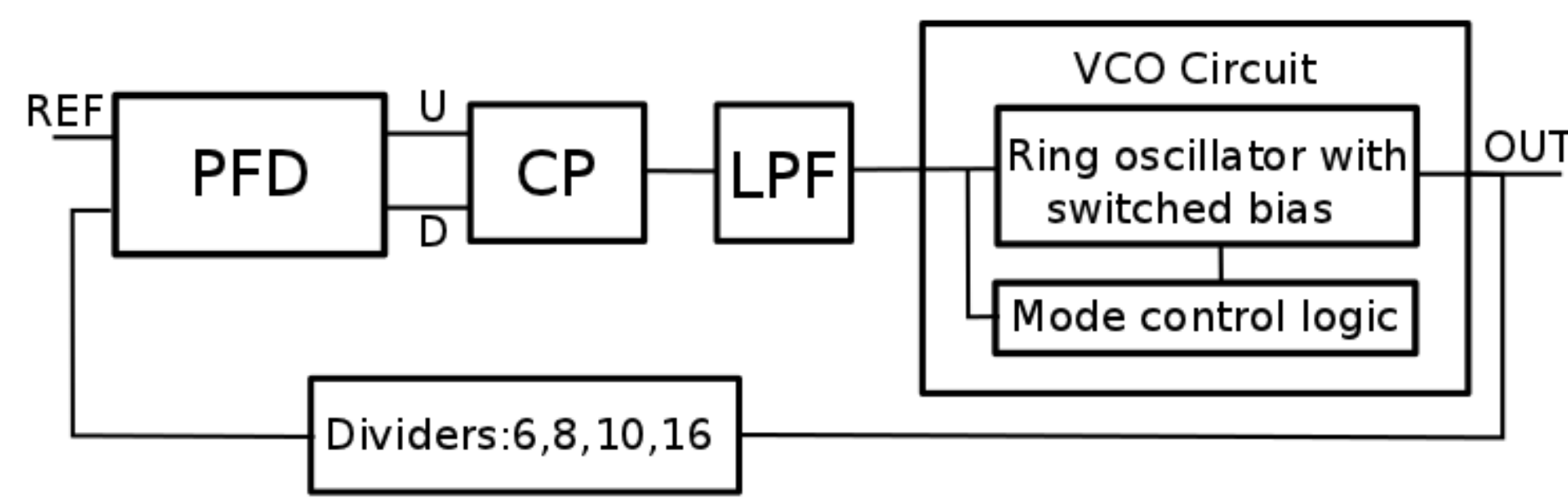
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## INTRODUCTION

In modern and future detector systems of particle physics experiments data serialization and subsequent transmission becomes increasingly important, particularly in the context of continuously growing number and density of read-out channels. The serialization and data transmission aspects are currently under study for the luminosity detector at the future linear colliders (ILC/CLIC) and for strip tracker readout in LHCb upgrade experiment. Since the readout architecture of these experiments comprises an ADC in each channel the data serialization from multi-channel ADC needs to be implemented. After that a fast power-efficient serial data transmission out of detector is required [1]. To allow two serialisation levels a variable frequency range PLL with different clock division factors is required. In this work we discuss the development of the key block for serialization and data transmission i.e. the PLL.

## PLL ARCHITECTURE

A standard second order Phase-Locked Loop architecture was chosen for the PLL design. It contains a Phase and Frequency Detector (PFD), a Charge Pump (CP), a Low Pass Filter (LPF) and a Voltage Controlled Oscillator (VCO) [2].

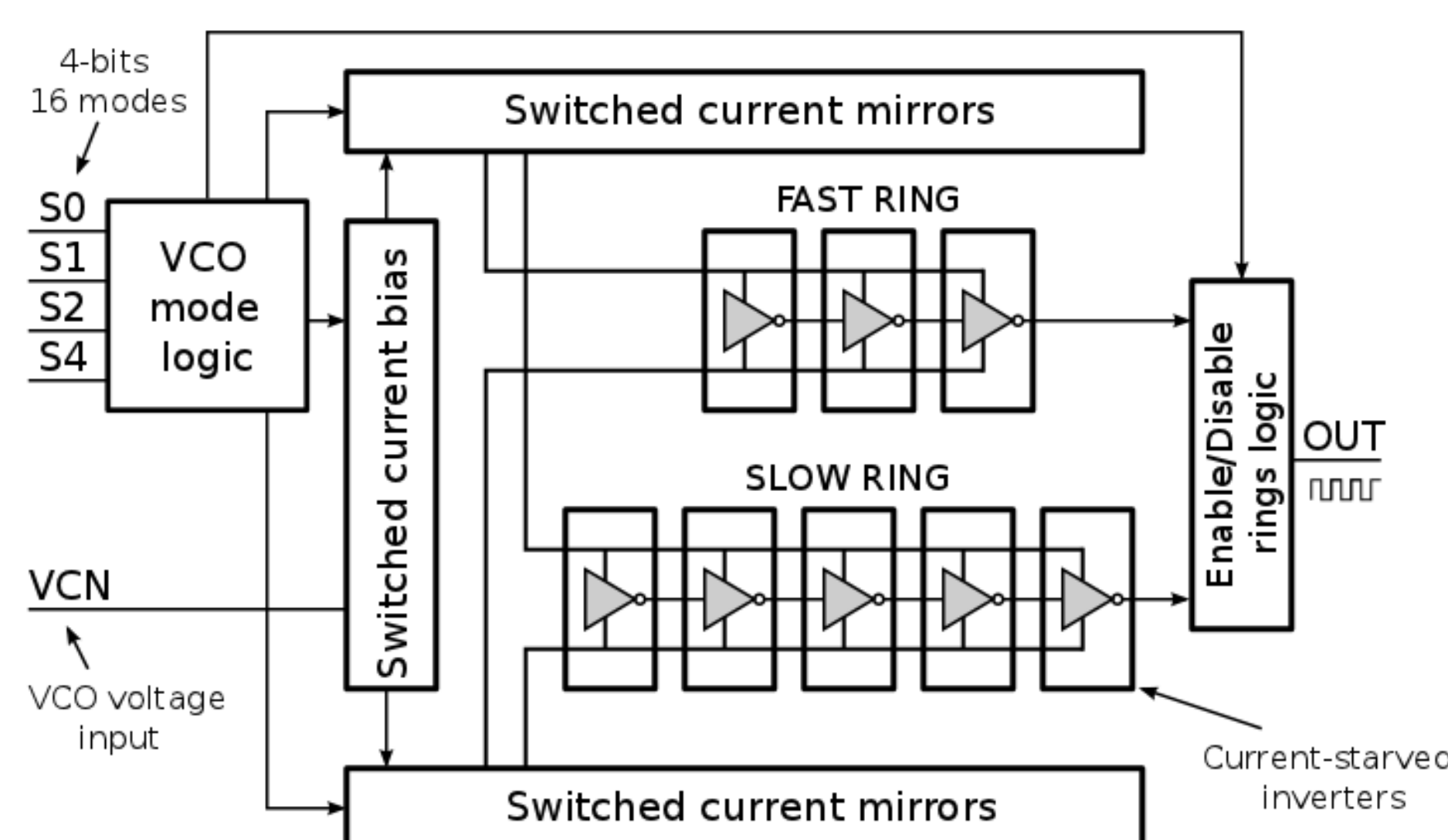


Variable clock division factors 6, 8, 10 or 16 are implemented in PLL feedback loop making it more flexible. For instance it may be used to serialise output bits from 6, 8 or 10-bit ADC. The design was optimized for highest clock frequency and lowest power consumption. The simulations show that PLL should work up to 3.5 GHz.

The PLL was fabricated in IBM 130 nm technology. It occupies  $300 \mu\text{m} \times 300 \mu\text{m}$ .

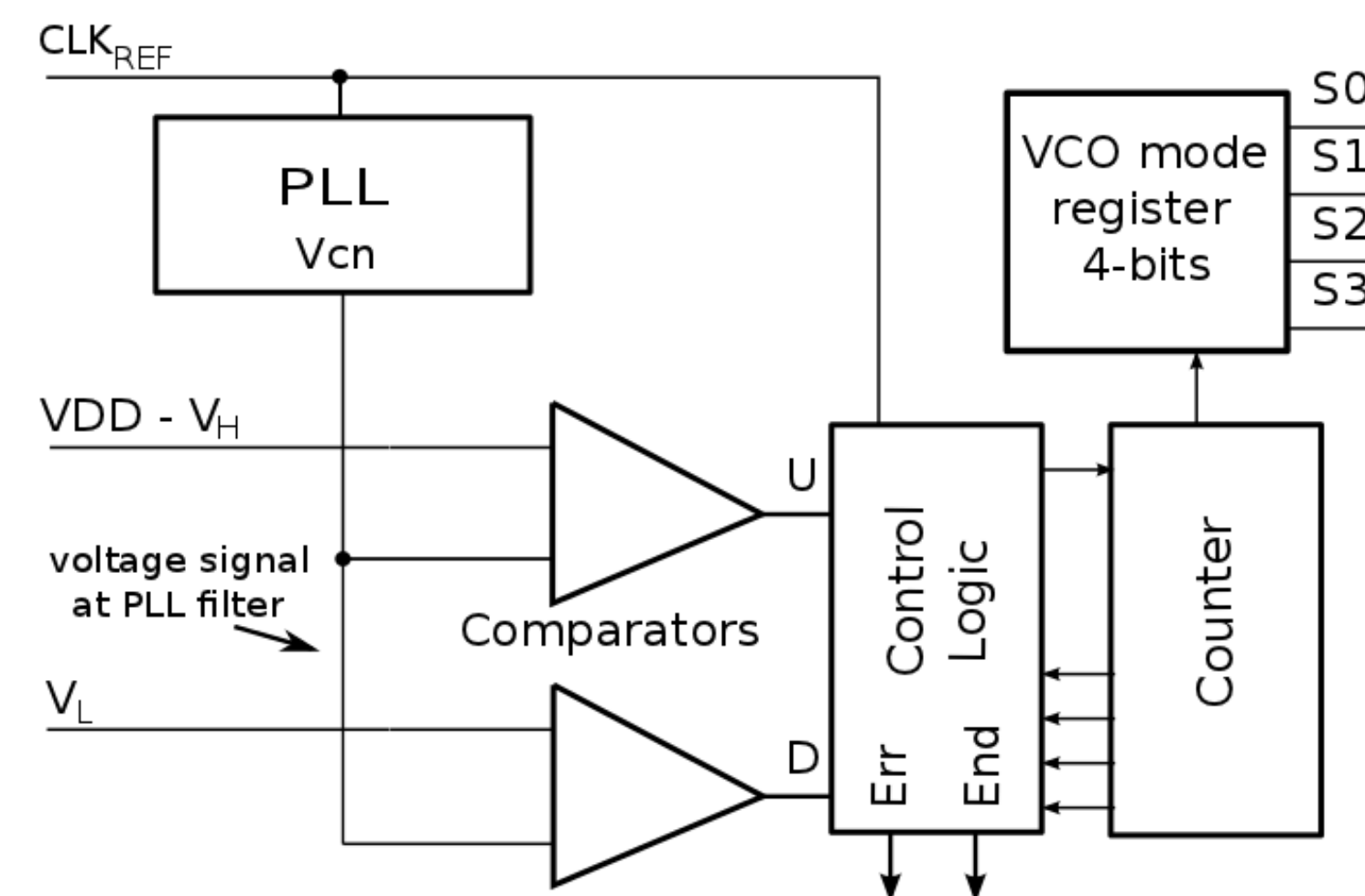
## VCO ARCHITECTURE

To obtain the highest frequency and the lowest power, VCO contains two separate oscillator rings, with different number of delay elements. The "current starved" inverters were used in the VCO design [3].



The VCO operates in 16 modes for which different oscillator rings and bias currents are used. The VCO mode logic, depending on the selected mode, switches the multiplication factor in current mirrors, controls the current bias gain and enables/disables the oscillator rings.

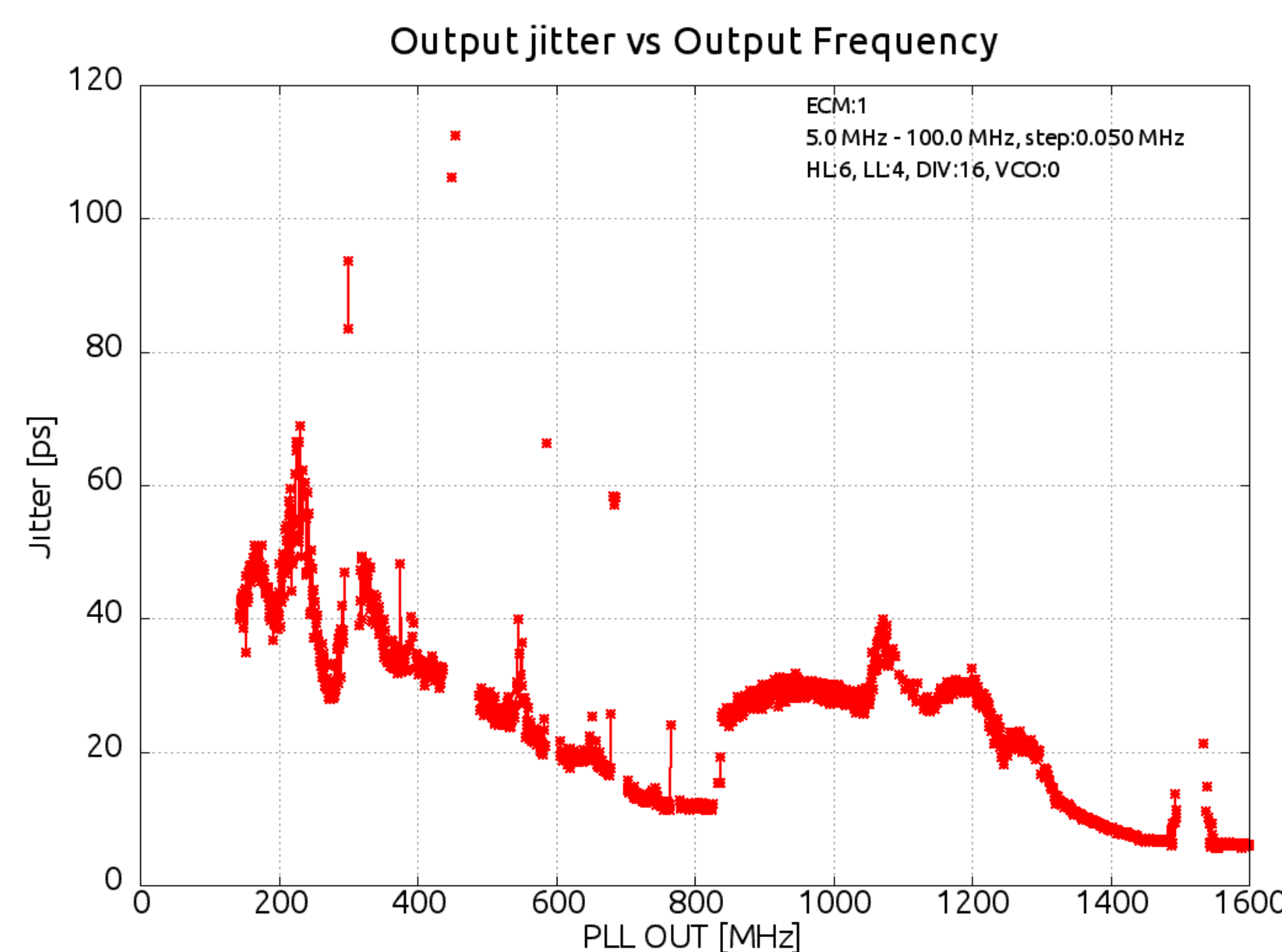
## AUTOMATIC VCO MODE SET



Comparators check whether PLL filter signal  $V_{cn}$  is greater than  $V_{DD} - V_H$  or lower than  $V_L$ . If  $V_{cn} > V_{DD} - V_H$  (VCO too slow) the mode register is switched to faster mode. If  $V_{cn} < V_L$  (VCO too fast) the VCO mode register is switched to slower mode. When  $V_{cn}$  voltage is between  $V_{DD} - V_H$  and  $V_L$  the mode is not changed.

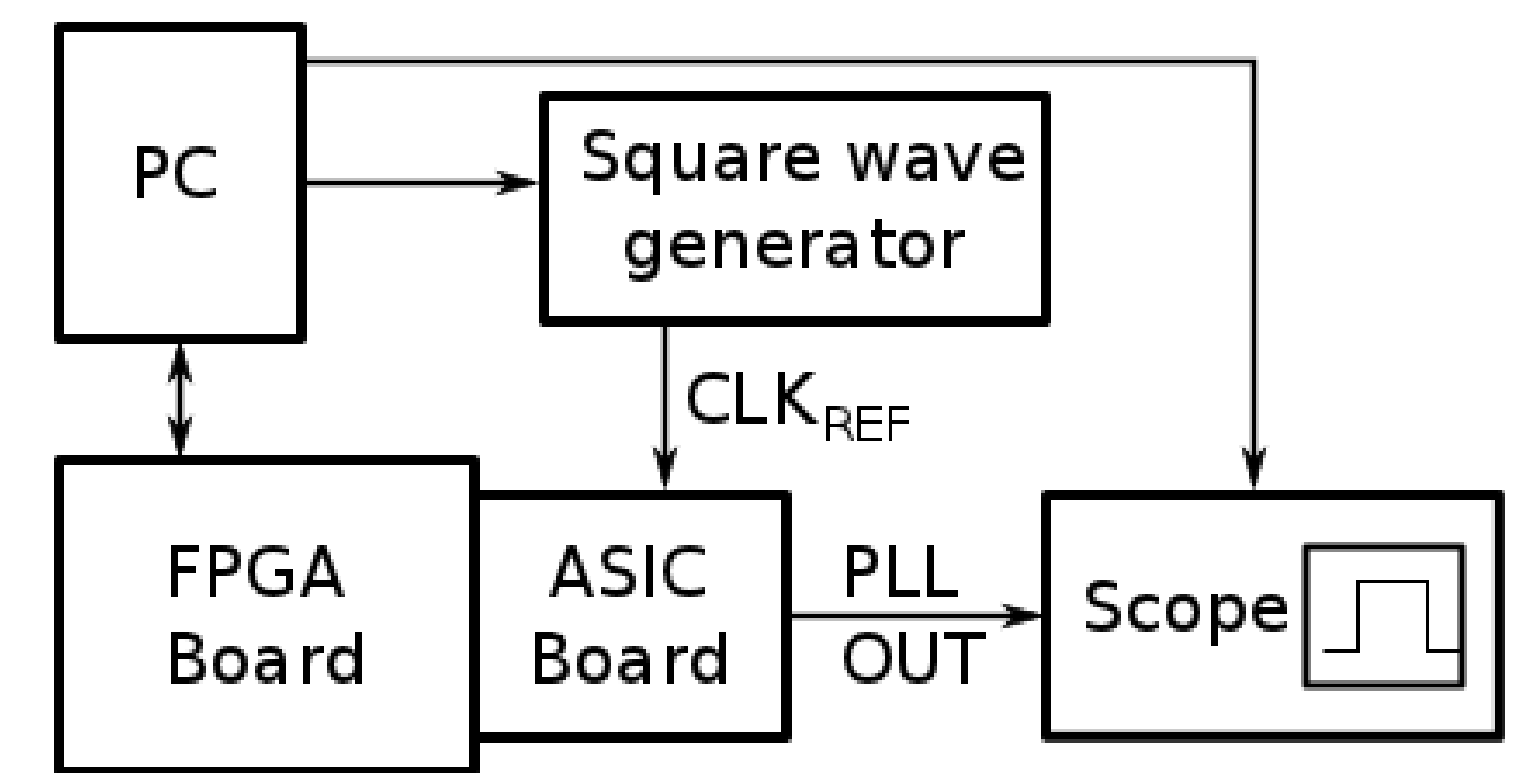
## MEASUREMENTS RESULTS

The measurements were done at default 1.2 V power supply in the frequency range 20 MHz - 1.6 GHz. Right plot confirms the proper circuit operation. There are few gaps in the whole PLL frequency range - VCO modes do not overlap - this does not agree with post-layout simulations and need to be corrected for next submission. The curves in the plot show that all four division factors work properly. Automatic mode change was positively verified.



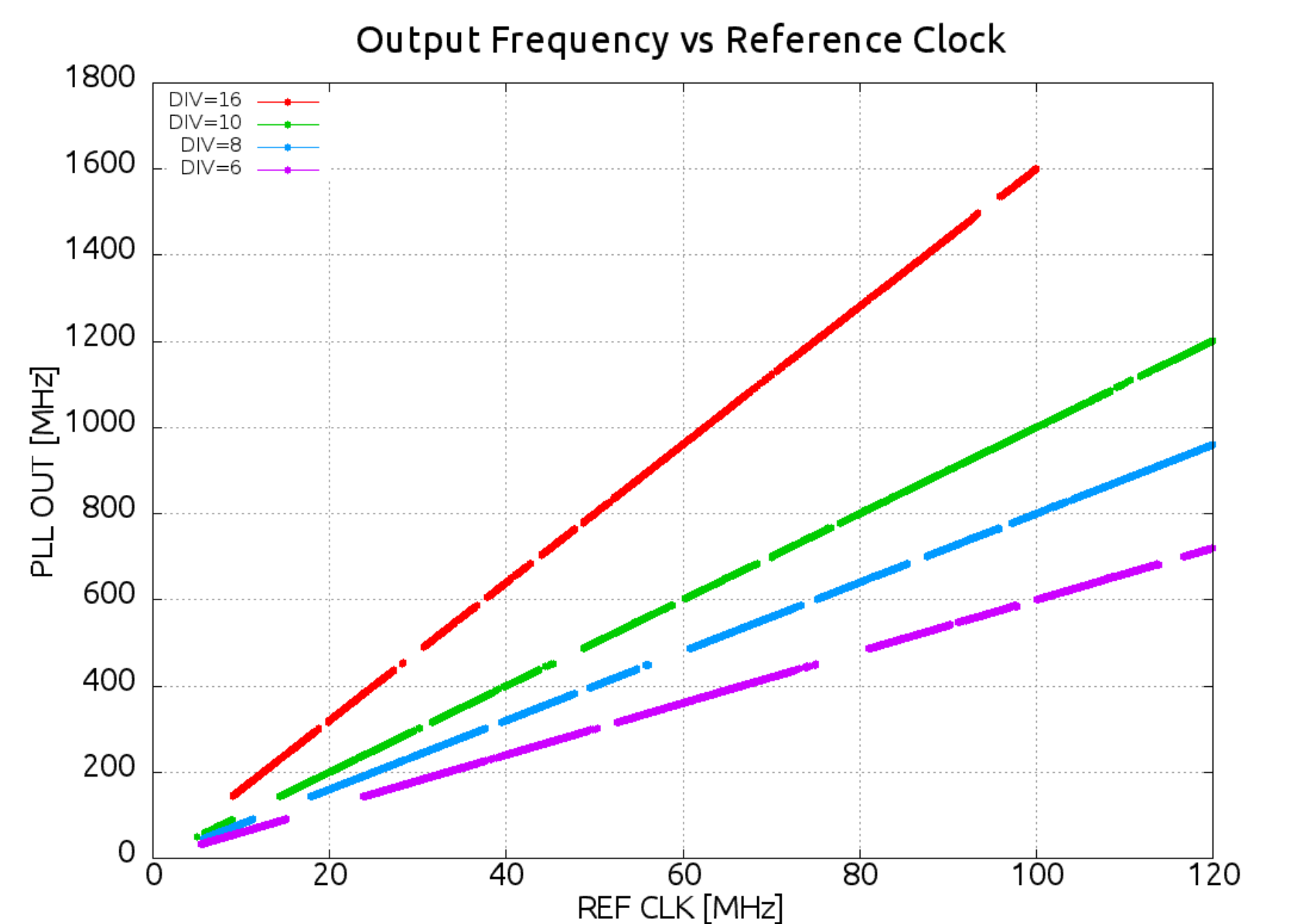
The power consumption was measured at the default 1.2 V supply voltage, and for division factor equal 16. As seen on the right plot, it scales linearly with PLL clock frequency for each specific VCO mode. At 1 GHz the PLL consumes around 0.6 mW.

## MEASUREMENT SETUP

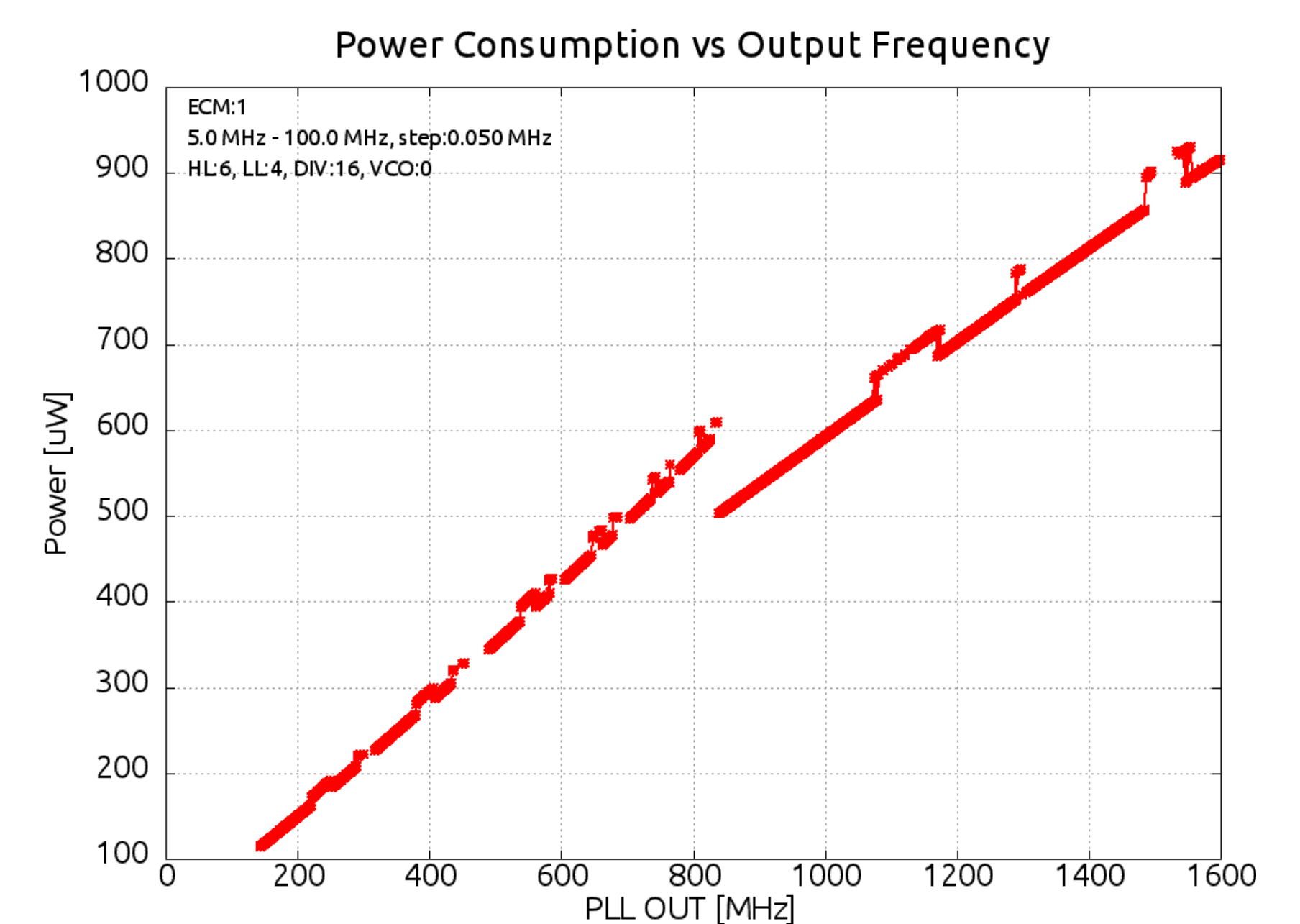


Setup used for PLL measurements contains:

- Test board containing: ASIC, clock buffers, voltage regulators and current bias circuitry, digital level converters
- FPGA board, controlled by PC, was used to configure ASIC via slow control interface
- Square wave generator (Agilent 81150A)
- 40GSps scope (Agilent DSA90804A)



The jitter (left plot) was measured as standard deviation of PLL time period. The obtained jitter values (15-70 ps), although sufficient for foreseen applications, are higher than expected and will be carefully studied for next submission. These results were measured for division factor equal 16 but other dividers give very similar results.



## SUMMARY AND FUTURE PLANS

A wide frequency range, low power PLL, with automatic VCO mode switching, was designed, fabricated and tested. The measurements show that the PLL is fully functional in frequency range 20 MHz - 1.6 GHz and the automatic switching works correctly. Very low power consumption (0.6 mW @1 GHz) was measured. To build a general purpose PLL few issues need to be improved in next prototype fabrication:

- The gaps in PLL frequency range should be eliminated
- The PLL jitter should be reduced
- Faster I/O needs to be design to verify higher PLL frequencies

## ACKNOWLEDGMENTS

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- [3] S. Moorthi, D. Meganathan, M. Shankar, R. Sridhar, J.R.P. Perinbam, A low-jitter phase-locked loop architecture for clock generation in Analog to Digital Converters. RAICS, 2011 IEEE