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# Development of variable frequency, power Phase-Locked Loop (PLL) in 130nm CMOS technology

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The design and measurements results of low power Phase-Locked Loop (PLL) prototype for applications in particle physics detectors readout systems are presented. The PLL fabricated in 130nm IBM technology was designed and simulated for frequency range 10MHz-3.5GHz. Internal voltage controlled oscillator (VCO) should work in 16 frequency ranges/modes, switched either manually or automatically. Preliminary measurements done in frequency range 20MHz-1.6GHz showed that the ASIC is functional and generates proper clock. The PLL power consumption at 1GHz and division factor equal 10 is about 0.6mW. As one of main design goals the automatic VCO mode change was positively verified.

## Summary

In modern and future detector systems of particle physics experiments, the data serialization and subsequent transmission with highest possible rate and lowest power becomes increasingly
important, particularly in the context of continuously growing number and density of readout channels. The serialization and data transmission aspects are currently under study for the luminosity detector at the future linear colliders (ILC/CLIC) and for strip tracker readout in LHCb upgrade experiment. Since the readout architecture of these experiments comprises an ADC in each channel the data serialization from multichannel ADC needs to be implemented. After that a fast power-efficient serial data transmission out of detector is required. To allow two serialisation levels a variable frequency range PLL with different clock division factors is required.

In this work we discuss the development of the key block for serialization and data transmission i.e. the PLL. The design was optimized for highest clock frequency and low power consumption. The simulations show that PLL should work up to 3.5GHz. A standard second order Phase-Locked Loop architecture was chosen for the PLL design. It contains a Phase and Frequency Detector (PFD), a Charge Pump (CP), a Low Pass Filter (LPF) and a Voltage Controlled Oscillator (VCO). The “current starved” inverters were used in the VCO design. To obtain the highest frequency and the lowest power, VCO contains two separate oscillator rings, with different number of delay elements. The VCO operates in 16 modes for which different oscillator rings and bias current are used. Variable clock division factor equal 6,8,10 or 16 may be set in PLL feedback loop making the design more flexible. For instance it may be used to serialise output bits from 6, 8 or 10-bit ADC.

The full circuit was designed, simulated and fabricated in 130nm IBM technology. The PLL layout occupies 300um x 300um. The prototype measurements were done in the frequency range 20MHz-1.6GHz at default 1.2V power supply and showed the proper circuit operation. Due to setup limitations higher frequency modes were not verified. In these measurements the VCO modes were switched manually. In the next step the automatic mode change was also positively verified in the same frequency range. It was also verified that all clock division factors are working properly. For the default 1.2V power supply, division factor equal 10 and at 1GHz PLL clock the measured power consumption was about 0.6mW. The power consumption scales linearly with PLL clock frequency at specific VCO mode. Power consumption to frequency ratio is smaller for higher frequencies, and depends on currently activated oscillator ring.

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