AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Development of variable sampling rate low power 10-bit SAR ADC in 130 nm IBM technology

Jakub Moroń,
M. Firlej, T. Fiutowski, M. Idzik, Sz. Kulis, K. Swientek
AGH-UST

Faculty of Physics and Applied Computer Science
AGH University of Science and Technology

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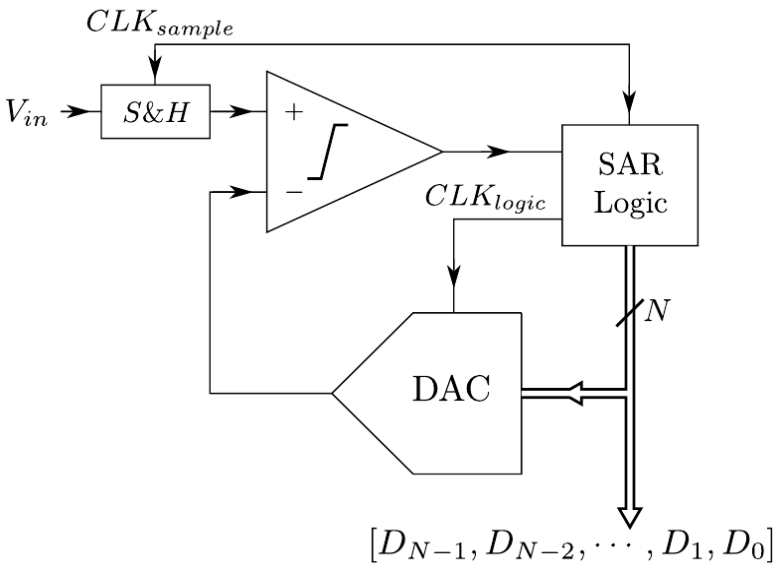
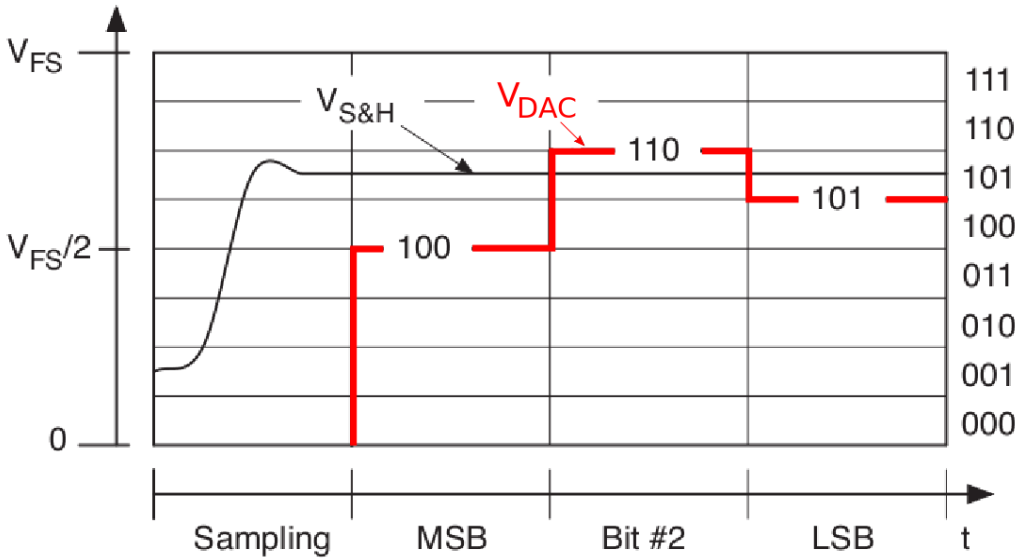
Agenda

- Successive Approximation Register (SAR) architecture
- Key aspects of DAC in SAR ADC:
  - Capacitance switching schemes
  - Split DAC architecture
- Design of SAR ADC
- Performance measurements of prototype ADC:
  - Theory of dynamic measurements
  - Measurement setup
  - Results of static and dynamic measurements
- Summary and future plans

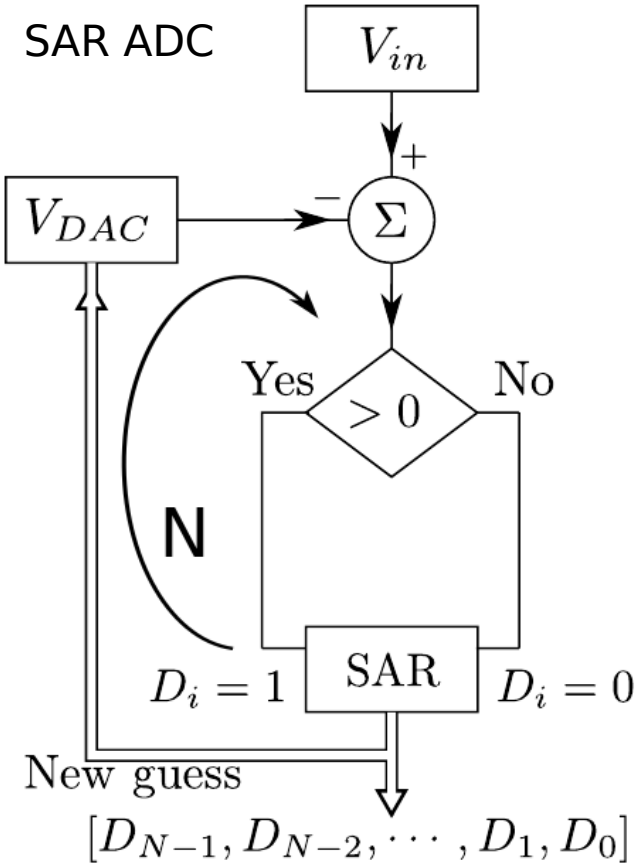
SAR architecture
Fundamentals of operation





- Comparison between sampled input voltage and reference DAC output voltage
- Comparison result → change reference DAC output voltage closer to input sample
- Each consecutive voltage change is half of the previous one
- Operation is repeated N times for N-bit ADC

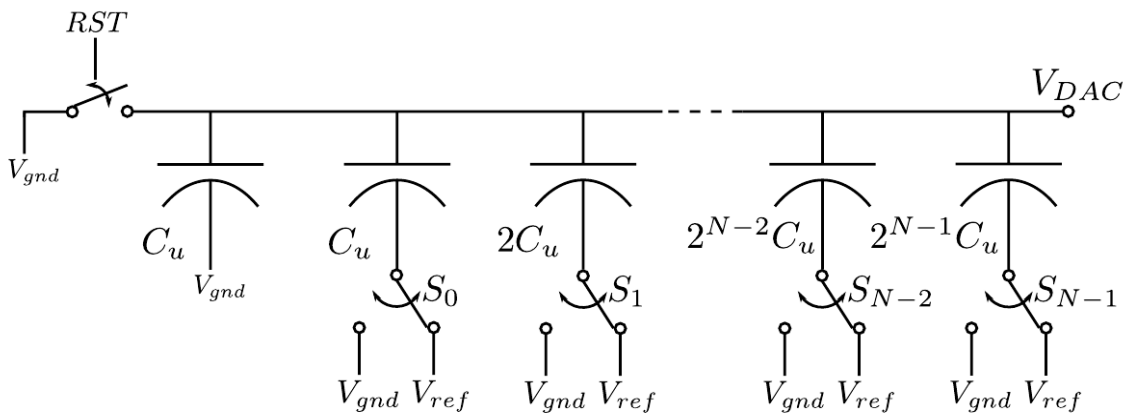
SAR architecture
Advantages and disadvantages



+ Power and area-efficient architecture – ***same circuitry is used in loop N-times***

+ SAR ADC contains: single comparator, two DACs (differential) and SAR logic – ***fits well to modern digital CMOS technologies***

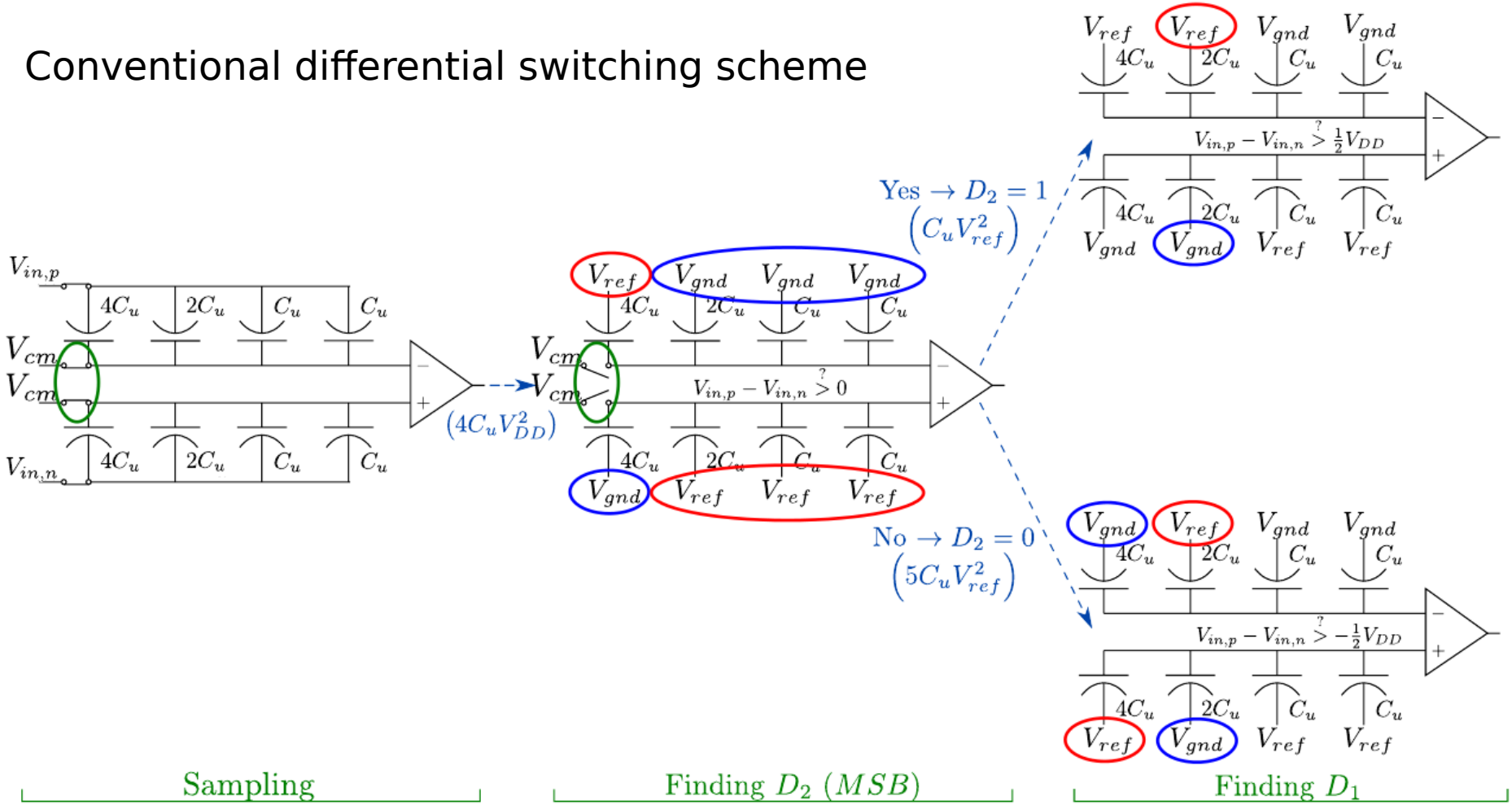
+ DAC network is usually capacitive - ***no static power, serves also as S/H circuit***



– Limited sampling rates – ***but with modern CMOS technology (~100nm) above 100MSps 10-bit ADCs are reported***

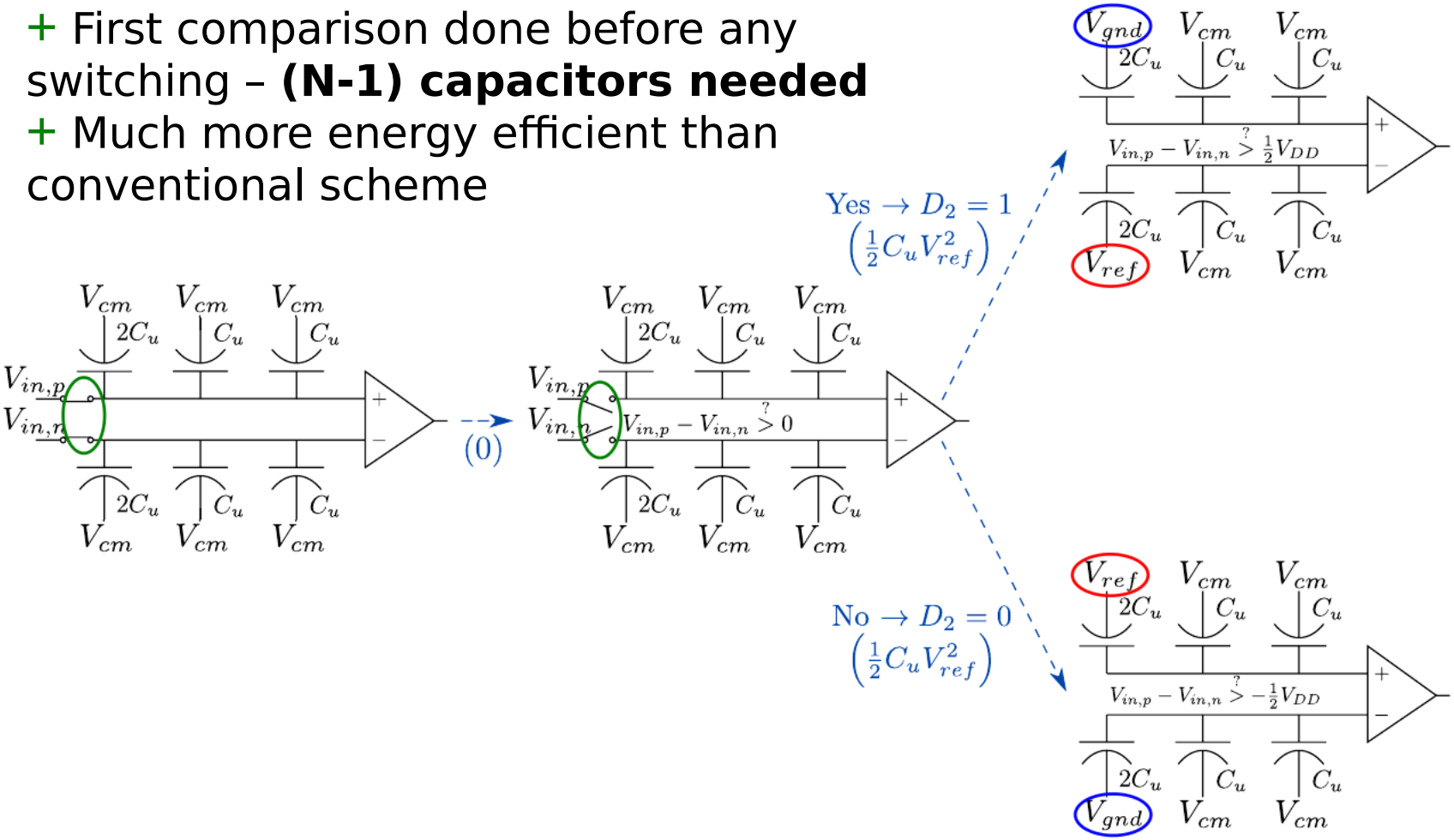
Key aspects of DAC in SAR ADC: Differential DAC switching scheme and energy

Conventional differential switching scheme



Key aspects of DAC in SAR ADC: Merged Capacitor Switching (MCS) scheme Chosen architecture

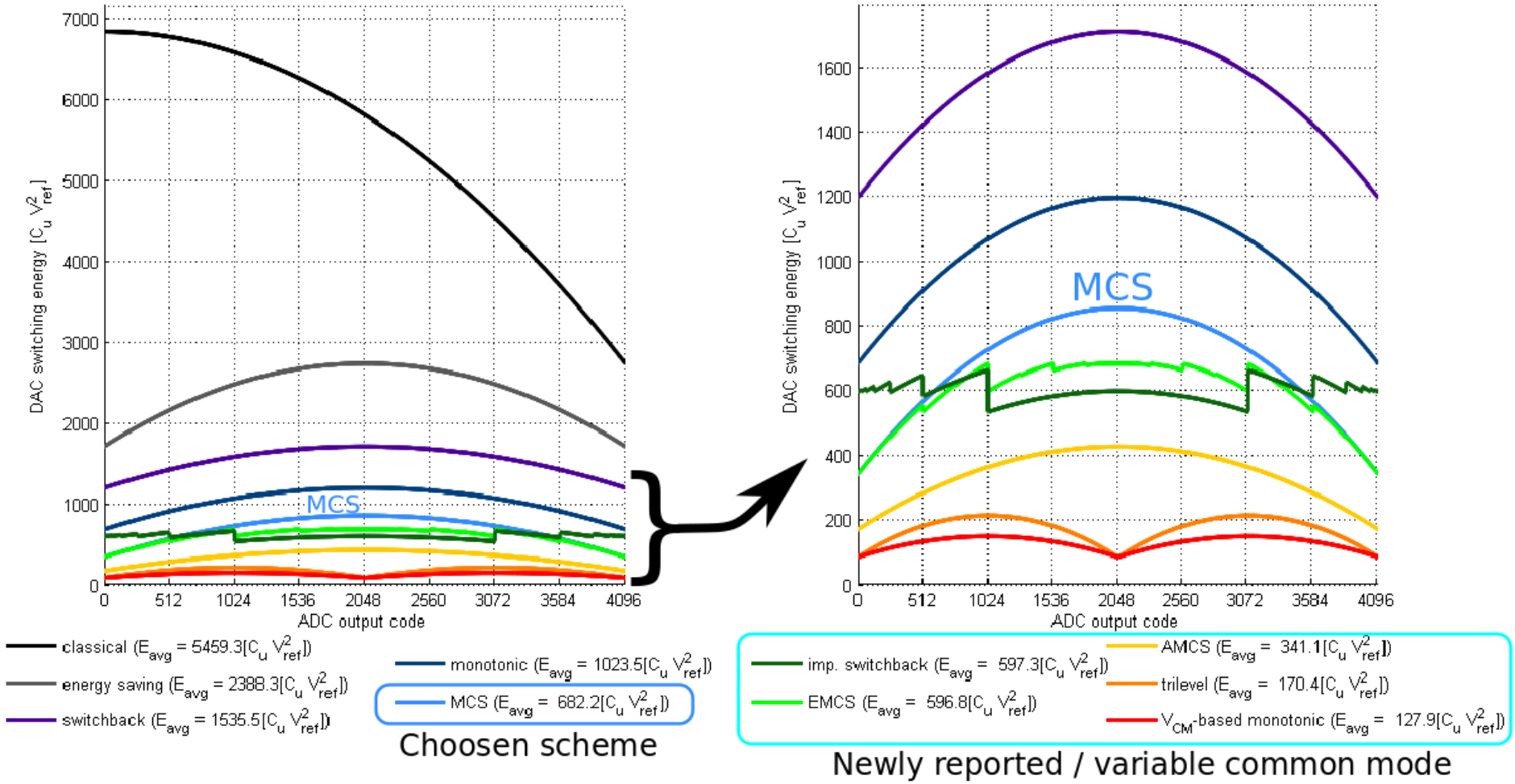
+ First comparison done before any switching – **(N-1) capacitors needed**
+ Much more energy efficient than conventional scheme



Key aspects of DAC in SAR ADC
DAC switching energy:
Various SAR configurations.

- With CMOS technology scaling digital power consumption is decreasing rapidly - so minimizing analog power (DAC, comparator) is of main interest
- Huge progress has been obtained in the last ~10 years in optimizing capacitive DAC configurations and their switching schemes
- Various DAC switching configurations were proposed
  - **Conventional (100% power consumption)**
  - 2 step switching (~10% power saving)
  - Charge sharing (~24% power saving)
  - Split capacitor (~37% power saving)
  - Energy saving (~56% power saving)
  - Set and down (~81% power saving)
  - Vcm-based (~87% power saving)
  - **Merge Capacitor Switching (MCS) (~93% power saving)**
  - During the last year some new were proposed (up to ~98% power saving)

Key aspects pf DAC in SAR ADC
DAC switching energy:
Switching scheme comparison



Key aspects of DAC in SAR ADC
Capacitors noise and matching considerations

Noise

- Thermal switch noise of sampling circuit – kT/C

$$\frac{kT}{C} < \frac{\sigma^2}{12}, \sigma = \frac{V_{ref}}{2^N}$$

$$C > 12\,kT\left(\frac{2^N}{V_{ref}}\right)$$

- For V_{ref}=1 V:

N=6 bits	C >	0.2 fF
N=8 bits	C >	3.3 fF
N=10 bits	C >	52.0 fF
N=12 bits	C >	830.0 fF

Switch noise is negligible

Matching

Capacitance density in IBM 130nm:

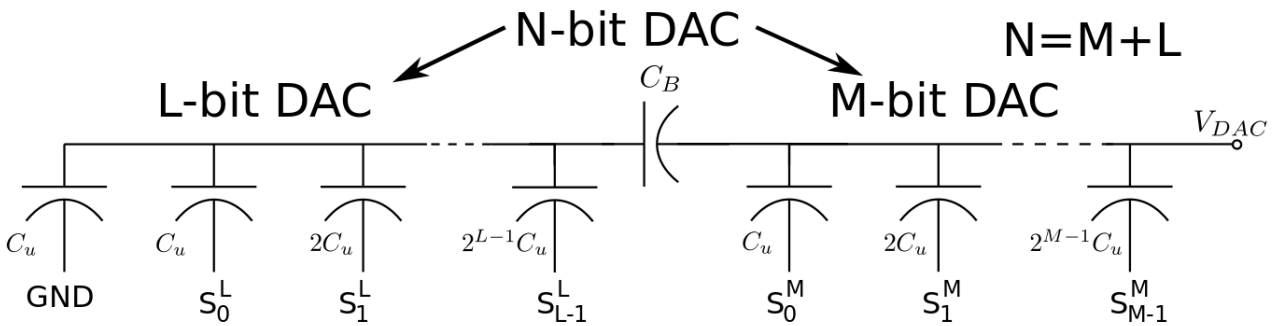
- VNCAP M1-M2 ~0.4fF/um^2
- MIMCAP ~2fF/um^2

Mismatch (%) at 3σ:

- VNCAP 10x20 μm^2 (~80fF): ~5%
- MIMCAP 6x7 μm^2 (~80fF): ~0.7%
- MOM – no model exist, matching unknown...

MIMCAP has high density and good matching

Key aspects of DAC in SAR ADC
Splitted DAC



- N-bit DAC splitted into two DACs connected via series unit capacitor

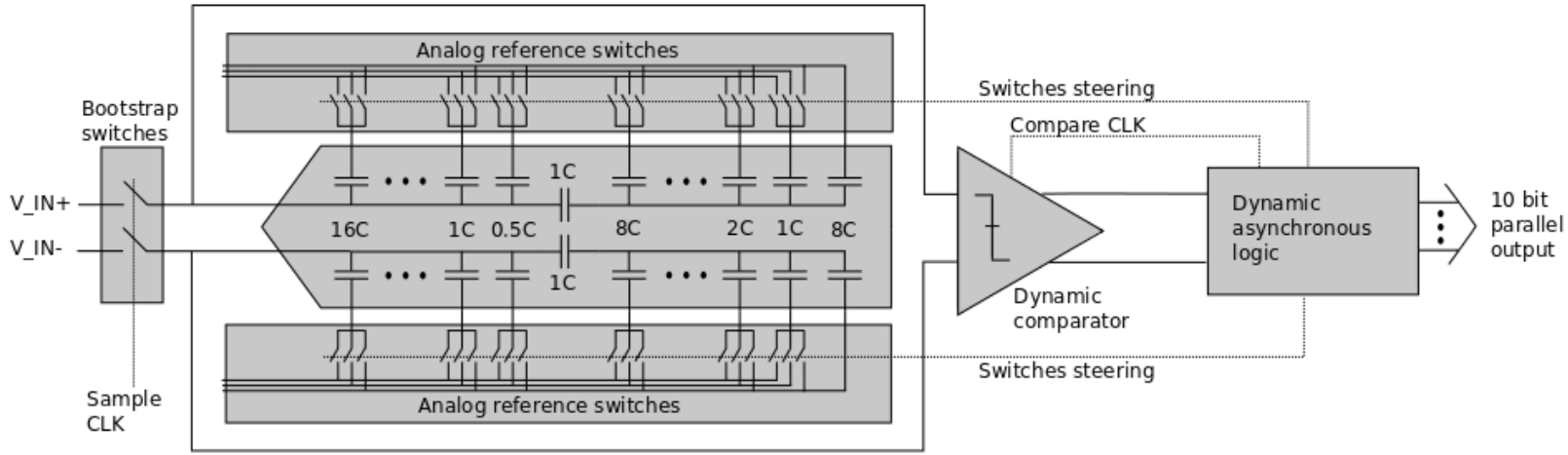
M	L	C_u [fF]	C_{total} [pF]	No. of C_u	~Area [μm²]
9	0	5.66 → 30	15.33	512	7079
8	1	11.29 → 30	7.65	257	3553
7	2	22.5 → 30	3.81	131	1811
6	**3**	**44.64**	**2.81**	**71**	**1461**
5	4	87.87	2.72	47	1903
4	5	170.07	2.55	47	3684
3	6	317.47	2.22	71	10388
2	7	544.24	1.63	131	32857
1	8	725.65	0.73	257	85947

- **C_u** – minimal unit capacitance ensuring 3σ matching within 0.5LSB Technology limit – two 60fF capacitor in series - 30fF

$$C_u = \frac{9}{2\sqrt{2}} 2^{2L}\left(2^M - 1\right) K_\sigma^2 K_C$$

$$K_\sigma = 4.12 \frac{\%}{\mu m} \qquad K_C = 2.05\,\mu m$$

Design of SAR ADC
Chosen architecture of 10-bit SAR ADC



Architecture of 10-bit ADC

- Differential segmented/split DAC with MCS switching scheme – ***ultra low power***
- Dynamic comparator – ***no static power consumption, power pulsing for free***
- Asynchronous logic – no clock tree – ***power saving, allows asynchronous sampling***
- Dynamic SAR logic – ***much faster than conventional static logic***

Design consideration:

- Variable sampling frequency (up to ~50 MS/s) and power consumption
- Power consumption 1-2 mW at 40 MS/s
- 146 µm pitch, ready for multichannel integration

Design of SAR ADC
Dynamic comparator

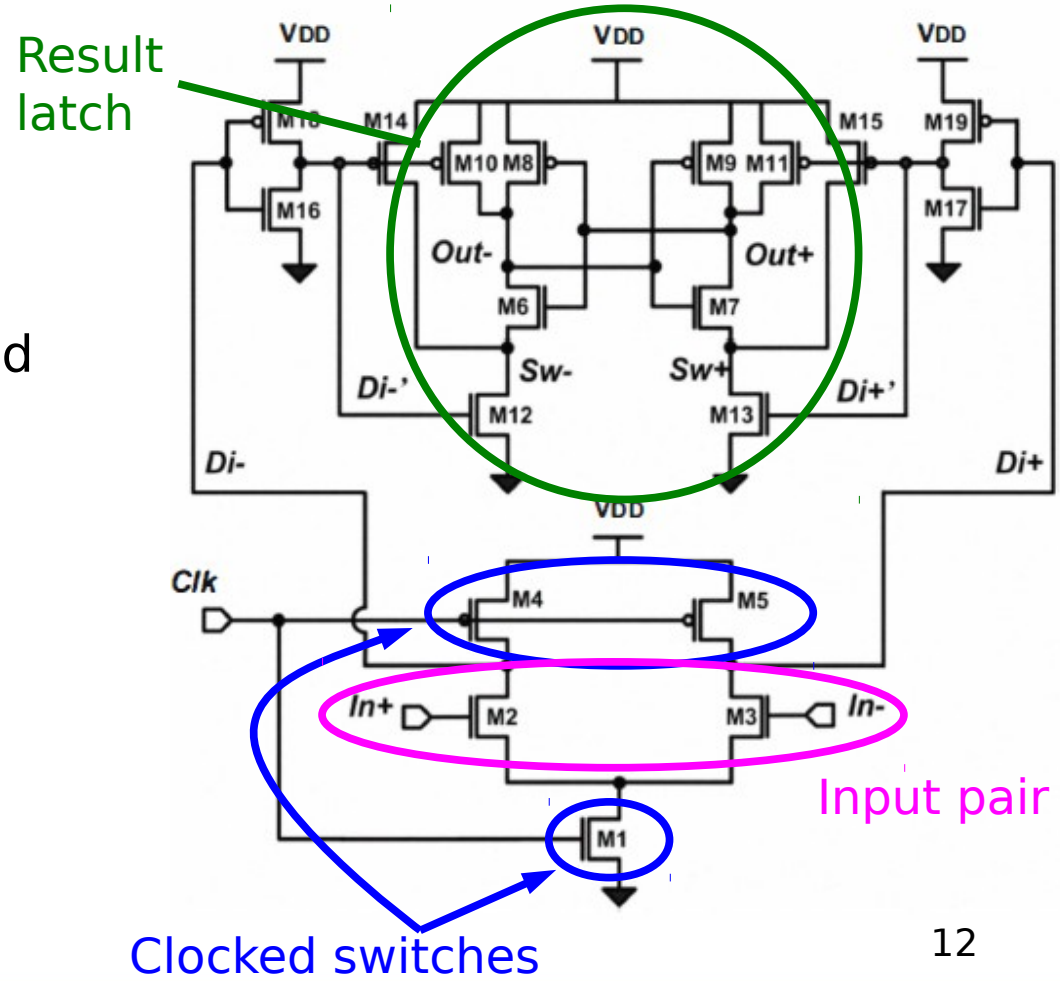
H.J. Jeon, Y-B. Kim, M. Choi "Offset voltage analysis of dynamic latched comparator", IEEE 54th Int. Midwest Symp. On Circuits and Systems, 2011

Dynamic comparator

- Comparison performed on rising edge of clock signal
- Reset (low clock level) needed before next comparison

Pros and cons:

+ No direct path current
+ Low power consumption
– Dead time needed for reset



Design of SAR ADC
Dynamic logic – idea of operation

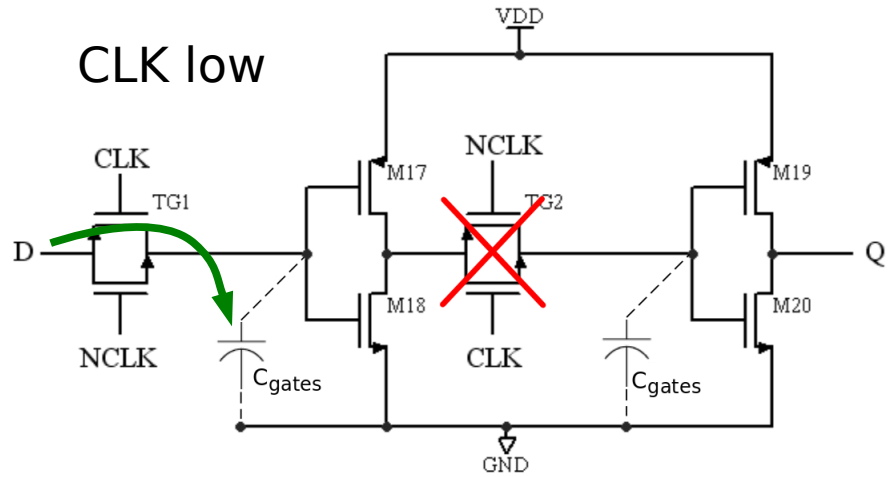
Dynamic D-type flip-flop:

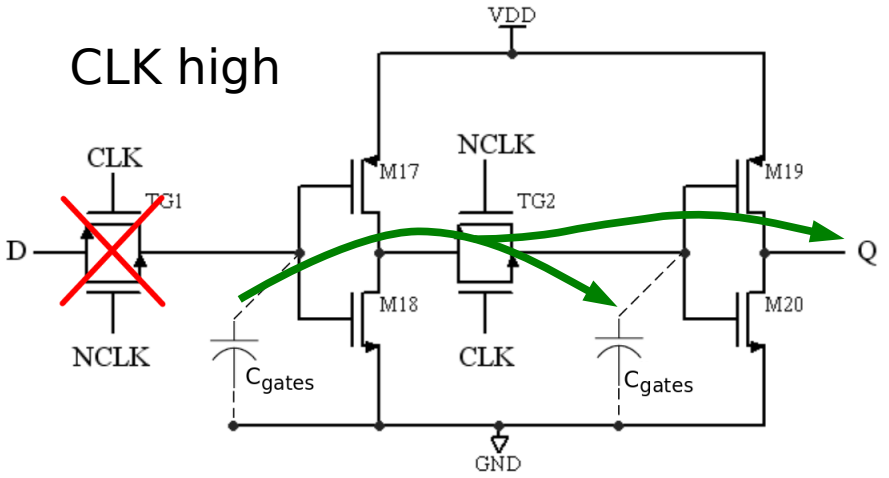
- Bit (voltage level) stored on inverter gate capacitance

+ Very fast - only two small transistor gates need to be recharged on each clock slope

– Clock needs to run continuously (or static reset is needed)

– Manual layout



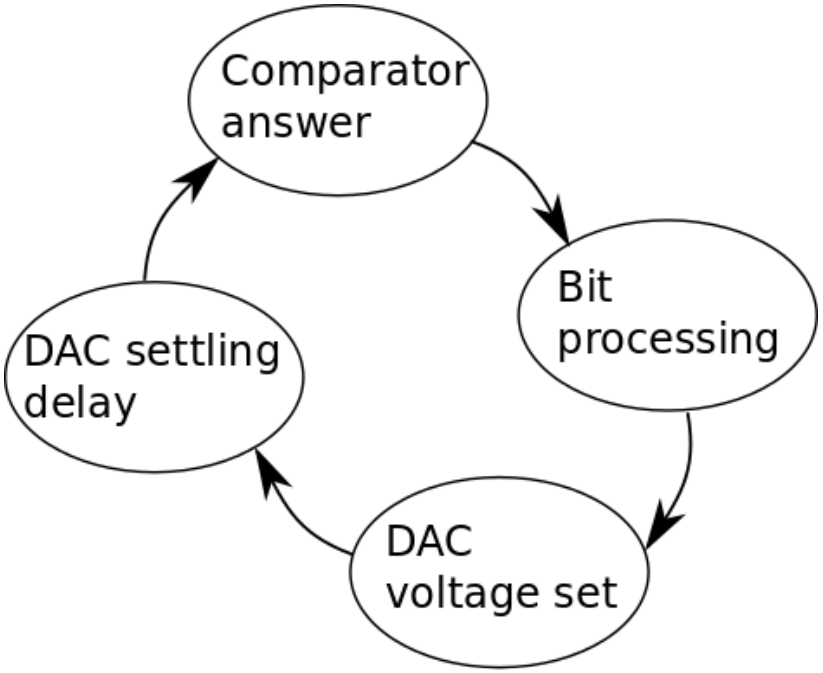


Flip-flop architecture	Signal propagation time [ps]	Power consumption [µW/clk cycle]
Static	155	2.62
Dynamic	**50**	**2.58**

Dynamic flip-flop is 3 times faster

Design of SAR ADC
Asynchronous logic – no fast clock distribution

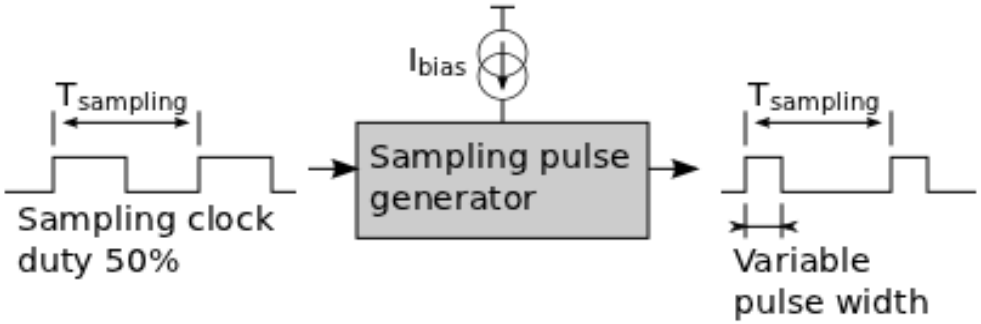
- To operate at 40MS/s 10-bit ADC have to convert single bit in approximately 2ns
- Each bit conversion require at least two clock cycles – generation and distribution of 1GHz clock is needed for synchronous operation
- Asynchronous logic → data flow releases actions in sequence

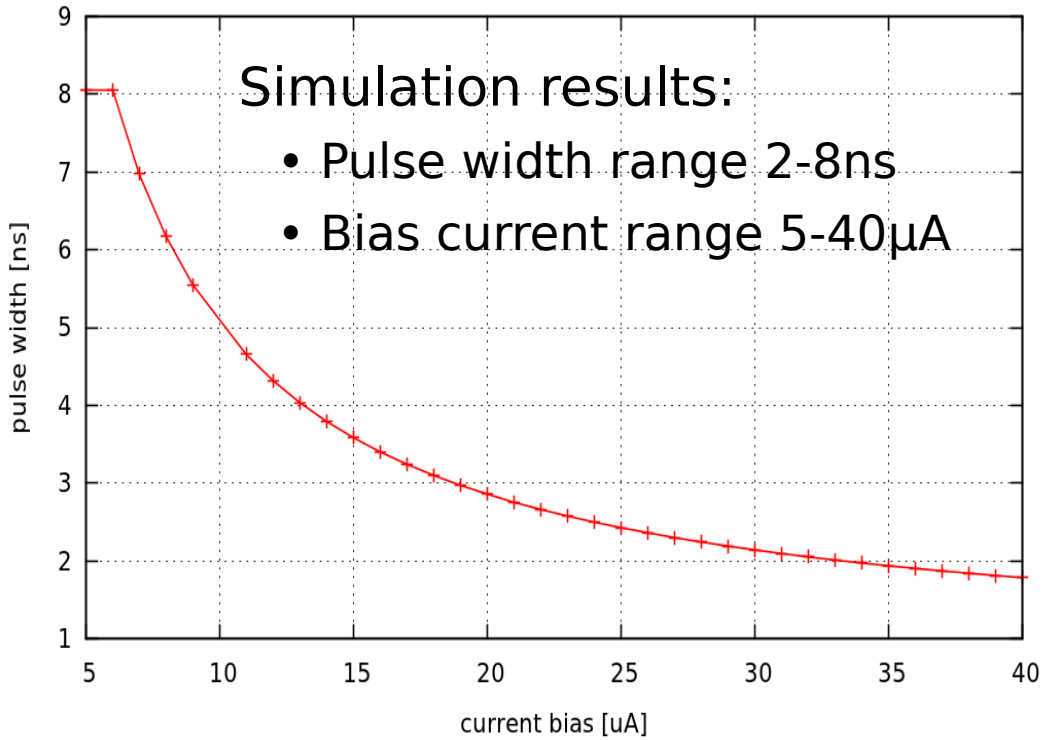


+ No fast clock distribution needed – a lot of power saved

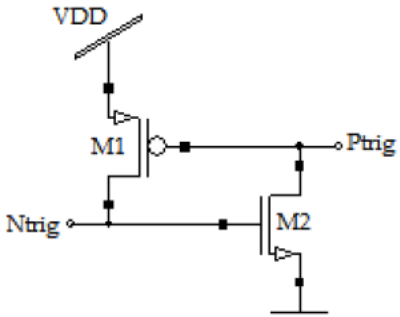
+ Single slope of sampling signal starts the conversion → ADC can operate in **asynchronous mode**

Design of SAR ADC
Design of sampling pulse generator



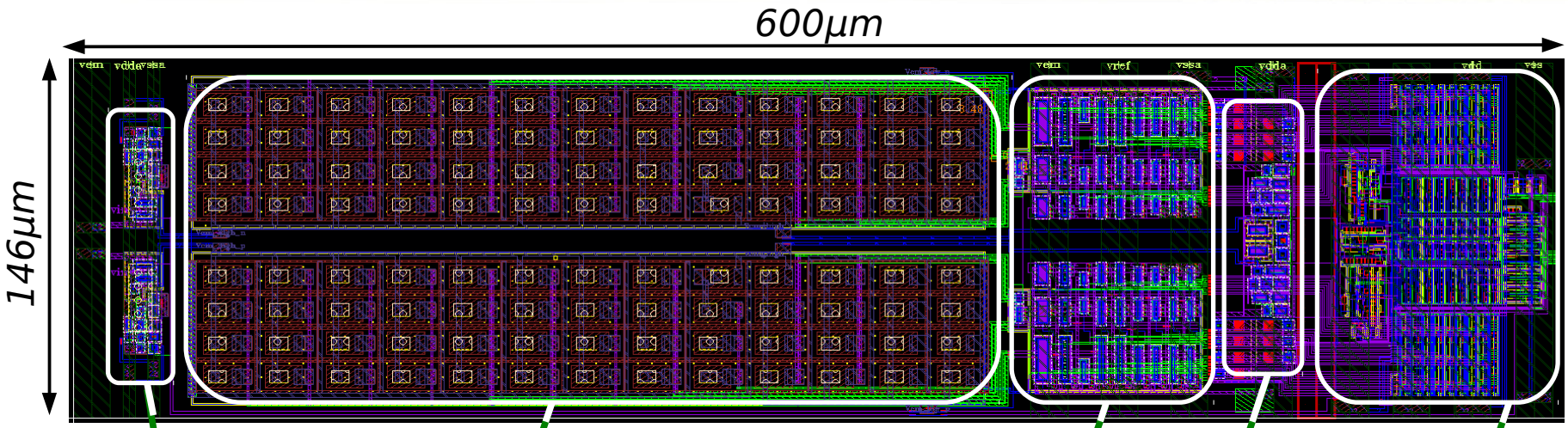


Generator of sampling pulse converts 50% duty external sampling clock into internal variable width pulse (controlled by I_{bias})

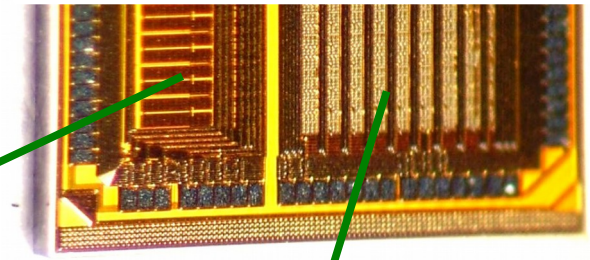


Pulse generator design is based on MOS thyristor delay circuit.

Design of SAR ADC
Channel layout



- Prototype channels fabricated to prove the performance
- Design ready for multichannel ASIC with pitch 146µm



Design submitted and fabricated in 2012

ADC performance measurements: Theory of dynamic measurements

Input signal S_i

ADC transfer function T_{ADC}

Output data $O_D = S_i \cdot T_{ADC}$

Discrete Fourier Transform (DFT) of output data

$$F(x_n):\ X_k = \sum_{i=0}^{N} x_n \exp\left(\frac{-i2\pi kn}{N}\right) \qquad F(O_D) = F(S_i \cdot T_{ADC}) = F(S_i) \otimes F(T_{ADC})$$

If input signal is pure sine wave with frequency equal to the one of DFT fundamental frequencies, deconvolution is straightforward since DFT of input signal is Kronecker delta:

$$S_i = \sin(kf_{base}) \Rightarrow F(\sin(kf_{base})) = \delta_k \qquad f_{base} = \frac{f_{sample}}{N}$$

$$F(S_i) \otimes F(T_{ADC}) = \delta_k \otimes F(T_{ADC}) = \underline{F(T_{ADC})}$$

ADC performance measurements
Theory of dynamic measurements

DFT of ADC transfer function → spectrum for given sampling frequency and input sine frequency

$$F(T_{ADC}) = f(f_{sample}, f_{sine})$$

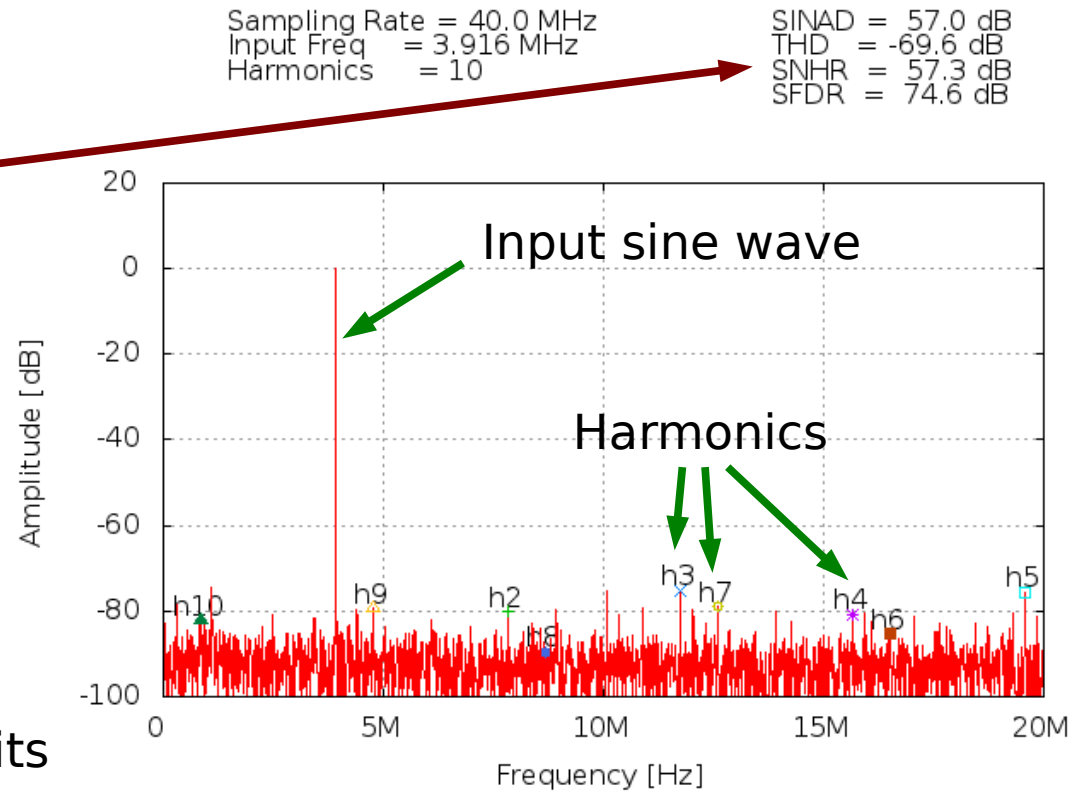
Dynamic metrics calculated from obtained DFT, i.e.:

- **SINAD** – signal to noise and distortion (harmonics) ratio

$$SINAD = 20\log_{10}\sqrt{\frac{X_{sine}^2}{\sum_{k=1,k\neq sine}^{N/2} X_k^2}}$$

- **ENOB** – effective number of bits

$$ENOB = \frac{SINAD - 1.76}{6.02}$$



ADC performance measurements: Measurements setup – main board

DFT and data analysis – custom software

Differential function generator – Agilent 81160A

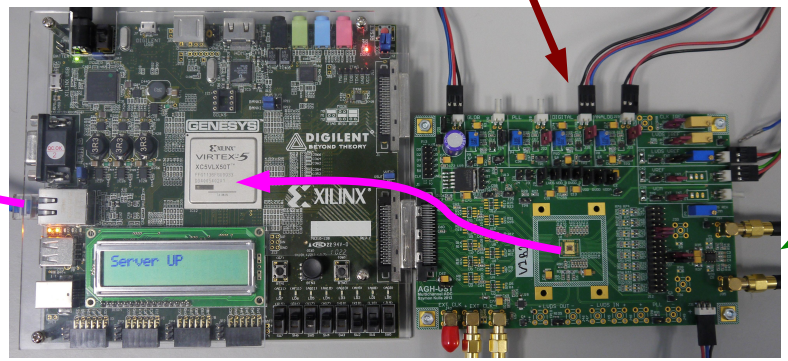
Power supply

Input sine

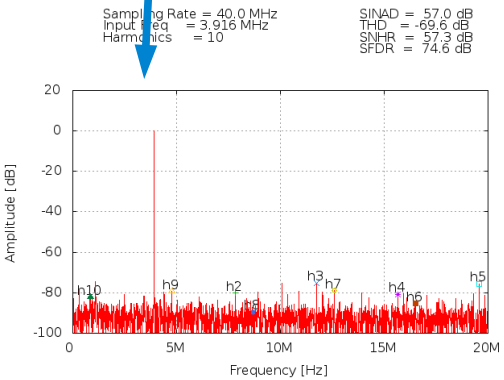
Sample clock

Results

Sampled data (**low bitrate**)



Sampled data (**high bitrate**)

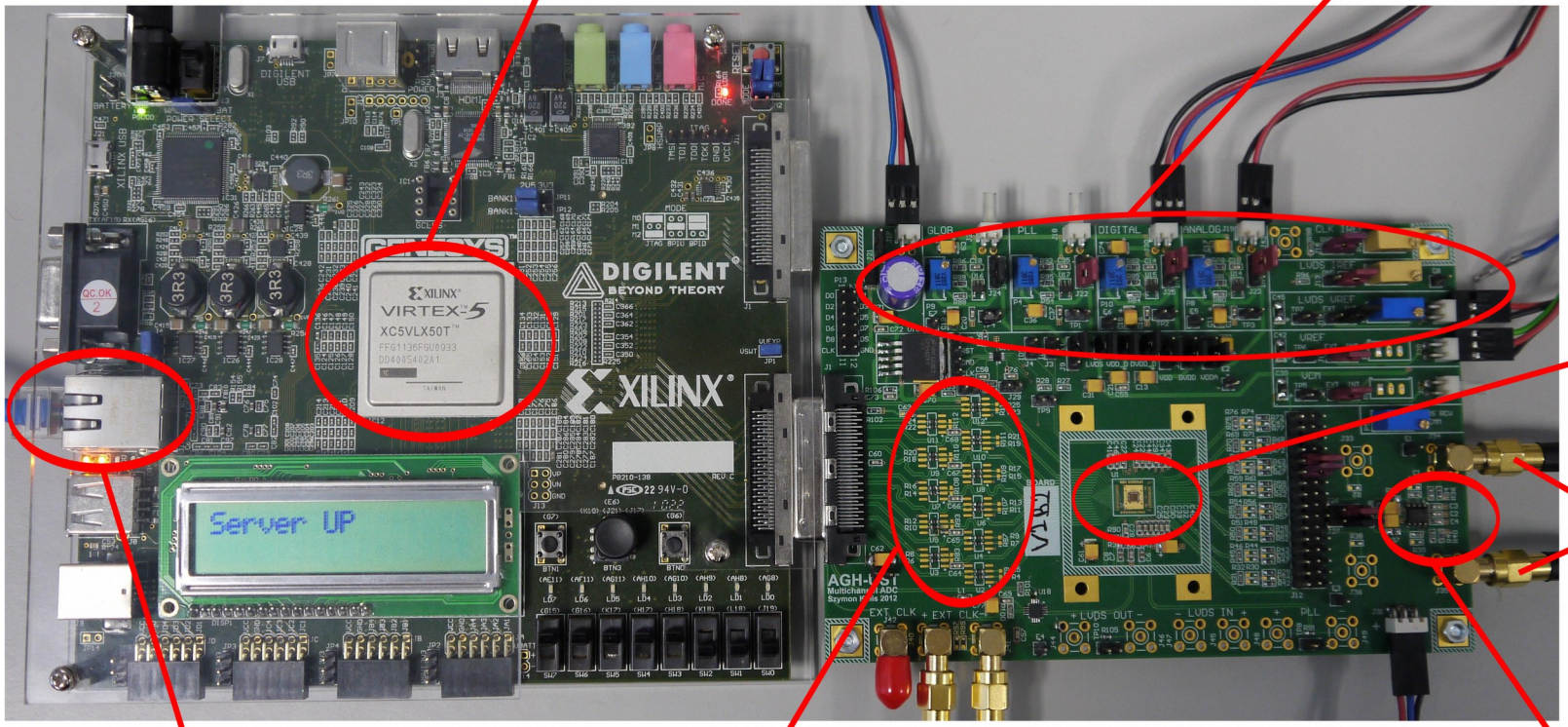


DAQ – receive fast transmission from ADC (up to 500Mb/s), store the assumed amount of data (ie. 4096 samples) and sends to PC via Ethernet for offline analysis.

ADC performance measurements: Measurement setup – main board

DAQ (VIRTEX-5 FPGA)

ADC bias and power supply



10b SAR ADC

Input sine

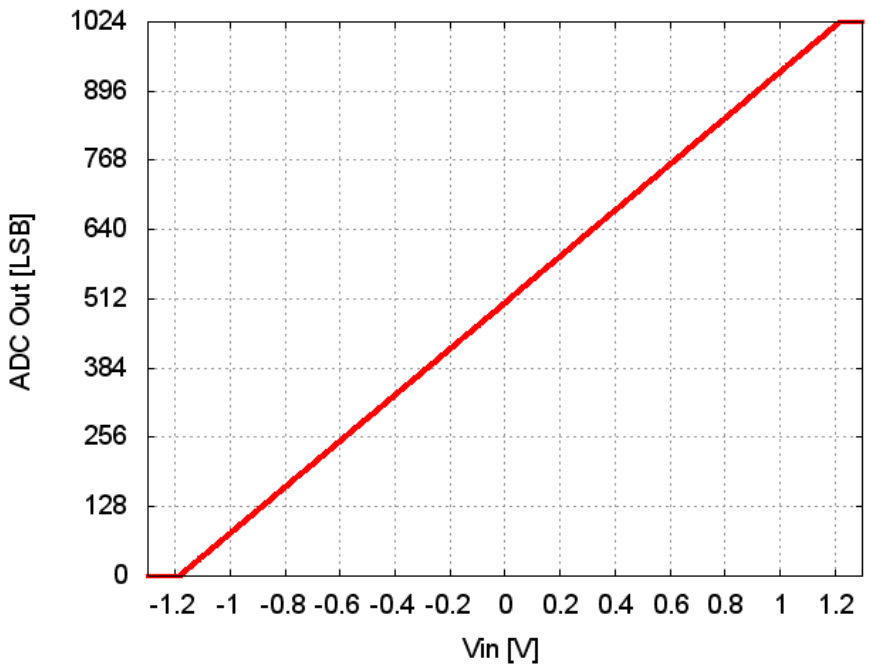
PC data link (Ethernet)

ADC output data - parallel or serial (SLVS)

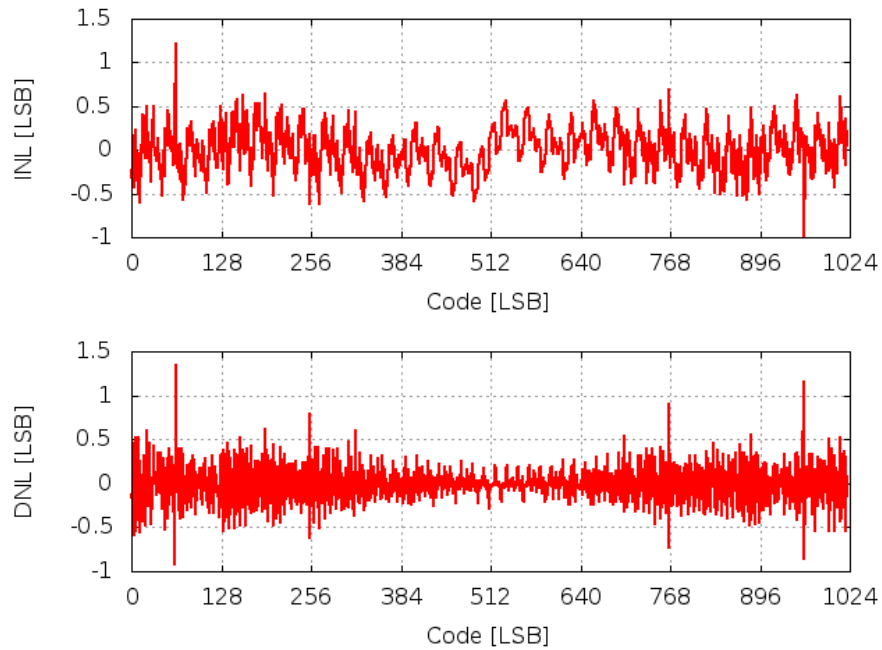
Input differential low pass filter

Measurements results
10-bit SAR ADC - Static measurements

Transfer function

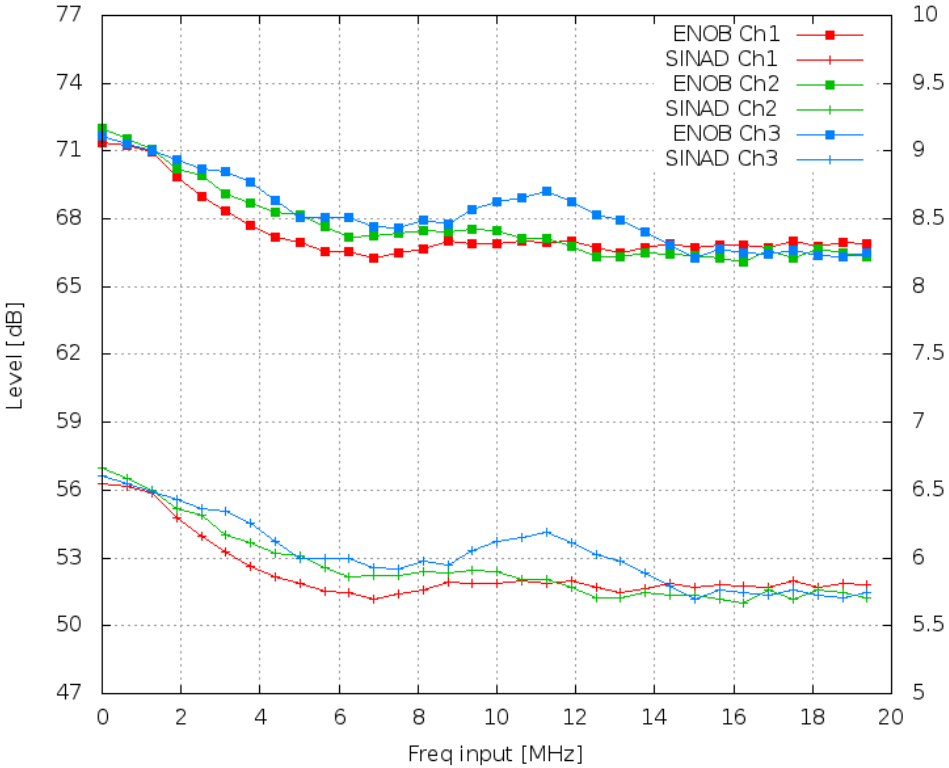


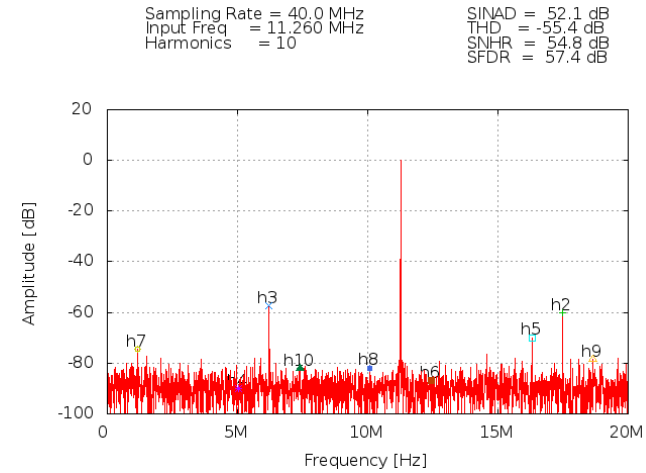
INL/DNL measurements

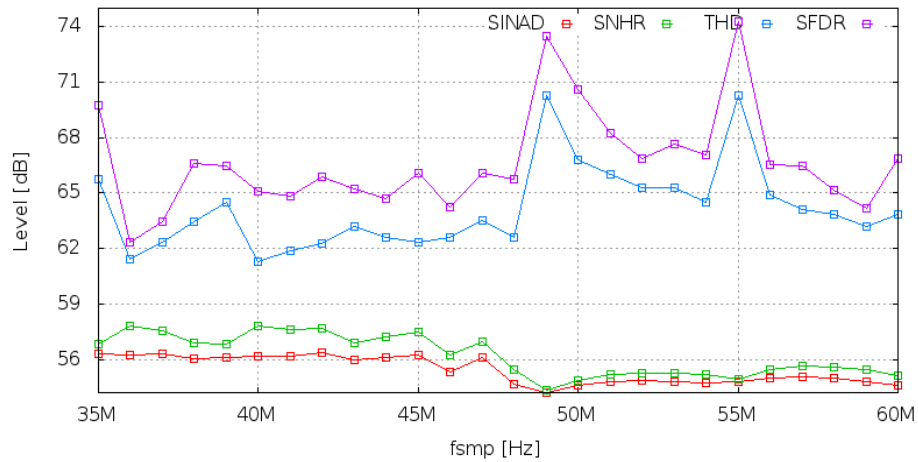


- ADC is alive and works in the whole input signal range
- There are some codes with worse linearity (some improvements in DAC layout are needed)

Measurements results:
Dynamic – input and sampling frequency

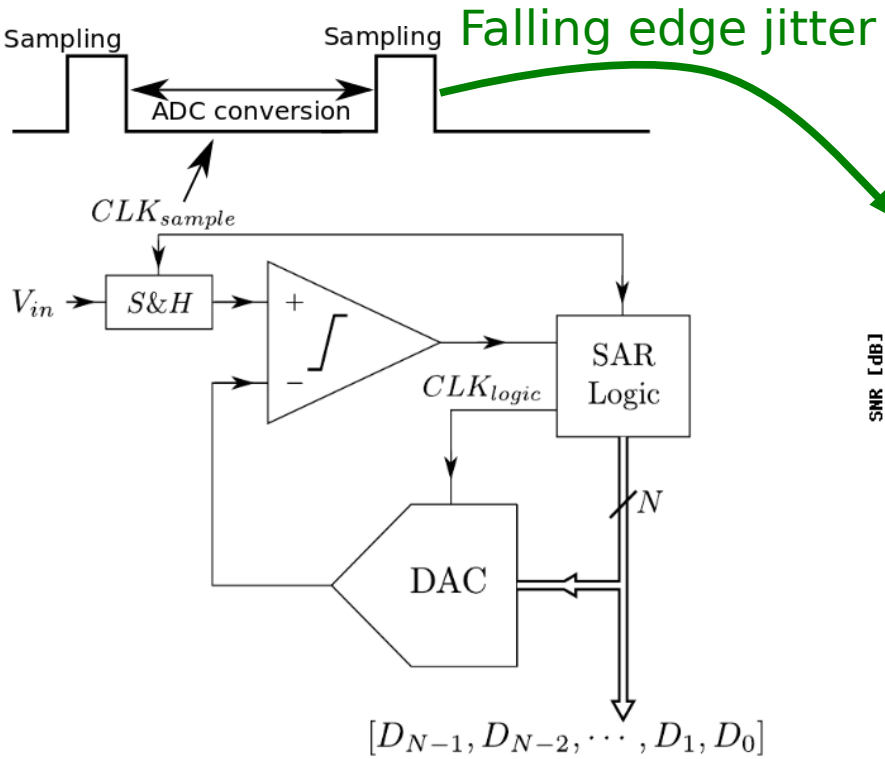


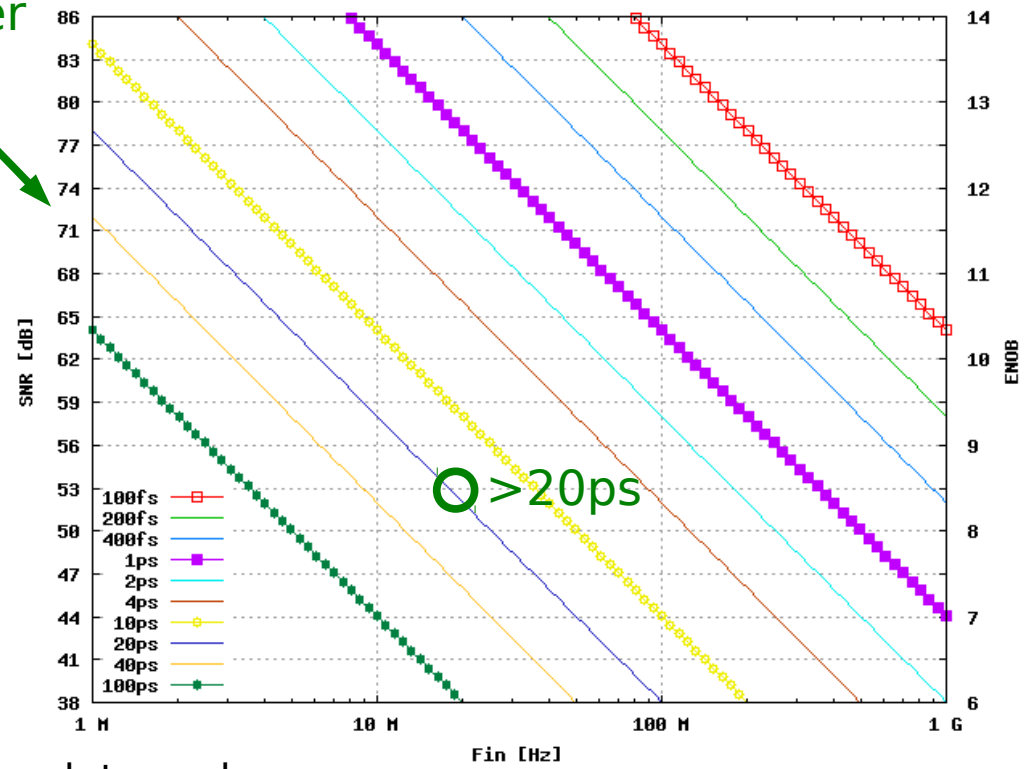




- ADC works **up to about 60 MHz sampling frequency**
- ENOB decrease with input frequency – **jitter** – see next slides

ADC performance measurements
Resolution vs sampling clock jitter…



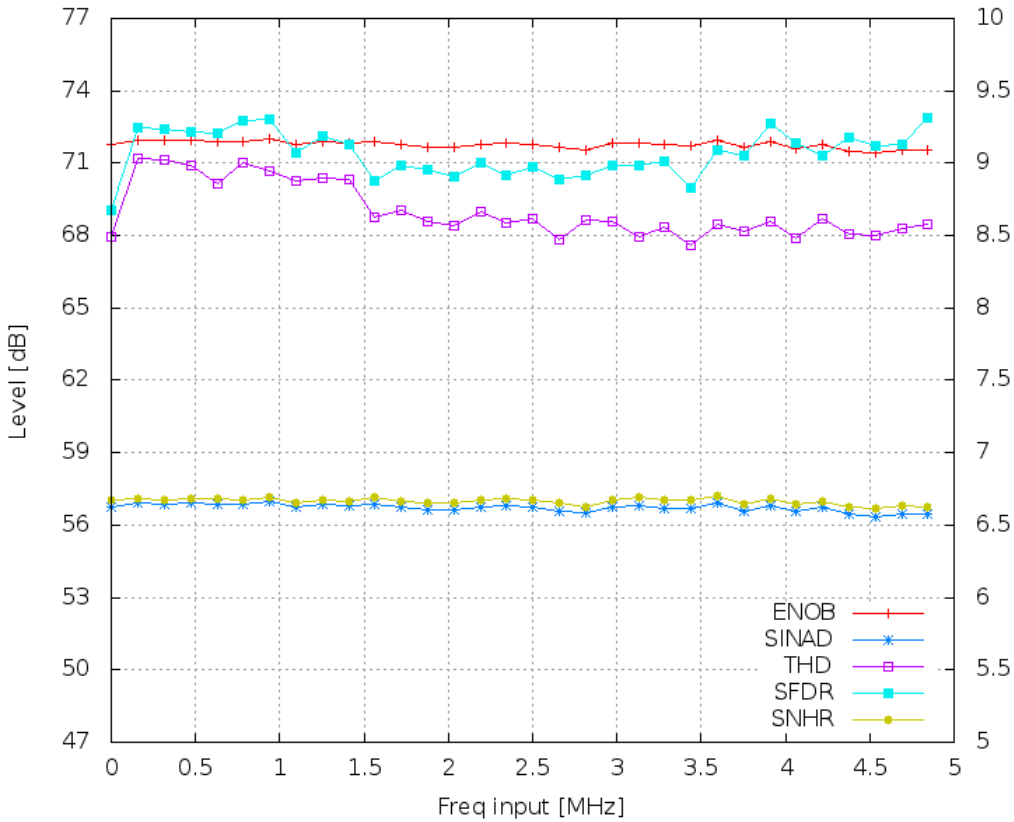


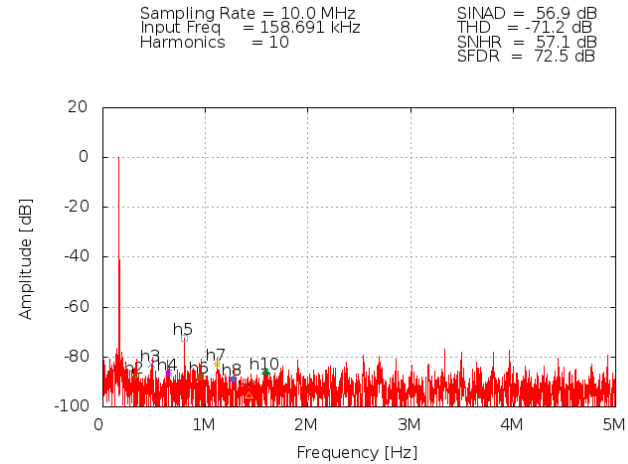
- Sampling time steered by triggering pulse duty cycle
- Non-50% duty cycle triggering pulse generated by internal circuit → introducing jitter – although post-layout simulations showed very small jitter, in reality it was larger than expected → it caused worsening of the ENOB

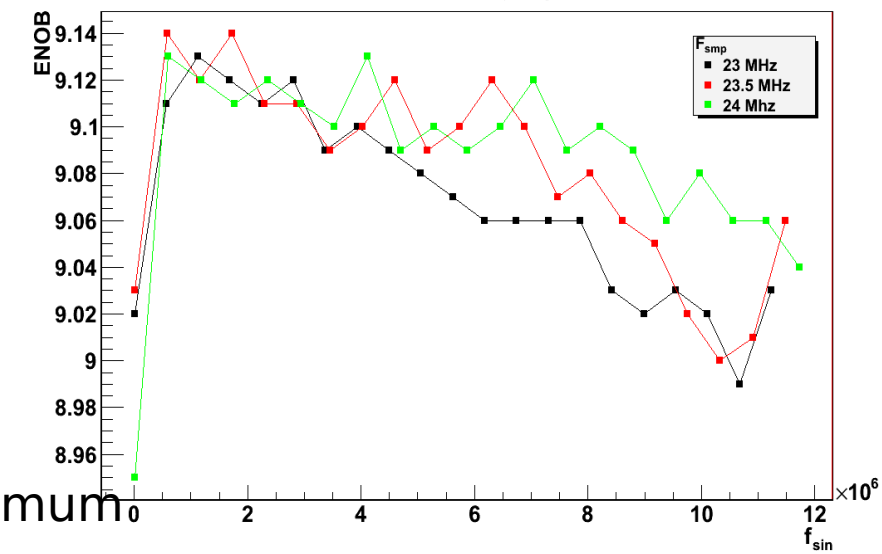
\+ Temporary solution – use 50% duty cycle external clock (low jitter) as triggering pulse

– Max. ADC sampling frequency dropped below 25 MHz

Measurements results:
Dynamic measurements – clock improvement

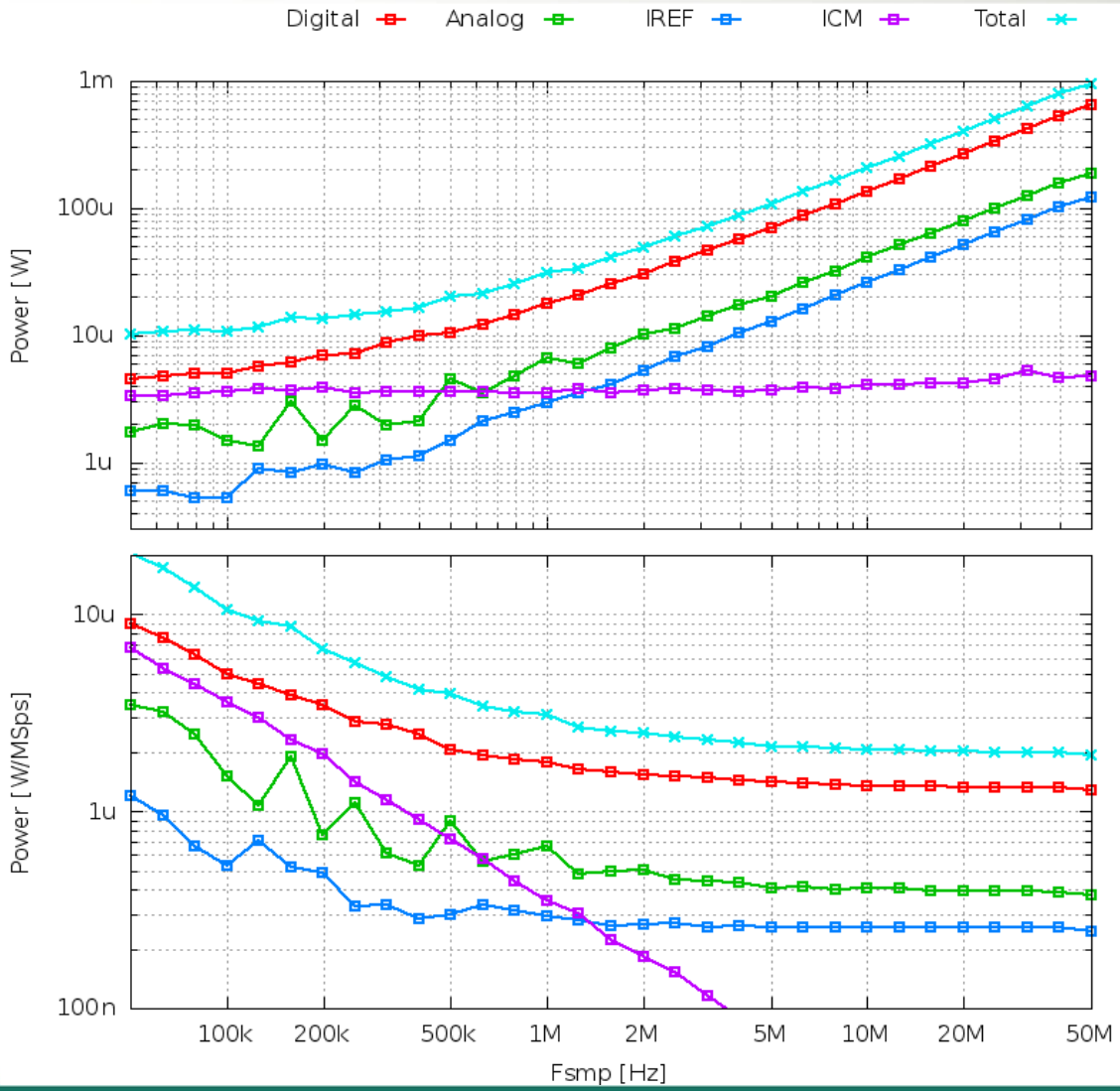






- Clock improvement allows to obtain **ENOB>9.2** up to Nyquist, lowering maximum sampling frequency below 25 MS/s

Measurements results
Power consumption vs sampling frequency



- Power consumption is about **1 mW per channel at 40 MS/s** - in agreement with simulations

Summary and Plans

- Fully dynamic SAR ADC with asynchronous logic was designed and fabricated
- ADC power consumption varies proportionally to sampling frequency (up to 60MHz)
- Power pulsing comes for free in the chosen architecture
- Effective resolution ENOB ~ 9.2 bit for sampling frequencies below 25 MHz, for higher frequencies ENOB drops to ~8.5 bit due to large jitter
- At 40 MHz sampling frequency ultra low power of ~1mW was obtained

- Linearity and resolution worse than simulated
- Too large jitter of sampling pulse

Will be addressed in next submission... Together with all multichannel aspects