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Development of variable sampling rate, low power 10-bit SAR ADC in 130 nm IBM technology

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The design and preliminary measurements results of 10-bit Successive Approximation Register (SAR) Analog to Digital (ADC) converter are presented. The prototype of the SAR ADC was designed and fabricated in 130 nm IBM technology. Preliminary measurements show that the ASIC is functional and the obtained ENOB (effective number of bits) is of about 9.2 bits. Power consumption of the ADC is around 1.1 mW per channel at nominal sample rate 40 MS/s. Maximum sampling frequency is around 50 MHz.

Summary

Nuclear pulse digitization is essential in the modern and future detector systems of particle physics experiments. Multichannel readout systems require a power and area-efficient analog to digital converters (ADC), particularly in the context of continuously growing number and density of readout channels. The Successive Approximation Register (SAR) ADC architecture allows to meet these two fundamental requirements giving additionally other features highly expected in readout system, such as power pulsing and the possibility of avoiding high frequency clock tree.

In this work we discuss the development of 10-bit SAR ADC for readout system of the luminosity detector at the future linear colliders (ILC/CLIC). We have designed a prototype ADC in 130 nm CMOS IBM technology. The ADC layout was prepared to target the multichannel implementation. The prototype ASIC comprises also a sampling pulse generator for generation of few ns pulses.

A fully differential architecture was chosen for the ADC design. It contains a pair of bootstrapped switches, a pair of Digital to Analog (DAC) converters which also perform the sample and hold task, a dynamic comparator and asynchronous dynamic control logic. To lower the power consumption the Merge Capacitor Switching (MCS) scheme was used allowing to reduce the DAC switching energy up to 93 percents compared to the conventional SAR ADC switching scheme. Dynamic architecture was chosen for both comparator and control logic to eliminate the static power consumption and so to obtain the power pulsing feature without any additional effort. Asynchronous control logic require only sampling clock and so avoids the fast clock distribution across the whole ASIC. The full circuit was designed, simulated and fabricated in 130 nm IBM technology. The ADC layout occupies 146 um x 600 um. The static measurements of fabricated ASIC showes that ADC prototype works satisfactorily with DNL below 1 and INL in range -1 to 1.1. Dynamic measurements show the ENOB around 9.2. Maximum sample rate of tested ADC is around 50 MS/s in agreement with simulations. For the default 1.2 V power supply and at 40 MHz sampling frequency the measured power consumption is around 1.1 mV. Sampling frequency is variable up to 50 MHz and the power consumption scales linearly with it.The detailed characterization of the ADC performance is in progress.

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