



Contribution ID: 144

Type: Poster

Simulation of ATLAS SCT module response to LHC beam loss scenarios

Wednesday, 25 September 2013 18:06 (1 minute)

In the event of beam loss at the LHC, ATLAS inner detector components nearest the beamline may be subjected to unusually large amounts of radiation. Understanding their behavior in such an event is important in determining whether they would still function properly. We built a SPICE model of the silicon strip module electrical system to determine the behavior of its elements during a realistic beam loss scenario, and to decide which further tests of the silicon strip detector system are necessary. We found that the power supply and bias filter characteristics strongly affect the module response in such scenarios.

Summary

Previous tests of the ATLAS silicon strip detector front-end readout electronics, the ABCD ASIC, have confirmed the ABCD's design specifications. That is, it can withstand 5 nC of charge deposited over a time interval of 25 ns due to front-end protection structures [1]. Simulations of beam loss suggest that sensors will have a rather uniform particle flux of up to 0.5×10^6 MIP (1.9 nC) per strip, every 25 ns [2]. A finite charge collection time that scales as $q^{1/3}$ due to charge screening effects [3] means that charge collection of successive pulses can overlap, possibly resulting in large, continuous currents going to strip implants. Since the readout electrodes are near ground potential due to input impedance of the ABCD chip, high implant potential can lead to breakdown of the coupling capacitors. Our work investigates what role, if any, each of the silicon strip detector components play in dissipating charge on the implants or preventing these charges from accumulating. We also consider what effect this has on the resulting charge deposited into the ABCD. We simulate a beam loss scenario with various time profiles, e.g. where the charge of each pulse increases linearly from 0 to 1.9 nC over a time span of 100 ms.

To investigate the behavior of the silicon strip detectors during a beam loss scenario as described above, we have built a SPICE model. Our model includes the power supply, bias filter, sensors, ABCD front-end, and cables. Cables are incorporated using a standard R-L-C lumped element model. The power supply is built using a standard voltage source with other components to give it current limiting behavior. The bias filter is a network of resistors and capacitors, and completely matches its specified circuit diagram. Other components of the model are not standard. Here we provide only a brief overview of their implementation. For the purposes of this study, we assume the ABCD front-end can be completely modeled by the base-emitter behavior of its input transistor. Thus, we use a diode whose behavior is tuned in SPICE to match data curves from previous studies. We explicitly model the response of the punch-through protection structures [4], and the dependence of the injected charge on the bias voltage. Combinations of circuit elements simulate time-dependent charge injection into the sensor and the expected response of the implant strip, coupling capacitor and readout strip, along with the bias resistors and bias ring.

We find that the system behavior is strongly affected by three self-limiting phenomena:

- The power supply current limit affects the sensor bias potential during the ramp-up of the incident flux.
 - The resistors in the bias filter further reduce the bias voltage on the sensors due to the voltage drop across them.
 - The reduced bias voltage on the sensor leads to smaller depletion depth which results in less collected charge.
- These effects provide a larger measure of safety during beam loss events than we have previously assumed.

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Session Classification: Poster