

TWEPP 2013 - Topical Workshop on Electronics for Particle Physics



Report of Contributions

Contribution ID: 0

Type: **Oral**

How to create successful open hardware projects - about White Rabbits and open fields

Wednesday, September 25, 2013 2:49 PM (26 minutes)

CERN's accelerator control group has embraced "Open Hardware" (OH) to facilitate peer review, avoid vendor lock-in and make support tasks scalable. A web-based tool for easing collaborative work was set up and the CERN OH Licence was created. New ADC, TDC, Fine delay and carrier cards based on VITA and PCI-SIG standards were designed and drivers for Linux were written. Often industry was paid for developments, while quality and documentation was controlled by CERN. An innovative timing network was also developed with the OH paradigm. Industry now sells and supports these designs that find their way in new fields.

Summary

The CERN team responsible for the infrastructure that controls the accelerators decided in 2009 that it would put a strong effort in making sure that new electronics would be available as "Open Hardware". By having access to all design information, CERN is able to correct bugs immediately, can repair or rebuild and improve electronics even when the original developer or company is not able to do so anymore.

Unfortunately, at that time no open designs were available with the required functionality, nor was there an infrastructure present that allowed professional engineers to easily collaborate and share information. Therefore a web-based collaboration tool (ohwr.org) was first developed where all design data could be stored, issues could be tracked and communications made. The CERN Open Hardware Licence was created because existing licences did not cover the specific needs for hardware developments.

The team decided that to stimulate collaborations new hardware would be based on VITA and PCI-SIG standards such as FMC (FPGA Mezzanine Card), PCI Express and VME64x. As system-on-chip interconnect the public domain Wishbone specification would be used while drivers for Linux would be written.

Rather general purpose ADC, TDC and Fine Delay mezzanines that can be mated with VME64x and PCI Express carriers are examples of boards that were developed in this way. Often help was called in from industry for development work, while the CERN team reviewed the results and finalised them to have consistent quality and documentation. Particular effort was spent on making reusable firmware, high quality production specifications and on setting up comprehensive production test systems.

In the same period the team needed to develop a new timing network for CERN's future control systems. From the start this so-called White Rabbit project was set up as a collaboration between institutes and industry. This innovative network allows sub-ns precision synchronization of many nodes over a span of more than ten kilometres while it simultaneously can be used to send Ethernet data. The developed White Rabbit switch, hardware and firmware allow for novel applications such as wide area triggering and sub-ns time tagging of data and make the open hardware projects even more appealing.

To guarantee that the projects could easily find their way to other users without being dependent on CERN, engineering companies were asked to not only produce the hardware for CERN but also to add them to their own product catalogue. To assure quality CERN closely followed the production. By April 2013 sixteen companies have been involved in the development, production

and sales of over ten open hardware and related open software projects. These same companies also support the designs, allowing the scaling of the number of users.

The open hardware designs originally made for CERN are now finding their way in diverse fields such as telescope arrays, national metrology networks and industrial applications which makes them even more interesting to the participating companies while the sharing of experience improves the quality and efficiency of these publicly-funded projects.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: 1

Type: **Poster**

Upgrade of the Muon Sorter in the Cathode Strip Chamber Level 1 Trigger System at CMS

Tuesday, September 24, 2013 6:25 PM (1 minute)

We report the results of our efforts in the past year to upgrade the Cathode Strip Chamber (CSC) Muon Sorter at CMS. After presenting an overview of the existing CSC Track Finder hardware and upgrade requirements we describe the modification of the existing board and transition to a new Muon Sorter. Then we discuss the improved sorting algorithm and its implementation in firmware. Current status and future plans are outlined in the conclusion.

Summary

The top level of the Level 1 Trigger System in the Cathode Strip Chamber (CSC) detector at CMS consists of the Track Finder (TF) crate with 12 Sector Processors (SP) and one Muon Sorter (MS) board. The MS provides sorting of up to 36 trigger objects from the SP boards, selects the four best (by a definable criterion) ones, and transmits then to the Global Trigger crate of CMS. With the anticipated LHC luminosity increase above $10^{34} \text{cm}^{-2}\text{s}^{-1}$ at higher energy of 6.5-7 TeV/beam the CSC TF needs to be upgraded. The new CSCTF will be robust to higher occupancies, provide improved transverse momentum assignment and increased precision of the muon output variables. A transition from the current 9U VME electronic standard to the more flexible uTCA and utilization of the Xilinx Virtex-6 and Virtex-7 FPGAs, with multiple embedded gigabit links, will allow us to build a higher performance TF such that the MS functions can be performed by one of the SP modules. We present here the results of our efforts in the past year to upgrade the CSC Muon Sorter, including the short term modifications of the existing VME board, long-term transition to the uTCA as well as firmware development for both of these projects.

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Session Classification: Poster

Contribution ID: 2

Type: **Oral**

Pixel front-end development in 65 nm CMOS technology

Tuesday, September 24, 2013 11:10 AM (25 minutes)

Upgrade of luminosity of the LHC (HL-LHC) imposes severe constraints on detector tracking systems in terms of radiation hardness and ability to cope with high hit rates. One possible way of keeping track with increasing luminosity is usage of more advanced technologies. Ultra deep sub-micron CMOS technology allows design of complex and high speed electronics with high integration density. In addition these technologies are inherently radiation hard. We present a prototype of analog pixel front-end designed in 65 nm CMOS technology with applications oriented to upgrade of the ATLAS Pixel Detector. Aspects of ultra deep sub-micron design and performance of the analog pixel front-end circuits will be presented.

Summary

We present a prototype of a pixel analog front-end FE-T65-1 designed in 65 nm CMOS technology. The development of this integrated circuit has been motivated by a need of a new read out chip to operate ATLAS pixel detector after high luminosity LHC upgrade.

The test chip contains an array of 32 pixels with pixel size of $180 \times 25 \mu\text{m}^2$. Four flavors of the pixel electronics have been implemented. The pixels differ by architecture of charge sensitive amplifier (constant current reset or switched reset) and comparator (continuous and dynamic comparator). Analog part of every pixel is equipped with tunable input capacitance allowing determination of noise as a function of input capacitance. Digital part is identical for every pixel and contains configuration register and hit counter.

Performance of each version of FE-T65-1 has been evaluated in terms of noise, time-walk and threshold dispersion.

Noise performance of the pixel front-end depends on the input capacitance of the charge sensitive amplifier (CSA) and also on the version of the analog circuitry. CSA with switched reset exhibits systematically lower noise ($\text{ENC} = 113 \text{ e}^-$) with respect to CSA with constant current feedback ($\text{ENC} = 144 \text{ e}^-$). This effect is attributed to the absence of ballistic deficit of the switched CSA and therefore this CSA has higher gain and lower noise. An excessive noise contribution has been found in the pixel versions with the dynamic comparator possibly due to additional switching activity in the pixel ($\text{ENC} = 183 \text{ e}^-$ resp. 157 e^-).

The dynamic performance of the front-end electronics greatly depends on power budget. Peaking time of the CSA as well as the comparator contributes to the time-walk. Time difference between large hit (20 ke^-) and small hit (2 ke^-) with threshold of 2 ke^- has been studied. In order to avoid delay exceeding 25 ns (one bunch crossing at the LHC) power consumption of the pixel with constant current CSA and with continuous comparator must be increased up to $18 \mu\text{W}$ per pixel. The dynamic comparator (clocked at frequency of 40 MHz) has a very small intrinsic time-walk with respect to the CSA and therefore overall power consumption to meet 25 ns criteria is $10 \mu\text{W}$ per pixel. The versions with switched CSA meet 25 ns criteria with power consumption of $15 \mu\text{W}$.

Another important property of many pixel front-end chip is threshold dispersion. Every pixel in the test matrix have slightly different threshold. The mean value of the threshold dispersion is about 400 electrons. In order to compensate this effect, every pixel contains 5-bit DAC allowing threshold adjustment locally in every pixel. Applying threshold tuning procedure the threshold

dispersion has been reduced well below 30 electrons for every pixel version.

To summarize the results achieved with FE-T65-1 the overall analog performance of this prototype is least comparable with the existing ATLAS pixel front-end chip FE-I4 designed in 130 nm technology.

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Session Classification: ASICs

Contribution ID: 3

Type: **Oral**

Single Event Upset Studies Using the ATLAS SCT

Thursday, September 26, 2013 11:10 AM (25 minutes)

Single Event Upsets (SEU) are expected to occur during high luminosity running of the ATLAS SemiConductor Tracker (SCT). The SEU cross sections were measured in pion beams with momenta in the range 200 to 465 MeV/c and proton test beams at 24 GeV/c but the extrapolation to LHC conditions is non-trivial because of the range of particle types and momenta. The SEUs studied occur in the p-i-n photodiode and the registers in the ABCD chip. Comparisons between predicted SEU rates and those measured from ATLAS data are presented. The implications for ATLAS operation are discussed.

Summary

Single Event Upsets (SEU) are a cause for concern for the inner detectors at the High Luminosity LHC (HL-LHC). It is therefore important to understand the SEU rates observed in the current detector during LHC operation. In the ATLAS SCT, SEUs are expected to occur in the on-detector p-i-n photodiode which receives the optical Timing, Trigger and Control data. An error in the receipt of the trigger signal will cause a silicon detector-module to lose synchronisation with the rest of the detector. Therefore even low SEU rates can lead to significant loss of data. Registers in the front end ASIC for the SCT can be flipped by SEUs. While the loss of data in the pipeline or buffer will be negligible, the effects of SEUs on the static registers will have long lasting effects. For example, bit flips within the threshold register can increase or decrease the charge threshold required to register a hit. This may result in either loss of hit efficiency or high noise for data from that ASIC until the registers are reconfigured.

The SEU cross sections for the p-i-n photodiodes and the ABCD registers were measured in pion and proton test beams with a limited range of momentum and the results will be briefly reviewed. The SEU rates in the p-i-n diodes were determined by monitoring the rates of module desynchronisation. In principle these results can be used to predict the SEU rates during LHC operation, however there are many non-trivial corrections that need to be evaluated: the largest correction is due to the range of particle type and the spectrum at the LHC. A first approximate correction was estimated by scaling the SEU cross sections with measured hadron-proton cross sections. Ongoing studies will improve this by using hadron nucleus cross sections. The test beam data were all taken at fixed angles between the beam and the devices whereas the particles in LHC operation will cross the detectors at a range of angles. LHC data were used to study the effect and determine a correction factor. For the SEUs in the p-i-n diodes, correction factors were also estimated to allow for the bunched nature of the LHC operation compared to the DC test beams. The SEU rates in the p-i-n diodes are very sensitive to the p-i-n currents and this was also accounted for in comparisons between test beam and LHC operation. Overall reasonably good agreement between the predicted and measured SEU rates was found. This gives confidence in the ability to extrapolate test beam results to HL-LHC operation.

Finally the implications for ATLAS operation are discussed. The loss of module synchronisation is mitigated by the automatic reconfiguration of individual modules if errors are detected by online monitoring. The effect of ASICs becoming noisy due to SEUs is reduced by detecting this from the online monitoring and reconfiguring that module. In addition all modules are resynchronised every 30 minutes to ensure all registers are correctly set.

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Session Classification: Optoelectronics and Links

Contribution ID: 4

Type: **Poster**

Radiation hard programmable delay line for LHCb Calorimeter Upgrade

Tuesday, September 24, 2013 5:00 PM (1 minute)

This paper describes the implementation of a SPI-programmable clock delay chip based on a Delay Locked Loop (DLL) in order to shift the phase of the LHC clock (25 ns) in steps of 1ns, with a 4ps jitter and 18ps of DNL. The delay lines will be integrated into ICECAL, the LHCb calorimeter front-end ASIC in the near future. The stringent noise requirements on the ASIC imply minimizing the noise contribution of digital components. This is accomplished by implementing the DLL in differential mode. To achieve the required radiation tolerance several techniques are applied: double guard rings between PMOS and NMOS transistors as well as glitch suppressors and TMR Registers. This 5.7 mm² chip has been implemented in CMOS 0.35um technology.

Summary

Delay lines are commonly used in high energy physics experiments since synchronization is critical for such kind of applications. The operating principle of digital delay lines is very simple: the user can set an arbitrary delay and thus compensate the latency introduced, for example, by cables or fibers.

This paper describes the implementation of a SPI-programmable (Serial Peripheral Interface) 4 triple channel (12 clock outputs) delay line based on a Delay Locked Loop (DLL) and developed for the LHCb electromagnetic and hadronic calorimeter upgrade. The user can configure up to 25 different clock phases to cover the 25 ns LHC clock in 1ns steps. The DLL is adjusted by means of two control voltages: the former is automatically generated by the phase comparator and charge pump circuit, while the later is externally adjusted by the user. This dual adjustment provides an operating range of 17.45 to 39.88ns, wider enough to ensure that systematic process or environmental variations will not prevent working properly with the LHC clock. The differential design as well as the use of weak inverters to ensure 180° phase and the implementation in 0.35um technology favors the minimization Differential Non Linearity (DNL), which is equal to 18ps for each 1ns delay element.

Despite this delay line chip can operate in standalone mode, it will be integrated into the next LHCb calorimeter front-end ASIC (ICECAL) in the near future, and consequently, the stringent noise requirements of the ASIC analog components must be met by the digital components and thus by the delay line. Therefore, the fully differential design of the DLL aims to reduce the switching noise produced by delay lines. The use of double guard rings also decreases the noise propagation through the substrate. The clock jitter induced by transient noise is lower than 4ps.

Design methodology of this chip prototype is also determined by the radiation environment where DLLs will operate. ICECAL chips will be mounted on ECAL front-end boards (FEBs), located inside the LHCb cavern. Moreover, the energy increase of the LHC machine (from 7 to 14 TeV) will increase the potentially dangerous ionizing radiations and thus, the probability of suffering from single event effects. The design must tolerate SEUs, SETs and SELs. The probability of suffering SELs is reduced by increasing the distance between PMOS and NMOS transistors and inserting double guard rings between them, so that PMOS and NMOS transistors are confined inside islands of the same transistor type. SEUs are avoided by implementing Triple Modular Redundancy Registers to store the DLL configuration and fault tolerant Finite State Machine in the SPI Slave. Finally,

reset signals are protected from SETs by means of glitch suppressors.

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Session Classification: Poster

Contribution ID: 5

Type: **Poster**

Simulation of the ATLAS sTGC trigger for the Phase-I new small wheel detector upgrade

Wednesday, September 25, 2013 6:21 PM (1 minute)

A Verilog Behavioral simulation of sTGC trigger will be presented based on the current baseline concept with particular focus on the Level 1 latency obtained. Data for this trigger is taken from detector simulations with Garfield and PSpice, current measurements made in the existing small wheel, and FLUGG simulation of the arrival times of hits at high luminosities. These simulations will become the HDL that is used to compile the ASIC in the 130nm IBM CMOS process. The CERN designed GBT serializer is to be included in the ASIC for transmission of the resulting trigger information to the rim of the nSW.

Summary

The primary trigger of the ATLAS New Small Wheel (NSW) is based on the sTGC detector. A behavioral Verilog simulation of the detector and on-chamber electronics has been developed and the results will be presented. The detector has been characterized with Garfield and Spice with detailed comparison to test beam data. This characterization of the detector has been coded in Verilog and extended to include the front-end ASD chip of the NSW, the VMM. This software is used as a test bench for stimulating the trigger processing circuitry, the trigger data serializer (TDS) chip. Both the VMM and the TDS chips are radiation tolerant ASICs. The TDS accepts both pad and strip data from the sTGC. Pad data is immediately sent to circuits on the rim of the NSW where track roads are formed. Strip data is captured by the TDS chip and stored awaiting confirmation from the track roads. Once confirmed, the strip data is serialized and send off-chamber. Data rates and particle arrival times are provided by a combination of existing muon data and FLUGG simulation. The algorithms and data flow through the TDS chip will be exhibited as well as the measured latency. The TDS output includes a Verilog simulation of the GBT serializer provided by the CERN microelectronics group

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Session Classification: Poster

Contribution ID: 6

Type: **Poster**

Single-event upset tests on the readout electronics for the pixel detectors of the PANDA experiment.

Tuesday, September 24, 2013 6:00 PM (1 minute)

The Silicon Pixel Detector (SPD) of the PANDA experiment is the closest one to the interaction point and therefore the sensor and its electronics are the most exposed to radiation. The Total Ionizing Dose (TID) issue has been addressed by the use of a deep-submicron technology (CMOS 0.13 μm) for the readout ASICs. While these technology are very effective in reducing radiation induced oxide damage, they are also more sensitive to Single Event Upset (SEU) effects due to their extremely reduced dimensions. This problem has to be addressed at the circuit level and generally leads to an area penalty. Several techniques have been proposed in literature with different trade-off between level of protection and cell size.

A subset of these techniques has been implemented in the PANDA SPD ToPiX readout ASIC, ranging from DICE cells to triple redundancy. The two prototypes have been tested with several ions at the INFN-LNL facility in order to measure the SEU cross section.

Comparative results of the SEU test will be shown, together with an analysis of the SEU tolerance of the various protection schemes and future plans for the SEU protection strategy which will be implemented in the next ToPiX prototype.

Summary

The PANDA experiment is one of the key projects at the future Facility for Antiproton and Ion Research (FAIR), which is currently under construction at GSI, Darmstadt. The PANDA experiment will perform precise studies of antiproton-proton annihilations and reactions of antiprotons with nucleons of heavier nuclear targets.

The silicon pixel system is the innermost detector and therefore the sensor and its electronics are the most exposed to radiation. For what concerns the electronics, the Total Ionizing Dose (TID) issue has been addressed by the use of a deep-submicron technology (CMOS 0.13 μm) for the readout ASICs. These technologies offer a better resistance to radiation as well as more dense integration with respect to previous technology nodes. However, they are also more sensitive to Single Event Upset (SEU) effects due to their extremely reduced dimensions. This problem has to be addressed at the circuit level which generally lead to an area penalty. Several techniques have been proposed in literature with different trade-off between level of protection and area penalty.

A subset of these techniques have been implemented and tested on the two prototypes of the pixel readout ASIC for PANDA (ToPiX). In ToPiX v2, latches based on the Dual Interlocked storage CELL (DICE) architecture were implemented for the pixel cell registers in order to save area, while standard DFF have been used for the end of column logic. The chip was tested with several ions ranging from Oxygen to Bromine with energies in the range of 100-200

MeV (depending on the ion) and at both 0 and 30 degrees at the SIRAD Facility of the Laboratori Nazionali di Legnaro (LNL) of INFN. A saturation cross section of $2e-8$ cm²/bit with an energy threshold of about 0.5 MeV has been measured for the DICE latches of the pixels, while for the standard DFF the saturation cross section was $2.6e-8$ cm²/bit with a threshold close to 0. In the PANDA environment, at the average value of 2×10^7 interactions/s in the case of hydrogen target, these values corresponds to ~ 3 SEU/hour per chip in the configuration register and between 130 and 200 in the end of column logic. These SEU rates are not easily manageable by an on-line correction system. In order to improve the SEU immunity, the ToPiX v3 was designed with Triple Modular Redundant (TMR) latches for the pixel registers and Hamming encoding for the end of column logic. The chip has been tested at LNL with a similar set of ions and the results are under analysis. In the same test, a second chip designed in the same technology but with a full logic triplication was also tested for comparison. Comparative results of the SEU test will be shown, together with an analysis of the SEU tolerance of the various protection schemes and future plans for the SEU protection strategy which will be implemented in the next ToPiX prototype.

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Session Classification: Poster

Contribution ID: 7

Type: **Poster**

The eCDR, a Radiation-Hard 40/80/160/320 Mbit/s CDR with internal VCO frequency calibration and 195 ps programmable phase resolution in 130 nm CMOS

Wednesday, September 25, 2013 4:37PM (1 minute)

A clock and data recovery IP, the eCDR, is presented which is intended to be implemented on the detector front-end ASICs that need to communicate with the GBTX by means of e-links. The programmable CDR accepts data at 40, 80, 160 or 320 Mbit/s and generates retimed data as well as 40, 80, 160 and 320 MHz clocks that are aligned to the retimed data. Moreover, all the outputs have a programmable phase with a resolution of 195 ps. The radiation-hard design, integrated in a 130 nm CMOS technology, operates at a supply voltage between 1.2 V and 1.5 V.

Summary

The GBT project, currently under development as part of the LHC upgrade program, aims at the realization of a radiation-hard chipset to be used as an on-detector transceiver to implement radiation-hard optical links between the counting room and the detector front-ends. In order to establish the communication between the front-ends and the GBT by means of the e-links, the presented CDR has been developed. This eCDR operates with 40, 80, 160 or 320 Mbit/s data to comply with the e-links specification. Apart from recovering the received data, the eCDR also generates in-phase clocks at 40, 80, 160 and 320 MHz, regardless of the data rate. These clocks can be used as a local reference for the front-ends. The eCDR is implemented in a 130 nm CMOS technology, it is able to operate at a supply voltage between 1.2 V and 1.5 V and is fully radiation-hardened. In order for a CDR to lock, its VCO should oscillate at a frequency very close to the incoming data rate. The eCDR incorporates 2 measures to accomplish this, namely an external and an internal calibration system. The external calibration phase-locks the VCO to an external reference clock before initiating the CDR operation. On the contrary, the internal calibration system does not require an external reference and can bring the VCO close to the required oscillation frequency all by itself. The frequency generated by the internal calibration can be set with a 6-bit word. Excellent temperature stability of 96 ppm/°C has been shown in simulation.

When the eCDR is locked, the loop is controlled by means of a phase-detector (PD) measuring the phase difference between the divided VCO clock and the incoming data. The VCO control voltage is then steered to compensate for this difference. When switching between the calibration phase and CDR operation or in the case of an SEU, it can happen that the VCO frequency deviates significantly from the data frequency. Because the loop based on the PD has a limited locking range, a frequency detector (FD) loop has been incorporated as well in order to extend the locking range. The dynamics of the 2 loops can be set independently.

As mentioned before, the output clocks of the eCDR, which are always in-phase with the retimed data, can be used as a reference for the front-end. To make these clocks even more useful, their phase, as well as the phase of the retimed data, can be set with a very fine resolution of 195 ps. As such, the output clocks can be aligned to the bunch crossing or to another clock in the front-end. This has been realized by making use of the 16 phases of the 8-stage differential VCO running at 320 MHz.

The eCDR has been conceived as a radiation-hard circuit. Therefore, all digital blocks are triplicated

while the analog cells have been designed to minimize the effect of SEUs. The used technology is inherently tolerant to total ionizing dose. The eCDR consumes less than 40 mW.

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Session Classification: Poster

Contribution ID: 8

Type: **Poster**

Acquisition and control command system for power pulsed detectors

Tuesday, September 24, 2013 6:11PM (1 minute)

A DAQ system is developed within the SiW Ecal CALICE collaboration. It provides a flexible and scalable architecture, compound of three parts. A detector interface (DIF) extracting data from frontend electronics and sending them as packets. Two levels of data concentration, control clock and fast command fanout. The two cards, named DCC and GDCC, use respectively FastEthernet and GigaEthernet. A software suite (named Calicoes), for controlling DAQ, detector chips, acquiring data from GigaEthernet, decoding frontend readout to various formats and aggregating data. Overall architecture, performance in test beam and prospects for use with hundreds of thousands channels are discussed.

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Session Classification: Poster

Contribution ID: 9

Type: **Oral**

Ultra-thin packaging technologies for CMOS pixel sensors: embedding in kapton foils

Friday, September 27, 2013 11:30 AM (25 minutes)

Monolithic CMOS Pixels (MAPS) integrate on the same silicon substrate the radiation sensor element with the processing electronics.

Their thickness can be very small: typically less than 50 μm . This allows for very small material budget, if not spoiled by other mechanics elements. In order to demonstrate feasibility of large area, ultra-light sensor ladders ($< 0.1\%$ radiation length) based on MAPS, we develop novel packaging method. Thinned sensors are embedded in polymer (kapton) film, electrical connection to pads are implemented by aluminum deposition following by lithography steps (no wire bonding). Details of ladder design and electrical tests results are presented.

Summary

Monolithic CMOS Pixels (MAPS) integrate on the same silicon substrate the radiation sensor element with the processing electronics.

Their thickness can be very small: typically 20 μm for active silicon (sensor plus electronics) and less than 10 μm for interconnections (several metal-insulator layers). Therefore MAPS can be thinned down to less than 50 μm , without losing their tracking performance. This allows very small material budget and construction of non-planar (cylindrical) detector layers: thin silicon is quite flexible. In order to demonstrate feasibility of large area, ultra-light ($< 0.1\%$ radiation length) sensor ladders we develop novel packaging method. Thinned sensors (< 50 microns) are embedded in polymer (kapton) film, electrical connection to pads are implemented by metal deposition (sputtering) and lithography steps (no wire bonding). The fabrication is based on slightly modified process (existing at CERN) for flexible multi-layer PCB fabrication, in which aluminum is used for all metal interconnections. For the demonstration of this new packaging method, medium size CMOS sensor (Mimosa 26, approximately 2x1 cm sq.) has been chosen. In the first iteration, a single-chip flex module has been fabricated and electrically tested. Two metal layers are used to provide connection down from the bonding pads on Mimosa 26 up to the micro-connector and few capacitors (standard SMD components) on top of the stack. Production of module with two chips and four metal layers (two reserved for power supply planes) is in progress and should be finished within few weeks. The final demonstrator module with six Mimosa 26 chips is planned soon after. The dimensions and the material budget of that demonstrator (12x1 cm sq.) are similar to that required by the inner layer of Vertex Detector for the International Linear Collider. We present details of ladder design adapted for large area coverage, followed by electrical tests results, thermal study consideration and minimum ionizing particle tracking performance. Possible improvements of the process will be also proposed.

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Session Classification: TOPICAL (Packaging & High Density Hybrids)

Contribution ID: 10

Type: Oral

High speed readout electronics development for frequency-multiplexed kinetic inductance detector design optimization

Tuesday, September 24, 2013 11:11 AM (24 minutes)

Microwave Kinetic Inductance Detector (MKID) are a promising solution for space-borne mm-wave astronomy. To optimize their design and reduce the impact of the primary Cosmic Rays interaction with the substrate, the phonon propagation in the silicon substrate must be studied. A dedicated fast readout electronics, using channelized Digital Down Conversion for monitoring up to 16 MKIDs over a 100MHz bandwidth was developed. Thanks to the fast ADC sampling and steep digital filtering, In-phase and Quadrature samples, having a high dynamic range, are provided at 2MSPS. This paper describes the technical solution chosen and the results obtained.

Summary

The microwave kinetic inductance detectors are an alternative to traditional bolometers for mm-wave astronomy. They consist of a high-quality superconducting resonant circuit electromagnetically coupled to a transmission line and they are designed to resonate in the microwave domain. Their resonances lie between 1 to 10GHz and have loaded quality factors exceeding 10^5 , corresponding to a typical bandwidth of about 100kHz. As the MKIDs resonant frequency can easily be controlled during manufacturing, it is possible to couple a large number of MKIDs to a single transmission line without interference and therefore to perform a frequency-multiplexed readout. Their self resonant frequencies are proportionally sensitive to the incident sky power, but also to the ballistic phonons induced by cosmic rays direct interaction in the substrate. Indeed, due to the metal layer thinness and a much smaller physical area of the MKIDs compared to the substrate, the MKIDs themselves have a negligible cross section to cosmic rays. To fully study the phonon diffusion, a dedicated fast readout electronics was required. These electronics can be used for different purposes: either for time-resolved phonon-mediated detection of high-energy interactions from cosmic rays or for optimization of the MKID array design.

The required electronic fulfills two purposes. At first, it builds a frequency comb having all its tones adjusted to the different resonators center frequencies; this excitation signal is injected in the detector. Then, at the output of the transmission line coupled with the MKIDs, the resultant signal is acquired and analyzed in order to determine the time dependent phase and amplitude variation of each sinusoids. Since the MKID resonator frequencies are above several GHz, the electronics does not drive directly the array. Consequently, the frequency comb is generated at baseband and up-converted to the frequency band of interest by hybrid mixers. The array output signal is down-converted back to baseband and then processed by the electronics.

A channelized Digital Down Conversion (DDC) solution was implemented to reach high sampling rate (2MSPS) and meanwhile allowing a high dynamic range. Each DDC features a quadrature Direct Digital frequency Synthesis (DDS) (14 bit CORDIC generator), two digital mixers and two multirate steep digital filters. The digital filters are composed of two successive Cascaded Comb Integrator filters (CIC) followed by two polyphase Finite Impulse Response (FIR) filters (40 coefficients). The second CIC filter has a programmable decimator allowing the tuning of the sampling rate.

Consequently, the electronic developed is FPGA centered (Xilinx Virtex6) to provide adequate computing power and features a dual 16 bit DAC and one 14 bit ADC, all clocked at 250MHz. This

frequency permits to cover a 100MHz of useful bandwidth, which is sufficient to excite and read-out a transmission line fitted with 16 MKIDs, provided they are adequately separated in frequency.

Each DDC channel is equipped with a trigger system that allows the data recording only when the signal module exceed a threshold.

After a quick overview of the MKID and their readout technique, this presentation will describe the technical solution chosen and the results obtained.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: 11

Type: **Poster**

Consolidation of the radiation tolerant programmable power supply cards for the LHC beam screen heaters

Wednesday, September 25, 2013 5:49PM (1 minute)

For the next LHC run it is required to install 200 W of heating capacity to regenerate the beam screen by desorption of gas trapped on its walls. In the LHC, there are 272 beam screen heaters and the associated electronics limits the heating capacity to 25 W. These electronics are mostly installed inside the LHC tunnel and exposed to its radiation environment.

This paper describes the basic functionalities of the new card and the work done for designing and qualifying under radiation an analog signal multiplexer and a power switch capable of coping with the grid voltage.

Summary

The beam screens are equipped with resistive heating elements of 100 Ω to provide a power of up to 200 W to raise its temperature up to 90 K. This raise of temperature results in the release of gas molecules trapped on the beam screen. During beam operation, the heating power is limited to 25 W, which is also the limit of the currently installed cards. During the next shutdown, 272 power supply cards will be consolidated to raise their limit from 25 W to 200 W. The increased power will be available for use whenever there is no beam in the LHC.

The consolidation requires the development of a new electronics card reusing parts of the existing design that proved to operate reliably.

The consolidated card supports both DC (0-50 V, 0-2 A) and AC (50-230 VAC, 0-4 A) modes of operation. For the new AC mode, the card uses isolation transformers and power MOSFETs with pulse width modulation (PWM) regulating power from the AC grid. For the selection of the radiation tolerant power MOSFETs, a radiation campaign took place at CERN's CNRAD experimental area during 2012. CNRAD offers a mixed radiation field, similar to the one in the LHC tunnel. Three different commercial power MOSFET electronics were tested at CNRAD for approximately 5 months to simulate LHC operation of many years. The MOSFETs were tested both in passive (standalone) and active (230VAC grid applied) modes. All types of power MOSFETs survived the passive tests and one MOSFET type survived the active tests. The total integrated dose (Gy), equivalent neutrons (>1 MeV) and hadrons (>20 MeV) exceeded the radiation requirements of the design. This is true for all 3 MOSFET types because during LHC irradiation (beam ON) the MOSFETs are disconnected.

The heater power cards provide measurements of the delivered current and voltage (AC and DC), of the protection thermometer (thermocouple or resistive sensor) and of some analog measurements used to correct variations on the amplifiers or the ADC. To reduce cost and simplify the design, it was decided to use analog switches. Two analog switches using a radiation-hard technology and one commercial part were considered. For the commercial switch, two radiation campaigns took place; one at CNRAD exceeding the radiation design target and a second at the Proton Irradiation Facility (PFI) of Paul Scherrer Institute (PSI) in Zurich, CH. No failure was observed up to a tested TID of 2.3 kGy-Si at PSI (230 MeV protons).

The highest priority of the design is the safety of the LHC machine. The card satisfies all identified issues that could result in hazardous situations requiring intervention in the LHC vacuum envelope during LHC shutdowns. Extensive feedback information is available to provide online

error identification and diagnostics that could be used, as well, for assessing the ageing of the card components.

The new power card is designed to safely operate in the LHC environment even in close proximity to the higher radiation regions of the dispersion-suppressors.

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Presenter: TRIKOUPIS, Nikolaos (CERN)

Session Classification: Poster

Contribution ID: 12

Type: **Poster**

VIPRAM –2D Prototype and 3D Design

Wednesday, September 25, 2013 4:43 PM (1 minute)

Associative memory based track finding has been proven to provide a unique solution to fast silicon-based track trigger in the hadron collider environment. Future LHC experiments will demand greater speed and more patterns. While it is unlikely that scaling of 2D technology will satisfy the needs in a cost effective way, 3D Vertical Integration offers the possibility of dramatic improvements. The Vertically Integrated Pattern Recognition Associative Memory (VIPRAM) concept has been presented before. In this talk, we present details of the 2D prototype design, test results of fabricated chips with comparison to simulation studies and future project directions.

Summary

The VIPRAM R&D project has two goals. The first is the increase in pattern density through the use of vertical integration and circuit and geometrical (layout) enhancements. The second is the increase in speed and the improvements in system interface, especially with regard to Level 1 Tracking Trigger applications, through the use of system, circuit and layout enhancements. From the beginning, our design methodology has been to develop concepts and circuitry in 2D to confirm functionality as economically as possible and then translate, where necessary, those ideas into 3D. The first step taken by the VIPRAM Project was the development of a 2D prototype (protoVIPRAM1) in which the associative memory building blocks were laid out with an eye toward future vertical integration. In fact, the associative memory building blocks were laid out as if this was a 3D design. Room was left for as yet non-existent Through Silicon Vias and routing was performed to avoid these areas. The vertical integration approach taken thus far by the VIPRAM project reconfigures the pattern recognition algorithm into CAM cells and Control cells each of which ultimately will be integrated on different 3D Tiers. In protoVIPRAM1, there are four independent but identical CAM cells for each Control cell arranged into a unit called a protoLeg. Each protoLeg contains all the memory, comparison circuitry and evaluation logic necessary to perform the pattern recognition algorithm for one complete 4-layer road. protoVIPRAM1 is an array of 32 by 128 protoLeg cells. The readout circuitry is deliberately simplified to allow direct performance studies of the CAM and Control cells. protoVIPRAM1 was designed and fabricated in a 130nm Low Power CMOS process that has been used previously in High-Energy Physics 3D designs. The design has been thoroughly simulated at all levels and the prototype has been tested both for functionality and performance using a custom test setup. These simulation and test results will be presented and compared in this talk.

protoVIPRAM1 is a natural starting point for the project. The next two steps will be done in parallel and will, in fact, feed off of one another. protoVIPRAM3D takes the circuitry designed in protoVIPRAM1 and vertically integrates it. The Control cells are moved onto a Control Tier and the CAM cells become a CAM Tier. A maxim of this project is that given properly designed sub-circuits, vertical integration is a solution to pattern density limitations. protoVIPRAM2D, on the other hand, attempts to improve the readout speed of the associative memory chips and bring the system-level interface to maturity using conventional 2D VLSI with an eye towards Level 1 trigger applications. Several of the ideas created for protoVIPRAM1, most notably the square layout of the CAM cells and the simplified readout architecture, are being used as stepping stones for increasing readout speed and flexibility. The talk will cover the design and status of protoVIPRAM2D and

protoVIPRAM3D as well as the goals and directions of the project.

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Presenter: HOFF, Jim (Fermilab)

Session Classification: Poster

Contribution ID: 13

Type: **Oral**

SPADIC - Self-triggered charge pulse processing ASIC for CBM-TRD

Thursday, September 26, 2013 11:10 AM (25 minutes)

For the readout of the transition radiation detectors of the upcoming CBM experiment at FAIR, a self-triggered multi-channel mixed signal ASIC for signal amplification, digitization, and processing is under development.

The SPADIC 1.0 chip has 32 channels, each composed of a charge sensitive amplifier, a 9 bit pipelined ADC continuously running at 25 MHz sampling rate and a programmable digital filter for detector specific tasks such as tail cancellation and baseline correction.

The readout of whole signal snapshots is triggered by hit detection logic in each channel, or by selected neighbor channels. Data messages from the channels are multiplexed to a single output data stream preserving the order in which the hits were recorded.

The proper function of the ASIC has already been demonstrated in the lab and at a CERN beamtime. Further characterization is going on.

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Presenter: KRIEGER, Michael (University of Heidelberg)

Session Classification: ASICs

Contribution ID: 14

Type: Oral

A new Rad-Hard DC/DC buck converter ASIC for LHC experiment upgrades

Wednesday, September 25, 2013 9:50 AM (25 minutes)

In view of production for Phase1 LHC experiment upgrades a new DC/DC buck converter ASIC prototype has been designed and integrated in a commercial 0.35um technology.

This circuit is called FEAST and it has been designed for radiation tolerance up to the tracker levels and it can operate in strong magnetic field. In particular resistance to Single Event Transient has been enhanced in comparison to previous prototypes.

It provides stable voltage conversion from 12V to 600mV-5V with efficiency above 80%. It embeds also protection circuits as over-current, input under-voltage and over-current.

FEAST design details, first functional and radiation tests will be presented.

Summary

In view of LHC experiment upgrades, where the front-end electronics will require higher current at lower voltage, it is necessary to study a new power distribution scheme. We propose a solution based on inductor-based DC/DC buck converters, which allow local regulation, form an input voltage up to 12V to an output voltage in the range 600mV-5V.

The converter should work in a radiation environment with a magnetic field higher as high as 4T. For this reason, and in view for production for Phase1 upgrades, custom air core inductors have been developed in order to optimize the efficiency of the converter.

In this context a radiation hard buck converter ASIC, called FEAST, has been designed and integrated in a commercial 0.35um technology with high voltage extension. This converter operates at a switching frequency of 1.5-2MHz, with an inductance 200nH-400nH and output current from 0 to 4A.

Although the previous prototype (AMIS5, presented in TWEPP 2012) was functional, a number of issues needing to be addressed before production readiness were observed. In particular sensitivity to Single Event Transient has been detected during heavy ions irradiations. In order to identify the sensitive nodes, a pulsed laser test has been done and the found weak points has been reinforced or re-designed in FEAST.

In AMIS5, p-in-Nwell diodes are widely used as gate protection clamps in circuits working at 12V. After accurate tests and contact with the foundry we discovered that these diodes, when polarized in forward region, behave like bipolar transistors. The result is a "leakage" current (5-7 mA) flowing from Vin to substrate. Hence in FEAST these diodes has been changed with diode-connected transistors.

Additionally in FEAST the turn-off procedure has been completely re-designed in order to avoids stuck states detected in AMIS5 in some corner conditions (for example with fast input voltage transients from 10V to below 3V in less than 100us).

Samples of these circuits are expected back for testing in August, and first results - including some radiation tests at our X-ray machine - will be presented together with a detailed description of the functionality of FEAST. Plans for the pursue of the work will be presented, and in particular the organization for mass production for Phase1 upgrade.

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Session Classification: Power, Grounding and Shielding

Track Classification: Power

Contribution ID: 15

Type: **Poster**

Metrics and Methods for TTC-PON System Characterization

Tuesday, September 24, 2013 5:34PM (1 minute)

A new generation FPGA-based Timing-Trigger and Control (TTC) system based on emerging Passive Optical Network (PON) technology is being investigated to potentially replace the existing off-detector TTC system used by the LHC experiments. The new system must deliver trigger and data with low and deterministic latency as well as a recovered bunch clock with picosecond-level jitter. It also offers major improvements over its predecessor: bi-directionality as well as higher capacity. This article focuses on the figures of merit used to characterize the various flavours of TTC-PON system architectures, and on the techniques used to extract them.

Summary

The Timing-Trigger and Control (TTC) system is a crucial system dedicated to synchronization of experiment electronics to the LHC beam. Currently, it is a unidirectional network extensively deployed in all major detectors distributing the LHC bunch clock and the level-1 trigger accept decision (L1A) as well as individually addressed or broadcast commands to the various detector sub-partitions. To match the needs for increased payload capacity and to provide bi-directionality, a feature absent from the legacy TTC, a new generation TTC system is being investigated for off-detector use, based on Passive Optical Network technology (PON). A PON is a bidirectional (but single fibre) point-to-multipoint network architecture in which optical splitters are used to enable a master node or Optical Line Terminal (OLT) to communicate with typically 64 slave nodes or Optical Network Units (ONUs). It is based on mature devices, as the PON is nowadays the most successful solution worldwide for deploying FTTx networks.

A first TTC-PON demonstrator was built in 2010 during early investigations made at CERN, using commercial FPGAs and 1-Gigabit Ethernet PON transceivers. The first and very promising results motivated the work to explore the emerging XG-PON technology in order to better fit the user requirements in terms of latency and payload.

With the aim of proposing first prototypes for 2015, the present phase of the TTC-PON project consists of exploring several types of PON technologies and architectures being developed for commercial access networks. One or several potential solutions will be then identified and adjusted to experiment-specific TTC requirements in terms of bandwidth, clock recovery, upstream and downstream latency, as well as system feasibility, price, and compatibility with legacy TTC.

To fully evaluate and compare the performance of the existing and future TTC-PON system prototypes, a detailed set of characterization methods and criteria has been developed. The complete set consists of two groups: those that assess the functionality of the system; and those that relate to the various aspects of the enabling PON technology. The former cover: latency, payload size, recovered clock phase/jitter, and error detection/correction capability. Those related to the technology include: split ratio, dynamic range, upstream burst-mode sensitivity penalty, and CDR phase acquisition time. These parameters are evaluated by measuring Bit Error Rate (BER) and upstream Packet Loss Ratio (PLR) with changing network parameters such as split ratio, relative power ratio and phase of upstream consecutive packets, duration of the silence period between packets and training pattern duration. This article describes the metrics characterizing a TTC-PON network, the methods used to assess them and the results obtained so far.

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Session Classification: Poster

Contribution ID: 18

Type: Oral

The RCU2 - A Proposed Readout Electronics Consolidation for the ALICE TPC in Run 2

Tuesday, September 24, 2013 3:15 PM (25 minutes)

The RCU2 - A Proposed Readout Electronics Consolidation for the ALICE TPC in Run 2

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On behalf of the the ALICE TPC Collaboration

This paper presents a proposed optimization of the ALICE TPC readout for running at full energy in the Run 2 period after 2014. During these three years an event readout rate of 400 Hz with a low dead time is envisaged for the ALICE central barrel detectors. A new component, the Readout Control Unit 2 (RCU2), is being designed to increase the present readout rate by a factor of at least 2. The immunity to radiation induced errors will also be significantly improved by the new design.

Summary

A peak luminosity of $1 \text{ to } 4 \times 10^{27} \text{ cm}^{-2} \text{ s}^{-1}$ for Pb-Pb collisions is expected during the Run 2 period between Long Shutdown 1 and Long Shutdown 2 of the Large Hadron Collider. To take full advantage of these running conditions, an event readout rate of 400 Hz with low dead time of the experiment has been envisaged for the ALICE central barrel detectors, assuming a typical mix of trigger conditions. The readout rate of the current readout electronics saturate for central Pb-Pb events at about 320 Hz with 100% dead time, so actions must be taken to meet the demands of Run 2. Additionally, stability problems due to radiation effects have been observed in Run 1. These are expected to be worse with the increased energy and luminosity in Run 2.

The current Time Projection Chamber (TPC) readout electronics consist of 4576 Front End Card (FECs) that are read out by 216 Readout Control Units (RCUs). One RCU connects to a maximum of 25 FECs via two branches of a wide multidrop parallel bus. The RCU consist of a motherboard that hosts two mezzanine cards, The Detector Control System (DCS) card and the Source Interface Unit (SIU). The DCS card interfaces the DCS by Ethernet and the Trigger, Timing and Control (TTC) system via an optical interface. The SIU connects optically to the Data Acquisition (DAQ) System using the Direct Data Link (DDL) protocol. The bottleneck of the current readout electronics is the multidrop parallel bus between the FECs and the RCU.

In order to meet the requirements of Run 2 a new Readout Control Unit, the RCU2, will replace the present RCU board. The RCU2 will improve the readout-scheme such that the maximum readout rate of the TPC can at least be doubled, while also decreasing the susceptibility to radiation related errors. The RCU2 will host a MicroSemi Smartfusion2 FPGA. This is a state-of-the-art flash-based System-on-Chip (SoC) FPGA that promises very high radiation tolerance. Given the tight schedule, the architecture and infrastructure surrounding the RCU2 is left untouched. This imposes strict constraints to the design. For instance, the RCU2 must be housed in the same location as the present RCU, and the connection to the DCS, TTC and DAQ must be done reusing the existing cabling. The RCU2 will connect the same number of FECs as the current RCU, but by using four branches instead of two. By utilizing the increased parallelism in the FPGA design, as well as upgrading to the 5 Gbps DDL2 protocol, early calculations show that an increase in the readout rate by a factor of approximately 2.6 can be achieved.

The first prototype of the RCU2 is estimated to be ready later this year and the goal is to have the final design ready for mass production by spring 2014. This paper will give an overview of the RCU2, and a special focus will be given to the actions taken to increase the data rate and improve the radiation tolerance of the design.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

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Type: **Poster**

Common Read-Out Receiver Card for the ALICE Run2 Upgrade

Tuesday, September 24, 2013 5:21 PM (1 minute)

The ALICE experiment uses custom FPGA-based computer plug-in cards as interface between the optical readout link and the PC clusters of Data Acquisition (DAQ) and High-Level Trigger (HLT). The previous cards for DAQ and HLT have been developed as independent projects and are now facing similar problems with obsolete major interfaces and limited link speeds. A new common card has been developed to enable the upgrade of the read-out chain towards higher link rates while providing backward compatibility with the current architecture. First prototypes could be tested successfully and showed interest from other collaborations.

Summary

The ALICE Read-Out Receiver Cards (RORCs) used during Run1 implement the Detector Data Link (DDL) protocol via two optical links as interface to the detector frontend electronics and a PCI-X or PCIe Gen1 interface to the host PC. All previous versions of these boards are limited in link speed around the currently used 2.125 Gbps and the PCI-X interface used by some of the boards is hardly available any more in recent server systems. Coming towards Run2, some detectors are considering a higher read-out link rate. In order to overcome the interface limitations and provide room for link speed upgrades a new board has been developed as a common project of Data Acquisition and High-Level Trigger.

This Common Read-Out Receiver Card (C-RORC) holds a Xilinx Virtex-6 FPGA coming with a PCI-Express 8 lane Gen2 interface to the host PC and serial transceivers able to run at up to 6.6 Gbps. An optical interface with 12 links using parallel optical modules has been implemented to cover a complete TPC sector of 6 links with a single board on DAQ side while sending a copy of all data to the HLT with the remaining 6 links. This improved data locality allows earlier combination of data from different links and simplifies data collection for later processing stages. Detector data is transported from the FPGA into the host memory using Direct Memory Access (DMA). The FPGA provides sufficient logic resources to implement a 12 channel DMA engine and the possibility to do online data preprocessing. A flexible configuration management system ensures the correct configuration of the FPGA and allows to monitor, change and re-trigger the FPGA configuration process through sideband signals even if the PCIe interface is down. Two independent on-board DDR3 sockets for regular SO-DIMM memories as used in most mobile computers provide additional fast storage to the board.

The first C-RORC prototypes have been produced and could already be tested extensively. The board is detected reliably as 8 lane Gen2 PCIe device from the host machine and the custom DMA engine allows to push data into the host memory using the full available PCIe bandwidth. The DMA engine firmware implements scatter-gather DMA to allow non-continuous physical memory on the host machine. The software interface is realized with a custom microdriver and a userspace library. The compatibility and the throughput of the optical links using the DDL protocol could be verified with a test setup at CERN where the C-RORC was connected to the existing readout hardware. Higher optical link rates could be tested with pseudo-random bit sequences using two interconnected C-RORC boards. The DDR3 memory sockets could be confirmed to be working with different SO-DIMM modules up to 1066 Mbps.

Summarizing all hardware tests the board is perfectly suitable for operation in the current ALICE readout architecture and enables upgrades of detector readout links and preprocessing algorithms. Furthermore, the ATLAS experiment has comparable hardware requirements on the upgrade of their readout system and is strongly considering to also use this newly developed C-RORC.

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Session Classification: Poster

Contribution ID: 24

Type: Oral

A 65-nm-CMOS-process-based 10-Gbps VCSEL driver

Thursday, September 26, 2013 9:50 AM (25 minutes)

A VCSEL driver has been designed and fabricated in a SMIC 65-nm CMOS process. The preliminary testing results show the ASIC can work at 10 Gbps without peaking or emphasis structures. Due to the thin gate oxide of the technology and large size transistors used in the design, the VCSEL driver is potential radiation tolerant. We will present the irradiation testing results in the conference. To the best of our knowledge, the ASIC is the first VCSEL driver designed in a 65-nm CMOS process for high energy particle physics experiments.

Summary

In this paper, we present a Vertical-Cavity Surface-Emitting Laser (VCSEL) driver ASIC fabricated in a 65-nm CMOS process of Semiconductor Manufacturing International Corporation (SMIC). To the best of our knowledge, the ASIC is the first VCSEL driver designed in a 65-nm CMOS process for high energy particle physics applications.

The design objective is to amplify a 2-mA differential input current to an 8-mA VCSEL modulation current at 10 Gbps. The ASIC consists of three-stage current amplifiers without the use of any inductor peaking or emphasis structures. The VCSEL driver provides a pair of 50-ohm pull-up resistors at the output nodes for impedance matching. The ASIC is biased with a DC current of 6 to 8 mA. The modulation and the biasing currents are externally adjustable.

The VCSEL driver ASIC bare die has been bonded to a printed circuit board and the electrical performance is measured using a high-speed oscilloscope. When the input is a $2^{17}-1$ pseudo-random binary sequence (PRBS) running at 10 Gbps, the measured peak-to-peak jitter in the electrical eye-diagram is less than 20 ps (0.2 UI). The rise and fall times are about 50 ps without the use of any peaking or emphasis structures. With an input of 200 mV, the output current is 4.6 mA under a differential 100- Ω -ohm load. The measured transition times are larger than the simulated results and the measured amplitude is slightly less than the simulated one. The reason is still under investigation. The ASIC will be tested to drive a VCSEL and the testing results will be reported in the conference. The ASIC has been packaged in a 52-pin QFN package. The packaged chips will be extensively tested and the testing results will be reported in the conference.

The SMIC 65-nm CMOS process has a thin gate oxide and is potentially radiation tolerant for total ionizing dose effects. The ASIC is a current driver with large transistor size and is potentially radiation tolerant for single event effects. We will conduct irradiation testing within the next few months and will present the radiation performance of the VCSEL driver in the conference.

For future work, we plan to further improve the VCSEL driver design by adopting inductor peaking or emphasis structures to extend the bandwidth and to also include digital control interface circuit.

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Session Classification: Optoelectronics and Links

Contribution ID: 25

Type: **Oral**

LogAmp electronics and optical transmission for the new SPS beam position measurement system.

Wednesday, September 25, 2013 3:40 PM (25 minutes)

A new front-end electronics is under development for the SPS Multi Orbit Position System (MO-POS). Based on logarithmic amplifiers, it allows to measure the beam position and to resolve the multi-batch structure of the SPS beams. Analogue data are digitized at 10 MS/s and packed in frames by an FPGA. On every turn, a frame is sent to the readout board, via a 2.4 Gb/s optical transmission link. The first prototype has been successfully tested with several SPS beams. The system description and the first measurement results are reported.

Summary

The SPS Beam Position Monitors (BPM) are installed in the vacuum pipe and distributed all around the ring. They consist of opposite electrodes (A and B), either on the horizontal plane or on the vertical plane, which provide signals directly proportional to both beam position and beam intensity. In order to resolve the multi batch structure of the beam a new electronics is under development for the Multi Orbit Position System (MOPOS).

The analogue part of the Front-End (FE) board is based on Logarithmic Amplifiers (LA) and a differential stage which gives a direct measurement of the beam position ($\text{Log}(A)-\text{Log}(B)$).

For each BPM, the input stage is made of a low-pass structure that minimizes the bunch shape variation during acceleration, followed by band-pass filters, which create suitable signals for LAs. Three LA stages are necessary to cover the large SPS dynamic range related to different kind of particles, energies, and filling schemes. Each plane generates three analogue position signals, called Delta 200 MHz, Delta 40 MHz Low Sensitivity and Delta 40 MHz High Sensitivity. Finally the summation of the logarithmic outputs of each LA gives a kind of beam intensity measurement, which will be used to detect the beam presence and validate the acquisitions.

The digital part of the FE board consists of an octal 14-bit ADC (Analog Devices), an FPGA (Xilinx Spartan6) and a Small Form-factor Pluggable (SFP) optical transceiver. Analogue data are digitized at 10 MS/s and serialized. In the FPGA, each ADC measurement is tagged with a time-stamp with respect to the rising-edge of the SPS turn-clock. Data are then packed in frame every turn and transmitted to the readout board using a 2.4 Gb/s optical transmission link.

The FE board is designed to be placed in the SPS tunnel, where a dose rate of 100 Gy/y is foreseen in the worst working condition. Several components, such as the LAs, the ADC drivers and the voltage regulators have already been validated under radiation. The FPGA, the ADC and the SFP for the final version have still to be selected.

A preproduction of the new MOPOS system will be installed in 2013 in an SPS sextant. At least for one year, both systems, the current and the new-one, will run in parallel to validate the new MOPOS electronics.

The first FE prototype, installed out of the ring and connected to a "shoe-box"(vertical BPM) and to a Stripline (horizontal BPM), has been successfully tested using several SPS beams. The beam injection oscillations have been measured in both planes. Beam bumps of +/- 5 mm and +/- 2.5 mm have been reconstructed with the foreseen precision, while the +/- 1 mm bump measurements are affected by the ADC-Drivers noise. An optimized circuit is under production. The system description and a sample of the first measurements are reported.

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Presenter: DEPLANO, Caterina (CERN)

Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: 26

Type: **Oral**

Development and Testing of an Upgrade to the CMS Level-1 Calorimeter Trigger

Wednesday, September 25, 2013 11:10 AM (25 minutes)

The LHC will restart in 2015 with a higher centre-of-mass energy and luminosity. To allow the CMS physics programme to fully exploit these increases the CMS Level-1 trigger must maintain similar efficiencies for searches and precision measurements to those achieved in 2012. With an average of 50 interactions occurring in each bunch-crossing, it will be challenging to select interesting physics events within the readout bandwidth limitations. The CMS calorimeter trigger is being upgraded to enable the more sophisticated algorithms needed to handle the high-luminosity conditions and to add the flexibility to adapt to changing LHC performance and physics priorities. The design of the upgraded system is summarised, performance of the prototype hardware presented, and the results of integration tests between subcomponents shown.

Summary

When the LHC resumes operation in 2015, the higher centre-of-mass energy and high-luminosity conditions will require significantly more sophisticated algorithms to select interesting physics events within the readout bandwidth limitations.

The planned upgrade to the CMS calorimeter trigger will achieve this goal by implementing a modular and flexible system based on the micro-TCA electronics standard with Advanced Mezzanine Card (AMC) modules based on the latest Xilinx Virtex 7 FPGAs with up to 144 high-speed optical serial links, running at speeds up to 10 Gbps. Two variants of AMC modules are planned for the upgrade differing principally in the configuration of optical link I/O.

The upgrade will improve the energy and position resolution of physics objects, enable much improved isolation criteria to be applied to electron and tau objects and facilitate pile-up subtraction to mitigate the effect of the increased number of interactions occurring in each bunch crossing.

The design of the upgraded system is summarised, including hardware, software and firmware. Particular emphasis is placed on the results of prototype testing and the experience gained which is of general application to the design of such systems. For example, studies of high-speed signal integrity, advanced firmware systems for link alignment and monitoring, and novel version management tools for firmware.

The integration of prototype cards into a test system with Ethernet communication, trigger data-flow, timing control and a data-acquisition path is presented. Software and firmware for upgraded calorimeter trigger algorithms have been developed and results on their performance, including latency and FPGA resource usage will also be presented.

First results from integration tests between subcomponents are also included and finally future plans are summarised.

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Session Classification: Trigger

Track Classification: Trigger

Contribution ID: 27

Type: **Poster**

TRB3 264 Channel High Precision TDC Platform and Its Applications

Wednesday, September 25, 2013 4:55 PM (1 minute)

The TRB3 features four FPGA-based TDCs with <20 ps RMS time precision between two channels and 256+4+4 channels in total. One central FPGA provides flexible trigger functionality and GbE connectivity including powerful slow control. We present recent users' applications of this platform following the COME&KISS principle: Successful test beamtimes at CERN (CBM), in Juelich and Mainz with an FPGA-based discriminator board (PaDiWa), a charge-to-width FEE board with high dynamic range, read-out of the n-XYTER ASIC and software for data unpacking and TDC calibration in ROOT. We conclude with an outlook on future developments.

Summary

The 4+1 FPGA board "TRB3" can serve various applications in experimental particle physics and beyond due to its general-purpose design. It uses FPGAs as complex commercial electronic components while realizing the remaining auxiliary parts with simple standard components. Consequently, the board provides flexible connectivity by eight SFP ports and mezzanine extensions for every FPGA including a high pin-out for the peripheral FPGAs. We call this concept COME&KISS: COMplex COMmercial Elements & Keep It Small and Simple. This ensures a wide range of applications in data acquisition scenarios as well as a long-term maintainability of the platform.

Usually, in each of the four peripheral FPGAs a tapped delay line TDC is implemented with <20 ps RMS time precision between two channels providing 64 channels plus one reference channel. The TDCs are used for leading edge measurements or by using the TDC channels in pairs, one can additionally extract the width of the digital pulse. The central FPGA serves as a flexible central trigger system and manages slow control and read-out of the peripheral FPGAs over a single gigabit Ethernet connection. The project provides a comfortable, robust and modular software environment, ranging from low-level register access to the FPGA firmwares on the command line to high-level control via web2.0 technologies. This is complemented by comprehensive specifications and documentation.

To convert the analog signals from the detector to digital pulses suitable for the TDC, the front-end electronics board PaDiWa was designed using the differential input buffers of an FPGA as discriminators with a PWM generated voltage as a variable threshold. However, the charge information of the pulse extracted from time over threshold is usually not precise enough for calorimeters. Thus, the leading edge measurement can be complemented by a modified Wilkinson ADC circuit, which encodes the charge in the width of the digital pulse delivered to the TDC. A proof-of-concept board was successfully

tested and a version with an improved dynamic range is currently designed. Both approaches follow again the COME&KISS principle, already enabling other groups to use the existing FEE boards without major modifications. The overall reliability, flexibility and performance of this platform was proven in three test beamtimes with different detectors and FEEs at CERN (CBM), in Juelich and Mainz with up to 2400 channels, of which results are shown.

Furthermore, the TRB3 can be used as an infrastructure to read out specialized integrated solutions using the peripheral FPGAs, for example to provide a timing reference, transport the acquired data to the eventbuilder and slow control configuration of the chip. This was realized for the n-XYTER ASIC. Additionally, the platform enables every user group to profit from common software developments, such as a ROOT unpacker for the TDC datastream including the necessary calibration of the delay lines.

Finally, we present planned extensions of the platform: The detection of leading and trailing edge in a single TDC channel, which doubles the number of channels per board for timestamp and width measurements, and the integration in data acquisition frameworks such as DABC.

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Session Classification: Poster

Contribution ID: 30

Type: **Poster**

The CLARO-SiGe, a front-end ASIC for precise timing measurements at low power

Tuesday, September 24, 2013 5:01 PM (1 minute)

The CLARO-SiGe is a prototype ASIC for single photon counting with pixellated photomultipliers, designed to sustain a high counting rate at low power.

Each channel is made of a charge amplifier to readout the current pulses on a low impedance node and a discriminator with a settable threshold to count the pulses above threshold.

The architecture of the whole channel is differential.

The threshold of the discriminator is set through a small current injected through a dummy amplifier, which guarantees the symmetry of the differential configuration.

Each channel has two discriminators which can be operated at different speeds, in order to obtain the highest time resolution on the fast channel, while rejecting crosstalk signals thanks to the slower channel which is less sensitive to crosstalk.

Counting rates up to 40 MHz can be sustained.

The overall power consumption is about 1 mW per channel.

Summary

The CLARO is an ASIC for single photon counting with pixellated photomultipliers, designed to sustain a high counting rate at low power.

It is primarily designed to readout multi-anode photomultipliers (Ma-PMTs) in the upgraded LHCb RICH detectors.

The first 4 channel prototype, named CLARO-CMOS, was realized in a 0.35 CMOS technology, achieving a power consumption of about 1 mW/channel with counting rates up to 10 MHz.

A timing resolution down to 10 ps RMS for typical single photoelectron signals was demonstrated with the CLARO-CMOS on the test bench.

Another prototype was also designed in a 0.35 SiGe-CMOS technology, named CLARO-SiGe.

Whereas the CLARO-CMOS has four channels, the CLARO-SiGe has only two channels. The main purpose of the design is to test the difference between the two technologies, namely the larger readout speed which can be achieved at the same power consumption with SiGe transistors with respect to 0.35 μm MOS devices.

As in the case of the CLARO-CMOS, each channel is made of a charge amplifier to readout the current pulses on a low impedance node and a discriminator with a settable threshold to count the pulses above threshold.

From the point of view of channel architecture, the design features a number of improvements over the CLARO-CMOS.

The architecture of the whole channel is differential.

The threshold of the discriminator is set through a small current injected through a dummy amplifier, which guarantees the symmetry of the differential configuration.

The AC coupling between the amplifier and the discriminator which was present in the CLARO-CMOS was also removed.

Each channel has two discriminators which can be operated at different speeds, in order to obtain the highest time resolution on the fast channel, while rejecting crosstalk signals thanks to the slower channel which is immune to crosstalk.

Counting rates up to 40 MHz can be sustained.

The overall power consumption is about 1 mW per channel.

References:

CLARO-CMOS, a very low power ASIC for fast photon counting with pixelated photodetectors
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Journal of Instrumentation 8 (2013) C01029

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Session Classification: Poster

Contribution ID: 33

Type: Oral

Real-time Topology Processing in the ATLAS Level-1 Calorimeter Trigger

Wednesday, September 25, 2013 11:35 AM (25 minutes)

In 2015 the Large Hadron Collider will run with increased center-of-mass energy and luminosity. To maintain trigger efficiency against increased pileup rates, event topology information will be added to the ATLAS Level-1 real time data path and processed by a new Topology Processor (L1Topo). In phase-I, a new digital readout for the Liquid Argon calorimeters will provide finer granularity and depth segmentation in the electromagnetic layer to new Level-1 feature extractors (FEX) for improved EM, tau and jet identification. We present the topology and phase-I trigger upgrades to the ATLAS Level-1 trigger.

Summary

Luminosity upgrades to the LHC will mean that the ATLAS Level-1 trigger must deal with higher pileup while maintaining manageable trigger rates and high efficiency. Over the 2013-14 shut-down, firmware and hardware upgrades to the existing Level-1 Calorimeter Trigger (L1Calo) will add object coordinates and ET to the real time data path, and a new topology processor (L1Topo) will be added to Level-1. EM and hadronic tower sums are received in L1Calo by the Preprocessor, which in turn feeds two parallel processor subsystems the Jet/Energy-sum Processor (JEM) and Cluster Processor (CP). Jets and EM/hadronic clusters are identified by Jet/Energy-sum modules (JEMs) or Cluster Processor modules (CPMs), respectively. Common Merger Modules (CMMs) receive CPM/JEM results over backplane links and produce system-wide results. The upgrade to L1Calo includes upgraded CPM and JEM firmware to send trigger object data across the backplane at increased data rates. The current CMMs will be replaced by new "CMX" modules capable of receiving and processing the high-speed backplane data, and sending them over high-speed optical links to a new topological processor (L1Topo) subsystem. L1Topo will be capable of performing geometrical cuts and correlations, as well as calculate such complex observables as invariant mass. Real-time L1Topo output will be sent to the Central Trigger Processor CTP, where the final Level-1 accept decision is taken. In addition to the L1Topo architecture, we present crucial aspects of topology algorithm development, including optimal bandwidth, FPGA resources and latency. At phase-I in 2018, the luminosity of LHC will be increased to $\sim 3 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$. To improve the ATLAS Level-1 Trigger performance at phase-I, changes are needed at both the ATLAS detector and the Level-1 Trigger system. New on-detector electronics, the digital Tower Builder Board, will be installed on the Liquid Argon Calorimeter to provide trigger higher-granularity calorimeter information. New algorithms running in additional hardware will be added to the existing Level-1 Trigger to process these data, which are expected to give the required trigger performance with higher LHC pileup of phase-I running. The new off-detector digital processing chain will consist of two subsystems: a Digital Processor System (DPS) will perform digital filtering on the new digital calorimeter data and a feature extractor subsystem with Electron and Jet processors (eFEX, jFEX) will identify calorimeter trigger signatures. The eFEX will be designed as a modular subsystem, housed in two ATCA crates and consisting of around 20 modules, each receiving data on about 200 optical fibres at 6-10 Gb/s. These input optical fibres will go through dense optical backplane connectors in the ATCA Zone-3 area and terminate on parallel embedded optical receivers near FPGAs on the main modules. Information describing objects identified by the FEX subsystems will

be sent over optical fibres to a Topology Processor subsystem. We also present the motivation for architectural design choices, latest test results, and high-speed link simulations.

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Session Classification: Trigger

Track Classification: Trigger

Contribution ID: 39

Type: Oral

Irradiation Tests and Expected Performance of Readout Electronics of the ATLAS Hadronic Endcap Calorimeter for the HL-LHC

Wednesday, September 25, 2013 11:10 AM (25 minutes)

The readout electronics of the ATLAS Hadronic Endcap Calorimeter (HEC) will have to withstand an about 10 times larger radiation environment at the future high-luminosity LHC (HL-LHC) compared to the LHC design values. The radiation damages of the front-end electronics made in GaAs technology could significantly affect the HEC performance. Recent measurements of neutron and proton irradiation tests performed at LAr temperatures are reported, which allow an improved assessment of the expected degradation in HL-LHC conditions. These measurements are furthermore applied to simulations of the calorimeter performance. Results from replacement technologies, like Si CMOS, are also presented.

Summary

The Hadronic End-cap Calorimeter (HEC) of the ATLAS experiment at the CERN Large Hadron Collider (LHC) is a copper-liquid argon sampling calorimeter in a flat plate design. The pre-amplifier and summing (PAS) systems is the heart of the HEC read-out electronics and is realized in GaAs ASIC technology. The PAS devices are installed inside the LAr cryostat directly on the detector. They have been proven to operate reliably in LHC conditions, within safety factors. At the future high-luminosity LHC (HL-LHC), however, the front-end electronics will have to withstand an about 10 times larger radiation environment compared to the design values for LHC. Radiation damages in HL-LHC conditions could therefore significantly affect the HEC performance.

The GaAs ASIC has been exposed to neutron and proton radiation with fluences corresponding to ten years of running of the HL-LHC. Neutron tests were performed at the NPI in Rež, Czech Republic, where a 36 MeV proton beam is directed on a thick heavy water target to produce neutrons, delivering an integrated fluence of about 4×10^{15} n/cm² (in terms of 1 MeV-equivalent NIEL in GaAs at ATLAS). The proton irradiation was done with 200 MeV protons at the PROSCAN area of the Proton Irradiation Facility at the PSI in Villigen, Switzerland, up to an integrated fluence of 2.6×10^{14} p/cm². In-situ measurements of S-parameters in both tests allow the evaluation of frequency dependent performance parameters, like gain and input impedance, as a function of fluence. The non-linearity of the ASIC response has been measured directly in the neutron tests at warm. The signal response of the irradiated samples was analyzed furthermore at cold, i.e. at LAr temperatures. In particular these results allow an improved estimation of the expected performance degradation of the HEC.

The measured gain parameters and non-linearity of the ASIC response were applied to Monte-Carlo simulations of the HEC detector in order to extract the expected energy resolution and performance of jet measurements.

For a possible replacement of the PAS chips, alternative technologies are investigated and exposed to similar neutron radiation levels. In particular, IHP 250 nm Si CMOS technology has turned out to show good performance and match the specifications required. The corresponding results will also be presented.

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Session Classification: Radiation Tolerant Components and Systems

Contribution ID: 40

Type: Oral

Phase-I Upgrade of the Trigger Readout Electronics of the ATLAS Liquid-Argon Calorimeters and the Expected System Performance

Tuesday, September 24, 2013 2:51 PM (24 minutes)

The Phase-I luminosity upgrade of the LHC, planned for 2018, requires an improved trigger performance of the LHC detectors in order to suppress increasing pile-up noise. In the Phase-I upgrade of the read-out electronics of the ATLAS LAr Calorimeters high-granularity signals are provided to the Calorimeter trigger system for improved trigger feature extraction. The general design of the future LAr Calorimeter read-out system is being presented, including the newly developed system components for analog and digital signal processing, and high-bandwidth optical data transmission. Recent results of the simulated system performance for digital signal filtering and trigger feature identification will also be reported.

Summary

The ATLAS Liquid Argon (LAr) calorimeters produce a total of 182,486 signals which are digitized and processed by the front-end and back-end electronics at every triggered event. In addition, the front-end electronics is summing analog signals to provide coarsely grained energy sums, called trigger towers, to the first-level trigger system, which is optimized for nominal LHC luminosities. However, the pile-up noise expected during the High Luminosity phases of LHC will be increased by factors of 3 to 7. An improved spatial granularity of the trigger primitives is therefore proposed in order to improve the identification performance for trigger signatures, like electrons, photons, tau leptons, jets, total and missing energy, at high background rejection rates.

For the first upgrade phase in 2018, new LAr Trigger Digitizer Board (LTDB) are being designed to receive higher granularity signals, digitize them on detector and send them via fast optical links to a new LAr Digital Processing System (LDPS). The LDPS applies a digital filtering and identifies significant energy depositions in each trigger channel. The refined trigger primitives are then transmitted to the first level trigger system to extract improved trigger signatures.

This talk will present the general concept of the upgraded LAr calorimeter readout together with the various electronics components to be developed for such a complex system. The R&D activities as well as architectural and performance studies undertaken by the ATLAS LAr Calorimeter group will be described. The on-going design of mixed-signal front-end ASICs, of radiation tolerant optical-links, and of the high-speed off-detector FPGA based LDPS units will be presented.

The presentation will be completed by the simulated performance of the future system. In particular, recent studies of digital filter algorithms for energy reconstruction and bunch crossing identification based on FIR filters and on filters applying an active event-by-event pile-up correction are reported, together with the expected trigger performance exploiting the new fine-granularity read-out.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: 42

Type: **Oral**

Performance of the ALICE PHOS trigger and improvements for RUN 2

Wednesday, September 25, 2013 2:50 PM (25 minutes)

This paper will discuss the performance of the PHOS level-0 trigger and planned improvements for RUN 2. Due to hardware constraints the Trigger Region Unit boards are limited to an operating frequency of 20 MHz. This has led to some ambiguity and biases of the trigger inputs. The trigger input generation scheme was therefore optimized to improve the performance. Proposed actions to further improve the performance and possibly eliminate the impact of the biased trigger inputs will also be presented. A level-1 trigger input is currently also being developed and tested.

Summary

The Photon Spectrometer (PHOS) is one of the sub-detectors of the ALICE experiment, which shall generate level-0 and level-1 trigger inputs to the Central Trigger Processor (CTP). The PHOS level-0 trigger system consists mainly of two parts, 40 Trigger Region Unit (TRU) boards and 1 Trigger-OR (TOR) board. Local level-0 trigger inputs are generated by the TRUs according to the analog-sum singles, which represent the energy of the detected photons, and further processed by the TOR from which the final level-0 trigger input is sent to the CTP.

Ideally, level-0 trigger inputs should be issued at the peak point of the analog-sum signals, last for 25 ns (bunch spacing), and arrive at the CTP at a fixed time within the trigger input time window of 400-800 ns. However, due to hardware constraints the TRU operating frequency is limited to 20 MHz. As a result the level-0 trigger input pulses are wider than the bunch spacing, and furthermore, a phase shift of 25 ns can be induced between different TRUs due to the variation in the stabilization time of PLL clock outputs. This can lead to some ambiguity as the arriving time of the level-0 trigger input to the CTP may vary depending on which TRU generated the initial signal.

To reduce the impact of the TRU phase shift two trigger input generation schemes, short trigger scheme and long trigger scheme, were proposed. According to a performance comparison, the latter scheme was selected. It keeps the trigger input active as long as the corresponding analog-sum signal is above threshold, which results in a common time slot that can be aligned with trigger inputs from other sub-detectors.

The PHOS level-0 trigger system has been working with an acceptable efficiency and purity. This paper will discuss the performance of the PHOS trigger in light of the issues mentioned above, and look at possible actions for LS1 aiming to further improve the performance. For example, one suggested approach that can be implemented in the TOR to eliminate the phase shift between the TRUs and reduce the length of the trigger input, is to measure the average distance, at the beginning of a run, from the generated level-0 trigger input to the confirmed level-0 trigger from the CTP, and then re-synchronize the TRU trigger inputs accordingly.

In addition, a level-1 trigger input is being developed and tested in the lab. It will provide a more robust cluster energy estimate which allows to derive three level-1 trigger signals simultaneously for different energy thresholds. It is planned to be commissioned at Point 2.

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Session Classification: Trigger

Contribution ID: 43

Type: **Poster**

The high voltage power supplies of the CREAM experiment

Wednesday, September 25, 2013 5:24 PM (1 minute)

Abstract :

The environment conditions of the Long Duration Balloon flight are the worst possible for high voltage electronics which must survive at the altitude of 40km and a pressure of 5mbar in the Payload of the CREAM (COSMIC Ray Energy And Mass) balloon. Three different high voltage power supplies (1400V, 2000V and 12000V with a maximum consumption of 20 mA per module) were developed at LPSC for 3 CREAM sub-detectors.

The power supplies developed were based on two specific constraints. First, the sensitive cosmic ray detectors need very low noise and stable power (mettre un exemple si il te reste des mots). Secondly, the operation near the minimum of the Paschen curve lower the breakdown voltage to 300V/mm compared to 1KV/mm at sea level.

Summary

Long duration balloon flights around Antarctica occur under the worst possible environmental conditions for high voltage power supplies and no commercial modules were able to survive those conditions and to conform the requirements of the CREAM experiment. A dedicated design was then required for three different HV modules. Twenty -12kV modules with a very low noise requirement ; a hundred -1400V modules with a small size and low consumption ; Eight 3D modules specifically designed to fit inside the gas tubes and exiting polarization board.

When designing a high voltage power supply on a long duration balloon flight, it is first necessary to design the module with an extremely efficient protection against discharges which create corona and damage the device. A specific mixture was used to protect the electronic device, adapted to the high temperature variations, before the launch (>-20°C) in flight (~25°C) and during recovery (>-60°C). During the flight, the temperature is controlled and the metallic structure is used to evacuate heat by thermal radiation. The next step is to design the high voltage power supply using the solar panel, batteries and other secondary converters supplying -10V and +30V. Low current consumption from 9.5mA to a max of 20mA per module was also required. There were three families of modules supplying: -1400V for 1600 photomultipliers (for CHERCAM); +2000V used with 84 tubes with CF4 gas tube (for TRD) and -12000V connected to 40 hybrids photodiode (for the CALORIMETER).

Self-made sinusoidal transformers were built to create the heart of the module and they were used in the control loop. A dedicated mechanical housing was produced (UNAM) and provide shielding cavities for the high voltage filter, The Kokroft Volton with the high voltage divider and the control board. A low output ripple of 1.5mV at 12kV was obtained with this configuration.

These 3 different modules required thermal cycling and vacuum test validation at 5 mbar in spike detection mode. All the modules were constrained with five ramps from -40°C to +60°C. Evolution of output voltage, input current, temperature and pressure were monitored during thermal vacuum tests. The minimum of the Paschen curve was tested by varying the pressure from 1 to 20 mbar and detecting input current and output voltage spikes. If the corona effect is significant, the module is rejected.

Most of the faults observed on the test bench were from the HV test load which was also in the vacuum but is now well protected. Furthermore, the modules were integrated and tested at CERN for calibration before each flight.

Since 2008, these methods and the high voltage power supplies developed, ensured the success of embedded flights by balloon around Antarctica, and they will be used for the International Space Station next year.

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Session Classification: Poster

Contribution ID: 45

Type: **Poster**

Quality Assurance and Functionality Tests on Electrical Components during the ATLAS IBL Production

Tuesday, September 24, 2013 5:52 PM (1 minute)

During the shutdown 2013/14, for the enhancement of the current ATLAS Pixel Detector a fourth layer (Insertable B Layer, IBL) consisting of 14 staves is being built and will be installed between the innermost layer and a new beam pipe. A new read out chip

generation has been developed and two different sensor designs, a rather conventional planar and a 3D design, have been flip chipped to these front ends. New staves

and module flex circuits have been developed as well. Therefore, a production QA test bench has been established to test all production staves before integration with the new beam pipe.

Quality assurance measurements under cleanroom conditions, including temperature and humidity control, are performed on the individual components during the various production steps of the IBL, namely connectivity as well as electrical tests and signal probing on individual parts and assembled subsystems.

The pre-assembly QC procedures, the capabilities of the stave qualification setup, and recent results from stave testing are presented and discussed.

Summary

The Large Hadron Collider (LHC) is the largest and highest-energy particle accelerator in the world. The Pixel Detector is a subsystem of the ATLAS detector. It has 80 million channels and provides a lot of data to be used for identification and reconstruction of primary and secondary vertices.

During the shutdown 2013/14, for the enhancement of the current ATLAS Pixel Detector a fourth layer (Insertable B Layer, IBL) consisting of 14 staves is being built and will be installed between the innermost layer and a new beam pipe. A new read out chip

generation has been developed and two different sensor designs, a rather conventional planar and a 3D design, have been flip chipped to these front ends. New staves

and module flex circuits have been developed as well. Therefore, a production QA test bench has been established to test all production staves before integration with the new beam pipe.

With this setup all production staves will be tested to ensure the installation of only those staves which fulfill the IBL criteria. Quality assurance measurements under cleanroom conditions, including temperature and humidity control, are performed on the individual components during the various production steps of the IBL, namely connectivity as well as electrical tests and signal probing on individual parts and assembled subsystems.

The pre-assembly QC procedures, the capabilities of the stave qualification setup, and recent results from stave testing are presented and discussed.

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Session Classification: Poster

Contribution ID: 46

Type: **Poster**

DEPFET active pixel sensors for the vertex detector of the Belle-II experiment

Tuesday, September 24, 2013 6:12 PM (1 minute)

Active pixels sensors based on the DEPFET technology will be used for the innermost vertex detector of the future Belle-II experiment. The increased luminosity of the e+e- SuperKEKB collider entails challenging detector requirements, namely: low material budget, low power consumption, high precision and efficiency, and a huge readout rate. The DEPFET active pixel technology has shown to be the most suitable solution for this purpose. A review of the different aspects of the detector design (sensors, readout ASICS and supplementary infrastructure) and the results of the latest thinned sensor prototypes (50 μm) will be described.

Summary

The active pixel silicon sensor DEPFET technology has been chosen for the innermost vertex detector of the future Belle-II experiment in Tsukuba, Japan. The expected instantaneous luminosity of the future e+e- collider (SuperKEKB) is $\sim 8 \times 10^{35} \text{ cm}^2/\text{s}$ which is 40 times higher than the world record set by the former KEKB. The new vertex detector has to cope with stringent requirements in terms of performance and space allocation. It will have to deal with an increased event rate and higher background while still providing a high precision position measurement by minimizing the impact of the multiple scattering on the spatial resolution thanks to keeping the material budget the lowest possible.

The DEPFET technology has shown to be the most suitable for the two innermost layers of the vertex detector, close to the interaction point. This technology combines the detection together with the in-pixel amplification by the integration, on every pixel, of a field effect transistor into a fully depleted silicon bulk. An excellent spatial hit resolution can be achieved thanks to the low material budget while still having a high signal over noise performance. For Belle-II, DEPFET sensors with pixel sizes of $50 \times 50 \mu\text{m}$ and thinned down to $75 \mu\text{m}$ are currently being constructed. In the first prototypes, with a pixel layout close to the final Belle-II design and thinned down to $50 \mu\text{m}$, a S/N of ~ 35 and a spatial resolution below $10 \mu\text{m}$ has been measured in beam tests. A description of the key parameters of the sensor design and the different results of various prototypes tested in different test-beams will be presented.

The pixel matrix is read out in rolling shutter mode and different auxiliary devices are needed so a dedicated chain of ASICs has been developed. A DEPFET front-end module consists of a silicon frame where the DEPFET pixel matrix is implemented which also houses the steering and readout devices: Switcher-B, DCDB and DHP. The Switcher-B steers the control voltages of the DEPFET matrix, the DCDB is a multichannel ADC used to digitize the current signals from the sensors and the DHP performs the processing of the digital data, the module control and the data transmission at 1.8 Gbps rate. A general overview of the front-end module concept and mode of operation will be given.

Finally, also an outline of other supplementary systems like cooling, powering, mechanics, back-end electronics, etc. will be presented, together with the current status of the detector construction.

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Session Classification: Poster

Contribution ID: 49

Type: Oral

Soft Error Rate Estimations of the Kintex-7 FPGA within the ATAS Liquid Argon Calorimeter

Thursday, September 26, 2013 2:50 PM (25 minutes)

There is great interest in using Field Programmable Gate Arrays (FPGAs) within high-energy physics experiments due to their reconfigurability, ease of use, and support for high-speed serial I/O. SRAM-based FPGAs, however, are susceptible to radiation induced single event upsets. This paper estimates the soft-error upset rate of the Kintex-7 FPGA within the ATLAS Liquid Argon Calorimeter environment. Radiation experiments were performed on this device at the Los Alamos Neutron Science Center and the H4 beam line at CERN. Results from these experiments suggest that while single event upsets are present, they can be addressed with appropriate SEU mitigation techniques.

Summary

Field Programmable Gate Arrays (FPGAs) are an attractive alternative to application specific integrated circuits (ASICs) because of their in-field reprogrammability, low non-recurring engineering costs (NRE), and relatively short design cycle. They provide high logic density, access to the latest I/O standards, and can be designed with a variety of low-cost tools. FPGAs are increasingly used in non-traditional applications such as harsh environments and in safety critical systems. In particular, FPGAs are increasingly being used within high radiation environments such as spacecraft and high-energy physics experiments.

There is interest in exploiting the use of reprogrammable FPGAs within the ATLAS Liquid Argon Calorimeter (LAR). FPGAs are considered for data collection, simple processing, and communication functions. This environment, however, contains significant high energy hadrons that will upset the configuration memory, user memory, and block memory of the FPGA. This work evaluates the suitability of using the Xilinx Kintex-7 family of FPGAs within this environment by first, measuring its sensitivity to high energy hadrons with two radiation tests, and second, estimating the configuration upset rate within the ATLAS LAR environment.

The FPGA chosen for this work was the Xilinx Kintex-7 FFG900. This device was tested in a neutron beam at the Los Alamos Neutron Science Center in Los Alamos, New Mexico, USA, as well as in the H4 beam line within the North area of CERN in France. The purpose of these tests was to estimate the static upset cross section of the FPGA configuration memory and the internal block memory. To accomplish this, a simple design was created that uses all of the available block memory (BRAM) in the FPGA and limited control logic. The contents of the configuration memory and BRAM memory were periodically read and compared with the golden copy to identify upsets. After reading this memory, the contents are scrubbed and the procedure is repeated. The sensitive cross section was calculated by dividing the total upsets for each region by the total particle count that struck the FPGA per configuration bit. The same design and procedure were followed at LANSCE and H4.

The results from the LANSCE test suggest sensitive cross section of $7.49E-15$ n/cm² for the configuration memory and $6.69E-15$ for the BRAM memory. The results from the H4 test suggest a sensitive cross section of $1.51E-14$ HEH/cm² for configuration memory and $1.45E-14$ HEH/cm² for the BRAM memory.

The radiation environment of the ATLAS LAR environment has been modeled and simulations suggest that this environment will receive $3.1E10$ high energy hadrons per year. Multiplying the total particles by our cross section results and the number of configuration bits gives 41924 upsets per

year. This suggests a mean time between upsets of 12.5 minutes per device. Although the upset will occur relatively frequently, this upset rate is much larger than the scrubbing rate of these devices (less than a second). This result suggests that with appropriate mitigation and scrubbing, the Kintex-7 could be deployed within this environment. Future work will investigate configuration scrubbing architectures.

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Session Classification: Programmable logic, design tools and methods

Contribution ID: 50

Type: Oral

Next generation Associative Memory devices for the FTK tracking processor of the ATLAS experiment

Tuesday, September 24, 2013 12:00 PM (25 minutes)

The AMchip is a VLSI device that implements the associative memory function, a special content addressable memory specifically designed for high energy physics applications and first used in the CDF experiment at Tevatron. The 4th generation of AMchip has been developed for the core pattern recognition stage of the Fast TracKer (FTK) processor: a hardware processor for online reconstruction of particle trajectories at the ATLAS experiment at LHC. We present the architecture, design considerations, power consumption and performance measurements of the 4th generation of AMchip. We present also the design innovations toward the 5th generation and the first prototype results.

Summary

The AMchip ASIC is a VLSI device implementing a special kind of Content Addressable Memory (CAM) called associative memory (AM).

The main difference between a standard CAM and an AM is the possibility of the latter to identify correlations in data, while CAMs recognize single words. Precalculated coincidences of several data words received at different times are found by the AM in scrambled data streams. The correlations to be found can be also partial.

This function is especially useful for trajectory reconstruction in high energy physics applications. The data coming from different layers of the tracking detector is processed in parallel by the AM for pattern recognition and the ability to perform partial matching copes with the detector inefficiency. This approach was first used with great success by the CDF experiment at Tevatron with the SVT tracking processor where the pattern recognition stage was performed by an AM bank.

Since the first AM device of the late 90s several generations of AM chips has been developed. Here we present the 4th generation: AMchip04. This latest version has been specifically developed as a prototype for the FTK tracking processor for the ATLAS experiment at LHC. FTK is a second generation of tracking processor similar to SVT. The core pattern recognition function of FTK is performed by AM chips like in SVT.

The AMchip04 represents a major step in terms of design and technology with respect to the AMchip03 used in SVT. It has been developed in TSMC 65 nm CMOS technology using a mixed standard cells / full custom approach and it can store up to 8k patterns in a 14mm² die. The core associative memory block has been developed in full custom for maximum optimization in terms of power consumption and silicon area using several design optimizations. The control, I/O and computation logic is written in VHDL and synthesized in standard cells for faster development, re-usability and testability. For the first time it has been introduced the possibility to store ternary values (0, 1, X: don't care) in the AM bank. They will allow pattern recognition with variable resolution described in [doi:10.1109/ANIMMA.2011.6172856]. The chip is designed to run with a working frequency equal to 100 MHz.

The results of the tests performed on a batch of 100 AMchip04 dies is presented. Power consumption at different core clock rates is measured in detail with an estimation of the power consump-

tion of each component inside the chip (I/O, clock distribution, standard cell logic, full custom AM block). Consumption for a chip with a bigger pattern bank (64k) is projected to be under 1.9 W at 100 MHz. Yield is estimated.

Further development is needed toward a 5th generation of AM chip to meet the requirements to be installed in FTK experiment. We present the design and simulation results of an intermediate R&D mini@sic with 5th generation features: serialized I/O and lower consumption associative memory block.

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Session Classification: ASICs

Contribution ID: 52

Type: **Poster**

Pixel chip architecture optimization based on a simplified statistical and analytical model

Tuesday, September 24, 2013 5:02 PM (1 minute)

The technical challenges related to increased collision rates of the LHC will significantly affect detector electronics design. Efficient hit processing is achieved in pixel detectors by grouping pixel chips in regions, which share buffering logic. We present an approach to determine an optimized sharing strategy between pixels, depending on the shape of clustered hits in the detector. Simple statistical models of such shapes have been developed with respect to the position in detector where hits take place. Then the buffering performance of different pixel region configurations has been compared, showing significant improvement from architectures that do not feature pixel grouping.

Summary

New hybrid pixel detectors supporting hit rates up to 2GHz/cm² will be developed for future High Energy Physics experiments. In this scenario complex on-chip digital logic at the lowest possible power consumption will be designed requiring special techniques to develop a system working reliably.

We describe an approach to determine an optimized logic sharing in pixel chip arrays, depending on simplified shapes of clustered hits in a detector. A cluster is made of a certain number of hit pixels and its shape depends on a quantity of factors, e.g. position in the detector, pixel size, sensor thickness, discriminator threshold. In order to correctly process clustered hits each hit pixel should associate hit information to the same cluster without errors. This can be accomplished efficiently by grouping pixels in so-called pixel regions so that the buffering logic is shared between them. The optimal pixel region configuration to adopt is correlated to cluster shape. We have estimated the buffering performance of a set of pixel region configurations, with statistical assumptions on cluster shapes related to position in the detector. According to simulation data clustered hits shapes at the center of the barrel are symmetrical, while the ones at the edge are elongated along z direction. According to this we have respectively developed two simplified cluster shape models. The former have been modeled as square envelopes sized 3x3 pixels, where hit pixels inside it identify a cluster. For the latter one-dimensional shapes with variable z have been assumed; the more hit pixels constitute the cluster, the more elongated its shape is along z . Arbitrary statistical distributions have been constructed in order to provide information on the probability of each cluster model to be composed of a given number of hit pixels. From these assumptions we have calculated the required number of buffer locations for each pixel region configuration. We have quantified the bit depth of the hit information stored inside the shared buffer, as it depends on pixel region size. The study is currently being validated using detailed cluster footprint data from physics simulation in place of the simplified cluster model. Moreover, a suitable SystemVerilog verification environment is currently being developed to model the proposed pixel chip architecture in more detail. This verification environment will then be used for further architecture optimizations and will finally be used for extensive design verification.

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Session Classification: Poster

Contribution ID: 53

Type: Oral

Design of a Hardware Track Finder (Fast Tracker) for the ATLAS Trigger

Wednesday, September 25, 2013 3:15 PM (25 minutes)

The ATLAS Fast TracKer is a custom electronics system that will operate at the full Level-1 accept rate, 100 kHz, to provide high quality tracks as input to the Level-2 trigger. The event reconstruction is performed in hardware, thanks to the massive parallelism of associative memories (AM) and FPGAs. We present the advantages for the physics goals of the ATLAS experiment and the recent results on the design, technological advancements and testing of some of the core components used in the processor.

Summary

The existing three level ATLAS trigger system is deployed to reduce the event rate from the bunch crossing rate of 40 MHz to ~ 400 Hz for permanent storage at the LHC design luminosity of 10^{34} cm⁻² s⁻¹. When the LHC reaches beyond the design luminosity, the load on the Level-2 trigger system will significantly increase due to both the need for more sophisticated algorithms to suppress background and the larger event sizes. The Fast TracKer (FTK) will provide high quality tracks at the beginning of the Level-2 trigger, exploiting the massive parallelism of associative memories (AM) and FPGAs. We report innovative developments included in the detailed design of the system just completed.

An important characteristic of the system is its significant data reduction capability by clustering the incoming hits from the pixel sensors. This functionality will be implemented on a mezzanine board with two Spartan 6 FPGAs that process incoming data at full speed with small latency. The clustering algorithm is executed by multiple sliding window algorithms operating in parallel which achieve nearly linear processing time with respect to the number of readout hits.

The core of the system is composed of the associative memory board (AMBSLP) and a rear transition module (RTM) that have a very high computational power and I/O bandwidth. The AMBSLP is a 9U VME motherboard and contains four large mezzanines, the LAMBSLPs, where 64 AM chips are located. It has to support very large data traffic: a huge number of hits must be distributed at high rate with very large fan-out to all AM chips and a huge number of roads must be collected and sent to the RTM. A network of high speed serial links characterizes the bus distribution on the AMBSLP: 12 input serial links provide a 24Gb/s input bandwidth to the LAMBSLPs, and 16 output serial links are received from the LAMBSLPs for a total of 32Gb/s output bandwidth.

The RTM card for the FTK has to perform very intensive tasks: providing the input for the AMBSLP and doing a preliminary determination of the goodness of fit for the track candidates. The RTM needs access to the VME bus for configuration, setup and monitoring, something that is not normally possible for rear modules. This feature has been achieved using the J2 feed-through pins to communicate with the front module, extending the local data and address VME buses. Finally we will report on the studies to optimize the construction of the pattern bank used in the system. In order to make maximal use of variable resolution pattern recognition, which is achieved with ternary AM cells (storing 0, 1 or “don’t care” values) included in the new AM chips. We have performed extensive simulation studies searching for the best trade-off to maintain good efficiency and high rejection of random coincidences. We have found that even using a limited number of ternary cells, we can make a pattern bank that performs well in the harsh conditions expected for the LHC after the Phase-I luminosity upgrade.

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Session Classification: Trigger

Track Classification: Trigger

Contribution ID: 54

Type: Oral

Design and Performance of the VMM1 ASIC for Micropattern Gas Detectors

Thursday, September 26, 2013 11:35 AM (25 minutes)

Measurements of the first prototype VMM1 ASIC designed at Brookhaven National Laboratory in 130 nm CMOS and fabricated in spring 2012 are presented. The 64-channel ASIC features a novel design for use with several types of micropattern gas detectors. The data driven system measures peak amplitude and timing information in tracking mode including sub-threshold neighbors and first channel hit address in trigger mode. Several programmable gain and integration times allows the flexibility to work with Micromegas, Thin Gap Chambers (TGCs), and Gas Electron Multiplier (GEM) detectors. The IC design and features are presented along with measurements characterizing the performance of the VMM1 such as noise, linearity of the response, time walk, as well as calibration and performance measurements taken with a Micromegas detector.

Summary

The VMM1 is the first in a series of front-end ASICs designed for use with Micromegas and Thin Gap Chambers (TGCs) for ATLAS Upgrade. It features a range of gains and peaking times to allow use with other types of micropattern gas detectors as well. It incorporates several innovative features to allow operation in a fast trigger mode in the ATLAS Level 1 trigger as well as in a time projection mode for precision track reconstruction. The VMM1 features smart token passing reading out only those channels above threshold and their nearest neighbors in order to reduce the bandwidth and increase the potential for new physics.

The VMM1 design incorporates many features including an adjustable response that can be chosen based on different applications. The expected signal on a strip varies depending on the type of gaseous detector, detector capacitance, geometries such as gas gap and strip spacing, and gas amplification properties to name a few examples. The VMM1 can be tuned to optimize signal processing to take advantage of the full measurement range in order to get the most precise measurement values. For example, the simulation of the design performance predicts a charge resolution of approximately 5000 e⁻ for a 25 ns peaking time and 200 pF capacitance and a timing resolution of 1 ns for a 1 V signal amplitude.

The first iteration of the VMM was very successful with positive results in test bench and test beam conditions with Micromegas, TGC's, and GEM detectors. Measurements of the performance of the peak/time detection including noise, linearity, and time walk will be presented. The functionality of the threshold trims and threshold sub-hysteresis features will also be demonstrated. The performance will also be assessed using Fe55 and Sr90 with a Micromegas detector for calibration and signal resolution. Finally, we will give a summary of the new features of the VMM2, which is expected to be fabricated in fall 2013.

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Session Classification: ASICs

Contribution ID: 55

Type: **Poster**

Design and characterization of a GAPD pixel detector prototype for future particle trackers

Wednesday, September 25, 2013 4:44 PM (1 minute)

A monolithic GAPD (Geiger-mode Avalanche PhotoDiode) detector aimed to particle tracking at future linear colliders is being developed. A first prototype of a bidimensional GAPD pixel array has been designed and fabricated with a conventional 0.35 μm HV-CMOS process. The experimental characterization of the device shows that the expected noise counts generated by the sensor can be reduced to $\sim 10\text{E-}7$ fake pulses per bunch by time-gating the detector in the nanosecond scale while reducing the working temperature to $-20\text{ }^\circ\text{C}$. The design and complete characterization of the GAPD detector will be presented at the conference.

Summary

Physics aims at the ILC and CLIC projects impose such stringent requirements on detector systems that exceed those met by any previous technology. Amongst other novel detector systems, GAPD (Geiger-mode Avalanche PhotoDiodes) detectors are being developed to track high energy particles at future linear colliders. These sensors offer outstanding qualities, such as an extraordinary high sensitivity, ultra-fast response time and virtually infinite gain, apart from compatibility with standard CMOS technologies. In particular, GAPD detectors enable the direct conversion of a single particle event onto a CMOS digital signal in the sub-nanosecond time scale without the utilization of either preamplifiers or pulse shapers. As a result, GAPDs can be read out after each single bunch crossing. However, the generated signals are due not only to the absorbed radiation, but also to the intrinsic noise phenomena of the sensor which are originated by dark counts, after-pulses and cross-talks. Because the noise signals cannot be distinguished from real particle events and worsen the detector occupancy, solutions to reduce the sensor noise that are compliant with the severe specifications of next generation particle colliders are investigated.

A first prototype of a GAPD detector designed and fabricated as a proof of concept of such devices aimed to future particle trackers is presented in this contribution. The detector consists of a 10 x 43 GAPD pixel array in which the sensors and the readout electronics have been monolithically integrated with a conventional 0.35 μm HV-CMOS process. The pixels are composed of a 20 μm x 100 μm GAPD and a readout circuit that comprises 8 transistors only to achieve a 67% fill-factor, which is of the highest values that can be obtained with conventional 2D technologies. The fill-factor can be further increased to values close to 100% with the utilization of 3D technologies. The array presents an average DCR (Dark Count Rate) of 67 kHz at 1 V of excess bias. The array is operated in a time-gated mode (i.e. periodically activated and deactivated) to reduce the probability to detect the sensor noise down to $\sim 10\text{E-}4$ fake counts per bunch with an active period of 4 ns. Nevertheless, these figures can be further improved to $\sim 10\text{E-}7$ fake counts per bunch with the reduction of the working temperature to $-20\text{ }^\circ\text{C}$. The array is sequentially read out row by row during the quiet intervals between two consecutive bunch crossings. Measured results demonstrate that the proposed techniques are advantageous in improving the SNR (Signal-to-Noise Ratio), dynamic range and spatial resolution of the detector. The performance of the GAPD detector in beam-tests at CERN-SPS has also been explored. Details about the design and experimental characterization of the GAPD detector will be presented at the conference.

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Session Classification: Poster

Contribution ID: 59

Type: **Poster**

Pulsed power distribution for power supply isolation and remote 2-wire point-of-load regulation for the ATLAS Pixel Detector

Wednesday, September 25, 2013 5:25 PM (1 minute)

High common mode offset voltages can arise in the ATLAS Pixel detector module communication links that could prevent new Pixel Detector modules from taking data because of the present grounding and power supply schemes. Isolation of all the detector module electronics supply channels eliminates this risk. We propose that it is possible to provide inexpensive, reliable and serviceable power channel isolation by exploiting the ac characteristics of the installed ATLAS Pixel power distribution system. We also show how it is possible to achieve remote, 2-wire point-of-load voltage regulation by using pulsed power over existing Pixel cables.

Summary

The present ATLAS Pixel Detector shares each power supply channel across 6 or 7 detector modules, although cables are installed for each module power supply channel all the way to the power sources in the rack rooms, 80 m away from the detector. This power supply channel sharing breaks the electrical isolation among each group of modules.

By itself, this power channel sharing doesn't create a problem for detector operation but the Pixel grounding scheme includes a common point on each detector module for the return circuits of the digital power supply and analog power supply channels required for module operation. Furthermore, all the digital supply return lines are connected to a common grounding point in the detector package.

Under high beam luminosity conditions that require currents greater than 1 A in the digital supply for a module, this power sharing and grounding scheme can lead to return current paths that cause significant voltage offsets between the optical readout circuits and those same 6 or 7 modules in a group that are sharing a power channel. This offset can disrupt communication with the module, causing its loss for data taking. The new electronics to be installed with the next Pixel Detector upgrade, presently under construction, have a much more limited common mode offset voltage range than the currently installed detector modules, which will continue operating in the upgraded detector.

We present a proposal for economically achieving low voltage power supply isolation for each ATLAS Pixel Detector module electronics power supply channel by using an isolated ac power signal to drive the existing Pixel cable plant. Besides providing individual channel isolation, this method offers the possibility to limit the risk of damage to the Pixel detector module electronics from the failure of the nearby voltage regulator. We further show that it is possible to design an ac power isolation system by adding circuitry to the existing power distribution equipment in a way that doesn't require rewriting complex operation and monitoring software programs.

Results are shown for lab tests with a 100 m sample of the digital power cable used in the ATLAS Pixel Detector. The time response has been measured for various loads, power source frequencies and currents. The frequency response of the isolated power system is predicted by simulations and verified by S-parameter measurements of the cable sample.

The requirements to fully develop the proposed isolated power system are presented. This includes the limitations of the electronics simulators normally used for electronic designs involving transmission lines and suggests methods for working around these limitations. Evaluation of power

source frequencies and signal shapes for ac power distribution in terms of efficiency, cost and safety for the Pixel Detector modules are also included.

Additional advantages arising from implementation of the proposed isolation technology are demonstrated, including improved transmission efficiency and lower maintenance costs, as compared to the present Pixel power distribution system.

In the present ATLAS Pixel Detector power distribution system there is a risk that under high current operating conditions, a common mode offset voltage can develop between a Pixel detector module and its optical communication system, which receives and transmits data for module readout and operation. This offset can be high enough to cause upgrade module electronics, which operate with lower offset voltage ranges, to be inoperable with the installed Pixel modules, as was learned in the recent Pixel project to reconstruct and modify parts of the existing Pixel Detector package. Another instance of mixing new electronics with the existing detector module electronics comes with the Pixel Detector upgrade presently under construction, which will add a new layer of detector modules.

Providing electrical isolation for each power supply channel on each module eliminates the risk of disruptive offset voltages arising between the existing Pixel Detector module electronics and new modules operating with a more limited common mode offset voltage range.

Currently, voltage regulators near the ATLAS pixel detector are used, however, upgrades to the LHC will lead to a radiation environment that is too high to allow this configuration. The present Pixel power distribution system also carries a risk of subjecting a module's electronics to damaging voltage levels should the nearby voltage regulator fail. There are other limitations that arise for the design of voltage regulators to be used in an area of high radiation, limited heat removal capacity, highly restrictive mass limitations for physics reasons and little to no possibility to gain access for maintenance.

The advantages of achieving reliable remote point-of-load voltage regulation on detector modules for the high luminosity Pixel upgrade are clear.

We propose to exploit the ac transmission line characteristics of the installed Pixel power distribution system to achieve electrical isolation of each of the electronics power supply channels on each Pixel detector module. It is shown through lab tests of real Pixel Detector components, and on a scaled down Pixel detector, that electrically isolated ac powering of the installed power distribution system can be cost effective, reliable and efficient.

Furthermore, we show that another benefit of ac power distribution can be precise remote point-of-load regulation for future Pixel Detector module electronic designs over the same two wires that deliver power to the detector module electronics. Test results are shown that demonstrate the feasibility of remotely sensing the precise voltage at a power supply channel point-of-load – the detector module electronics – by use of ac power distribution over existing Pixel power cables. It is shown that this can be done without using inductors within the very large magnetic fields of ATLAS. Because the point-of-load voltage can be accurately monitored across the 80 m length of a Pixel power distribution system, the remote voltage regulator circuitry can be located in the rack rooms, which can be much more easily accessed for maintenance than can the hall where the ATLAS Detector sits and where the regulator is safe from exposure to damaging radiation.

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Session Classification: Poster

Track Classification: Power

Contribution ID: 60

Type: **Poster**

Single event upsets in the readout control FPGA of the ALICE TPC detector during the first LHC running period

Wednesday, September 25, 2013 5:51 PM (1 minute)

This paper will present and discuss measurement results of single event upsets in the readout control FPGA of the ALICE Time Projection Chamber during the first LHC running period. The measurements have been performed during stable beam conditions for proton-proton, proton-lead and lead-lead collisions.

Summary

The use of programmable logic devices such as FPGAs is a very attractive solution for High Energy Physics applications. With the ability to be reprogrammed in the field, FPGAs offer the flexibility to continuously develop and update already deployed instrumentation. However, a major caveat of SRAM based FPGAs are their susceptibility to radiation. As the configuration of the FPGA is stored in SRAM memory, single event upsets in this configuration memory may lead to a malfunction of the FPGA design. In the main tracking detector of ALICE, the Time Projection Chamber, a total of 216 SRAM based FPGAs are used to control the read out of data from the detector. A dedicated reconfiguration solution has been implemented to continuously detect and correct any SEUs in the configuration memory of these FPGAs. During the first LHC running period this reconfiguration solution has detected and corrected thousands of single event upsets and a summary of these measurements will be presented. Previously presented measurement data collected during $(s_{NN})^{1/2} = 7$ TeV proton-proton collisions will in this paper be updated with new results from $(s_{NN})^{1/2} = 8$ TeV proton-proton collisions, $(s_{NN})^{1/2} = 2.76$ TeV lead-lead collisions, and the very recent $(s_{NN})^{1/2} = 5.02$ TeV proton-lead collisions. The results will be compared to available Monte Carlo simulation data and discussed in light of the expected operational conditions for post LS1 and LS2 running periods, and future upgrade plans for the readout electronics.

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Session Classification: Poster

Contribution ID: 61

Type: Oral

A multichannel Time-to-Digital Converter ASIC with better than 3 ps-rms time resolution

Tuesday, September 24, 2013 10:15 AM (25 minutes)

The development of a new multichannel, fine-time resolution time-to-digital converter (TDC) ASIC is currently under development at CERN. A prototype TDC has been designed, fabricated and successfully verified with demonstrated time resolutions of better than 3ps-rms. Least-significant-bit (LSB) sizes as small as 5 ps with a differential-non-linearity (DNL) of better than +/- 0.9 LSB and differential-non-linearity (INL) of better than +/- 1.3 LSB respectively have been achieved. The contribution describes the implemented architecture and presents measurement results of a prototype ASIC implemented in a commercial 130 nm technology.

Summary

Very high time resolution detectors are getting ever increasing attention in the HEP community. Novel sensor designs have demonstrated time resolutions in the sub 10 ps-rms domain. To extract the full potential of such new sensor designs, fine-time resolution measurements in the ps regime have become necessary. A new multichannel, fine-time resolution time-to-digital converter targeted to full-fill the requirements of upcoming HEP detectors like the ATLAS AFP, CMS HPS or LHCb TORCH and many other HEP R&D programs is currently under development in the microelectronics section (PH-ME) at CERN. For one single design to be suitable for a larger set of applications a high degree of flexibility is required.

The TDC architecture is based on a Delay-Locked-Loop (DLL), with 32 elements, running with a 1.56 GHz clock frequency generating 20 ps LSB sizes. To achieve 5 ps LSB sizes, in a successive stage, a resistive time-interpolation concept is employed. Only one instance of the DLL and time interpolation circuit is implemented per ASIC and shared across all the channels. Distribution buffers are implemented to distribute the fine-time code of the interpolator to the respective channels. An on-chip adjustment feature is provided to compensate for device mismatches introduced by the fine-time interpolator and the distribution buffers. The adjustment only needs to be applied to a set of channels, avoiding the need for per-channel calibration.

To limit the susceptibility to power supply noise, the architecture has been developed to sustain fast signal slopes and short signal propagation paths of all timing critical signals. Process-voltage-temperature (PVT) variations are compensated by the feedback mechanism of the DLL. This auto-adjust feature of the DLL also gives raise to trade-off time-resolution against power consumption by changing its input clock frequency, offering less demanding applications to profit from a lower power consumption. A clock synchronous counter is added to extend the dynamic range of the interpolator.

A prototype, implemented in a commercial 130 nm technology, has been designed, fabricated and successfully tested. The fine-time interpolator together with 8 channels with different configurations have been implemented. To characterize the linearity of the TDC, a code density test has been performed. After calibration a differential-non-linearity (DNL) and integral-non-linearity (INL) of +/- 0.9 SLB and +/- 1.3 LSB has been achieved. The single-shot precision of the TDC has been evaluated by means of a time-difference measurement for different wire length differences. Across the whole measurement series a single-shot precision of better than 2.44 ps-rms has been demonstrated. The full prototype consumes between 34 mW/channel to 42 mW/channel. Lowering the input clock frequency to 781 MHz (= 10 ps LSB sizes), the power consumption can be reduced to 21 mW/channel and 26 mW/channel respectively. The architecture exhibits a time shift of -0.19 ps/mV and a temperature dependence of 0.44 ps/deg. With the measurement precision of

the test setup, inter-channel crosstalk between two neighboring channels has been evaluated to be below ± 1 LSB.

The prototype circuit has been found to be a suitable candidate for a full TDC development meeting the special requirements of next generation HEP detector designs. The delicate time interpolation circuit, will only need minor changes to be expanded from 8 channels to a larger set of channels. To allow to run at lower input clock frequencies (e.g. 40 MHz) and increase the dynamic range of the demonstrator ASIC a PLL and a counter will be added to such a new ps resolution TDC.

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Session Classification: ASICs

Contribution ID: 62

Type: Oral

MISTRAL & ASTRAL: Two CMOS Pixel Sensor Architectures dedicated to the Inner Tracking System of the ALICE Experiment

Tuesday, September 24, 2013 2:50 PM (25 minutes)

A detector, equipped with 50 μm thin CMOS Pixel Sensors (CPS), is being designed for the upgrade of the Inner Tracking System (ITS) of the ALICE experiment at LHC. Two CPS flavours, MISTRAL and ASTRAL, are being developed at IPHC aiming to meet the requirements of the ITS upgrade. The first is derived from the MIMOSA28 sensor designed for the STAR-PXL detector. The second integrates a discriminator in each pixel to improve the readout speed and power consumption. This paper will describe in details the sensor development and show the preliminary test results.

Summary

A major motivation for the upgrade of the Inner Tracking System (ITS) of the ALICE experiment is to extend the physics reach for charmed and beauty particles down to low transverse momenta. This requires a substantial improvement of the spatial resolution, material budget and the data rate capability of the ALICE-ITS. To achieve this goal, the new ITS is going to be equipped with 50 μm thin CMOS Pixel Sensors (CPS) covering either the 3 innermost or all the 7 layers of the detector.

In order to improve the sensor performances in terms of radiation hardness and readout speed, the sensor design at IPHC has migrated from a 0.35 to a 0.18 μm CMOS Imaging Sensor process. At the end of 2011, a first prototype, called MIMOSA32, was designed to validate the process. After the return from the foundry, the chip was extensively tested in the laboratory and at the CERN-SPS with $O(10^2)\text{GeV}$ hadron beams, before and after irradiation with a combined dose of 1Mrad and 1013neq/cm². A MIP detection efficiency of $\sim 100\%$ was measured at an operating temperature of 30°C.

In parallel with the process validation, two different sensor architectures, called MISTRAL and ASTRAL, are developed at IPHC. MISTRAL is derived from the ULTIMATE (MIMOSA28) sensor designed for the STAR-PXL detector. It is based on a column parallel read-out with amplification and correlated double sampling (CDS) inside each pixel of $22 \times 33 \mu\text{m}^2$. Each column is terminated with two high precision discriminators in order to read out 2 rows simultaneously. The matrix is read out in a rolling shutter mode (200ns/2-rows). The discriminator outputs are processed through an integrated zero suppression logic (SUZE02). The first level of the SUZE02 searches windows of 4×5 pixels which contain hit cluster information. The sparsified results are stored in 4 SRAM blocks allowing either continuous or triggered readout. The data are serialised onto a $\sim 1\text{Gbit/s}$ serial link. The MISTRAL sensor will have an active area of $\sim 1 \times 3 \text{cm}^2$ with a power consumption of $< 350 \text{ mW/cm}^2$ and a readout speed of $\sim 30 \text{ k frames/s}$. With its mature architecture, MISTRAL is presently the baseline sensor for the ALICE-ITS upgrade.

ASTRAL provides a further improvement of the MIMOSA28 architecture. The emerging architecture is called AROM (Accelerated Read-Out of Mimosa). Its read-out is based on a column parallel, rolling shutter mode, with an architecture similar to that of MIMOSA28. Thanks to the 0.18 μm CIS quadruple-well process, signal discrimination is embedded in each pixel. As a consequence, the analogue signals driving over centimetre long traces are replaced by the digital signals. This architecture has at least 2 advantages. The first one is a doubling of the pixel read-out frequency. The second is the power consumption reduction. With the same active area as MISTRAL, the expected power consumption of ASTRAL is $< 200 \text{ mW/cm}^2$ with a read-out speed of $\sim 60 \text{ k frames/s}$.

This contribution will discuss in details the design progress of the MISTRAL & ASTRAL sensors

and provide first test results of some of their prototyping chips.

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Session Classification: ASICs

Track Classification: ASICs

Contribution ID: 63

Type: **Poster**

SALT - new silicon strip readout chip for the LHCb Upgrade

Wednesday, September 25, 2013 4:35 PM (1 minute)

The LHCb detector, operating at the LHC proton-proton collider, has finished its Run I period. After more than two years of collision data taking the experiment accumulated corresponding integrated luminosity of around 3.1 fb^{-1} . The full recorded data sample will be used by physicists to search for New Physics and precise measurement of CP-violation in heavy flavor quark sector. Despite its superb performance it is clear that the LHCb experiment is statistically limited for a number of important

decay channels (such as $B_d \rightarrow K^* \mu \mu$ or $B_s \rightarrow \phi \mu \mu$). This, in turn, is related to the current data acquisition architecture which can acquire data at the top rate of 1.1 MHz at the instantaneous luminosity

close to $4 \times 10^{32} \text{ [cm}^{-2}\text{s}^{-1}]$. The LHC machine is already capable of delivering more than one order of magnitude higher luminosity that is presently used by the LHCb. This fact led the LHCb Collaboration to preparing a proposal regarding an upgrade of the LHCb spectrometer that would allow it to exploit higher luminosities (up to 2×10^{33}), greatly improve the trigger efficiencies for both hadronic and leptonic decay modes. The upgrade will allow the experiment to collect about 50 fb^{-1} of data. One of the most important topic of the LHCb upgrade is design and implementation of new front-end electronics allowing a full detector read-out at the bunch-crossing rate of 40 MHz. This will be further augmented by a software trigger that will be capable of processing the data at the same rate. This talk presents a novel design of the common readout chip for silicon strip detectors which will be able to digitise the analogue signal on-detector and subsequently perform digital processing and zero-suppression.

Summary

New front-end readout chip - SALT (Silicon ASIC for LHCb Tracking), is being currently designed by the Krakow group and will be used in the tracking system of the modernised LHCb experiment. The new chip must perform synchronously full processing and zero suppression of the raw data stream. This is a novel approach to the design of custom readout electronics circuits intended for the experimental High Energy Physics application. The SALT ASIC (Application Specific Integrated Circuit) can be used to instrument all silicon micro-strip sub-detectors of the upgraded LHCb spectrometer. Additionally, its back-end part may be employed in the readout systems of the scintillating fiber tracker

and the new RICH detector. This note aims at providing a detailed description of the digital processing chain that needs to be implemented within the chip.

Silicon microstrip sensors are being considered for the upgrade of the VELO (Vertex Locator), TT (Trigger Tracker) and IT (Inner Tracker) subsystems. It is therefore crucial for the LHCb upgrade that a FE readout chip

suited to this detector technology is developed. The R&D effort has indeed already started. Specifications for the chip design have been devised for the VELO, TT and IT strip detector options. The chip will integrate 128 individual readout channels implemented in the IBM 130 nm CMOS technology. From the operational point of view each channel will consist of an AC-coupled analogue FE amplifier-shaper, followed by a

6-bit ADC. The ASIC functionality will include zero-suppression and an interface with the GBT chip that will handle the high speed off-detector data transmission. A slow control block will be part of the design.

Commonalities with a SiPM (Silicon Photon Multiplier) FE readout chip for scintillating fibres will also be studied. Apart perhaps from the analogue FE part, the two applications might be able to share a large part of the chip design and developments. A first version of the 6-bit ADC and analogue FE block were recently submitted for manufacturing as part of a multi-project wafer.

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Presenter: SWIENTEK, Krzysztof Piotr (AGH University of Science and Technology (PL))

Session Classification: Poster

Contribution ID: 67

Type: **Poster**

Developments on DC/DC converters for the LHC experiment upgrades

Tuesday, September 24, 2013 5:50 PM (1 minute)

Prototypes of DC/DC converters were designed and built with the aim of satisfying the foreseen working parameters in the Phase 2 LHC experiments, using both MOSFETs and more recent devices like SiC and GaN transistors. Optimization of their design, based on the comparison between the simulated and measured thermal, electrical and mechanical performance, is in progress, and many improvements are under implementation.

Many tens of samples, chosen among the devices commercially available in the three different technologies, Si, SiC and GaN, were electrically characterized and tested under gammas, neutron, proton and heavy ion radiation, also using a combined run method.

Summary

Since three years the Apollo collaboration is developing technologies for designing high power DC/DC converters and high current Point of Loads (POL) able to cope with the electrical, mechanical and environmental requirements of the upgrades planned by the LHC experiments for both Phase 1 and Phase 2[1].

Several improvements on the power converter prototype described in [1] were implemented, mainly:

- the planar transformer made by multilayer printed circuit boards was replaced by a similar one made of thicker copper windings to better dissipate the internal heat and reduce copper losses;
- a specific heat sink was simulated, designed and manufactured, in order to remove most of the generated heat using a liquid coolant;

- a better thermal coupling between the transformer and the heat sink and a more robust connection to the external cables, which contributed to decrease the internal temperature of the transformer. The final paper will report on the detailed design and on the performed measurements, also including other improvements in progress like the replacements of controller and auxiliary converter.

High current POLs ($I_{out} \geq 20$ A) based on Gallium Nitride devices (GaN) are under evaluation. Several GaNs were electrically characterized using a dynamic test bench to be able to contemporarily measure the device currents and voltages during the switching time on inductive loads. They were also irradiated with protons at 7 MeV, using a Van der Graaf accelerator available at the INFN Laboratori Nazionali di Legnaro, up to $4 \cdot 10^{14}$ proton/cm², with good results.

The design of POLs with GaNs in the output stage is in progress, using a standard Buck topology, and its characterization will be shown.

Studies on core materials able to work in B field > 1 T without saturating is still in progress. With two starting materials and six binder combinations, twelve kinds of feedstock were developed and tested. Debinding and sintering in reducing atmosphere are the critical steps towards the target, and some optimization is still needed.

Device performance under radiation is a key feature of the project. Last year, commercial 200V/20A power MOSFETs were extensively tested with combined runs, first using a ⁶⁰Co source, available at the ENEA Calliope facility in Casaccia, up to 9.6 kGy, and after some weeks the same samples were irradiated with a ⁷⁹Br heavy ion beam at 150 MeV. The degradation of the gate oxide induced by gammas severely reduces the SEE sensitivity of the devices, and some samples failed because of a SEGR taking place at a lower voltage.

Power MOSFETs and Silicon on Carbide devices (SiCs) were also irradiated with neutrons, up to $6 \cdot 10^{12}$ 1MeV equivalent n/cm², at the ENEA Tapiro facility in Casaccia. Irradiation with protons of the same type of devices is still in progress at the Cyclotron facility of the INFN Laboratori Nazionali del Sud, Catania.

Combined runs on gammas and heavy ions are in progress for GaNs, while further neutron and proton tests are planned for summer 2013.

[1] M. Alderighi et al.: Power converters for future LHC experiments, TWEPP2011

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Session Classification: Poster

Contribution ID: 73

Type: **Poster**

10 Order of OF Magnitude Current Measurement Digitizers for the CERN Beam Loss Systems.

Wednesday, September 25, 2013 6:01 PM (1 minute)

A wide range current digitizer card is needed for the acquisition module of the beam loss monitoring systems in the CERN Injector Complex. The fully differential frequency converter allows measuring positive and negative input currents with a resolution of 31nA in an integration window of 2 μ s. Increasing the integration window, the dynamic range covers 2 \cdot 10¹⁰ were the upper part of the range is converted by measuring directly the voltage drop on a resistor. The key elements of this design are the fully differential integrator and the switches operated by an FPGA. The circuit is designed to avoid any dead time in the acquisition and reliability and failsafe operational considerations are main design goals. The circuit will be discussed in detail and lab and field measurements will be shown

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Presenter: VIGANO, William (CERN)

Session Classification: Poster

Contribution ID: 74

Type: **Oral**

Development of variable sampling rate, low power 10-bit SAR ADC in 130 nm IBM technology

Tuesday, September 24, 2013 9:50 AM (25 minutes)

The design and preliminary measurements results of 10-bit Successive Approximation Register (SAR) Analog to Digital (ADC) converter are presented. The prototype of the SAR ADC was designed and fabricated in 130 nm IBM technology. Preliminary measurements show that the ASIC is functional and the obtained ENOB (effective number of bits) is of about 9.2 bits. Power consumption of the ADC is around 1.1 mW per channel at nominal sample rate 40 MS/s. Maximum sampling frequency is around 50 MHz.

Summary

Nuclear pulse digitization is essential in the modern and future detector systems of particle physics experiments. Multichannel readout systems require a power and area-efficient analog to digital converters (ADC), particularly in the context of continuously growing number and density of readout channels. The Successive Approximation Register (SAR) ADC architecture allows to meet these two fundamental requirements giving additionally other features highly expected in readout system, such as power pulsing and the possibility of avoiding high frequency clock tree.

In this work we discuss the development of 10-bit SAR ADC for readout system of the luminosity detector at the future linear colliders (ILC/CLIC). We have designed a prototype ADC in 130 nm CMOS IBM technology. The ADC layout was prepared to target the multichannel implementation. The prototype ASIC comprises also a sampling pulse generator for generation of few ns pulses.

A fully differential architecture was chosen for the ADC design. It contains a pair of bootstrapped switches, a pair of Digital to Analog (DAC) converters which also perform the sample and hold task, a dynamic comparator and asynchronous dynamic control logic. To lower the power consumption the Merge Capacitor Switching (MCS) scheme was used allowing to reduce the DAC switching energy up to 93 percents compared to the conventional SAR ADC switching scheme. Dynamic architecture was chosen for both comparator and control logic to eliminate the static power consumption and so to obtain the power pulsing feature without any additional effort. Asynchronous control logic require only sampling clock and so avoids the fast clock distribution across the whole ASIC. The full circuit was designed, simulated and fabricated in 130 nm IBM technology. The ADC layout occupies 146 μm x 600 μm . The static measurements of fabricated ASIC shows that ADC prototype works satisfactorily with DNL below 1 and INL in range -1 to 1.1. Dynamic measurements show the ENOB around 9.2. Maximum sample rate of tested ADC is around 50 MS/s in agreement with simulations. For the default 1.2 V power supply and at 40 MHz sampling frequency the measured power consumption is around 1.1 mV. Sampling frequency is variable up to 50 MHz and the power consumption scales linearly with it. The detailed characterization of the ADC performance is in progress.

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Session Classification: ASICs

Contribution ID: 75

Type: **Poster**

Development of variable frequency, power Phase-Locked Loop (PLL) in 130nm CMOS technology

Tuesday, September 24, 2013 5:03 PM (1 minute)

The design and measurements results of low power Phase-Locked Loop (PLL) prototype for applications in particle physics detectors readout systems are presented. The PLL fabricated in 130nm IBM technology was designed and simulated for frequency range 10MHz-3.5GHz. Internal voltage controlled oscillator (VCO) should work in 16 frequency ranges/modes, switched either manually or automatically. Preliminary measurements done in frequency range 20MHz-1.6GHz showed that the ASIC is functional and generates proper clock. The PLL power consumption at 1GHz and division factor equal 10 is about 0.6mW. As one of main design goals the automatic VCO mode change was positively verified.

Summary

In modern and future detector systems of particle physics experiments, the data serialization and subsequent transmission with highest possible rate and lowest power becomes increasingly important, particularly in the context of continuously growing number and density of readout channels. The serialization and data transmission aspects are currently under study for the luminosity detector at the future linear colliders (ILC/CLIC) and for strip tracker readout in LHCb upgrade experiment. Since the readout architecture of these experiments comprises an ADC in each channel the data serialization from multichannel ADC needs to be implemented. After that a fast power-efficient serial data transmission out of detector is required. To allow two serialisation levels a variable frequency range PLL with different clock division factors is required.

In this work we discuss the development of the key block for serialization and data transmission i.e. the PLL. The design was optimized for highest clock frequency and low power consumption. The simulations show that PLL should work up to 3.5GHz. A standard second order Phase-Locked Loop architecture was chosen for the PLL design. It contains a Phase and Frequency Detector (PFD), a Charge Pump (CP), a Low Pass Filter (LPF) and a Voltage Controlled Oscillator (VCO). The "current starved" inverters were used in the VCO design. To obtain the highest frequency and the lowest power, VCO contains two separate oscillator rings, with different number of delay elements. The VCO operates in 16 modes for which different oscillator rings and bias current are used. Variable clock division factor equal 6,8,10 or 16 may be set in PLL feedback loop making the design more flexible. For instance it may be used to serialise output bits from 6, 8 or 10-bit ADC. The full circuit was designed, simulated and fabricated in 130nm IBM technology. The PLL layout occupies 300um x 300um. The prototype measurements were done in the frequency range 20MHz-1.6GHz at default 1.2V power supply and showed the proper circuit operation. Due to setup limitations higher frequency modes were not verified. In these measurements the VCO modes were switched manually. In the next step the automatic mode change was also positively verified in the same frequency range. It was also verified that all clock division factors are working properly. For the default 1.2V power supply, division factor equal 10 and at 1GHz PLL clock the measured power consumption was about 0.6mW. The power consumption scales linearly with PLL clock frequency at specific VCO mode. Power consumption to frequency ratio is smaller for higher frequencies, and depends on currently activated oscillator ring.

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Presenter: FIRLEJ, Mirosław (AGH University of Science and Technology (PL))

Session Classification: Poster

Contribution ID: 76

Type: Oral

A prototype hybrid pixel detector ASIC for the CLIC experiment

Tuesday, September 24, 2013 3:15 PM (25 minutes)

A prototype hybrid pixel detector ASIC whose design is tuned to the requirements of a vertex detector for CLIC is described and first electrical measurements presented. The chip has been designed using a commercial 65 nm CMOS technology and comprises a matrix of 64 x 64 square pixels each measuring 25 μm on the side. The main features include simultaneous 4-bit measurement of Time-over-Threshold (ToT) and Time-of-Arrival (ToA) with 10 ns accuracy, on-chip data compression scheme and power pulsing capability.

Summary

CLIC is a high energy linear particle accelerator which is currently under study at CERN. The requirements of its vertex detector concerning material budget, spatial resolution and, in particular, time stamp precision led to the design of a prototype hybrid pixel detector readout chip. A 65 nm low-power CMOS technology was chosen for the design. Preliminary studies were carried out at CERN to evaluate the radiation hardness of the technology [1]. A prototype fully featured chip with a matrix of 64 by 64 pixels was fabricated and tested. The pixel dimensions are 25 x 25 μm^2 pixels, allowing a subpixel spatial resolution of 3 μm . Each pixel contains an analog front-end consisting of a preamplifier with a Krummenacher feedback network [2], a fast comparator and a 4-bit Digital-To-Analog converter for threshold equalization. Each pixel can measure 4-bit Time over Threshold (TOT) and 4-bit Time of Arrival (TOA) simultaneously, with a pulse counting mode available for calibration purposes. The time-stamping accuracy is 10 ns due to a 100 MHz acquisition clock being broadcast to all pixels during the acquisition phase. In order to reduce crosstalk and noise, this clock is sent to each pixel with a different phase, using the delays of the clock buffers to implement this solution. All digital circuits were implemented with standard IP cells from the foundry and high-Vt (low-power) cells were used for low-speed circuits.

The readout is frame based, i.e. the data is read out from the chip after the acquisition and between CLIC pulse trains. To minimize the readout time and the power consumption, a configurable data compression scheme is implemented directly on-chip, allowing to skip the readout of pixels (or groups of pixels) without a valid hit. Simulations show that this solution is optimal for an expected occupancy of between 2% and 5%. The readout uses a single data line with a global 320 MHz clock, which is gated to each pixel column to minimize power consumption.

Due to the low power requirement of the vertex detector (less than 50 mW/cm^2), a power pulsing feature has also been implemented. Most of the analog structures in the pixel can be switched to a low power consumption state after the data acquisition has been completed. In order to minimize sudden changes in total power consumption, the power on/off of the array is applied one pixel column at a time, with configurable a delay between columns.

Electrical characterization has been done using a custom PCB connected to an FPGA for automated testing. Test results will be presented.

[1] S. Bonacini, P. Valerio, R. Avramidou, R. Ballabriga, F. Faccio, K. Kloukinas, and A. Marchioro. "Characterization of a commercial 65 nm CMOS technology for SLHC applications". *Journal of Instrumentation*, 7(01):P01015–P01015, January 2012.

[2] F. Krummenacher. "Pixel detectors with local intelligence: an ic designer point of view". *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 305(3):527–532, 1991.

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Presenter: VALERIO, Pierpaolo (CERN)

Session Classification: ASICs

Contribution ID: 78

Type: Oral

QIE10: A New Front-End Custom Integrated Circuit

Thursday, September 26, 2013 12:00 PM (25 minutes)

We present results on a new version of the QIE (Charge Integrating Encoder), a custom Application Specific Integrated Circuit (ASIC) designed at Fermilab. Developed specifically for the measurement of charge from detectors in high-rate environments, this most recent addition to the QIE family features 3 fC sensitivity, 17-bits of dynamic range with logarithmic response, a Time-to-Digital Converter (TDC) with sub-nanosecond resolution, and internal charge injection. The device is capable of dead-timeless operation at 40 MHz, making it ideal for calorimetry at the Large Hadron Collider (LHC). We present bench measurements and integration studies that characterize the performance, radiation tolerance measurements, and plans for deployment in the Atlas and CMS detectors as part of the Phase 1 and Phase 2 upgrades.

Summary

The QIE10 is the newest version in the family of QIE devices designed at Fermilab. It integrates input charge pulses in 25 nS time slices over a large dynamic range and digitizes the result with approximately constant resolution over the entire dynamic range. This is accomplished in a novel way by simultaneously integrating the input charge on four different ranges which are scaled by factors of 8. One of the ranges is selected for digitization based on the signal size. The selected output is digitized using an on-chip, pseudo-logarithmic, 6-bit flash ADC (FADC). The FADC bin size doubles several times over its full range, so that the bin size at the top of the FADC is 8 times the bin size at the bottom of the FADC. Since the 4 integrator ranges are also scaled by a factor of 8, the end result is that the QIE resolution (the FADC bin size divided by the signal magnitude) is held between 0.7% and 1.4% over the entire dynamic range of the QIE, which is approximately 17 bits.

This scheme provides a floating point digitization of the input charge at 40 MHz. The QIE10 digital output consists of 6 bits of mantissa (FADC outputs), 2 bits of exponent (range code), and 6 bits of TDC, which provides digitized pulse arrival time with respect to the 25 ns clock. The QIE operation is pipelined with 4 phases to allow dead-timeless operation, so a 2-bit “CapID” code is also provided to indicate which phase is associated with each result. Ideally, each phase or CapID has identical response, but in practice there can be small differences in the pedestal at the low end. The ability to adjust the pedestal of each phase is provided via the program shift register. The digital output result for a given integrated input pulse has a 4 clock period latency. Since the QIE10 is pipelined with 4 phases, it is integrating the input charge for the CapID0 phase while outputting the digitized result of the previous CapID0 integration. A block diagram of the device is shown in Fig. 1.

The new version of the QIE differs from earlier versions in several ways. QIE10 is the first QIE chip to be designed in the AMS 0.35 μ SiGe BiCMOS process. This will give greater radiation-hardness performance. The new design also has a factor of ten greater dynamic range than the previous version, from 30 pC up to 300 pC. Also, many different operational parameters can now be programmed via a serial program shift register (optional, since the register is set to default values upon power-up). A delay-locked loop and a timing discriminator with programmable threshold have been added in order to form a pulse-arrival TDC with 0.5ns resolution. The digital outputs provide data on each edge of the clock, for an effective 80 MHz parallel readout rate. The digital outputs can deliver true LVDS, as opposed to the “pseudo-LVDS” outputs of previous QIE chips. The device is in an advanced stage of prototyping. We have fully-functional devices that we have tested at the bench, and have also begun studies with detectors and integration into read-out

systems. We (will) have performed radiation tolerance studies. This is a joint development project. The device will be used in the CMS Phase-1 upgrade for the hadronic calorimeter, and is a candidate for use in the Atlas Phase-2 upgrade for the Tile Calorimeter. We will present the status of the project, and our plans going forward.

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Session Classification: ASICs

Contribution ID: 81

Type: **Poster**

Mitigation of Radiation and EMI effects on the Vacuum Control System of LHC

Wednesday, September 25, 2013 6:03 PM (1 minute)

The 26 km of vacuum chambers where circulates the beam of LHC (Large Hadron Collider) must be maintained under UHV (Ultra High Vacuum) to minimize the beam interaction with residual gases, and allow the operation of specific systems. The vacuum is measured by several thousands of gauges along the accelerator. Bad vacuum measurements may trigger a beam dump and close the associated sector valves. The effects of radiation or EMI (Electromagnetic Interferences) on components that may stop the machine must be evaluated and minimized. We report on the actions implemented to mitigate their impact on the vacuum control system.

Summary

The electronics of the vacuum control system are mainly located in the service areas. These underground areas are isolated shielded from the tunnel where the beam travels. Particle interactions with residual gases, collimators, and or other equipment (e.g. due to beam instabilities) are the source of ionizing radiation, with a rich and varied energy spectrum. With the rising of LHC's energy and intensity, some service areas have become too much exposed to these radiations, despite the available shielding, and can lead to malfunctions due to SEE (Single Event Effects). This resulted in an increase of equipment failures leading to beam dumps, which are time expensive for the machine operation. During the last runs of 2012, switching power supplies in valve controllers were destroyed; blocking of PLC (Programmable Logic Controller) CPUs (Central Processor Unit) were observed, most probably due to radiation-induced effects.

A shielding and relocation project was already born in 2010 to mitigate these types of events for the LHC at higher energies and intensities. During the LS1 (first long shut down), the vacuum control system will be mainly concerned in point-7 of the LHC: over 27 racks will be relocated and 350 cables must be extended into the new safe area; new features will be added, such as remote reset for slave PLC. This project will require the complete shutdown of vacuum controls for more than a year, during the dismantling activities; the NEG (Non-Evaporable Getters) activation and the bake-out of the vacuum chambers will require a minimal local control system to meet the established schedule of the LS1.

Some equipment is installed in the tunnel, without any shielding, and are subject to ionizing radiations, with a level depending on the location. The vacuum in the arcs is currently measured by active gauges, providing an analog signal 0-10V sent along twisted pairs to the PLCs installed into the protected areas. In order to better understand their tolerance, a test under radiation will be performed. Furthermore, a new and more accurate active gauge is under evaluation: it is also planned to be tested under radiation to evaluate the probable life time with an increasing beam energy and intensity.

Radiation is not the only source for disturbance or system failures: the electromagnetic environment in the tunnel and service areas is rich in interference sources. Given the dimensions of the machine, long cables are required to connect the instrumentation to the controllers; ground loop and coupling issues can easily become annoying and should be avoided, especially when signal levels are very low. A study to reduce measurement noise on ionization gauges was conducted: the first steps were applied during the 2012 winter technical stop. All the triaxial cables have been tested and repaired where necessary. A filter has been introduced in the shielding, to reduce coupling on the central conductor. The modification of the electronics in the controller was also

conducted during 2012, to center the measure and make a better filtering before sampling to be less susceptible to electromagnetic interferences.

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Session Classification: Poster

Contribution ID: 83

Type: **Poster**

Longevity of CMS ECAL Electronics

Tuesday, September 24, 2013 6:01 PM (1 minute)

The CMS Electromagnetic Calorimeter (ECAL) has played a vital role in the discovery of the Higgs Boson and other physics requiring the precise detection and measurement of electrons and photons. It is a homogenous lead tungstate scintillating crystal calorimeter with on-detector electronics based mainly on CMOS 0.25um ASICs and rad-hard gigabit optical links. The ECAL provides sums of energy of groups of up to 25 crystals, which are read-out at 40 MHz to be used as part of the level-1 trigger. On-detector circular buffers store the digital signals, with 12-bit precision, for up to 6.4us, sending the data out upon reception of a level-1 trigger. The ECAL will continue to be a critical component of CMS throughout the remainder of LHC operation, as well as during the precision study of, for example, Higgs physics at the High Luminosity LHC (HL-LHC) from about 2023 onwards. We assess the ability of the existing on-detector electronics to meet the demanding requirements of high luminosity running until 2035, including studies of the longevity of the electronics components and their susceptibility to ionizing and non-ionizing radiation. We conclude with an outline of possible upgrades to the electronics, both on-detector and off-detector.

Summary

The CMS electromagnetic calorimeter (ECAL) is used to detect and measure the energy of photons and electrons produced in collisions at the LHC. It has played a vital role in the discovery of the Higgs Boson and other physics requiring the precise detection and measurement of electrons and photons. It is a homogenous lead tungstate (PbWO₄) scintillating crystal calorimeter with on-detector electronics based mainly on CMOS 0.25um ASICs and rad-hard gigabit optical links. The ECAL provides sums of energy of groups of up to 25 crystals, which are read-out at 40 MHz to be used as part of the level-1 trigger. On-detector circular buffers store the digital signals, with 12-bit precision, for up to 6.4us, sending the data out upon reception of a level-1 trigger. The on detector electronics readout systems is organized in 4 different electronics boards, named "Motherboard" (MB), "Very Front End" (VFE), "Low Voltage Regulators" (LVRB) and "Front End" (FE). The MBs, installed near the crystals, route signals and power supply of Avalanche Photodiodes (APD) used to detect scintillation light coming from crystals as well as host the other boards (FE, LVRB). There are 4 VFEs and 1 LVRB boards for each MB installed vertically through connectors. The former host the preamplifier used to condition the signal coming from the APD and the analog to digital converter, the latter contains all the regulators used to generate the different low voltages (5, 3.3, 2.5 Volts) needed from the electronics starting from a single 5V generated from a system located in the CMS service cavern. The FE board, installed on top of the VFEs and LVRB through connectors, contains the FENIX ASICs used to buffer the energy values before to be send to the data acquisition sub-system through the optical link. The study of these four boards in order to understand their longevity is relevant because the ECAL will continue to be a critical component of CMS throughout the remainder of LHC operation, as well as during the precision study of, for example, Higgs physics at the High Luminosity LHC (HL-LHC) from about 2023 onwards. We assess the ability of the existing on-detector electronics to meet the demanding requirements of high luminosity running until 2035, including studies of the longevity of the electronics components and their susceptibility to ionizing and non-ionizing radiation. Different study approaches will investigate the electronics reliability starting from statistics on the data we have concerning failure rates during

the 2008-2012 running periods. In addition, failure analysis using existing military standards on reliability prediction of electronics equipment, measurements of critical parameters (temperature, humidity, ...) and accelerated aging test on spare boards and components. Information collected from the previous analysis will be the base to take a decision in the ECAL electronics upgrade activities forecast for the next years (2014-2021).

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Session Classification: Poster

Contribution ID: 85

Type: **Poster**

A DC-DC Conversion Powering Scheme for the CMS Phase-1 Pixel Upgrade

Tuesday, September 24, 2013 5:51 PM (1 minute)

A novel powering scheme based on the DC-DC conversion technique will be exploited to power the CMS Phase-1 pixel detector. DC-DC buck converters for the CMS pixel project have been developed, based on the AMIS5 ASIC by CERN. We will show the performance of these devices, including efficiency and line and load regulation at various temperatures. Reliability studies based on a preseries of 200 DC-DC converters as well as mass production techniques for the inductor and the magnetic shielding will be presented. Results from system tests of the full power chain of the pixel barrel detector will be discussed.

Summary

The CMS pixel detector will be replaced during the 2016/2017 shutdown with a device that features a higher hit efficiency, a smaller material budget and an improved radiation-tolerance. The new pixel detector will have one more layer of pixel modules with respect to the present detector, both in the barrel part and the end caps. A novel powering scheme based on the DC-DC conversion technique will be exploited to power the new detector, which comprises 1.9 times the channels of the present device.

We have developed DC-DC buck converters for the CMS pixel project, based on the AMIS5 ASIC by CERN. We will show the performance of these devices, including efficiency and line and load regulation at various temperatures, and a comparison of switching noise for various board layouts. A preseries of 200 DC-DC converters will allow us to study the quality and reliability with large statistics, for example with thermal cycling. Mass production of the toroid inductor and the magnetic shielding of the inductor was established and will be presented.

A prototype of the full power chain of the pixel barrel detector, comprising of 26 DC-DC converters, a DC-DC converter motherboard, the final power supplies (adapted to the DC-DC conversion scheme), further PCBs and cables, high voltage boards, a two-phase CO₂ cooling system, and the CMS pixel modules themselves, has been set up. Electrical and thermal results from these system tests will be discussed.

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Session Classification: Poster

Contribution ID: 87

Type: Oral

10Gbps TCP/IP streams from the FPGA for the CMS DAQ Eventbuilder Network

Thursday, September 26, 2013 3:15 PM (25 minutes)

For the upgrade of the DAQ of the CMS experiment in 2013/2014 an interface between the custom detector Front End Drivers (FEDs) and the new DAQ eventbuilder network has to be designed. For a loss-less data collection from more than 600 FEDs a new FPGA based card implementing the TCP/IP protocol suite over 10Gbps Ethernet has been developed. We present the hardware challenges and protocol modifications made to the TCP in order to simplify its FPGA implementation together with a set of firmware and hardware tests and performance measurements which were carried out with the current prototype. The measurements include tests of TCP stream aggregation and congestion control.

Summary

The CMS data acquisition (DAQ) collects data from more than 600 custom detector Front End Drivers (FEDs). In the current implementation data is transferred from the FEDs via 3.2 Gbps electrical links (SLINK) to custom interface boards, which transfer the data to a commercial Myrinet network based on 2.5 Gbps optical links.

During 2013 and 2014 the CMS DAQ system will undergo a major upgrade to face the new challenges expected after the upgrade of the LHC accelerator and various detector components. Particularly, the DAQ Myrinet and 1 Gbps Ethernet networks will be replaced by 10/40 Gbps Ethernet and Infiniband.

The interfaces to the FED readout links will be implemented with a custom board (FEROL) based on an Altera FPGA. The board supports two 10 Gbps and two 6 Gbps interfaces via four SFP+ cages. One 10 Gbps interface implements Ethernet for connection to the new DAQ eventbuilder-network. Three interfaces are used to read out data from upgraded FEDs via a basic point-to-point protocol.

For a reliable data transmission into the eventbuilder network we chose to implement the TCP/IP protocol suite on top of 10Gbps Ethernet interface in the FPGA. TCP/IP is a well known, reliable and standard protocol suite already implemented in the all mainstream operating systems. TCP contains congestion control which allows us to efficiently merge several low bandwidth TCP streams to one faster interface in Ethernet switch. The stream merging greatly reduces the amount of the network equipment required for the new DAQ network.

To limit the implementation complexity we designed a simplified version of the TCP protocol. Several simplifications were possible because our data traffic flows only in one direction and because the DAQ network topology is fixed and designed with sufficient throughput to avoid packet congestion. But we preserved the full compliance with the RFC 793. Therefore we can use a PC with the standard Linux TCP/IP stack as a receiver.

The main simplifications includes:

1. We reduced the number of required TCP states from 11 to 3. The FEROL can open TCP connection and keeps the connection open until it is terminated. If an error is detected, the connection is terminated immediately.
2. The TCP complex congestion control was reduced to exponential back-off to decrease the throughput when temporary congestion is detected. A fast-retransmit algorithm is also implemented to improve the throughput in case a single packet loss is detected.

The current prototype board is equipped with low cost Altera Aria II GX FPGA, where 30% of the available resources are required for the TCP/IP and Ethernet interface. The board also contains 512MBytes of DDR2 memory for input and TCP socket buffer. Two TCP/IP engines were implemented allowing to open one or two simultaneous TCP streams.

The preliminary results show a maximum stable throughput of 9.7 Gbps for a direct connection between the FEROL prototype and a PC. With 16 TCP streams from 8 prototypes merged into one 40 Gbps interface via a switch we achieve 39.6 Gbps of stable data throughput.

We found that the maximum throughput is greatly sensitive to the receiver's PC configuration. In particular hyper-threading setting and network card IRQ and CPU affinity settings have to be tuned to achieve optimal performance.

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Session Classification: Programmable logic, design tools and methods

Contribution ID: 90

Type: **Poster**

A New High-Speed Optical Transceiver For Data Transmission at the LHC Experiments

Tuesday, September 24, 2013 5:35 PM (1 minute)

We report on the development of a new commercial off-the-shelf optical transceiver as a candidate for the transmission of data from the detector to the counting room for experiments at the Large Hadron Collider (LHC). The device is manufactured by Molex using CMOS integrated silicon photonics developed by Luxtera. A transceiver contains four RX and four TX channels operating at 10 Gbps each, and is packaged in a QSFP+ format. The approach features superb manufacturing costs, power consumption, scalability, and reliability. We present performance measurements, radiation tolerance measurements, and plans for deployment in the ATLAS experiment at the LHC.

Summary

We report on the development of novel commercially-available optical transceivers as a candidate technology for high-speed data transmissions from the ATLAS detector at the LHC to the counting room. These devices are manufactured by Molex using CMOS-integrated silicon photonics developed by Luxtera, a ground-breaking platform for building high-speed optical interconnects. A candidate transceiver is required to be radiation-tolerant, highly-reliable, cost-effective, with low bit-error-rate (BER), and with low power consumption. The proposed device satisfies all the requirements even after exposure to ionizing radiation.

Entire functionality of a transceiver is implemented in a single chip containing four RX and four TX channels operating at 10 Gbps each. Optical devices and transistors are constructed side-by-side monolithically in the silicon. The optical chip is directly coupled single-mode optical fibers packaged into a ribbon cable. The single-mode fibers can be operated at higher speeds if that is needed in the future. Modulation in the TX channels is done by Mach-Zehnder interferometers fed by a single continuously-running laser. This design enables cost-effective manufacturing and high reliability of the device.

The radiation tests have been performed using gamma-rays from Co60, neutrons, and energetic protons. Results of the tests demonstrate that the product is a promising solution for radiation-intense environments such as at the ATLAS experiment at CERN. During the tests we have monitored characteristics of the device such as BER, temperature, consumed power.

We plan to deploy these devices for transmissions of data from the Tile (hadronic) calorimeter of the ATLAS detector to the counting room in about 2022. Before that they will be tested in the demonstrator project. The transceivers can also be utilized for other sub-systems of the ATLAS detector.

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Session Classification: Poster

Contribution ID: 91

Type: **Poster**

The management of large cabling campaigns during the Long Shutdown 1 of LHC.

Tuesday, September 24, 2013 6:13 PM (1 minute)

The consolidation and upgrade of the cabling infrastructure of the CERN accelerator complex is one of the most critical activities of the LHC Long Shutdown 1. This implies an extraordinary challenge in terms of project management, resource and activity planning, quality control and manpower organization. About 1000 km of both copper and optical fiber control cables have to be newly installed or replaced, representing an investment of about 15 MCHF.

The preparation phase of this project started well before its implementation, by defining technical solutions and setting financial plans for staff recruitment and material supply. Enhanced task coordination was further implemented by deploying selected competences to form a central support team. A tool for progress monitoring was developed to facilitate the dynamic redistribution of manpower.

Summary

The Large Hadron Collider (LHC) at CERN entered into its first two-year-long shutdown period (Long Shutdown 1, LS1) in February 2013. During this period the entire CERN accelerator complex, will undergo major consolidation and upgrade works, preparing the machines for LHC operation at nominal energy (7 TeV/beam).

In this framework one of the most important activities is the removal, replacement and installation of copper and optical fiber cables used for instrumentation, networking and control systems. Around 1000 kilometers of cables, distributed in different machine areas, will be installed. This activity will be carried out mainly by the Cabling and Optical Fiber (CF) section in the Electrical Engineering group (EL) of the CERN Engineering Department (EN).

The activity requires substantial project management efforts and a massive deployment of resources, consisting of CERN staff and external contractors, to complete all the expected tasks within the planned dates. A progress monitoring method was defined to manage the extraordinary increase of cabling projects (about four times more the normal yearly workload of the section, for a total investment of roughly 15 MCHF).

The section's structure was enhanced, introducing support functions for assisting the management in the critical coordination aspects. Five contracts were set up with external firms to carry out the planned cabling projects. Supply of qualified material was organized as from 6 months to one year in advance.

All the cabling installations were grouped by geographical campaigns to facilitate the resource and material distribution and to optimize the intervention time in those areas. The campaign time-slots have been fitted in the planning by increasing as much as possible parallel tasks and by looking for a good compromise between the accelerators' priorities and users' requests. Resource optimization was finally achieved by smoothing manpower peaks where possible.

The development of a specific progress monitoring tool guaranteed the weekly monitoring of the cabling activities, allowing for a dynamic redistribution of the resources in case of delayed or anticipated schedule.

This paper describes how this method was implemented and presents the achieved results.

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Session Classification: Poster

Contribution ID: 92

Type: **Poster**

An Ultra-Fast Data Acquisition System for Coherent Synchrotron Radiation with YBCO Terahertz Detectors

Tuesday, September 24, 2013 6:14 PM (1 minute)

The recording of coherent synchrotron radiation requires DAQ systems with high temporal resolution. To resolve ultra-short terahertz pulses emitted by single bunch YBCO superconducting thin film detectors have been developed. A novel data acquisition system for sampling of the individual ultra-short terahertz pulses with high accuracy and real-time data processing is presented. The DAQ system is designed to sample the fast pulse signals with sampling times down to 3 ps. The data acquisition and the terahertz YBCO detectors have been tested at the synchrotron ANKA at KIT. The concept and the first results with single and multi-bunch filling pattern are discussed.

Summary

Since a few years coherent synchrotron radiation (CSR) generated by short electron bunches is provided at the ANKA light source. Electron bunches can be filled in up to 184 buckets with a distance between two adjacent bunches of 2 ns corresponding to the RF system frequency of 500 MHz. Arbitrary filling patterns can be used to study the interaction of adjacent bunches in CSR. To detect and study the THz emission characteristics of CSR over multiple revolutions a detector system based on thin $\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}$ (YBCO) superconductor film detectors can be used. The intrinsic response time of YBCO thin films is only a few picoseconds and allows one to resolve the signal of individual bunches even within a multi-bunch environment. Response transients excited by CSR THz pulses as short as 17 ps has been determined as the FWHM at the output. A novel system for fast and continuous sampling of the individual ultra-short terahertz pulses has been developed. The setup is accomplished by real-time data processing based on high-end graphics processing units (GPUs). The data acquisition system consists of detector, low-noise amplifier, fast pulse sampling FMC board, readout board and the readout PC. The analog output of the low noise amplifier operating at ambient temperature is connected to the fast sampling board. Four samples are recorded in parallel for each terahertz pulse with programmable sampling times in the range of 3 to 100 ps. The readout board provides programmable logic (FPGA) and large memories for on-line data processing and temporary storage. The FPGA performs an on-line pulse reconstruction and calculates both the peak amplitude of each pulse and the time between consecutive bunches with a picosecond time resolution using fast waveform sampling technics. Finally, the data is transmitted to the readout computer. The readout interface is realized by a bus master DMA engine connected to PCI Express endpoint logic to ensure a high data throughput of up to 2 GByte/s. The fast pulse sampling board and the high data throughput board have been tested with terahertz YBCO detectors at ANKA. Multi-turn measurements of CSR have turned out to be an important diagnostic tool for storage rings with short bunch operation. With the DAQ system it is possible to resolve the bursting behavior of single bunches even in a multi-bunch environment to study the bunch-bunch-interactions.

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Session Classification: Poster

Contribution ID: 93

Type: Oral

The Read-Out Driver (ROD) card for the ATLAS experiment: commissioning for the IBL detector and upgrade studies for the Pixel Layers 1 and 2

Tuesday, September 24, 2013 3:40 PM (25 minutes)

The upgrade of the ATLAS experiment at LHC foresees the insertion of an innermost silicon layer, called Insertable B-layer (IBL). IBL read-out system will be equipped with new electronics. The Readout-Driver card (ROD) is a VME board devoted to data processing, configuration and control. A pre-production batch has been delivered in order to perform tests with instrumented slices of the overall acquisition chain, aiming to finalize strategies for system commissioning. In this contribution both setups and results will be described, as well as preliminary studies on changes in order to adopt the ROD for the ATLAS Pixel Layers 1 and 2.

Summary

During the first long shutdown of the LHC collider in 2013/14, the Atlas experiment will be equipped with an innermost silicon layer, called IBL. Read-out electronics have been redesigned in order to accomplish the IBL performances. A new front end ASIC (FE-I4) has been designed as well as new off-detector devices. The latter are two 9U-VME cards called Back-Of-Crate and Read-Out Driver (ROD). The ROD is devoted to data processing, configuration and control of the overall read-out electronics; the number of total boards to be installed on the experiment is . The design is based on modern FPGA Xilinx devices: one Virtex-5 with embedded PowerPC for enhanced control purposes and two Spartan-6 gathering the front-end output, building the events and processing data in dedicated calibration runs. After the first prototyping samples a pre-production batch has been delivered with a finalized layout.

In this contribution it will be described strategies, setups and tests developed for the goal of commissioning the ROD cards into the IBL acquisition system.

In particular, it will be shown how integration tests have been performed by increasing the level of system complexity: slices of the IBL read-out chain are being instrumented and ROD performances are verified in a test bench mimicking a small-size final setup.

In parallel, the firmware is developed and certified under work-cases similar to the ones expected during the IBL data taking. Major achievements from the tests performed with the overall acquisition chain will be emphasized, since their accomplishment is crucial for the successful commissioning of the system.

This contribution will report also an outlook on the possible adoption of the IBL ROD for ATLAS Pixel Layer 1 and 2. The higher luminosity that will be foreseen into LHC after future upgrades will require more performances for the acquisition system, especially in term of throughput. Estimation of future requisites for the electronics of Layer 1 and 2 will be show and last, it will be discussed whether the adoption of the IBL ROD or an upgraded version could be a viable solution.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: 94

Type: **Poster**

Performance evaluation of multiple (16 channels) sub-nanosecond TDC implemented in low-cost FPGA

Wednesday, September 25, 2013 6:08 PM (1 minute)

NA62 experiment Straw tracker frontend board serves as a gas-tight detector cover and integrates two CARIOCA chips, a low cost FPGA (Cyclon III, Altera) and a set of 400Mbit/s links to the backend. The FPGA houses 16 sub-nanosecond resolution TDCs with derandomizers and an output link serializer. Evaluation methods, including simulations, and performance results of the system in the lab and on a detector prototype are presented.

Summary

The frontend board (cover) receives the signals from the straws over a flexible PCB called a web board. The cover has been designed to serve several functions, such as distribution of the high voltage for the straws, gas tight detector encapsulation and electronics read out. The charge received is processed in an 8 channel CARIOCA chip, each channel consists of a preamplifier, shaper, base line restorer, comparator and LVDS driver. The LVDS output is fed to the low cost FPGA where the time to digital conversion (TDC) takes place.

The implementation of the TDC on the FPGA is based on the multiple phase-shifted clocks generated by the embedded PLL. Though the maximum clock frequency allowed is still on the sub-GHz region, one can achieve sub-nanosecond resolution by using two 320 MHz clocks at 90 degrees of relative phase. Sampling the LVDS inputs at rising and falling edges of both clocks and carefully designing the tracks and clock domain crossings in the FPGA, we manage to have a fine time measurement of 0.774 ns at 40 MHz input clock. The transition times, along with the identifier of the signal's origin and signal quality information are formed in 24 bit words, which are queued, transformed using the 8b/10b protocol and serialized. The output of the FPGA is routed directly to the RJ45 connector, using the pre-emphasis function of the Cyclon III true LVDS transmitter and can be received at a rate of 400 Mbps per twisted pair up to 15 meters of cable away.

The initial approach for the evaluation of this system was the simulation of different firmware entities with realistic inputs. The TDC has shown outstanding behavior with a RMS of the measurements at 0.3 ns, while queuing structure and communications surpass the technical specifications given, making sure that data loss will be minimized. Several tests with the final prototype of the board have taken place, to support the simulation results. In the lab, routines to gather enough statistics for the TDC behavior with real inputs from the CARIOCA have been developed, which show no particular difference through the whole range of TDC fine measurement and RMS values between 0.7 and 1.5 ns, corresponding to rising or falling transitions, different pulses, attenuation, thresholds and CARIOCA channels. Further studies to verify the effect of different thresholds over realistic pulses in a range of duration and amplitude have been performed and the resulting resolution is fulfilling the requirements and even offering a safety margin. The system was connected to the 64

straw prototype and the tests were repeated over the length of the straw. With new software and small changes in the prototype, studies with cosmic radiation have taken place as a final evaluation of the system.

The performance evaluation of the frontend board shows that the architecture of the frontend electronics is fulfilling the NA62 experiment requirements with a large safety margin.

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Session Classification: Poster

Contribution ID: 96

Type: **Poster**

Development of CMOS Pixel Sensor with digital pixel dedicated to future particle physics experiments

Tuesday, September 24, 2013 5:04 PM (1 minute)

Two designs of CMOS pixel sensor with in-pixel analog to digital conversion have been prototyped in a 0.18 μm CIS process. The first design integrates a discriminator into each pixel within an area of 22 \times 33 μm^2 in order to meet the requirements of the ALICE-ITS upgrade. The second design features 3-bit charge encoding inside a 35 \times 35 μm^2 pixel which is motivated by the specification of the outer layers of ILD vertex detector. This work is to validate the concept of in-pixel digitization which offers higher readout speed, lower power consumption and less peripheral surface of active area compared to column-level charge encoding.

Summary

CMOS pixel sensors have become an attractive alternative in tracking and vertex detecting when priorities are given to high granularity and low material budget with sufficient readout speed and moderate radiation tolerance. The state-of-the-art ULTIMATE (MIMOSA28) sensor equipping the STAR-PXL upgrade was developed at IPHC and fabricated in a 0.35 μm OPTO CMOS process [1]. It features in-pixel signal amplification and CDS with column level discriminator followed by zero suppression circuit to provide sparse outputs. A rolling shutter mode is employed to read out the matrix row by row in favor of power consumption. However, future projects (ALICE upgrade, CBM-MVD, etc.) call for more demanding requirements especially in radiation tolerance and readout speed which cannot be satisfied by the current development utilizing 0.35 μm technology. A 0.18 μm CIS technology is chosen to replace the former 0.35 μm counterpart. It offers thinner gate oxide and a higher resistivity epitaxial layer which can improve radiation hardness in both ionizing and non-ionizing aspects. The radiation tolerance for this technology is well validated to be adequate for the upgrade of ALICE-ITS [2]. Furthermore, the availability of quadruple well allows implementing PMOS transistors inside pixel. This possibility together with smaller feature size and more metal layers offers the opportunity to integrate more features in a pixel.

This work develops the concept of in-pixel discrimination by a prototype sensor called AROM0. Compared with the column level discrimination, in-pixel discrimination sets the analog processing within the pixel and the strong analog buffer driving the long distance column line is no longer needed. Thus, the static current consumption per pixel is reduced from ~ 120 to ~ 10 μA and also the readout time per row can be halved down to 100ns due to small local parasitic.

The pixel of AROM0 has a pitch of 33 \times 22 μm^2 mainly driven by the specification of the ALICE-ITS upgrade. It is composed of three parts: a sensing diode, a pre-amplifier and a high precision discriminator. The performance of the first two parts has been validated in former chips. Thus the development of AROM0 focuses on the discriminator design and pixel integration. Three different architectures of discriminators have been developed employing different offset compensation schemes. Each version of pixels lies in its respective matrix of 32 \times 32 with 4 extra analog columns for sensing calibration purpose. And the array is read out in a rolling-shutter mode. Moreover, to further shorten the integration time, the double-row readout scheme is also implemented with one matrix of 16 \times 18 including 2 analog columns.

The functionality test of AROM0 as well as sensing calibration will be performed in July 2013. Based on AROM0, a larger prototype called AROM1 featuring double-row readout and full peripheral functionalities integrated on chip (internal bias, sequence management, JTAG, etc.) will be developed.

[1] I. Valin et al, A reticle size CMOS pixel sensor dedicated to the STAR HFT, 2012 JINST 7 C01102

[2] S. Senyukov et al., Charged particle detection performances of CMOS pixel sensors produced in a 0.18 μm process with a high resistivity epitaxial layer (arXiv:1301.0515)

The vertex detector (VTX) in ILD, as one of the two detectors for ILC, has two alternative geometries. One features 5 equidistant single layers, while the other one consists of 3 double layers. In both geometries, the sensors equipped in the innermost layer give the priority to the single point resolution ($\leq 3 \mu\text{m}$) and the integration time ($\leq 10 \mu\text{s}$) dominated by beamstrahlung background. The outer layers, which are less demanding in terms of spatial resolution ($\sim 4 \mu\text{m}$) and integration time ($\sim 100 \mu\text{s}$), are needed to consume much less power to avoid complex heavy cooling components that increase the material budget. To satisfy these requirements, a prototype sensor (MIMOSA-31) integrated with 4-bit ADCs ending the columns had been designed and is now under the test.

In this work, we proposed a new approach which implements at the pixel-level digitalization with the 3-bit charge encoding as an alternative solution for the outer layer of the VTX. Comparing to the chip-level and the column-level ADC, the pixel-level has several advantages. The digitalization of pixel output makes the readout speed to be not limited by bus capacitance, so the data readout is possible at very high bit rates. A large pixel array together with high frame rate can be achievable. Moreover, the digital output from the pixel requires no analog buffer with huge drive ability, but the digital buffers as alternatives consuming much less power. Pixel-level ADCs can also minimize the dead zone in the sensor. Although the pixel-level ADCs have many attractive features, the difficulties of design restrict its implementation.

The design of the CPS integrated with the pixel-level ADCs is in the face of the following constraints:

1. The spatial resolution requirement of the ILD-VTX limits the size of the pixel. To integrate a complete ADC into the compact pixel is a great challenge to design the circuit and layout.
2. To conform the required integration time, the high sampling speed is necessary.
3. The sensors for the outer layers of the VTX have the severe restriction on the power consumption.
4. The least significant bit (LSB) has the same value as the equivalent input noise of the sensing diode, demanding the noise of the ADCs to be minimized.
5. For CPS, as the sensing diode and the signal processing circuits are integrated on the same substrate, the interference in one pixel and the crosstalk between the neighboring pixels should not be neglected.

The first prototype, called MIMADC, which features of $35 \times 35 \mu\text{m}^2$ pixels integrated with in-pixel 3-bit ADCs, has been designed and fabricated in a 0.18 μm 1P6M CIS process. The MIMADC prototype contains three arrays of pixels with different ADC structures. This report focuses on one matrix of 16×16 pixels employing SAR ADC associated with the conversion time of 160 ns. The power consumption of each pixel is about $140 \mu\text{W}$ with the 1.8 V supply. The pixels are read out in the row by row rolling shutter mode, and the digital output signals are transferred through 4:1 multiplexers to be serially read out by the LVDS.

The preliminary laboratory experimental results are expected to be achieved in the Autumn 2013.

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Session Classification: Poster

Track Classification: ASICs

Contribution ID: 97

Type: **Poster**

The new NA62 LKr readout: first tests and future perspectives

Wednesday, September 25, 2013 5:36 PM (1 minute)

The NA62 experiment at the CERN SPS (Super Proton Synchrotron) accelerator aims at studying ultra-rare kaon decays. The high resolution Liquid Krypton (LKr) calorimeter, built for the NA48 experiment, is a crucial part of the NA62 photon-veto system. However, the back-end electronics of the LKr calorimeter has to be redone in order to accommodate the new requirements. The exhaustive specification was prepared and the decision to sub-contract the development and production of the acquisition board to industry was taken in 2011.

This paper presents the primary test results of the Calorimeter REAdout Module (CREAM) prototype delivered by the manufacture in March 2013. All essential features, analog performance, trigger properties, data processing and readout, are covered.

Summary

The CREAM is a 1-slot wide VME 6U form-factor module. One module houses 2×16 channels 40 MS/s ADC with a 14-bit dynamic range and an ENOB greater than or equal to 10-bit. The external reference sampling clock will be provided by the Timing, Trigger and Control (TTC) system designed for the LHC experiments.

Each of the CREAM input channels consists of an AC-coupled differential line receiver and a pulse shaper. A 14-bit DAC allows tuning the DC offset of each channel in order to correctly adjust the pedestals and to preserve the dynamic range. The signal is shaped before the ADC input into a differential semi-Gaussian signal with a 40 ns rise time and a 70 ns full width at half maximum (FWHM). During the data acquisition, the CREAM inputs are continuously digitized and written into an on-board pipeline memory. When the L0 trigger occurs, the control logic freezes the corresponding data samples from all channels and copies them into another memory partition for a possible readout in case a L1 trigger is received. The L0 trigger latency should not exceed 10 ms and the module must be able to store locally up to 400×10^3 14-bit samples per channel. The size of the data buffer is defined by the L0 trigger rate (nominally 1 MHz), the number of samples per event and by the duration of the data-taking phase (accelerator burst time, typically up to 10 s with a period of up to 50 s). For this reason, an 8 GB DDR3 SODIMM module was chosen to ensure necessary storage capacity for data from 16 channels, and fulfil form factor requirements. The data acquisition is performed via a 1 Gbit Ethernet link and, for test purposes, a low rate optional readout via a VME64 compliant interface is foreseen. Since for each event a large fraction of channels will only contain pedestal counts, various zero suppression algorithms are foreseen to reduce the data flow to the experiment event building farm.

In addition to the data processing and readout, digitised signals from the selected channels are summed up to build a Trigger SUM (Super-Cell) and sent to the experiment trigger system. The selection of the channels contributing to a particular Super-Cell, as well as the shape of Super-Cells (4x4 or 2x8), is programmable. The Trigger SUMs are readout via 4 differential 640 Mbit/s serial links sharing one standard Ethernet cable. All control, processing and communication functionalities of the board are implemented in a reconfigurable FPGA device. The 'basic' firmware should not use more than 40% of device capacity, in order to allow the integration of new data processing and/or trigger algorithms during the lifetime of the experiment.

In total, about 450 CREAM modules should be produced, tested and installed, in order to have the entire LKr calorimeter readout system operational by mid-2014.

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Session Classification: Poster

Contribution ID: 98

Type: Oral

Characterization of COTS ADC radiation properties for ATLAS LAr calorimeter readout upgrade

Wednesday, September 25, 2013 11:35 AM (25 minutes)

The ATLAS LAr calorimeters plan to upgrade the readout electronics for both Phase-I and Phase-II LHC luminosity upgrades. Detector signals will be digitized at the front-end, and data will be streamed out to the back-end system continuously. Therefore, radiation tolerant ADCs are key components for both upgrade phases.

This presentation will report on irradiation test results of commercial-off-the-shelf (COTS) ADCs that have potentials to be used in the readout electronics upgrade. Total-ionization-dose (TID) irradiation test results will be described, which has been used to pre-screen COTS ADCs for further studies. Various SEE studies of a candidate ADC with both neutron and proton beams will be presented. Finally, annealing studies following ATLAS policy on radiation tolerant electronics will be reported.

Summary

The Liquid Argon Calorimeter trigger readout electronics will be upgraded in the Phase-I ATLAS upgrade. All of the $\sim 40,000$ super-cell signals will be digitized at the front-end and streamed to the back-end digital signal processing system. In the Phase-II ATLAS upgrade all front-end boards will be replaced to digitize all of the 200,000 channels enabling for continuous streaming of data to the read out drivers. For both upgrade phases, a radiation tolerant analog-to-digital converter (ADC) is required in the front-end electronics. In the past 5 years many commercial-of-the-shelf (COTS) ADCs that fit our needs and which are manufactured in 180 nm or smaller feature sized technology became available. As smaller feature size devices appear to have larger radiation resistance we embarked on a test program to evaluate ADCs from different manufacturers.

The test strategy was to initially test candidates selected on the basis of their electric characteristics to total ionizing dose (TID). At a second stage we tested the candidates with the best performance to single event effects (SEE). TID tests were performed at the BNL Solid State Gamma Irradiation Facility. In total, 17 different ADCs were tested, with six of them surviving doses larger than 1 MRad(Si) with ADS5272 being the top performer. This component is particularly interesting as it has the shortest pipeline latency (162.5 ns), which is an important parameter to minimize the Level-1 trigger latency.

Based on these results we decided to perform an SEE test with ADS5272. To measure the single event upset rate we have performed an initial test at the Los Alamos National Laboratory LANSCE-WNR facility. This facility produces a neutron beam that nearly matches the expected neutron spectra at the position of the ATLAS LAr electronics with the maximum energy of 800 MeV. During the test we identified 13 SEU events for a total fluence of $\sim 2 \times 10^{11}$ n/cm² with one of them classified as a Single Event Function Interrupt (SEFI). After an occurrence of a SEFI the device becomes inoperable and if it cannot be reset easily, devising mitigation techniques becomes a tall task. The observation of SEFI led to a more detailed investigation of SEE properties at a much higher particle flux facilities, namely the IUCF and Boston MGH cyclotron facilities.

At the IUCF and MGH facilities three ADCs were irradiated with ~ 200 MeV protons to measure both SEU and SEFI cross sections. The ADCs were operated with and without periodical hardware reset, in order to study the effectiveness of mitigation.

The test results performed with high intensity proton beams revealed the presence of two different types of SEFI. One that can be reset externally and a second requires a power cycle. The latter happens infrequently at doses less than 130 kRad, with cross sections increasing steadily after this

point. The SEFI cross section is $\sim 8 \times 10^{-13} \text{ cm}^2$ when TID is less than 130 kRad. The SEU, or bit-flip happens randomly and it is not a function of deposited dose.

As the expected radiation field for the ATLAS LAr electronics is low but has a high flux of high energy neutrons, this results suggests that this ADC is a good candidate to be used in the ATLAS LAr calorimeter Phase I and Phase II upgrades. We will discuss the test results and mitigation strategies to cope with the occurrence of SEFIs. Discussion of low-dose-rate effects will also be made.

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Session Classification: Radiation Tolerant Components and Systems

Contribution ID: 101

Type: **Poster**

System Level and Production Tests of the CMS HCAL QIE10

Wednesday, September 25, 2013 5:37PM (1 minute)

The CMS Hadron Calorimeter (HCAL) is scheduled to be upgraded to increase longitudinal depth segmentation in the Barrel and Endcap regions and to improve anomalous signal rejection efficiency in the Forward Region. In order to achieve these goals, the phototransducers and the front-end and back-end electronics of the HCAL will be upgraded in stages over the next several years. New PMTs in the Forward Detector and silicon photomultipliers (SiPMs) in the Barrel and Endcap detectors will be read out with charge integrator and encoder (QIE) deadtimeless Flash ADCs operating at 40 MHz. During the HCAL Upgrade, the current QIE Version 8 (QIE8) chip will be replaced by the next generation QIE10 chip, which features a ten times greater dynamic range and the inclusion of TDC data with 0.5 ns resolution. The HCAL back-end electronics will be upgraded from a VME readout system to a micro-TCA architecture. We present the results of system integration tests of the QIE10 chip's operation within the full front-end to back-end electronics chain. We also present the current progress of production chip testing of the QIE10, which involves the robotic ASIC tester at Fermilab.

Summary

The timetable of operation at the Large Hadron Collider (LHC) includes a number of upgrades which will increase its center of mass energy and integrated luminosity. These changes will also result in a higher fake rate in the Compact Muon Solenoid (CMS) tracking and a lower energy resolution due to signal overlap in the calorimeters. The purpose of the LHC Phase 1 Upgrade is to mitigate these effects by replacing the pixel detector of the CMS Tracker, improving the Level 1 Trigger, and upgrading the detectors and electronics of the CMS Hadron Calorimeter (HCAL).

During the HCAL Upgrade, the current hybrid photodiodes (HPDs) in the Barrel and Endcap calorimeters will be replaced with silicon photomultipliers (SiPMs) and the PMTs in the Forward Calorimeter will be replaced with multi-channel models. The performance of the SiPM detectors significantly exceeds the performance of the HPDs, which allows for a finer depth segmentation within the upgraded detector. To accommodate these improved detection capabilities and the corresponding increase in signal channels, both the front-end and back-end electronics also need to be upgraded.

In the HCAL, the signal from the phototransducers is integrated over 25 ns periods and digitized by a charge integrator and encoder (QIE) ADC. As part of the HCAL Upgrade, the current Version 8 (QIE8) chip will be replaced by the Version 10 (QIE10). The QIE10 is specifically designed to accommodate the increase in detector sensitivity by featuring ten times the dynamic range as the QIE8, from 3 fC to 330 pC. The QIE10 also provides previously unavailable TDC information which supplies signal arrival time information to the experiment with half-nanosecond resolution. This information is crucial for background reduction, distinguishing products from different bunch crossings in situations with high pileup, and identifying anomalous noise in the phototransducers.

Before the QIE10 can be implemented in the detector, the prototype chip's functionality needs to be demonstrated through system integration tests and all packaged chips need to be verified by production testing.

System integration testing focuses on the QIE10 chip's performance within the whole signal flow, from the phototransducer through the front-end and back-end electronics. A PMT is connected

to a prototype QIE10 front-end electronics board which, in turn, communicates with a prototype HCAL micro-TCA back-end board. We flash the PMT with an LED to simulate in situ conditions and examine capacitor ID consistency, charge bin widths, range and subrange overlap, charge calibration accuracy, timing measurements, and component cross-talk. These tests not only show that the QIE10 is operating correctly, but allow us to identify subtle hardware and software issues that are only revealed after the entire readout chain.

The purpose of production testing is to batch test all of the packaged QIE10 chips in order to determine which are of sufficient quality to send to the CMS detector. Every chip used in the CMS detector needs to pass a series of benchmarks, which we measure using Fermilab's robotic ASIC tester.

We present the results of these tests and argue that the QIE10 is ready for implementation in the HCAL Upgrade.

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Session Classification: Poster

Contribution ID: 102

Type: Poster

Development of New Front-end Electronics for the Upgrade of the ATLAS Muon Drift Tube Chambers at High LHC Luminosity

Wednesday, September 25, 2013 4:42 PM (1 minute)

New ATLAS Monitored Drift Tube (MDT) chambers with reduced tube diameter (sMDT) - 15 mm instead of 30 mm - have been developed for LHC luminosity upgrades. The shorter lengths of the pulse trains due to the smaller tube diameter allow to operate the sMDTs at much higher rates, however the gain in efficiency is limited by the shaping scheme of the current ASD (Amplifier-Shaper-Discriminator) chip. We present measurements and simulations with alternative shaping using active baseline restoration (BLR), evaluate the possible improvement in efficiency, and report on the design of a new front-end chip implementing this feature (BLR).

Summary

We report on the development of a new front-end chip for the Monitored Drift Tube (MDT) chambers of the ATLAS muon spectrometer. These chambers consist of aluminum tubes with 30 mm diameter and a central sense wire with 50 μm diameter which is set to a potential of +3080 V. The drift tubes are operated with Ar/CO₂ (93/7) gas mixture at 3 bar, resulting in a gas amplification of 2×10^4 . The maximum electron drift time for hits near the tube wall is ~ 700 ns, ions can drift for several ms and cause long tails in the pulses.

The existing ASD (Amplifier-Shaper-Discriminator) front-end chip has been optimized for typical pulses of muon and background hits at rates of up to a few hundred kHz per channel. Bipolar shaping is used for baseline restoration compensating partly the long ion tails. The typical time needed to arrive at the baseline after a hit is approximately 500 ns which is fully sufficient for the referred rates and the typical MDT pulse lengths.

For high luminosity upgrades of the LHC, new drift tube chambers (sMDT) with reduced tube diameter - 15 mm instead of 30 mm - have been developed. They are operated with the same gas mixture and amplification as the 30 mm MDTs, leading to the slightly lower operating voltage of 2730 V. As the drift velocity in the gas mixture used decreases with increasing drift radii, the maximum drift time is reduced from ~ 700 to 185 ns, resulting in considerably shorter pulse trains. This allows to operate the sMDT chambers at much higher rates with high efficiency. Measurements of sMDT chambers equipped with the current MDT ASD chip under γ and proton irradiation rates of up to 1.5 MHz per channel show the efficiency gain at high background rates. The improvement is limited, however, by the undershoot of the bipolar shaping and the long baseline restoration time of 500 ns, respectively. Simulations suggest that reducing the baseline restoration time has the potential to improve the efficiency at rates of 1.5 MHz per channel further from $\sim 61\%$ to $\sim 76\%$. A possible approach for faster baseline restoration has already been implemented in the front-end chip of the ATLAS Transition Radiation Tracker (TRT), the ASDBLR chip, with active baseline restorer (BLR). We present simulations and measurements of such a chip with active baseline restoration on sMDT chambers and evaluate the possible improvement on the efficiency. Furthermore, we report on the development of a new front-end chip in IBM 130 nm CMOS technology as a replacement for the current MDT ASD which will be needed in the course of ATLAS MDT chamber and trigger upgrades. Active baseline restoration is planned to be implemented in this new chip as an optional feature, especially for high rate operation of sMDT chambers.

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Session Classification: Poster

Contribution ID: 103

Type: Oral

Petiroc and Citiroc : Front-end ASICs for SiPM read-out and ToF applications

Thursday, September 26, 2013 4:05 PM (25 minutes)

Petiroc and Citiroc are the two latest ASIC from Weeroc dedicated to SiPM read-out.

Petiroc is a 16-channel front-end ASIC designed to readout silicon photomultipliers (SiPMs) for particle time-of-flight measurement applications. It combines a very fast and low-jitter trigger with an accurate charge measurement.

Citiroc is a 32-channel front-end ASIC designed to readout silicon photo-multipliers (SiPM). It allows triggering down to 1/3 pe and provides the charge measurement with a good noise rejection. Moreover, Citiroc outputs the 32-channel triggers with a high accuracy (100 ps).

Each channel of both ASICs combines a trigger path with an accurate charge measurement path. An adjustment of the SiPM high voltage is possible using a channel-by-channel input DAC. That allows a fine SiPM gain and dark noise adjustment at the system level to correct for the non-uniformity of SiPMs.

Timing measurement down to 7 ps RMS jitter for Petiroc and 100ps RMS for Citiroc is possible along with 1 % linearity energy measurement up to 2500 pe. The power consumption is around 3.5 mW/channel for Petiroc and 2mW/channel for Citiroc, excluding ASICs outputting buffer.

Summary

Petiroc and Citiroc are the latest ASIC designed by Weeroc, a start-up company from the Omega microelectronics group of IN2P3/CNRS.

SiPM time resolution allows time-of-flight measurement with high accuracy. Petiroc is a 16-channel ASIC that features a front-end read-out chain composed of a fast DC-coupled amplifier, fast filtering and very low jitter discriminator for the time measurement and an optimized variable-gain shaper for high accuracy charge measurement. The main application of Petiroc is PET time-of-flight prototyping but can be used for any application that requires both sharp time resolution and precise energy measurement.

First measurement on Petiroc shows a time jitter around 7ps on 3 photoelectrons test pulses and 13ps on 1 photoelectron test pulses. Charge measurement has been measured and a 1% linearity has been measured up to 2500photoelectrons.

Citiroc is a 32-channel ASIC aimed to read-out SiPM without time of flight measurement. Each channel embeds a front-end read-out chain composed of two AC-coupled voltage low-noise preamplifier with variable-gain adjustment. The utility of the gain tuning on the preamplifiers is twofold. On the first hand it allows to compensate non-uniformity between channels by finely adjusting gain channel by channel, on the second hand, it allows to adjust the general gain of the amplification chain to adjust the read-out chain to the SiPM gain, allowing a large choice of SiPM on the system to be used.

Citiroc has a new channel-by-channel trigger chain composed of a fast shaper followed by two discriminators with individual channel-by-channel threshold adjustment to be able to trig on the first photo-electron and validate the trigger on the first few photoelectrons. That double trigger allows a great dark noise rejection at the first stage of the read-out chain and avoids saturating the DAQ with noise events. Each trigger channel can be masked in case of noisy channel, latched, or output the discriminator output as is depending on user needs. A general ASIC trigger is also

outputted through a 32-input trigger OR.

A testboard with intuitive software is available for both Petiroc and Citiroc.

Author: FLEURY, Julien (Weeroc)

Presenter: FLEURY, Julien (Weeroc)

Session Classification: ASICs

Track Classification: ASICs

Contribution ID: 106

Type: **Poster**

The optical link system in the Upgrade project of the Drift Tubes electronics in CMS

Wednesday, September 25, 2013 5:09 PM (1 minute)

The upgrade of the second level electronics of the muon Drift Tube (DT) in CMS is focused on improving the electronic system to maintain its reliability at High Luminosity LHC. The project foresees the relocation of the Sector Collector electronics from the CMS cavern to the counting room. The system requires an electrical to optical conversion operated by the Copper to Optical Fibre (CUOF) boards. Prototypes have been produced and tested under radiation environment and during cosmic runs integrated within the DT acquisition and trigger system. The excellent results of those tests triggered the full production for the complete DT system that will be installed starting by the end of this year.

Summary

The program of upgrade for the Drift Tube (DT) system of the Compact Muon Solenoid (CMS) experiment foresees the relocation of the Sector Collector (SC) electronics which includes the second level readout and trigger electronics from the CMS cavern to the counting room. This Upgrade project will allow the DT detector to develop a new trigger architecture that will be able to face the high event rate expected for the High Luminosity Large Hadron Collider (HL-LHC). The fulfilment of this project envisages to turn electrical signals into optical signals for a total number of 3500 optical channels that run at 480 Mb/s data rate. The optical signals will then be converted again into electrical signals in the CMS counting room where the Sector Collector electronics will be relocated. The electronic system is based on the Copper to Optical Fibre (CUOF) boards that will be positioned in the experimental cavern, in an environment where the radiation and the magnetic fields cannot be neglected. The complementary system for the Optical Fibre to Copper (OFCU) conversion will be positioned in the counting room, and will feed the DT data acquisition and trigger data streams. The CUOF electronics is composed of Mezzanines which convert the data into optical signals at high frequency. They are mounted on Motherboards which have the principal controls and monitoring functions of all the critical components. Different prototypes of mezzanines have been tested in an irradiation facility in conditions similar to what it is expected in HL-LHC. In this way all the chosen Components Off The Shelf (COTS) have been qualified and the global behaviour of the board passed the assessment with a very low Bit Error Rate (BER). In addition some integration tests of the electronics boards for the optical link in the full acquisition chain have been performed with the installation and running of the prototypes on the CMS experiment in the cavern under nominal magnetic field conditions. Real cosmic rays have been collected and further test pulse data have been generated and passed through the present system. Both the irradiation tests and the integration tests on the experiment have given positive results so to be confident to start the electronics mass production for the system. In the meanwhile the test set up for the qualification of the full production of the CUOF/OFCU boards is being prepared. The certification tests are focalised on the measurements of the BER as a function of the main parameters of the optical converter placed in the CUOF board. The installation of the DT optical links is planned to begin next autumn with the relocation of the SC electronics and the installation of the CUOF/OFCU system for a substantial number of channels both on the data and the trigger paths.

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Session Classification: Poster

Contribution ID: 107

Type: Oral

Design of the analog front-end for the Timepix3 and Smallpix hybrid pixel detectors in 130nm CMOS technology

Tuesday, September 24, 2013 3:40 PM (25 minutes)

This front-end contains a single-ended preamplifier with a structure for leakage current compensation, suitable to both signal polarities. Preamplifier and discriminator are required to be fast, to allow a Time-of-Arrival measurement with a resolution of 1.56ns. Time-Over-Threshold (TOT) is also measured; the monotonicity of TOT with respect to the input charge is greatly improved as compared to the previous Timepix chip. The analog area is only 55 μm x 13.5 μm .

The design of the front-end, the main features of the chips and the first measurements are presented.

Summary

An analog front-end for the Timepix3 chip has been designed and submitted. This same front-end is used also for the Smallpix chip, under development, and serves as a basis for the future Velopix chip, meant for the LHCb upgrade.

Among the applications for Timepix3 are readout of gaseous detectors (TPC), particle tracking in HEP, and dosimetry. Additionally, Timepix3 will be also extensively used in the power pulsing tests for the future Linear Collider.

Timepix3 is a 256x256 array of pixels with a pitch of 55 μm . Each pixel provides simultaneously 18-bit Time-of-Arrival (ToA) and 10-bit Time-Over-Threshold (TOT) measurements. The chip can be read out in a 0-suppressed data-driven mode with an expected maximum rate of 40Mcps/cm². The front-end contains a single-ended preamplifier, followed by a three-stage discriminator. A 4-bit current-mode DAC in each pixel corrects the pixel-to-pixel threshold mismatch by adding different currents to two differential branches of the discriminator.

The preamplifier uses a Krummenacher feedback [1], and can therefore handle signals of both polarities and compensate for their leakage currents. Since the measured quantity is TOT rather than preamplifier output amplitude, the feedback capacitance is as small as 3fF, and the output is already in saturation for incoming charges larger than 14ke⁻. Some modifications to the feedback network have been introduced to improve the TOT response for large positive charges (>100kh⁺); the TOT monotonicity with respect to the input charge is now much improved as compared to the previous Timepix chip [2]. The TOT saturates for negative charges larger than 150ke⁻ or positive charges larger than 500kh⁺.

The available area is only 740 μm ², due to the 55 μm pixel pitch and the massive digital functionalities included on-pixel. The pixel capacitance is expected to be in the range 25-50fF. The input pad sits on top of the digital part of the pixel; studies and simulations have been carried out to quantify and minimize the noise injection into the sensitive analog nodes.

In Timepix3, an internal clock running at a frequency of 640MHz sets the requirement of 1.56ns for the ToA resolution. Therefore, the analog front-end offers jitter and pixel-to-pixel timing mismatch below 1ns. This resolution targets gaseous detector applications.

Power pulsing features are added to the chip. Analog biasing is generated in the chip periphery, which can switch dynamically the front-end to a low-power state, implementing power pulsing cycles. Clock gating avoids digital switching power consumption during the off period of the power pulsing cycle.

The design of the front-end is presented together with the first measurements from Timepix3, which is expected back from the foundry in July.

- [1] F. Krummenacher, "Pixel detectors with local intelligence: an IC designer point of view," NIM A305, 1991.
- [2] X. Llopart et al., "Timepix, a 65k programmable pixel readout chip for arrival time, energy and/or photon counting measurements," NIM A581, 2007.

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Presenter: DE GASPARI, Massimiliano (CERN)

Session Classification: ASICs

Contribution ID: **108**Type: **Poster**

Prototype pixel detector in the SOI technology

Wednesday, September 25, 2013 4:41 PM (1 minute)

We present the prototype pixel detector built in the Silicon on Insulator (SOI) technology. The sensor matrix contains 1024 integrating type cells, read continuously out as a serial analog signal. The pixels are protected from the back-gate effect by the Buried P-Well implantations. Measured ENC value was found to be 130 electrons at 100us integration time. An on-chip prototype SAR ADC and a precise voltage reference and temperature sensors have been also included in the design

Summary

Based on a well established commercial process, the SOI pixel detectors offer a freedom in tight integration of the particle sensors and readout electronics. The weakly doped areas under the Buried Oxide layer (BOX), called Buried P (N) Well layers (BPW, BPN), have proved to successfully suppress the Back-gate effect, originating from the detector bias. Although almost sub-micron, the radiation hardness of the technology is not yet satisfactory; an improvement is expected by means of the BPW, BPN combinations and newly developed Double SiO₂ process extension, where the BOX contains thin layer of a weak conductor, which is supposed to reduce an electric field from the trapped charges.

The new pixel detector with the matrix of 1024 sensors was built in the Double SiO₂ technology, with the single BPW type protection. Two kind of pixels, with the same circuit but different layouts have been used in the matrix. The chip was made as an integration type detector, with capability of a continuous readout in the “rolling shutter” mode, where the signals from consecutive pixel rows are transferred out without interrupting the charge acquisition. The chip is driven by the simple set of the reset and clock signals. The upper limit of the clock frequency is 25MHz, what origins in the slew rate of the analog buffers used. For simplicity the same clock was used both for the sensor control and for the readout; the clock frequency determines the integration time. In addition to the pixel sensor system, two standalone blocks of electronics have been put. The first one, the Successive Approximation type (SAR) 10-bit ADC is foreseen to be applied in the pixel readout in next chip iterations. The second one was a precise, thermally stable voltage bandgap reference.

Preliminary measurements with the Am²⁴¹ source resulted in ENC value around 130 electrons at 100us integration time. Large difference between gain and noise of the pixels with different layouts have been observed. The bandgap source was operational, both as a voltage and temperature reference. The SAR ADC tests so far have not gave satisfactory results, mainly due to the test board parasitic coupling effects; the new test platform is currently under development.

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Session Classification: Poster

Contribution ID: **109**Type: **Poster**

DTCC, a Point-to-Point Link for Data, Trigger, Clock and Control over Copper or Fiber

Wednesday, September 25, 2013 5:13 PM (1 minute)

Upgrades of the LHC detectors target significantly higher event rates and higher bandwidth over custom links which transmit data, trigger, clock and control (DTCC) between the front-end and the readout units. We report on a DTCC point-to-point link protocol designed to work over 8B/10B encoding with 2 or 4 pair copper implementation or over optical fiber. A version of the DTCC protocol over standard CAT6 cables is already used by the Scalable Readout System (SRS) [1] as data/trigger uplink and clock/trigger/controls downlink. DTCC features an automatic low-skew phase adjustment inside a crate down to 500 ps.

Summary

Developed within the RD51 Collaboration, more than 80 institutions world-wide, the Scalable Readout System (SRS) is intended as a general purpose multi-channel readout solution for a wide range of detector types and detector complexities. The scalable architecture is based on high-speed point-to-point links - with no buses involved, facilitating scalability without any loss of performance - in which the DTCC (Data, Trigger, Clock and Control) link is a key component.

The DTCC link hosts all digital communications between the Front-End Cards (FEC) and the Scalable Readout Unit (SRU) for large SRS system (up to 82 kchannels). With digital front-ends, the DTCC link can be also used as interface between the FEC cards and the front-end electronics. Therefore, the DTCC link allows to establish a connection between all the elements of an SRS system. In this way, the user can manage each element of the chain from an online PC or farm, via 1, 10 GbE network ports or another application specific protocol, or even from a Passive Optical Network (PON) planned to handle trigger commands.

The DTCC link is a generic protocol that can be used in any system because of its high versatility. It offers different manners of use, over standard SFTP (Shielded Foiled Twisted Pair) Category 6/7 cables, HDMI cables (in both cases with LVDS signalling) and also by means of optical fiber (using FPGA transceivers) if higher data rates and/or a longer cables are required.

An outstanding characteristic of the DTCC link is its low-skew clock distribution based on the Digital Dual-Mixer Time Difference (DDMTD) method. Thus, all the FEC cards achieve a perfect synchronization, getting a low-skew between all of them, under 500 ps. This synchronization is reached dynamically and is independent of the length of the DTCC links. On the other hand, the link offers two data channels, with low and high priority. Both channels are time multiplexed using the out-of-band signalling provided by the 8B/10B encoding, with the exception that the high-priority channel can interrupt any ongoing data transmission, which is later resumed after completion of the high-priority transmission. In this way, the high-priority channel provided fixed latency necessary for the timing information (like trigger and flow control). The low-priority channel is sub-partitioned between DAQ data frames and Ethernet transmission for slow-control.

As described above, the DTCC link is a very important part of the SRS system since it makes possible for different experiments and applications within the collaboration to synchronize and configure the readout nodes, while gathering DAQ data from the detectors over the same link.

The architecture, implementations and outcome of the DTCC link will be presented.

[1] "Front-End Electronics for the Scalable Readout System of RD51"

S. Martoiu, H. Muller, J. Toledo NSS Valencia Oct. 23-29 Oct.2011
2011 IEEE Nuclear Science Symposium Conference Record N43-5, pp 2036-2038

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Session Classification: Poster

Contribution ID: 110

Type: **Poster**

A Full Mesh ATCA-based General Purpose Data Processing Board

Tuesday, September 24, 2013 6:26 PM (1 minute)

High luminosity conditions at the LHC pose many unique challenges for potential silicon based track trigger systems. Among those challenges is data formatting, where hits from thousands of silicon modules must first be shared and organized into overlapping eta-phi trigger towers. Communication between nodes requires high bandwidth, low latency, and flexible real time data sharing, for which a full mesh backplane is a natural fit. A custom ATCA Data Formatter board is designed with the goal of creating a scalable architecture abundant in flexible, non-blocking, high bandwidth board to board communication channels while keeping the design as simple as possible.

Summary

High luminosity conditions at the LHC pose many unique challenges for potential silicon based track trigger systems. This is true for both Level-1 and Level-2 trigger applications. Among those challenges is data formatting, where hits and clusters from many thousands of silicon modules must first be shared and organized into overlapping eta-phi trigger towers due to finite size of the beam's luminous region in z and the finite curvature of charged particles in the magnetic field. Communication between nodes requires high bandwidth, low latency, and flexible real time data sharing.

The first silicon based track trigger at the LHC will be the ATLAS Fast Tracker (FTK) at Level-2. Although FTK is designed for Level-1 Accept rates up to 100kHz, the data volume per event is quite large since all silicon modules (more than 86 million channels) are involved at high luminosity, therefore this is where challenging data formatting issues will be encountered for the first time. We have been developing data formatting solutions for high luminosity LHC conditions and the FTK Data Formatter system is the first targeted application. Early in the design process our simulations showed that sharing between Data Formatter nodes is asymmetric and highly dependent upon upstream cabling and detector geometry. A high bandwidth full mesh backplane is a natural fit for the Data Formatter system.

We have selected the Advanced Telecom Computing Architecture (ATCA) platform as it supports a robust full-mesh backplane in a reliable industry standard form factor. A custom ATCA Data Formatter board, called the Pulsar IIa, is designed around Field Programmable Gate Arrays (FPGAs). These FPGAs feature many high speed serial transceivers which are directly connected to the full mesh backplane and to fiber optic transceivers on a rear transition module (RTM). The overall design goal is to create a uniquely scalable architecture abundant in flexible, non-blocking, high bandwidth board to board communication channels while keeping the design as simple as possible.

Expandability and scalability are achieved through three mechanisms. First, each board supports up to four mezzanine cards connected to the main FPGAs. Each mezzanine card may contain FPGAs, pattern recognition ASICs, fiber optic transceivers, or any other custom hardware. Our mezzanine cards use the FPGA Mezzanine Card (FMC) standard which has become popular with Xilinx development boards and many third party vendors. Secondly, additional boards may be installed in the crate. Unlike a shared bus system, adding boards to the mesh network has a minimal impact on the system latency while dramatically increasing system processing power and I/O capability. Lastly, we have reserved several transceivers on rear transition modules (RTM) for dedicated serial links between boards in different crates.

The performance of the Data Formatter design meets and exceeds the FTK requirements. This high performance scalable architecture may find applications beyond tracking triggers, and may serve as a starting point for future Level-1 silicon based tracking trigger R&D for CMS and ATLAS. In this talk we describe our design methodology, prototype test results and experiences designing our first ATCA board.

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Session Classification: Poster

Contribution ID: 112

Type: **Poster**

Development of a digital trigger system to identify recoil protons at COMPASS-II

Tuesday, September 24, 2013 6:27PM (1 minute)

The GANDALF framework has been developed to deliver a high precision, high performance detector readout and trigger system for particle-physics-experiments such as the COMPASS-II experiment at CERN. Combining the high performance pulse digitization and feature extraction capabilities of twelve GANDALF modules, each comprising a Virtex-5 SX95T, with the strong computation power of a Virtex-6 SX315T FGPA operated on the TIGER module, we present a digital trigger system for a recoil proton detector.

Summary

For the deep-virtual-compton-scattering (DVCS) program at the COMPASS-II experiment the recoil proton detector CAMERA was built. CAMERA is able to perform time-of-flight and energy deposit measurements of the recoil protons in the scattering. Due to the fast risetime (below 3ns) and the high pile-up-rate in this detector region, the analog signals of the detector have to be digitized with high resolution prior of discrimination. In order to deliver a comprehensive readout-and-trigger-system, the GANDALF-Framework was designed.

In this application, the GANDALF modules are configured as analog-to-digital converters with a sampling of 1GSps and 12bit amplitude resolution. Through the implementation of a pulse-feature-extraction-algorithm in the Virtex-5 FPGA of the GANDALF module we are able to perform a streaming, dead time free feature extraction with high timing resolution (<10ps). The information is transferred continuously with low latency (<100ns) to the Trigger module (TIGER) for 'proton trigger' generation. Therefore, a high-speed link with 1 GB/s per module using the VXS backplane has been developed.

The TIGER module is placed in the center of the VXS crate where the pulse features, computed in real-time, of all 96 readout channels are combined to form the trigger decision. This allows the reconstruction of the proton track and its energy deposit on-the-fly. With the pulse feature information, the trigger is able to select specific proton signatures that are well known from Monte-Carlo simulations, such as the dependency of energy deposit on proton velocity in real-time.

The main challenge when implementing the digital trigger was to handle the vast amount of data coming from the GANDALF modules. With an expected hit rate of about 10 MHz per detector channel the design has to handle a total 12 GB data per second. This data, consisting of timestamp and amplitude information, has to be organized and coincidences between different detector channels have to be formed in order to reconstruct the proton tracks. The coincidences are computed digitally by comparing the timestamps of the hits. After the reconstruction of the proton tracks, look-up tables can be used to perform sophisticated cuts that take the whole event topology into account.

For the integration into the first level trigger of the experiment, the TIGER trigger decision has to be computed within less than 1 μ s. Furthermore, the emitted trigger signal has to have a fixed latency with respect to the beam particle. However, achieving a fixed latency within digital computations is not as natural as it is for analog trigger systems. Thus, a special technique to release the trigger was implemented. It allows to set the trigger latency to a specific value that correlates to the physics event without the need of changing cable lengths.

The trigger system was setup and commissioned successfully for the DVCS pilot run in 2012. It was mainly used for the calibration of CAMERA and in tagging mode to identify proton tracks

online for DVCS reactions.

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Session Classification: Poster

Contribution ID: 114

Type: Oral

APENet+ 34 Gbps Data Transmission System and Custom Transmission Logic.

Thursday, September 26, 2013 3:40 PM (25 minutes)

APENet+ is a point-to-point, low-latency, 3D-torus network controller integrated in a PCIe Gen2 board based on Altera Stratix IV FPGA.

We characterize the transmission system (embedded transceivers driving external QSFP+ modules), analyzing signal integrity, throughput, latency, BER and jitter at different data-rate up to 34Gbps.

We estimate the efficiency of custom logic able to sustain 2.6 GB/s per link with a memory consumption of 40KB, guaranteeing deadlock free routing and systemic awareness of faults.

Finally, we show the preliminary results obtained with next-generation FPGA embedded transceivers and propose a new protocol to increase the performance with the same memory consumption.

Summary

In future particle and astroparticle physics experiments an increasing importance has been recently achieved by high speed data transfer for trigger and data acquisition systems. We present final results of characterization of our data transmission system based on FPGA embedded transceivers driving external QSFP+ modules and the custom control logic implementing fault-awareness capabilities free of any detrimental effect on the data transmission performance.

The APENet+ project delivered a point-to-point, high performance, low latency, 3D torus network controller integrated in a PCIe Gen2 based board. The APENet+ board exploits 32 8.5Gbps embedded transceivers of Altera Stratix IV devices, obtaining the impressive aggregated bandwidth of 400 Gbps per single device.

The QSFP+ (Quad Small Form Pluggable) standard (SFF-8436) is a technology intended for high-density and low-power applications and specifies a hot-pluggable transceiver with a bandwidth of 40 Gbps per direction. The APENet+ card hosts 6 channels using the QSFP+ electrical and mechanical standard.

In order to produce the clearest signal and thus being able to increase signal clock frequency over the cable, Altera provides a Physical Medium Attachment (PMA). A fine tuning of the Equalization, Pre-emphasis, DC-Gain and Voltage Output Differential (VOD) is required.

Each transceiver implements an 8b/10b encoding to maintain the DC balance in the serial data transmitted and a byte ordering system at receiver side. Deskew logic and 128-bit word-level alignment is implemented to preserve data integrity along the four bonded lanes. Indeed, the 6 channels are bi-directional and can work simultaneously, reaching a data rate of 34 Gbps per direction.

We characterize all parts of our transmission system (transmission lines, connectors, cables) from the signal integrity point of view, then we characterize throughput, latency, bit error rate and jitter of the link at different data rates up to the maximum achievable data rate, with optical and electrical cables of different lengths.

The implemented control logic manages the data flow by encapsulating packets into a light, low-level, word-stuffing protocol able to detect transmission errors via CRC.

We develop a model of the transmission mechanism to estimate the efficiency of the control logic. The data transmission model is validated by comparison with actual performance achieved at dif-

ferent transceiver clock frequencies. We show the relation between the performance achieved with the adopted solution and the used memory resource. The current implementation of the data transmission system is able to sustain the link bandwidth of about 2.6 GB/s per link with a memory consumption limited to 40KB per link and guaranteeing a deadlock free routing with the adoption of virtual channels.

HPC systems in the peta/hexa-scale require techniques that aim at maintaining an acceptable Failure-In-Time ratio. The diagnostic messages necessary to create a systemic awareness of fault and critical events are embedded in the APENet+ transmission protocol to avoid performance degradation.

As conclusion, we show the preliminary results obtained with next-generation FPGA embedded transceivers of Altera Stratix V and propose a new data transmission protocol to increase the performance with the same memory consumption.

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Presenter: BIAGIONI, Andrea (INFN)

Session Classification: Programmable logic, design tools and methods

Contribution ID: 117

Type: Oral

Upgraded Readout and Digitizing System for the ATLAS Tile Calorimeter Demonstrator

Tuesday, September 24, 2013 12:00 PM (25 minutes)

During the shutdown of the ATLAS scintillating Tile calorimeter (TileCal) in 2013/14 one of its on-detector electronic modules will be replaced with a compatible hybrid module, which also serves as a demonstrator for future upgrades. This is being built to fulfill all requirements for the complete upgrade of the TileCal electronics in 2022 but augmented to stay compatible with the present system.

We describe a new Front End Board (FEB) that provides amplification and shaping, a Main Board that handles digitization and a high-speed communication Daughter Board. This system will permit us to acquire experience with a future fully digital readout system without disturbing the current analog trigger system.

Summary

In 2022 the LHC will undergo a major upgrade, with the aim to increase the average luminosity to a level more than an order of magnitude larger compared to the nominal value. To respond to the increased event rate it is necessary to provide more information to the early triggers in order to make them more selective. For the TileCal detector system this means directly reading out all information to the counting room rather than just reading out trigger tower data together with data from events selected by the first level trigger. However, this will require a complete redesign of all on- and off-detector electronics. To study how this can be achieved a demonstrator containing a possible (and probable) solution to how the on- and off-detector electronics can be implemented is currently under construction. This demonstrator will replace one module of the detector after the 2013/14 shutdown and run in parallel with the current electronics. The on-detector hardware part will be divided into four types of boards, each one with a dedicated purpose. These are: the Front-End boards, the MainBoard, the DaughterBoard and the High Voltage Power Supply.

The DaughterBoard, developed at Stockholm University, is a key component responsible for the multi gigabit data communication with the off-detector as well as for controlling and monitoring of all the on-detector electronics. To reach the demonstrator goal, the hard- as well as the firmware has to be thoroughly tested, verified and later proven to be sufficient radiation tolerant.

Although a first generation of the DaughterBoard (reported last year) addressed some of the issues much remained to be studied with a second prototype. The hardware features of the second generation DaughterBoard have now been tested and verified, including the electrical characterization of the gigabit transceiver performance at 10Gbps and user IOs at 600Mbps for Single Data Rate (SDR). The firmware was adapted to the upgraded hardware of the second generation, which now included a Kintex7 FPGA and a QSFP+ module for high speed communication. Furthermore the clock layout was revised allowing reception of a 4.8Gbps data stream encoded with the GBT protocol and transmitting data with either 5Gbps or 10Gbps which can be received without losing synchronization with the 40MHz LHC clock. Using this communication framework, loopback tests with different setups were performed using two different custom evaluation boards.

As a result the second generation DaughterBoard is a major step towards a working demonstrator. At this point most of the functionality of the second prototype has been verified and the process of manufacturing a final functional prototype has already started. If proven sufficiently radiation tolerant, this hardware will be used in the TileCal demonstrator project and inserted into the detector in the middle of 2014.

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Presenter: MUSCHTER, Steffen (Stockholm University)

Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Track Classification: Systems

Contribution ID: 119

Type: **Poster**

Design of an FPGA-based embedded system for the ATLAS Tile Calorimeter front-end electronics test-bench

Wednesday, September 25, 2013 6:04 PM (1 minute)

The portable test bench (VME based) used for the certification of the Tile calorimeter front-end electronics has been redesigned for the LHC Long Shutdown (2013-2014) improving its portability. The new version is based on a Xilinx Virtex 5 FPGA that implements an embedded system using a hard core PowerPC 440 microprocessor and custom IP cores. The PowerPC microprocessor runs a light Linux version and handles the IP cores written in VHDL that implement the different functionalities (TTC, G-Link, CAN-Bus) Description of the system and performance measurements of the different components will be shown.

Summary

The architecture of the Tile Calorimeter back-end electronics, as most of the others ATLAS sub-detectors is based on the VME standard. All the functionalities needed for the data read-out and the configuration of the front-end boards and the trigger were designed using this standard.

As it is very common in HEP VME systems were deployed also in the standalone test benches that are used during the LHC shutdowns in the campaign of detector maintenance for the verification and certification of the FE electronics.

A new version of the test bench has been designed and built for the LHC Long Shutdown (2013-2014) with the aim of improving the portability of this tool and to explore new architectures.

The new test bench is based on a commercial Xilinx ML507 development board housing a Virtex 5 FPGA which includes a hard core PowerPC 440 processor. The boards include an SFP optical connector, an Ethernet port 10/100Mbit, USB and serial ports and a huge number of GPIOs.

To manage all the components in an effective way, a complete embedded system has been designed using the hard core PowerPC 440 processor. Custom IP cores are written in VHDL to interface the FPGA with the hardware components connected.

This architecture allows the replacement of the CPU, TTCvi and TTCex VME boards and the ODIN cards used in the previous system using two IP cores which are connected to the SFP module on the board: the Glink and the TTC IP cores. The Glink IP core receives digital data from FE electronics through a GTX transceiver and decodes it similarly as the Agilent HDMP 1034 chipset does in the ODIN card. After decoding the data is stored on a RAM memory until user reads it. The Glink IP core also computes two types of CRC using the received data packet, one for each of the 16 DMU and one for the whole packet.

The TTC IP core generates and handles the TTC commands needed to configure and control the front-end electronics during tests. A VHDL component encodes and multiplexes the desired commands into the A and B channels using the BCM (Biphase Mark Code).

One CAEN V792 VME ADC was used to measure the analog trigger signal in the old system. This is replaced by a custom made ADC board which is controlled through the ADC IP core. This configures the two ADC chips (ADS5271) and handles the data using the Xilinx ISERDES blocks to deserialize the data at a data rate of 480Mbps per channel.

Other custom IP cores are used to control two other custom boards, the PMT High Voltage and a LED driver using GPIOs.

The embedded system runs a light and custom embedded Linux version developed with the ELDK 4.2 toolchain. All the custom IP cores contains a set of registers connected to the PowerPC processor via the PLB bus, this allow the embedded Linux to manage the hardware in a friendly way.

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Presenter: CARRIO ARGOS, Fernando (Universidad de Valencia (ES))

Session Classification: Poster

Contribution ID: 120

Type: **Poster**

The sROD Module for the ATLAS Tile Calorimeter Phase-2 Upgrade Demonstrator

Tuesday, September 24, 2013 6:15PM (1 minute)

TileCal is the central hadronic calorimeter of the ATLAS experiment at the Large Hadron Collider at CERN. The main upgrade of the LHC to increase the instantaneous luminosity is scheduled for 2022. The High Luminosity LHC, also called upgrade phase-2, will imply a complete redesign of the read-out electronics in TileCal. In the new read-out architecture, the front-end electronics aims to transmit full digitized information to the back-end system in the counting room. Thus, the back-end system will provide digital calibrated information with enhanced precision and granularity to the first level trigger to improve the trigger efficiencies. The demonstrator project has been envisaged to qualify this new proposed architecture. A reduced part of the detector, 1/256 of the total, will be upgraded with the new electronics during 2014 to evaluate the proposed architecture in real conditions. The sROD module is designed on a double mid-size AMC format and will operate under an AdvancedTCA framework. The module includes one Xilinx Kintex 7 and one Xilinx Virtex 7 for data receiving and processing, as well as the implementation of embedded systems. Related to optics, the sROD uses 4 Avago MiniPODs to receive data from the front-end electronics and 2 Avago MiniPODs to send control commands to the front-end and for communication with the first level trigger. A QSFP optical module is also included for expansion functionalities and a SFP module to maintain compatibility with the existing hardware. A complete description of the sROD module for the demonstrator including the main functionalities, circuit design and the control software and firmware will be presented.

Summary

The main upgrade to increase the luminosity of the Large Hadron Collider (LHC) at CERN is scheduled for 2022. It will imply a complete redesign of the readout electronics of the central hadronic calorimeter (TileCal) of the ATLAS experiment. The TileCal demonstrator project has been envisaged to verify the new proposed architecture in real conditions. Thus, a reduced part of the detector will be equipped with this new architecture during the 2014 shutdown.

The sROD demo module represents the core of the back-end electronics of the TileCal demonstrator project and it will include all the functionalities required for the new proposed read-out architecture. It should provide high speed optical links to receive data from the on-detector electronics, pipeline memories with programmable depth, reception of L1 trigger signal, transmission of processed data to DAQ system as well as preprocessor functionalities for pulse recognition, feature extraction and merging of cell sums and optical links for data transmission to the L1-Calo system.

It is designed in a double mid-size Advanced Mezzanine Card (AMC) to be operated into an Advanced Telecommunications Computing Architecture (ATCA) carrier or in a Micro Telecommunications Computing Architecture (μ TCA) framework.

The sROD demo module is populated with a Xilinx Virtex 7 FPGA with 48 MultiGigaBit Transceivers (MGTs) connected to four Avago MiniPOD receiver modules to receive the data from the on-detector electronics whereas one transmitter module provides the uplink for on-detector configuration. A QSFP+ connector has been included to evaluate this radiation tolerant technology for the future system. Furthermore, a SFP+ optical connector provides back compatibility with one

input link for reception of trigger information and one output link for data transmission to the present ROD module.

On the other hand, a Xilinx Kintex 7 FPGA with 24 MGTs implements the preprocessor functionalities and the interface with the L1-Calo system through one Avago MiniPOD transmitter. Flash and RAM memories are used to implement embedded systems in both FPGAs which will include an operating system to handle the communication with external modules and with the ATCA backplane.

Power connection to the ATCA carrier is managed by the Module Management Controller mezzanine which implements the Intelligent Platform Management Interface (IPMI) communication standard for manage the hot swap power sequence with the ATCA system.

The sROD demo module includes other peripherals as two USB interfaces and one 10/100 Ethernet port. One slot for a FPGA Mezzanine Card (FMC) is available to extend the sROD demo board functionalities.

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Presenter: MORENO, Pablo (Universidad de Valencia)

Session Classification: Poster

Contribution ID: 123

Type: **Oral**

The CMS MTF7 Trigger Board

Wednesday, September 25, 2013 12:00 PM (25 minutes)

One of the workhorses for the CMS Level-1 Muon Trigger upgrade is the Muon Trackfinder board with a Virtex-7 generation FPGA (MTF7). Optimized to handle large input bandwidth for data from the different muon sub-detectors, the board also has 1 Gigabyte of fast access memory to be used as a look-up table while assigning muon momenta. We discuss the challenges and solutions for implementing the design with all these characteristics within the uTCA form factor, as well as projected performance, and results from test-stand runs with available prototypes.

Summary

To accommodate the increase in energy and luminosity of the upgraded LHC, the CMS Endcap Muon Trigger system has to be significantly modified. To provide the best track reconstruction, the Trigger system must now import all available trigger primitives generated by Cathode Strip Chambers and by certain other subsystems, such as Resistive Plate Chambers. In addition to massive input bandwidth, this also requires significant increase in logic and memory resources.

To satisfy these requirements, a new Sector Processor unit is being designed. This unit follows the micro-TCA standard recently adopted by CMS. It consists of three modules. The Core Logic module houses the large FPGA that contains the processing logic and multi-gigabit serial links for data exchange. The Optical module contains optical receivers and transmitters; it communicates with the Core Logic module via a custom backplane section. The Pt Lookup Table (PTLUT) module contains large amount of low-latency memory that is used to assign the final Pt to reconstructed tracks. The name of the unit –Modular Track Finder –reflects the modular approach used in the design.

The talk presents the details of the hardware and firmware design of the prototype unit based on Xilinx's Virtex-6 FPGA family, as well as results of the conducted tests. Also presented are plans for the pre-production prototype based on Virtex-7 FPGA family.

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Presenter: MADORSKY, Alexander (University of Florida (US))

Session Classification: Trigger

Contribution ID: 124

Type: Oral

The FPGA based Trigger and Data Acquisition system for the CERN NA62 experiment

Wednesday, September 25, 2013 3:40 PM (25 minutes)

The main goal of the NA62 experiment at CERN is to measure the branching ratio of the ultra-rare $K^+ \rightarrow \pi^+ \nu \bar{\nu}$ decay, collecting about 100 events to test the Standard Model of Particle Physics. Readout uniformity of sub-detectors, scalability, efficient online selection and lossless high rate readout are key issues. The TDCB and TEL62 boards are the common blocks of the NA62 TDAQ system. TDCBs measure hit times from sub-detectors, TEL62s process and store them in a buffer, extracting only those requested by the trigger system. During the NA62 Technical Run at the end of 2012 the TALK board has been used as prototype version of the L0 Trigger Processor.

Summary

The NA62 experiment at the CERN SPS aims at measuring the ultra-rare kaon decay $K^+ \rightarrow \pi^+ \nu \bar{\nu}$ as a highly sensitive test of the Standard Model (SM) and a search for New Physics. The detection of this process is very difficult due to the smallness of the signal and the presence of a very large background. NA62 aims to collect about 100 signal events in 2 years of running. The devices used for this purposes are a general-purpose trigger and data acquisition board (TEL62) and its mezzanine cards (TDCB) hosting high-performance TDC chips.

The TDCB houses 4 HPTDC chips developed at CERN, receiving from the front-end electronics the discriminated signals whose leading and trailing times are measured with 100ps LSB. The data are then buffered before being read periodically by the on-board FPGA, which adds a time-stamp and a counter to the data stream and addresses it to the TEL62. Several other features are implemented in the TDCB firmware, including a TDC data simulator for testing purposes, the possibility of triggering front-end board calibration signals through an output line and the controller for two on-board 2 MB SRAM memories.

The TEL62 is the main device of the NA62 TDAQ; about 100 cards will be installed on the experiment. The board architecture is based on a star topology: 4 Pre-Processing (PP) FPGAs are connected to a single SyncLink (SL) FPGA. The 4 PPs are directly connected to the 4 mezzanines, for a total of 512 input channels. The amount of data arriving from the TDCs can be up to a few tens of MB/s per channel, depending on the sub-detector. Data are organized in packets, each one related to time frames of 6.4 μ s duration. The PP has the duty of collecting and merging the data and then of organizing them on the fly in a 2GB DDR2 memory, where each page is related to a well defined 25 ns window. Whenever a trigger arrives the data within a programmable number of 25 ns time windows around the trigger timestamp are collected and sent to the SL. The PP data are merged and synchronized inside the SL, pre-processed and stored in a 1MB QDR SDRAM which sends data packets through 4 Gigabit Ethernet links hosted on a custom daughter card to a computer farm that performs additional cuts and eventually writes events to permanent storage.

The system has been extensively tested at the end of 2012 during the NA62 Technical Run. The TALK board, a TEL62 multifunction daughter board, has been used as L0 Trigger Processor (L0TP): it merges trigger primitives arriving from several subdetectors and sends trigger decisions back. The TALK board design was started by the need to provide a trigger interface between the TTC and the old NA48 trigger distribution system, in order to read the LKr calorimeter with the NA48 readout hardware during the Technical Run. Additional functions in the firmware have been added:

driver for the calibration of the calorimeter, test bench controller for the characterization of the new CREAM boards for the LKr readout, and prototype of L0TP. The board has been designed around a Cyclone 3 FPGA, with 5 Ethernet interfaces driven by the Marvell 88e1111 chip and using the Ethernet MAC IP core from More-than-IP. A 1M-16bit word memory is available. As trigger distribution, the board sends trigger requests received from the TTCrx interface to the LKr readout and in addition a list of timestamps is stored in a memory which is readout at the end of burst and sent to the LKr readout PC farm for the event stamping.. The prototype L0TP implements the logic to receive both NIM triggers and primitive packets generated by TEL62s, received through some of the five Ethernet channels. Communication with the PC is also done through an Ethernet interface. Besides the operation as a daughter board for the TEL62, we have developed a 6U VME frame to use the TALK board inside a VME crate.

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Session Classification: Trigger

Track Classification: Trigger

Contribution ID: 125

Type: **Poster**

Design of a deterministic link initialization mechanism for serial LVDS interconnects

Wednesday, September 25, 2013 4:58 PM (1 minute)

The Compressed Baryonic Matter experiment at FAIR in Darmstadt has special requirements on the Data Acquisition Network. One of them is deterministic latency of all links from the back-end to the front-end, which enables synchronization in the whole read-out tree. Since front-end electronics (FEE) contains mixed-signal circuits for processing of detector raw data, special ASICs were developed. DDR LVDS links are used as interconnects between FEEs and readout controllers. An adapted link initialization mechanism ensures determinism for them by balancing cable lengths, adjusting phase differences and handling of environmental behavior. After re-initialization timing precision has to be on bit-clock level.

Summary

The front-end electronic ASICs consist of an analog part to amplify and digitize raw signals from the detector and a digital part, which contains modules as a registerfile, the CBMnet, providing the network protocol, and an LVDS serializer/deserializer. The transceivers use 8B/10B coding to achieve DC-balance. Fault tolerance is assured by using K-characters with hamming distance for special characters correction and CRC secured data with retransmission functionality. Because of restricted design space at the FEBs, an additional wire provides a clock to abstain from crystal oscillator. Data bandwidth in back-end direction can be increased by using unbalanced links, which means up to four lanes are supported for data transmission from the FEE while only one link is used for management data to the FEE.

The readout controller (ROC) design, which can aggregate data from up to four front-end ASICs to one back-end node, is currently running on a Xilinx evaluation board SP605. It will soon be replaced by a custom-made solution. The whole design and due to clock distribution all front-ends, run with the recovered clock or derived fractions from the high-speed serial link to the back-end. In addition, this receive clock is jitter-cleaned and then used for the transmit part to guarantee a source synchronous and deterministic behavior.

The front-end SerDes PHY has to delay the outgoing signals to assure that all FEE word-clocks run in phase. This adjustment allows to receive deterministic latency messages (DLM) in the front-ends synchronously. The returned data stream has to be aligned since it will not run in phase with the bit-clock due to e.g. diversifying cable lengths. Therefore, the Xilinx built-in SelectIO logic resources are used as ILogic and a delay adjust mechanism ensures that data sampling is done in the middle of the eye. An IODelay cell moves the phase of the signal by 256 taps per clock-period. The resulting measurement is used to find the transitions in the incoming serial bitstream and calculate the sampling position.

After phase alignment on bit-clock level is done, the initialization of the SerDes physical coding sublayer (PCS) is taking place. While sending specific secured character, the barrel-shifters in ROC and FEE deserializer arrange the bit sequence to the word clock.

Finally, to obtain a simultaneous arrival of a DLM in all front-ends, the clock and data signals will be delayed to assure DLM arrival after a fix time period. Measurement DLMs are sent through the links to calculate time values for every lane for inter lane adjustment. Therefore, front-end ASICs simply reflect them to the ROC and the round-trip time can be measured. After initialization, the

word-clocks run in phase with less than 2ns difference. All links to the front-end ASICs provide a deterministic latency for DLMs. Latest tests showed the successful transmission and deterministic arrival of messages at the front-ends.

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Presenter: SCHATRAL, Sven (University of Heidelberg)

Session Classification: Poster

Contribution ID: 127

Type: **Poster**

STiC - A Mixed Mode Silicon-Photomultiplier Readout ASIC for Time-of-Flight Applications

Tuesday, September 24, 2013 5:05 PM (1 minute)

STiC is a mixed mode readout ASIC for Silicon-Photomultipliers developed in the UMC 180nm CMOS technology. The chip has been designed for the EndoToF PET-US project and aims at providing a high timing resolution to high energy physics and medical imaging applications. The signal is read out and discriminated by a dual threshold method. A low threshold discriminator provides a high precision trigger signal while a linearized time-over-threshold method maintains a good energy resolution. An integrated TDC with 50ps bin size is used to digitize the trigger signals. A 16-channel prototype has been produced and measurements have been performed to quantize the performance of the ASIC.

Summary

The STiC chip is a mixed mode ASIC developed in 0.18um UMC CMOS technology for Silicon-Photomultiplier (SiPM) applications with very high timing resolution. It is designed for time-of-flight (ToF) measurements in high energy physics and medical imaging applications and dedicated in particular to the ENDOToFPET-US project, which aims at providing a powerful endoscopic time-of-flight PET system for early prostate and pancreas cancer diagnostics. The goal of this endoscopic system is to provide a spatial resolution in the order of 1 mm which necessitates a time-of-flight resolution of 200 ps FWHM.

In order to achieve this high timing resolution the STiC ASIC has a differential readout structure reducing the influence of noise sources. The connection scheme to the SiPMs can be either differential or single-ended. The timing and energy information, which are both required for a high resolution PET system, are encoded in two time stamps which are obtained by discriminating the signal with two different thresholds. A low threshold discriminator providing a high precision trigger signal is used as the timing trigger. A second discriminator with a higher threshold is used to implement a linearized time-over-threshold discrimination providing a good energy resolution. A combined signal of the trigger outputs is then processed by a TDC with a bin size of 50ps which has been developed at the ZITI Heidelberg. An integrated digital part stores the data and transfers it over a LVDS serial link to the DAQ system. In order to compensate the high temperature dependence of SiPMs, the STiC ASIC is capable of tuning the sensor bias voltage.

A 16-channel prototype has been submitted in April 2012 and measurements have been carried out to quantify the chip performance. The SiPM bias DAC shows a linearity of 700mV, which exceeds the required 500mV tuning range for temperature and bias variations. An analog test channel has been used to characterize the performance of the analog input stage. A scan of the time-over-threshold output width with respect to the total injected signal charge shows a linear relationship for signal charges larger than 3pC maintaining the high

energy resolution of the charge measurement. In order to measure the single pixel time resolution of the chip a Hamamatsu MPPC (S10362-11-100) has been connected to this test channel and was illuminated by a fast laser system (PILAS PiL063SM) with a wavelength of 408nm. For the final trigger jitter after selecting the single pixel events and applying a time-walk correction using the time-over-threshold information a value of 180ps sigma was measured. This result is consistent with measurements using direct MPPC readout and is already close to the intrinsic time resolution

of the sensor.

Preliminary coincidence measurements using the full system chain have been performed and verify the functionality of the chip. The results obtained from the characterization are used to improve the final 64 channel chip version which is currently being developed and will be submitted this year.

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Presenter: HARION, Tobias (Kirchhoff-Institut Heidelberg)

Session Classification: Poster

Contribution ID: 131

Type: Oral

Trigger-less readout architecture for the upgrade of the LHCb experiment at CERN

Tuesday, September 24, 2013 4:05 PM (25 minutes)

The LHCb experiment has proposed an upgrade of its detector in order to collect data at ten times its initial design luminosity. The current readout architecture will be upgraded by removing the existing first-level hardware trigger whose efficiency is limited for hadronic channels at high luminosity. The new readout system will record every LHC bunch crossing and send data to a trigger selection process performed entirely by software running in a computing farm. Therefore, the new readout system must cope with higher sub-detector occupancies, higher rate and higher network load. In this paper, we describe the architecture, functionalities and technological challenges of such an upgraded system.

Summary

The LHCb experiment is planning a major upgrade during the LHC Long Shutdown 2 in order to increase the amount of recorded data by a magnitude factor of 10. Some sub-detector technologies will perform adequately in the upgrade environment, whilst others will be replaced. However, the upgrade requires the complete replacement of all Front-End electronics and data acquisition (DAQ).

A fully trigger-less 40 MHz readout architecture has been envisaged as the baseline for the upgrade of the LHCb readout architecture. The architecture aims at removing entirely the first-level hardware trigger in order to record every bunch crossing in the LHC and make every event available to the high-level software trigger. Such choice presents major challenges and technological solutions which are outlined in this paper.

In particular, we will focus our attention on the implementation of trigger-less Front-End electronics. The sub-detector electronics will run without the aid of a first-level trigger, recording and transmitting every LHC bunch crossing. Moreover, the Front-End electronics will profit from the development of a generic radiation-tolerant data link. We will present plans for the implementation of the Front-End electronics with this link and the implications of this choice on the entire readout architecture. Investigations are ongoing to evaluate the use of Field Programmable Gate Arrays (FPGAs) in FE environments, and these will be summarized.

New technologies for the readout and DAQ system are also envisaged. A common electronics board will be used as the backbone of the readout architecture. This board is based on Advanced Telecommunications Computing Architecture (ATCA) technologies, dense optical links and powerful FPGAs which allow for a highly integrated and cost-effective system. This board will take the role of a module to read data from sub-detector, but, thanks to its flexibility, will also take the role of specific control boards to supervise the entire readout system.

A new fast readout control system is being developed to transmit fast commands, timing information and clock to the entire readout electronics. This system will act as the supervisor of the entire readout system by distributing fast commands via optical links. Furthermore, this system will be interfaced to the global LHCb Experimental Control System and transmit configuration data to the Front-End electronics. The data bandwidth provided by the generic link allows the sharing of hardware resources for both fast and slow commands. The implementations and implications of such a solution are described in this paper.

Finally, new solutions and technologies for event building networks will also be presented as the new LHCb DAQ network will need to cope with a multi-Tb/s dataflow.

To conclude, we will outline plans for the development of the system over the next years and the technological challenges which will need to be faced during this period.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: 132

Type: **Poster**

Radiation tolerance tests of SRAM-based FPGAs for the possible usage in the readout electronics for the LHCb experiment.

Tuesday, September 24, 2013 6:02 PM (1 minute)

This paper describes radiation studies of SRAM-based FPGAs as a central component of the electronics for a possible upgrade of the LHCb Outer Tracker readout electronics to a frequency of 40 MHz. Two Arria GX FPGAs were irradiated with 20 MeV protons to radiation doses of up to 7 Mrad. During and between the irradiation periods the different FPGA currents, the package temperature, the firmware error rate, the PLL stability, and the stability of a 32 channel TDC implemented on the FPGA were monitored. Results on the radiation tolerance of the FPGA and the measured firmware error rates will be presented. The Arria GX FPGA fulfils the radiation tolerance required for the LHCb upgrade (30 krad) and an expected firmware error rate of $\sim 10^{-6}$ Hz makes the chip viable for the LHCb Upgrade.

Summary

The development of ASICs for the readout of high-energy physics experiments is time consuming and expensive, in particular for projects which only need a small number of readout chips. For the current LHC experiments the development of radiation hard or radiation tolerant ASICs was often the only solution to construct the high performance readout. Meanwhile, there exists high performance FPGAs with high bandwidth transceivers available which provide a large number of logic elements to realize even multi-channel TDC applications. Modestly radiation tolerant commercial SRAM-based FPGAs could provide viable solutions, at least for apparatus in regions with smaller radiation levels. FPGA based readout electronics would provide a higher flexibility at probably small costs than the development of complicated ASICs.

We have studied the radiation tolerance of the Arria GX FPGA from Altera on which a multi-channel TDC were implemented. The FPGA based design could be a possible option for the replacement of the readout electronics of the LHCb Outer Tracker detector to accommodate a 40 times higher readout speed. Two FPGAs were irradiated with 20 MeV protons at the Max Planck Institute for Nuclear Physics to study this.

For this test, a PCB was developed to carry the FPGA, which is pin compatible to the existing readout board of the LHCb Outer Tracker. The FPGA used in this test board, replaces the 32 channel TDC for drift time measurements, the OTIS chip and the GOL serializer chip. Both chips have to be replaced for the upgrade of LHCb to a 40MHz readout. The test boards were irradiated with protons leaving the beam vacuum through a 100 μm stainless-steel window, travelling through 8 cm of air to the FPGA. Before the irradiation, the beam profile was measured with a straw-tube module. Using these data, a simulation was written to describe the dose in the different parts of the experimental setup. In addition, three pairs of passive dosimeters (alanine) were used to measure the integrated dose at different spots in the beam profile. Simulation and measurements show a very good agreement.

During and between the irradiation periods, the different FPGA currents, the package temperature, the firmware error rate, the PLL stability and the stability of a 32 channel TDC were monitored. The behaviour of the different currents during irradiation with different intensities and durations as well as subsequent power cycles with reconfiguration of the FPGA will be described. In addition, the measured firmware error rate will be illustrated and compared to the Outer Tracker readout electronics environment of the LHCb upgrade scenario. The frequency and phase stability

of the PLL, which is not only crucial for the TDC will be shown. Also the stability of the TDC measurement and the change of the bin size versus dose will be presented.

The results of the irradiation campaign show that the Arria GX FPGA exceeds the required radiation tolerance of 30 krad for the upgrade of the LHCb Outer Tracker to a 40MHz readout with an expected firmware error rate of $\sim 10^{-6}$ Hz makes a usage of the chip in LHCb feasible.

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Session Classification: Poster

Contribution ID: 133

Type: **Poster**

Optical Fibre at HL-LHC

Tuesday, September 24, 2013 5:36 PM (1 minute)

We present results on all aspects of fibre reliability after exposure to the expected doses at HL-LHC. The results for the cold Radiation Induced Attenuation (RIA) are reviewed. The results of new studies of the effect of radiation on fibre bandwidth and mechanical reliability are presented. The fibre bandwidth was studied using measurements of chromatic dispersion and Differential Mode Delay (DMD). The mechanical reliability was studied using dynamic testing and the quality of the cladding was determined by micro-bending trials. These studies allowed us to qualify one SM fibre for use at HL-LHC.

Summary

The readout of the upgraded ATLAS and CMS detectors at HL-LHC will use high speed optical links. The fibres will receive a dose of up to about 500 kGy(Si). The fibres will be largely inaccessible during the 10 year operation. It is therefore vital to understand all aspects of fibre performance in this harsh environment. This paper will summarise the results that allow us to qualify multi-mode (MM) and singlemode (SM) fibres for use at the HL-LHC. The main effect of radiation damage on fibres is to increase the Radiation Induced Absorption (RIA) and this effect is exacerbated by the low temperature which reduces the rate of beneficial annealing. The cold RIA studies will be briefly reviewed.

This paper will focus on new results on two other aspects of radiation damage to fibres; the decrease in bandwidth and the degradation of the mechanical reliability. It is well known that the RIA is wavelength-dependent. Therefore according to the Karmers-Kronig relation, there must be an associated change in the real part of the refractive index. This effect on the chromatic dispersion will tend to reduce the fibre bandwidth. The high bandwidth MM fibres have very precisely defined refractive index profiles over the fibre core, in order to achieve the optimal modal bandwidth. Therefore even a very small change due to radiation damage, could potentially induce a large decrease in the modal bandwidth. We have studied these effects in collaboration with Prysmian for one of the MM fibres that we qualified for use at HL-LHC from the RIA perspective. The chromatic dispersion was studied by measuring the delay time over long lengths of fibre at several different wavelengths and the dispersion was determined by fitting analytic functions to the data. The modal bandwidth was studied using the Differential Mode Delay (DMD) technique. These studies allowed us to qualify a MM fibre from the perspective of bandwidth after radiation.

Very little was known about the mechanical reliability of fibres after radiation damage. We have studied the mechanical reliability of fibres before and after radiation damage for SM and MM fibres. The mechanical reliability of fibres decreases with time because of the growth of micro-cracks at the surface of the glass. The n-value (a proxy for lifetime) of the fibre was estimated from dynamic pull tests at different pull speeds. From our study of irradiated and unirradiated fibre using axial pull testing we were able to qualify one SM fibre from the perspective of mechanical reliability after radiation damage. On-going studies using 2-point bend tests aim to qualify a second SM fibre and two MM fibres. We also performed micro-bending trials and determined that the quality of the cladding was not affected by radiation damage.

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Session Classification: Poster

Contribution ID: 134

Type: Oral

Evaluation results of xTCA equipment for HEP experiments at CERN

Tuesday, September 24, 2013 9:51 AM (24 minutes)

The MicroTCA and AdvancedTCA industry standards are candidate platforms for modular electronics for the upgrade of the current generation of high energy physics experiments. The PH-ESE group at CERN launched in 2011 the xTCA evaluation project with the aim of performing technical evaluations and eventually providing support for commercially available components. Different devices from different vendors have been acquired, evaluated and interoperability tests have been performed. This paper presents the test procedures and facilities that have been developed and focus is given to the evaluation results including electrical, thermal and interoperability aspects.

Summary

The Telecommunication Computing Architecture (xTCA) is a series of specifications defined by the PCI Industrial Computer Manufacturer Group (PICMG) including AdvancedTCA (ATCA), AdvancedMC (AMC) and MicroTCA (MTCA). These specifications define a modular standard architecture by establishing physical, electrical and functional specifications and ensuring interoperability. xTCA offers a wide range of form factors and allows different levels of redundancy for power architecture, cooling system and management. This makes xTCA an interesting platform for a wide range of applications such as Military/Aerospace, Communications, Medical and Industrial. In 2009 the PICMG consortium, driven by the physics research community, released the MTCA.4 standard as a complementary specification to the MicroTCA. This specification defines the guidelines for the implementation of Rear Transmission Modules (RTMs) and provides precision timing for data collection electronics. Several independent groups at CERN and in external institutes have started to develop ATCA and MTCA modules and the question arises to how these modules should eventually be housed. In this framework, the PH-ESE group at CERN launched the xTCA Evaluation Project with the goal of providing technical evaluation of xTCA systems with a clear focus on the infrastructure equipment such as shelves, power supplies, power modules, cooling modules etc. The project includes electrical evaluation of power modules, thermal characterization of crates and IPMI functionality tests. The electrical evaluation of the power modules includes static and dynamic regulation tests, efficiency and power factor measurements, ripple and noise characterization and overcurrent protection test. The thermal test aims to estimate the cooling unit efficiency and the airflow homogeneity inside a shelf. The IPMI functionalities of commercial equipment have been tested using a commercial fully automated test suite for testing the Hardware Platform Management Software and IPMC firmware implemented in xTCA based systems. A complete test setup for ATCA and MTCA architectures has been built in our lab. AMC and RTM load modules have been developed in-house for electrical and thermal tests. The control and monitoring of the equipment under test is based on a Labview interface developed to automate the test procedure. During the test phases, several interoperability problems and technical issues have been uncovered and addressed by working in close collaboration with the manufacturers. This allowed us to acquire knowledge and experience with these new architectures. For each component a detailed evaluation report has been written. A number of reports are already available and can be consulted by anyone in need of some recommendation baseline to build up an xTCA system. This paper shows the test procedures and facilities used and reports the evaluation

results with a clear focus on the electrical, thermal and interoperability aspects of the tested xTCA equipment.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: 135

Type: **Poster**

The Charge Pump PLL Clock Generator Designed for the 1.56 ns Bin Size Time-to-Digital Converter Pixel Array of Timepix3 Readout Chip

Tuesday, September 24, 2013 5:06 PM (1 minute)

Timepix3 is a newly developed pixel readout chip which is expected to be operated in a wide range of gaseous and silicon detectors. It is made of 256 x 256 pixels organized in a square pixel-array with 55um pitch. Oscillators running at 640MHz are distributed across the pixel-array and allow for a highly accurate measurement of the arrival time of a hit. This paper concentrates on a low-jitter PLL that is located in the chip periphery. This PLL provides a control voltage which regulates the actual frequency of the individual oscillators, allowing for compensation of process, voltage and temperature variations.

Summary

The Timepix3 predecessor, labeled Timepix, originated from the successful Medipix2 ASIC developed at CERN. It was operated as active anode in various gaseous detectors with gas electron multipliers (GEMs) and MICROMEGAS for gas amplification. Such charge collection on the bare pixels of a especially developed ASIC is one of the readout concepts pursued for a TPC operated at a future linear collider. However, this application demands for several improvements now implemented in the recent Timepix3 ASIC.

The Timepix3 readout chip was designed by a collaboration of CERN, NIKHEF and the University of Bonn. It features an active surface of 1.4 x 1.4 cm². Each pixel contains an analog front end: a charge sensitive amplifier, a discriminator and a 4-bit digital-to-analog converter for threshold adjustment. Signals of positive and negative polarity can be processed. The digital part of the pixel includes a 10-bit time-over-threshold counter, a 14-bit coarse time-stamping register and a 4-bit fine time-stamping counter. Each pixel can be programmed to work on one of three different modes: Event counting & Integral ToT, Only ToA and ToA & ToT.

In order to avoid distributing a very high-speed clock signal into the pixel-array and to save the pixel area, eight pixels (called super pixel) share a high-speed voltage control oscillator (VCO) that is based on a small area RC ring-oscillator. A PLL circuit with an embedded replica of the ring-oscillator is located in the periphery of the chip. By distributing the control voltage rather than the clock signal to the pixel-array, all pixel-level ring-oscillators are forced to oscillate at 640MHz. This approach allows to stabilize the oscillation frequency by an external PLL, and hence to reduce the effect of fluctuations with respect to process parameter variations and temperature changes.

The developed PLL consists of a phase frequency detector (PFD), a charge pump, a third-order passive loop filter, a VCO and a digital divider. The PFD detects the phase and frequency differences between the reference and the feedback clock signal. These differences are converted into a control voltage by the charge pump and the loop filter. Once frequency and phase of the input reference are the same as those of the feedback clock signal, the voltage from the loop filter is used to control the pixel-level ring-oscillators for yielding a constant frequency of 640 MHz.

In August of 2011, a prototype called GOSSIPO4.1 has been designed and fabricated for verification of the basic Timepix3. It includes eight-pixel structures (i.e. super pixel) sharing one fast oscillator with a PLL control. The functionality of the PLL has been verified on this chip. The PLL generates a clock frequency of 640 MHz with a power consumption of 5 mW, at a supply voltage of 1.5 V. Measurements have shown the TIE jitter performance to be below 24 ps RMS at an additional 320

MHz output. The same PLL structure has been implemented in Timepix3, which was submit in May of 2013. The results of the Timepix3 PLL will be reported in this workshop.

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Session Classification: Poster

Contribution ID: 136

Type: Oral

Hardware, firmware and software developments for the upgrade of the ATLAS Level-1 Central Trigger Processor

Wednesday, September 25, 2013 9:50 AM (25 minutes)

The Central Trigger Processor (CTP) is the final stage of the ATLAS first level trigger system which reduces the collision rate of 40 MHz to a Level-1 event rate of 100 kHz. An upgrade of the CTP is currently underway to significantly increase the number of trigger inputs and trigger combinations, allowing additional flexibility for the trigger menu.

We present the hardware and FPGA firmware of the newly designed core module (CTPCORE+) module of the CTP, as well as results from a system used for early firmware and software prototyping based on commercial FPGA evaluation boards. First test result from the CTPCORE+ module will also be shown.

Summary

The Central Trigger Processor (CTP) is the final stage of the ATLAS first level trigger system which reduces the collision rate of 40 MHz to a Level-1 event rate of 100 kHz. The CTP makes the trigger decision based on a list of programmable selection criteria using trigger inputs from the calorimeter and muon trigger sub-systems as well as from other sources.

The CTP is entirely based on custom-built electronics modules housed in a single 9U VME64x chassis. The functionality of the CTP is largely implemented in FPGAs. However, due to the increasing luminosity of the LHC expected after the first long shutdown and the growing demands placed on the ATLAS Level-1 trigger system, the current CTP has reached its design limits.

Therefore an upgrade of the CTP is currently underway to significantly increase the number of trigger inputs to the CTP from 160 to 512, by operating the internal backplane at twice its design speed. In addition, the newly designed core module (CTPCORE+) of the CTP provides direct inputs for the potentially latency-critical signals from the Level-1 Topological Trigger Processor (L1Topo), which will also be deployed during the shutdown. With the CTPCORE+ module the number of trigger combinations that can be individually masked and pre-scaled will also increase from 256 to 512, allowing additional flexibility for the trigger menu. The timing backplane of the CTP and the output modules (CTPOUT+) will also be replaced in order to provide support for additional independent trigger partitions for calibration runs and detector commissioning. Finally, the upgraded CTPCORE+ will provide support for receiving trigger input signals over high-speed optical links for future trigger system upgrades (latency permitting).

We present the hardware and FPGA firmware of the newly designed CTPCORE+ module, as well as results from a system used for early firmware and software prototyping based on commercial FPGA evaluation boards. First test result from the final CTPCORE+ module will also be shown. The upgraded CTP will be deployed in the ATLAS experiment during 2014.

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Session Classification: Trigger

Contribution ID: 140

Type: **Poster**

Use of FPGA Embedded Processors for Fast Cluster Reconstruction in the NA62 Liquid Krypton Electromagnetic Calorimeter

Tuesday, September 24, 2013 5:23 PM (1 minute)

The NA62 experiment at CERN SPS aims to increase the precision in the measure of the Branching Ratio of the $K^+ \rightarrow \pi^+ \nu$ decay. The required background suppression level due to the decay $K^+ \rightarrow \pi^+ \pi^0$ can be achieved, among the others, implementing the photon veto in the angular range $[1,10]$ mrad by using a LKr calorimeter. This paper deals with the implementation of the LKr L0 trigger peak reconstruction algorithm on an FPGA by using a mixed architecture based on soft core embedded processors together with custom VHDL modules. This solution allows an efficient and flexible reconstruction of the energy-deposition peak.

Summary

The NA62 experiment at CERN SPS aims to study the rare kaon's decays $K^+ \rightarrow \pi^+ \nu$. In two years of data taking the experiment goal is to collect about 100 events with 10% of estimated background. The required background suppression level can be achieved by the use of kinematic discrimination and more others specific particles vetoes. The photon veto system design is focused on the suppression of the dominant background originated from the decay $K^+ \rightarrow \pi^+ \pi^0$. In particular, the role of the Liquid Krypton (LKr) high-performance electromagnetic calorimeter is to veto photons in the angular range $[1,10]$ mrad. The Calorimeter REAdout Module (CREAM) provides 40MHz sampling of the channels and each of them is digitized with a 14-bit resolution. The readout rate is up to 1MHz. The CREAM performs the summation of the selected channel samples, and sends the resulting "Super Cell" (32 tiles) data to the LKr L0 Trigger processor. This trigger system, composed of 36 TEL62 boards, has a three layer structure with consecutive layers connected each other with custom multi Gigabit links. The first layer, the Front End (FE), performs an accurate identification of the energy-deposition peak for a subset of calorimeter cells. The second layer, the first Concentrator stage, merges the peak information collected by the different FE boards and composes them to identify the clusters. The third layer, the second Concentrator stage, receives time ordered data from the previous layer and sends them to the L0 trigger processor.

This paper deals with the implementation of the photons' impact precise time computation algorithm. In particular, it will be presented the performances of such an algorithm on the ALTERA NiosII soft core embedded processors hosted on an FPGA. In order to improve the flexibility on the LKr L0 trigger system, thanks to the high density level of the last generation FPGA devices, we propose an architecture where, on a single device, the embedded processors can coexist together with some proprietary and custom VHDL modules. In this way, the parallel custom circuitual module will receive the data samples from the CREAM and it will be able to filter them with over threshold, peak in space and peak in time criteria. The "peak in time detection" event will give the start to the algorithm, implemented in C on a proper tailored embedded processor, that will reconstruct the energy-deposition peak on calorimeter. Finally, the occurrence time, the position and the energy will be properly coded to be sent to the custom Gigabit link and then to the first Concentrator. The possibility to fulfil the algorithm, or parts of it, on an embedded processor, that is programmable in high level programming language like C, makes the development and maintenance phases more feasible. Moreover the embedded processors are themselves customizable, which adds further

flexibility to the architecture. This mixed architecture, custom VHDL together with Soft Core Embedded processor, allows to develop an efficient and at the same time flexible fast computation.

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Session Classification: Poster

Contribution ID: 141

Type: Oral

SamPic0: a 16-channel, 10-GSPS TWDC digitizer chip for picosecond time tagging

Thursday, September 26, 2013 3:15 PM (25 minutes)

SamPic0 is a Time and Waveform to Digital Converter (TWDC) multichannel chip. Each of its 16 channels associates a DLL-based TDC providing a raw time with an ultra-fast analogue memory allowing fine timing extraction as well as other parameters of the pulse. Each channel also integrates a discriminator that can trigger it independently or participate to a more complex trigger. After triggering, the analogue data are digitized by an on-chip ADCs and only those corresponding to a region of interest are sent serially to the acquisition. The paper describes the detailed SAMPIC0 architecture and reports its main measured performances.

Summary

Time stamping with picosecond accuracy is an emerging technique opening new fields for particle physics instrumentation. For example, it permits the localization of vertices with a few mm precision, can help associating particles coming from a common primary interaction even in a high background or can be used for particle identification using Time of Flight techniques. It has been demonstrated that ps timing accuracy can be reached by sampling the detector signal in ultrafast analogue memories using Switched Capacitor Arrays (SCA) [1, 2] for reasonable power, space and money budgets. Moreover, the knowledge of the signal waveform permits extracting other useful parameters as charge, pulse width or risetime and optimizing the timing extraction algorithm during or even after data taking. Contrasting with the existing fast sampler chips usually designed for all-purpose application and requiring external electronics to be used for accurate timing, the SAMPIC0 chip, presented here, has been designed specifically for this type of application. SAMPIC0 is actually a technological demonstrator, but already usable for measurements with detectors, which is intended to be improved in the future to allow deadtime free operation. This chip, designed in the 0.18 μ m CMOS technology from AMS, integrates 16 measurement channels that can be operated independently or using a common trigger. Each of the channels integrates a discriminator, a 18-bit deep TDC and a 64-cell deep SCA. A 64-step DLL, common to all the channels, provides the multiphase clock used in the SCA and the TDC. This step, tunable from 100ps to 1ns, defines the TDC step as well as the SCA sampling frequency (1 to 10 GSPS). The input analogue signal is continuously sampled and stored at up to a rate of 10 GSPS in the 1GHz bandwidth analogue memory until an event is detected by the discriminator. A trigger signal is then generated, freezing the analogue memory, timestamping the event in the TDC and rising a flag indicating that an event is waiting from conversion and readout. The analog to digital conversion of the waveforms is performed in parallel over 11 bits for all the cells of the channels having detected an event. For this purpose, a 2 GHz Wilkinson ADC is associated with each analogue memory cell. Once this operation is finished, the data can be readout, using a 400MHz 14-bit LVDS bus, starting by the TDC data then followed by the SCA waveform for which it is possible to send only a zone of interest corresponding to the pulse. Once the SCA data has been converted, the channel is available for a new event so that the deadtime from a given channel of SAMPIC0 is of only 1 μ s. One major benefit of the proposed architecture is that it can use a rather slow discriminator as the latter provides only a trigger signal and not the actual timing accuracy which is derived from the sampled waveform.

The final paper will describe the chip architecture with more details and will give report of the performances measured on prototypes.

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Session Classification: ASICs

Contribution ID: 142

Type: **Poster**

Front end strategy for the daq system of a Kinetic inductance detector

Tuesday, September 24, 2013 6:16 PM (1 minute)

Cosmology studies call for accurate measurements of cosmic microwave background radiation anisotropies. A promising technique to achieve the required precision is based on big arrays of Kinetic Inductance Detectors (KID). In this paper, we describe, a new strategy to stimulate and read a KID array of 128 pixels based on FPGAs and analog to digital converters. The project can reach an analog bandwidth as high as 250 MHz and all pixels can be stimulated and read continuously and in parallel. Results are sent to an on-line PC based farm via Ethernet or PCIe protocol.

Summary

Cosmic microwave background radiation anisotropies calls for extreme precision measurement of photon energy in the range of 70 to 900 GHz. Recently, Kinetic inductance detectors, (KID) produced using silicon technique, have been shown to be useful to build big arrays. KIDs are superconductive bolometers, electrons are organized in Cooper pairs and an incident photon can break a pair, generating two quasi-particles. Thus changing their inductance. A measurement of the variation of the resonant properties of this detector permits to measure the energy of the impinging photon. each pixel is a resonator tuned on its own frequency. A feedline (composed of two strips) passes near each pixel. This feedline delivers a stimulus signal. If the stimulus signal is tuned on the resonant frequency of the pixel, the intensity of the signal is reduced and its phase is shifted. All pixels can be stimulated by a signal which contains all resonant frequencies: the comb signal. A simple and effective way to produce a comb signal is to produce N sinusoids (one for each pixel's proper oscillation frequency) and add them up. Digital system can generate sinusoids and make samples at regular interval of time. Each resonator has about 500 kHz of FWHM, so 2 resonant frequencies must be parted by a minimum of 1 MHz to be clearly distinguishable. Therefore a minimum bandwidth of 100 MHz (200 MHz clock frequency) is needed to stimulate the tones of 100 pixels. Field programmable gate arrays (FPGA) can be used in this environment because of their intrinsic capability of performing parallel computation. In this paper we describe a project and the strategy we have followed to create a stimulus which can be used to read 128 pixels. The FPGA chip we have used is XC7VX485T from Virtex 7 family of Xilinx. This chip has 2800 DSP48Es that are useful to generate sinusoids, add them up and to analyze on-board signal processed by KID array. We have successfully simulated a project that generates 128 tones with a period of clock of 2 ns, so we have 250 MHz of analog bandwidth. The same project, with on-chip signal analysis, can run at 300 MHz to achieving a bandwidth of 165 MHz. The signal after stimulating the KID array is received to be synchronized with itself and averaged in time. After this stage, data are delivered to a computer system. Data transmission protocols with the computer system are based on Ethernet and/or PCIe. Under normal circumstances earth microwave telescopes are modulated by a 10 Hz maximum oscillating signal. The bandwidth needed is about 50 Hz. Transmission rate can be computed multiplying the number of tones (128) by the rate modulation (50 Hz) and by the number of bits (16) of the cosine and sine signals results. This amounts to 205 kbps. The communication methods we use guarantee that data flowing at the expected physical rate can be collected since the Ethernet and the PCIe bandwidths are much higher.

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Session Classification: Poster

Contribution ID: 144

Type: **Poster**

Simulation of ATLAS SCT module response to LHC beam loss scenarios

Wednesday, September 25, 2013 6:06 PM (1 minute)

In the event of beam loss at the LHC, ATLAS inner detector components nearest the beamline may be subjected to unusually large amounts of radiation. Understanding their behavior in such an event is important in determining whether they would still function properly. We built a SPICE model of the silicon strip module electrical system to determine the behavior of its elements during a realistic beam loss scenario, and to decide which further tests of the silicon strip detector system are necessary. We found that the power supply and bias filter characteristics strongly affect the module response in such scenarios.

Summary

Previous tests of the ATLAS silicon strip detector front-end readout electronics, the ABCD ASIC, have confirmed the ABCD's design specifications. That is, it can withstand 5 nC of charge deposited over a time interval of 25 ns due to front-end protection structures [1]. Simulations of beam loss suggest that sensors will have a rather uniform particle flux of up to 0.5×10^6 MIP (1.9 nC) per strip, every 25 ns [2]. A finite charge collection time that scales as $q^{1/3}$ due to charge screening effects [3] means that charge collection of successive pulses can overlap, possibly resulting in large, continuous currents going to strip implants. Since the readout electrodes are near ground potential due to input impedance of the ABCD chip, high implant potential can lead to breakdown of the coupling capacitors. Our work investigates what role, if any, each of the silicon strip detector components play in dissipating charge on the implants or preventing these charges from accumulating. We also consider what effect this has on the resulting charge deposited into the ABCD. We simulate a beam loss scenario with various time profiles, e.g. where the charge of each pulse increases linearly from 0 to 1.9 nC over a time span of 100 ms.

To investigate the behavior of the silicon strip detectors during a beam loss scenario as described above, we have built a SPICE model. Our model includes the power supply, bias filter, sensors, ABCD front-end, and cables. Cables are incorporated using a standard R-L-C lumped element model. The power supply is built using a standard voltage source with other components to give it current limiting behavior. The bias filter is a network of resistors and capacitors, and completely matches its specified circuit diagram. Other components of the model are not standard. Here we provide only a brief overview of their implementation. For the purposes of this study, we assume the ABCD front-end can be completely modeled by the base-emitter behavior of its input transistor. Thus, we use a diode whose behavior is tuned in SPICE to match data curves from previous studies. We explicitly model the response of the punch-through protection structures [4], and the dependence of the injected charge on the bias voltage. Combinations of circuit elements simulate time-dependent charge injection into the sensor and the expected response of the implant strip, coupling capacitor and readout strip, along with the bias resistors and bias ring.

We find that the system behavior is strongly affected by three self-limiting phenomena:

- The power supply current limit affects the sensor bias potential during the ramp-up of the incident flux.
- The resistors in the bias filter further reduce the bias voltage on the sensors due to the voltage drop across them.
- The reduced bias voltage on the sensor leads to smaller depletion depth which results in less collected charge.

These effects provide a larger measure of safety during beam loss events than we have previously

assumed.

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Session Classification: Poster

Contribution ID: 145

Type: **Poster**

FEERIC, a very-front-end ASIC for the ALICE Muon Trigger Resistive Plate Chambers

Wednesday, September 25, 2013 4:39 PM (1 minute)

The ALICE Collaboration at the CERN-LHC has started a vast program of upgrades of the detector in the context of the increase of the luminosity of the LHC from 2018 on. The present very front-end electronics (VFE) of the Muon Trigger, whose acronym is ADULT, must be replaced to limit the aging of the Resistive Plate Chambers (RPCs) in the future expected operating conditions. For this purpose, the new VFE, FEERIC, will have to perform an amplification of the analog input signal (this is not the case for ADULT). This will allow to operate the RPCs in avalanche mode with a lower gain at the level detector gas, in comparison to the current situation.

This VFE represents 21,000 channels, distributed over 2400 electronics cards equipped with one or two FEERIC ASICs. A total of 3000 ASICs of 8 channels each is necessary. The future ASIC has to insure mainly the following functions: amplification, discrimination and LVDS output stage. FEERIC will be capable of handling bipolar signals varying from ± 20 fC up to ± 5 pC. A prototype chip has been designed using the $0.35 \mu\text{m}$ CMOS technology of AMS. The FEERIC ASIC description, technical choices and performance from simulations and tests will be presented.

Summary

The LHC upgrade plan foresees an increase of almost one order of magnitude of the p-p and PbPb collision rates after 2018. In order to reduce the aging speed of the RPC detectors of the ALICE Muon Trigger [1], [2], in such a context, it has been proposed to replace the present VFE ADULT [3] by a new one called FEERIC. Unlike ADULT, FEERIC should perform amplification of the analog input signal from the detector at the VFE level. With such a new feature, the RPCs could be operated in genuine avalanche mode with a reduction by one order of magnitude of the charge per signal produced in the gas. The requirements of the FEERIC ASIC can be listed as follows:

- It must process both positive and negative RPC signals, depending on the readout plane position relative to the electrode polarity;
- The requested dynamic range is from 20 fC to 5 pC, while the expected mean charge at the working point is

rather 50-100 fC;

- The level of noise should be limited to 2 fC rms;
- The time resolution must be better than 1 ns rms in the whole operating dynamic range;
- The time walk must be less than 1 ns over the whole operating dynamic range;
- The output signal width must be equal to 23 ± 2 ns;
- After a signal passing the threshold, the electronics must be blind during 100 ns;
- The output format is Low Voltage Differential Signaling (LVDS);
- It must present a 50 resistance at the input in order to match the characteristic impedance of the readout strips;
- The power consumption must be less than 100 mW per channel;
- It is constituted of 8 channels per ASIC.

The technology used to design this VFE is the low cost AMS 0.35 μm CMOS technology. One channel block diagram is composed of a transimpedance amplifier, a zero-crossing discriminator, a one shot and an LVDS output stage. The current preamplifier amplifies the input signal carried by the strip. Then a zero-crossing discriminator delivers a signal whose timing (relative to the input signal) is amplitude independent. The one shot permits to obtain an output signal width equal to 23 ns and after a signal passing the threshold, the electronics is blind during 100 ns. Finally, an LVDS output stage allows to drive an output signal of ± 350 mV on a resistive load of 100

The results obtained show the time resolution of FEERIC which depends on the jitter introduced by noise and the time walk essentially driven by the performance of the zerocrossing. The obtained time resolution is 300 ps rms for an input charge of 50 fC, and 100 ps rms for an input charge of 100 fC. Concerning the time walk, it is less than 600 ps for the whole charge range above 50 fC. The global power consumption per channel is estimated to 70 mW, with a 3 V power supply voltage.

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Session Classification: Poster

Contribution ID: 147

Type: Oral

Characterization of the CBC2 readout ASIC for the CMS strip-tracker high-luminosity upgrade

Thursday, September 26, 2013 9:50 AM (25 minutes)

The CMS Binary Chip 2 (CBC2) is a full-scale prototype ASIC developed for the front-end readout of the high-luminosity upgrade of the CMS silicon strip Tracker. The 254-channel, 130nm CMOS ASIC is designed for the binary readout of double-layer modules, and features cluster-width discrimination and coincidence logic for detecting high-PT track candidates. The chip was manufactured in January 2013 and has since been bump-bonded to a dual-chip hybrid and extensively tested. The CBC2 is fully functional and working to specification: we present the result of electrical characterization of the chip, including gain, noise, threshold scan and power consumption, together with the performance of the stub finding logic. Finally we will outline the plan for future developments towards the production version.

Summary

The CMS Binary Chip 2 (CBC2) is the latest version of the silicon strip readout ASIC being developed for the High-luminosity upgrade of CMS (Phase II). The CBC2 is a 254-channel, bump-bonded full-scale prototype which includes the functionality necessary to identify hits associated with high-PT tracks (“stubs”). Designed in 130nm CMOS, CBC2 is a binary readout ASIC building on the successful first CBC prototype: each channel comprises of pre-amplifier, shaper and comparator; the L1-triggered data are stored in a 256-deep digital pipeline and serially read-out un-sparsified. Unlike its predecessor, the CBC2 is designed to instrument double-layer modules and is therefore a substantially revised chip that includes major new features, such as the adoption of a bump-bonded layout, coincidence logic for stub finding and cluster-width discrimination, and twice the number of channels than its predecessor. The input channels are divided between top and bottom sensors allowing the chip to look for coincidences between the two layers: the position of these stubs can be read out serially for test purposes. A fast-OR test pad signals the presence of either stubs or input activity allowing self-triggering operation.

The CBC2 was delivered in January 2013: a manufacturing split provided wafers with metallization for either wire-bonding or bump-bonding. The wire-bonded prototypes were initially tested for a rapid performance evaluation: the CBC2 was characterized and found to be working well. The C4-processed chips were then probe tested on the wafer before being diced and mounted on a dual-chip hybrid. Together with the yield figures resulting from the wafer-probing of ~800 chips, we present the results of full electrical characterization, including gain, noise, linearity, threshold scans and power consumption. We also present a measurement of the performance of the on-chip LDO and DC-DC switched capacitor converter.

The dual-CBC2 module obtained by bonding microstrip sensors to the hybrid is an important milestone towards the 2S (“strip-strip”) module being developed for the outer Tracker. It allows for the data links between adjacent CBC2s to be exercised and, by incorporating only known-good dice with a high number of bump-bonded pads, these modules will provide a good indication of the assembly yield before a more extensive production is launched. Importantly, they also offer a unique opportunity to evaluate the performance and efficiency of the PT-cut concept in a realistic scenario such as a test beam.

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Session Classification: ASICs

Contribution ID: 148

Type: **Poster**

The readout electronic of EUSO-Balloon experiment

Wednesday, September 25, 2013 6:07PM (1 minute)

A complex readout electronic chain has been designed for the EUSO-Balloon project. It contains two elements: the EC units (9 of them) and the EC-ASIC boards (6). The EC unit includes 64-channel Multi-Anode Photomultipliers and a set of pcbs used to supply the 14 different high voltages needed by the MAPMTs and to read out the analog output signals. These signals are transmitted to the EC-ASIC boards which contain 6 SPACIROC ASICs each. During the year 2012, prototypes of each board were produced and tested successfully, leading to the production of the flight model pcbs.

Summary

EUSO-Balloon experiment is a pathfinder for the satellite mission JEM-EUSO [1] which goal will be to observe Extensive Air Shower produced in the atmosphere by the passage of the high energetic extraterrestrial particles above 10^{19} eV. Both instruments (balloon and satellite) will detect fluorescent UV photons released by the EAS thanks to Multi-anode photomultipliers (MAPMT) arranged in 6x6 matrices inside Photo Detector Modules. A set of lenses is used to focus the photons on the PDM which can be compared to a UV camera taking pictures every 2.5 μ s period (GTU).

The aim of the experiment is to launch a balloon, at 40 km of altitude, equipped with complete Photo Detector Module (PDM) and Data Processing systems. This project, supported by CNES, involves the whole JEM-EUSO collaboration and is meant to prove that constructing such an instrument is technologically possible and that the performances are satisfying. Moreover, complex trigger algorithms will be assessed and the main back ground (night glow) will be studied.

The readout electronic of the PDM can be divided in two parts:

- 9 EC (elementary cell) units
- 6 EC_ASIC boards, each one welcoming six SPACIROC ASICs

The EC units consist in four MAPMTs, arranged in a matrix of 2x2, and a set of 3 different boards (EC_dynode, EC_anode and EC_HV) which are used to supply 14 different high voltages (ranging from 20 V to 1000 V) and to collect the analog signals of the 64 channels of each MAPMT.

These analog signals are sent to the EC_ASIC boards, which are complex pcbs welcoming six SPACIROC ASICs [2]. This microelectronic chip has two main measuring modes running in parallel: the photon counting mode for each input and the charge-to-time conversion for groups of 8 channels, respectively allowing counting the number of photons detected in each pixel of the PDM and estimating the charge generated by the photons. The design was done using AMS SiGe 0.35 μ m process. The final chip dimensions are 4.6 mm x 4.1 mm (19 mm²).

The main specifications of this readout electronic are the following:

- Individual photon counting with a trigger efficiency of 100% for charger greater than 50 fC (1/3 of photo-electron for a gain of 10^6)
- Low power consumption (e.g. 1 mW/channel for the ASIC)
- Compactness of the boards to fit in the restricted volume available in the mechanic of the PDM
- Potting of the parts involving high voltage to avoid destructive sparking due to the low pressure (3 mbar) at 40 km of altitude

The tests carried out on the prototypes built during the year 2012, showed that the strategy taken was appropriate and that these specifications were satisfied thoroughly. During 2013, the flight model instrument will be integrated and tested before being launched in 2014.

This paper will present in detail the design of the EC unit and EC_ASIC as well as the tests performed on the prototypes.

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Session Classification: Poster

Contribution ID: 149

Type: Oral

Hybrid circuit prototypes for the CMS Tracker upgrade front-end electronics

Friday, September 27, 2013 10:10 AM (25 minutes)

New high-density interconnect hybrid circuits are under development for the CMS tracker modules at the HL-LHC. These hybrids will provide module connectivity between flip-chip front-end ASICs, strip sensors and a service board for the data transmission and powering. Rigid organic based substrate prototypes and also a flexible hybrid design have been built, containing up to eight front-end flip chip ASICs. A description of the function of the hybrid circuit in the tracker, the first prototype designs, results of some electrical and mechanical properties from the prototypes, and examples of the integration of the hybrids into detector modules are presented.

Summary

The increase of luminosity planned at the HL-LHC is setting up new constraints for the CMS Tracker that imposes its upgrade. The higher luminosity will result in a significant increase of the rate of events in the tracker that is addressed with the implementation of a binary readout tracker with higher density of channels, provided with a new Level 1 Track Triggering functionality. The new tracker consists of modules containing the sensors, hybrid circuits and all the data transmission and powering services. The modules will have strip - pixelated strip sensors on its inner layer, and strip-strip sensors on its outer and endcap layers. A dedicated front-end ASIC prototype was developed for the outer tracker layer modules, namely the CMS Binary Chip 2 (CBC2) that became available for testing in 2013, enabling the outer layer hybrid and module development.

In a first step, a rigid organic based substrate has been produced to enable the functional testing of a pair of CBC2 chips and to evaluate the high-density interconnection design constraints that are required for the connection of the ASICs with the strip sensors on both sides of the hybrid. This hybrid circuit was constructed as a six layers built-up substrate using a thin LCP core, following as much as possible the expected module design requirements. The CBC2 chips have been successfully tested on these hybrids, and the hybrids wire bonding and mechanical features to assemble them into modules have been evaluated.

A second prototype rigid substrate hybrid was built, using an aramid core aiming for an improved stiffness, but using the same design rules as those used for the first prototype. Eight dummy chips have been used per hybrid, aiming for a mechanical study of a full-scale rigid assembled hybrid, and in particular to test the feasibility of wire bonding and compatibility of the mechanical integration into a module. This prototype enabled also the testing of fine tracks and via test arrays for manufacturability and reliability studies.

A third prototype hybrid using a flexible circuit made on a polyimide substrate is at this time in production. The very high routing density allows limiting the number of layers to four. The flexible hybrid contains eight CBC2 chips, and the flexible substrate is to be wire bonded to a pair of 10 cm X 10 cm sensors. The circuit is representative of a real size substrate as intended for the modules assembly. This technology implies a different module design; it also requires the development of dedicated tools to embed stiffeners and to enable the manipulation and folding of the flex circuit with accuracy. Results from these prototypes are expected also by the time of the workshop.

For both these rigid and flexible hybrid, the respective issues concerning their integration into the outer tracker modules will be reported.

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Session Classification: TOPICAL (Packaging & High Density Hybrids)

Contribution ID: 150

Type: Oral

Power pulsing schemes for analog and digital electronics of the vertex detectors at CLIC

Wednesday, September 25, 2013 10:15 AM (25 minutes)

The precision requirements of the vertex detector at CLIC impose strong limitations on the mass of such a detector ($<0.2\%$ of X_0 per layer). To achieve such a low mass, ultra-thin hybrid pixel detectors are foreseen, while the mass for cooling and services will be reduced by implementing a power-pulsing scheme that takes advantage of the low duty cycle of the accelerator. The principal aim is to achieve significant power reduction without compromising the power integrity supplied to the front-end electronics. Voltage and current based power-pulsing schemes are proposed and their electrical features are discussed on the basis of measurements.

Summary

The vertex detector is the innermost detector at the proposed CLIC linear electron-positron collider. It is composed of several layers of pixel sensors and readout ASICs. In the central section the layers are arranged in "ladders". The precision physics requirements limit the material budget for sensors, readout, support, cooling and cabling to less than 0.2% of a radiation length (X_0) per detection layer. The power consumption of the readout electronics strongly impacts the required low material budget of the detector. To reduce the cable and cooling material, the average power per unit area has to be small (<50 mW/cm²). Collision at CLIC will occur in bunch crossings every 0.5 ns during a bunch train of 156 ns. The time between consecutive trains is approximately 20 ns. The readout ASICs can then be active during a time window containing the bunch train and remain idle in the other part of the cycle, thus reducing the average power. The use of the beam duty cycle to reduce the average power is known as power pulsing.

The use of a power pulsing scheme implies that the ASIC current consumption has to change suddenly from its idle value (few hundreds of mA) to full load (more than 40 Amps for a single ladder composed of 24 ASICs) within a few microseconds, then remain constant for enough time to record and process the events (few tens of microseconds) and finally drop back to the idle current value. During the bunch train, the power consumption is at its maximum and constant, and the supplied voltage has to remain within 5% of the nominal voltage in order to allow for a correct functioning of the readout ASICs. The latter is particularly challenging, considering the big transient that takes place before the readout process.

The analog and digital components of the ASICs have different constraints and therefore will be powered separately.

A dummy load emulating the power consumption of the analog electronics of half a ladder and a power-pulsing scheme based on a voltage source to power the analog circuitry of the ladder were presented at TWEPP 2012. The scheme consisted of DCDC converters placed 30 cm away from the ladder, charging storage silicon capacitors placed in the ladder through low mass flex cables. Low dropout regulators (LDOs) in the ladder provided local voltage regulation to each readout ASIC. The proposal was validated through simulations and measurements of prototypes, with an estimated contribution to the material budget of the ladder of 0.145% of X_0 .

A power-pulsing scheme based on a controlled current source made it possible to further decrease the material contribution to 0.06% of X_0 and to remove the need for DCDC converters along the powering path. It consists of a controlled back-end current source that charges the silicon capacitors in the ladder with low current during the idle time. In this way, the charging current is dramatically reduced to less than 100 mA for a whole ladder. A prototype of this back-end current source was implemented using an FPGA. A dummy load emulating the power consumption of the

digital components is currently being implemented. It will be used to compare the performance of both power-pulsing topologies.

The talk will introduce the requirements and the proposed powering schemes and present simulations and prototype measurement results of the performance for both the digital and analog components.

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Session Classification: Power, Grounding and Shielding

Contribution ID: 151

Type: **Poster**

FPGA-based, radiation-tolerant on-detector electronics for the upgrade of the LHCb Outer Tracker Detector

Tuesday, September 24, 2013 5:22 PM (1 minute)

The LHCb experiment studies B-decays at the LHC. The Outer Tracker straw tubes detects charged decay particles. The on-detector electronics will be upgraded to be able to digitize and transmit drift-times at every LHC crossing without the need for a hardware trigger. FPGAs have been preferred to application-specific integrated circuits to implement dead-time free TDCs, able to transmit data volumes of up to 36 Gbits/s per readout unit, including the possibility of performing zero suppression. Extensive irradiation tests have been carried out to validate the usage of field-programmable devices in the hostile environment of the LHCb tracking system.

Summary

The LHCb experiment is redesigning its readout and data-acquisition system: the on-detector electronics will no longer receive a trigger, but will instead ship all data to be buffered and selected through a full physics reconstruction. The Outer Tracker detector, an array of 54,000 straw tubes covering an area of 5x6 m² with 12 detection layers, provides accurate drift-time to the tracking system of the LHCb spectrometer. The digitization is performed by the on-detector electronics, which then serializes and optically transmits the data. A detector module packs 128 straw tubes (2.4m long and 4.9mm diameter). In the high track-density environment of LHC, the challenge of an accurate and dead-time-free digitization of a 5-bits drift-time is combined with that of the trigger-less transmission of up to 36 Gbits/s from each on-detector readout unit.

To meet these challenges, we have developed a system combining the ability to perform time-to-digital conversion at each LHC clock cycle in a dead-time-free fashion, with that of selecting only data from channels with valid hits(zero-suppression) to reduce the data volume to the counting house. Our technological choice fell on field-programmable devices rather than ASICs; this allowed us to develop a highly-configurable on-detector electronics: one can vary the data size and the number of channels per circuit, perform zero-suppression, data spying and histogramming, etc. Our R&D provided two solutions: one based on the Altera Arria GX family, including high-speed serial devices, and the other on the flash-based Actel (now Microsemi)ProAsic3 family in combination with external serial transceivers from the GigaBit Transceiver (GBT) project. This contribution focuses on the Actel-based implementation. A 32-channels TDC core has been implemented in an A3PE1500-FG484 (using roughly 40% of core resources): the 25ns period of the LHC clock is divided in 32 time bins obtained from the outputs of four 320 MHz phased-locked loops (two edges, shifted in phase by 90 degrees); data from four 8-bits shift-registers are combined into a 32-bits hit-register, then translated into a 5 bits drift-time. Zero-suppression is performed before data is stored in an output fifo, scrutinizing one channel per clock cycle and producing a hit-pattern word. Our design has been implemented and tested in prototypes of the on-detector electronics (including an FPGA-based emulator of the GBT). Pulses resembling our detector signals have been injected to verify the TDC response and data integrity after zero-suppression. Integral and differential linearity have been measured and the dead-time-free performance verified.

We expect the hottest spot of our on-detector electronics to absorb a dose of about 1.5 Gray for each inverse femtobarn of integrated luminosity. The performance of A3PE1500 FPGAs has been studied in a series of dedicated irradiation tests, including a specific test of the PLL performance,

demonstrating that our system remains operational up to about 300 Gray (30 krad). Although this is sufficient for our application, we are also investigating the performance of the newest SmartFusion line of Microsemi FPGAs, which is expected to be considerably more radiation tolerant and is a viable alternative for our design.

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Session Classification: Poster

Contribution ID: 152

Type: Oral

ROC chips for imaging calorimetry at the International Linear Collider

Thursday, September 26, 2013 3:40 PM (25 minutes)

Imaging calorimetry at the International Linear Collider requires highly granular and innovative detectors. Technological prototypes have been built and tested under the CALICE collaboration framework and FP6 EUDET, FP7 AIDA EU programs. These prototypes are readout by multi-channel chips named SKIROC2, SPIROC2 and HARDROC2, designed in SiGe 350 nm technology by the IN2P3 OMEGA group.

In this presentation, the ASIC architectures and test results on test bench and at system level will be described as well as first results of test bench measurements performed on HARDROC3, which is the first of the “3rd generation” chip to be submitted and where the 64 channels are handled independently to perform zero suppress on chip.

Summary

Imaging calorimetry at the International Linear Collider requires new detectors with one hundred million channels that will be read-out with calorimetric performance, that is percent accuracy over 16-bit dynamic range. The readout electronics must be highly integrated and ultra-low power (μW per channel compared to W at LHC) to be embedded inside the detectors.

To tackle these challenges, R&D started in 2000 under the CALICE collaboration framework and FP6 EUDET, FP7 AIDA EU programs. Several detector technologies have been proposed and tested: Tungsten/Silicon for the Electromagnetic Calorimeter (ECAL), scintillating tiles SiPM readout for an Analog Hadronic Calorimeter (AHCAL) and RPC/Micromegas/GEM for a Semi Digital Hadronic Calorimeter (SDHCAL).

Detector prototypes have been built and readout by “ROC” chips (Read Out Chips) named SKIROC, SPIROC and HARDROC and designed in SiGe 350 nm technology by the IN2P3 OMEGA group. They have similar requirements in terms of low noise, low power and radiation hardness and thus similar design: a low noise input stage for amplification, a slow channel for charge measurement, a trigger channel, a conversion stage for internal time and charge digitization and a complex digital part to manage the acquisition, the conversion and the read out.

Different front-end architectures have been integrated for the various sensors and, to optimize the commonalities between the various detector proposals, the chips share a common backend and readout scheme. In order to address the numerous challenges, three generations of chips have been foreseen. The first generation consisted in analog readout ASICs that allowed characterizing the detector concepts in test beam, referred to as CALICE physics prototypes. The second generation addresses the integration issues with embedded electronics and performs analog amplification, shaping, internal triggering, digitization and local storage of the data in memory. Thousands were produced in 2010 to equip CALICE technological prototypes and are being tested by IN2P3, DESY, CERN, and KEK groups for their detectors.

Zero suppression must be added in the 3rd generation chips, which is a major modification as it increases the complexity of the digital part. HARDROC3 was submitted in March 2013. It is the first of the 3rd generation chip to be submitted. It integrates 64 channels which are handled independently to perform zero suppress on chip and reduce the data volume. Other features such as triple voting to ensure SEU hardness, a I2C link to load slow control configurations and a Phase

Lock Loop to generate the clocks internally are also integrated. First testbench results are expected this summer.

The architecture and the performance of these chips on test bench and at the system level will be detailed in this presentation.

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Presenter: SEGUIN-MOREAU, Nathalie (U)

Session Classification: ASICs

Contribution ID: 154

Type: Oral

A GLIB-based uTCA demonstration system for HEP experiments

Tuesday, September 24, 2013 10:15 AM (25 minutes)

The Gigabit Link Interface Board (GLIB) project is an FPGA-based platform for users of high-speed optical links in high energy physics (HEP) experiments. The project delivers hardware, firmware/software and documentation as well as provides user support. These resources facilitate the development of evaluation platforms of optical links in the laboratory as well as triggering and/or data acquisition systems in beam or irradiation tests of detector modules. This article focuses on the demonstration of a triggering and data acquisition setup for HEP experiments using hardware and firmware/software resources provided by the GLIB project.

Summary

The Gigabit Link Interface Board (GLIB) project is a development platform for users of high-speed optical links in high energy physics (HEP) experiments. The major hardware component is an FPGA-based double-width Advanced Mezzanine Card (AMC) conceived to operate either inside a μ TCA shelf or on a bench with an optional link to a PC. In order to ensure the GLIB AMC compatibility with legacy and future interfaces as well as enhance its I/O bandwidth, some FPGA Mezzanine Cards (FMCs) have been developed. Besides hardware devices, the project delivers firmware/software, documentation and user support. These resources facilitate the development of evaluation platforms of optical links in the laboratory as well as triggering and/or data acquisition systems in beam or irradiation tests of detector modules.

This article focuses on the demonstration of a triggering and data acquisition setup for HEP experiments using hardware and firmware/software resources provided by the GLIB project. The setup comprises a back-end (BE) and a front-end (FE) part communicating through a Gigabit Transceiver (GBT)/Versatile Link (VL), the new bi-directional rad-hard link operating at 4.8 Gb/s. The BE consists of a uTCA shelf containing an AMC processor blade and a GLIB AMC equipped with a custom FMC for interfacing with a VME-based Trigger/Timing and Control (TTC) system. The FE part, due to the unavailability of GBT-based boards and compatible FE ASICs, consists of an emulated version of these devices. The role of the GBT chipset and the FE ASIC(s) is played by another GLIB AMC (operating on a bench) and a commercial FMC carrier, respectively. For the communication with the BE, the "GBT" GLIB AMC carries a VL FMC equipped with a VL transceiver (VTRx). For the emulation of the electrical link (e-link) communication between GBT and FE ASIC, both cards carry e-link FMCs.

Using that setup, we demonstrate the complete chain of a new-generation HEP system i.e. TTC reception at the level of the BE, forwarding of slow control, clock and trigger information to the FE through the downstream GBT/VL, emulation of e-link communication between GBT and FE ASIC at the level of FE as well as reception of FE data at the level of BE via the upstream GBT/VL and high-speed data readout by the AMC processor through the backplane of the shelf (Fat Pipes) using PCI Express x4 Gen2.

It is important to mention that a board featuring a GBT transceiver (GBTx) ASIC, an FPGA as well as SFP+/VTRx sockets, namely the GBT Stand Alone Tester (GBT-SAT) board, is currently under development. In case the GBT-SAT will be available and the GBTx well characterized, the board could play the role of the FE system instead of the GLIB, making the demonstration even more realistic. In that case, the on-board FPGA will emulate FE ASIC module operation.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: 155

Type: Oral

The proposed trigger-less TBit/s readout for the Mu3e experiment

Tuesday, September 24, 2013 11:35 AM (25 minutes)

The Mu3e experiment searches for charged lepton flavor violation in the rare decay $\mu \rightarrow eee$ with a projected sensitivity of 10^{-16} . Precise measurement of the decay product momentum, decay vertex and time is necessary for background suppression at rates of 10^9 muons/s. This can be achieved by combining an ultra-lightweight pixel tracker based on HV-MAPS with two timing systems. The trigger-less readout of the detector with three stages of FPGA-boards over multi GBit/s optical links into a GPU filter farm will be presented. In this scheme data from all sub-detectors is merged and distributed in time slices to the filter farm.

Summary

The Mu3e experiment searches for charged lepton flavor violation in the rare decay $\mu \rightarrow eee$. Since the decay $\mu \rightarrow eee$ is extremely suppressed in the standard model with a $BR < 10^{-50}$ any observation would be a clear sign of new physics. In order to measure or exclude this decay with a sensitivity of 10^{-16} , more than 10^9 muons/s have to be observed for one full year. The background for this measurements is either combinatorial or stems from the radiative decay $\mu \rightarrow eee\nu\nu$. Precise measurement of the decay product momentum, decay vertex and time is necessary for background suppression. The low momentum of the decay electrons leads to large multiple scattering and demands detectors of extremely low radiation length in the active volume of the experiment. The high vertex and momentum resolution is achieved with the help of a tracking system based on high voltage monolithic active pixel sensors (HV-MAPS) thinned to 50 μm . These sensors not only have on-chip analog electronics but also digital zero suppression and fast serializers. The necessary high time resolution is obtained by a scintillating fiber tracker and a scintillating tile hodoscope, both equipped with SiPMs.

The high and continuous muon decay rate of $10^9/\text{s}$ and the event size of 1kBit per decay lead to a considerable amount of data of 1 TBit/s. The data of the full detector has to be merged and time slices of this data must be distributed to the individual nodes of the event filter farm online. The trigger-less TBit/s readout of the detector is based on three stages of FPGA driven readout boards. The first stage is located near the sensors and receives serial zero-suppressed data from the HV-MAPS at 800 MBit/s per link. The corresponding front-end boards for the SiPM based detectors either utilize the DRS5 chip developed at PSI or the STiC TDC developed at the KIP in Heidelberg. In all cases the data is reformatted and send over optical multi GBit/s links to off-detector read-out boards. There is one off-detector readout board per sub-detector partition and PC sub-farm. The first part of the data distribution can be accomplished by connecting the eight optical outputs of one detector front-end board to four different off-detector readout boards belonging to one PC sub-farm each.

The off-detector readout boards distribute the data within one PC sub-farm over optical links. The optically transmitted data is received by one PCIe-board inside each of the twelve PCs of one sub-farm. These PCIe boards build blocks of events from the full detector with the help of powerful FPGAs and transmit large data sets at high speed via PCIe to the graphical processing units (GPUs). Preferably the communication between these FPGAs and the GPUs is realized using direct memory access (DMA). Tracking and event reconstruction runs on the GPUs with the purpose of reducing the background events by a factor >1000 . The remaining up to 100 Mbytes/s of data are written to a storage system via Gigabit Ethernet.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: 156

Type: **Poster**

The LHCb Muon Upgrade

Tuesday, September 24, 2013 6:17PM (1 minute)

The LHCb collaboration is currently working on the upgrade of the experiment to allow, after 2018, an efficient data collection while running at an instantaneous luminosity of $2 \times 10^{33}/\text{cm}^2\text{s}^{-1}$. The upgrade will allow 40 MHz detector readout, and events will be selected by means of a very flexible software-based trigger. The muon system will be upgraded in two phases. In the first phase, the off-detector readout electronics will be redesigned to allow complete event readout at 40 MHz. Also, part of the channel logical-ORs, used to reduce the total readout channel count, will be removed to reduce dead-time in critical regions. In a second phase, higher-granularity detectors will replace the ones installed in highly irradiated regions, to guarantee efficient muon system performances in the upgrade data taking conditions.

Summary

The LHCb collaboration is currently preparing the upgrade of the experiment to allow, after 2018, an efficient data collection while running at an instantaneous luminosity of $2 \times 10^{33}/\text{cm}^2\text{s}^{-1}$. The upgrade will permit 40 MHz detector readout, and events will be selected by means of a very flexible software-based trigger.

The muon system will be upgraded to allow the complete event readout at 40 MHz and to reduce the system dead-time in some regions of the apparatus that will become critical at the upgrade instantaneous luminosities.

The upgrade of the muon system will be performed in two phases. In the first phase the off-detector readout electronics will be redesigned to allow complete event readout at 40 MHz. The new boards (the new off-detector electronics boards, nODEs), compatible with the current ones to simplify installation, will incorporate a new VLSI rad-hard ASIC (nSYNC) that will perform muon hit time measurement, bunch-crossing synchronization, event frame generation and zero suppression functionalities. Both the non-zero suppressed muon hit information and the zero-suppressed hit time information will be sent via GBT optical links to the new LHCb readout boards, the so-called TELL40, which will perform the subsystem readout at 40 MHz. The TELL40 boards will be built according to the ATCA standard. Each board will host 4 AMC mezzanines, each one equipped with a high-end ALTERA Stratix V FPGA to provide data decoding, formatting, buffering and finally transmission to the high-level trigger farm via 10Gb Ethernet interface. The FPGA is so powerful that it will also allow the muon trigger algorithms to be implemented on it, simplifying the current system and making it more reliable.

In this first phase of the upgrade the boards used for the muon detectors front-end configuration (service boards, SB) and for the front-end pulsing for time alignment purposes (pulse-distribution module, PDM) will also be replaced with newer versions (respectively the nSB and the nPDM), to improve the detector configuration and monitoring speed and capabilities by making an optimal use of the bandwidth provided by the GBT links. The GBT-SCA ASIC will be used for this purpose, since it provides many digital interfaces that are compatible with the current muon detector front-end electronics.

Finally, in this first phase of the upgrade, part of the muon readout channel logical-ORs, performed by the so-called intermediate boards (IB) and used to reduce the total readout channel count in the current muon system, will be removed to reduce the dead-time in some already critical regions.

This first phase of the muon system upgrade will be completed by 2019, at the end of the LHC Long Shutdown 2 (LS2), to allow the LHCb operation at an instantaneous luminosity of $2 \times 10^{33}/\text{cm}^2\text{s}^{-1}$.

Only in a successive phase, the muon group is considering the installation of higher-granularity detectors, able to operate at the very high particle rates of the upgrade, in particular in the most irradiated regions of the first muon stations. These new detectors, to be built using Triple-GEM technology, will replace the current Multi-Wire Proportional Chambers and will guarantee improved detector aging properties and reduced system dead-time, to allow an efficient muon system performance in the severe upgrade data taking conditions.

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Session Classification: Poster

Contribution ID: 157

Type: **Poster**

Common control and readout board for the Calorimeter and Tracker Front-end electronics of the SuperNEMO experiment.

Wednesday, September 25, 2013 6:20 PM (1 minute)

SN_CROB board is the common Control and Readout Board for the Calorimeter and Tracker Front-end electronics of the SuperNEMO experiment.

SuperNEMO is the next-generation (0 $\nu\nu\bar{\nu}$) experiment based on a tracking plus calorimetry technique. The demonstrator is made of a calorimeter (700 channels) and a tracking detector (6000 channels). These detectors front-end electronics use an unified architecture based on similar crates. SN_CROB board gathers the front-end data from the calorimeter or tracker FEBs and sends them through Ethernet link to the DAQ. It extracts the Trigger Primitive from the front-end data and sends them through serial link to the Trigger Board.

Summary

Experimental search for the neutrinoless double beta decay (0 $\nu\nu\bar{\nu}$) is of major importance in particle physics because if observed, it will reveal the Majorana nature of the neutrino ($\bar{\nu}=\bar{\nu}$) and may allow an access to the absolute neutrino mass scale.

SuperNEMO is the next-generation (0 $\nu\nu\bar{\nu}$) experiment based on the technique of tracking and calorimetry detector. The construction of SuperNEMO demonstrator (one module) has started in 2012 and its installation is expected in 2014 in the Modane Underground Laboratory (LSM) located in the Frejus tunnel in France. Competitive results are expected by 2015.

The SuperNEMO demonstrator module is designed to measure both energy and time of flight of each beta particle emitted from $\bar{\nu}$ decays in the central source foil and to reconstruct their trajectories in order to guarantee the signature of 0 $\nu\nu\bar{\nu}$ decays.

The demonstrator is made of a calorimeter (700 channels) and a tracking detector (6000 channels). These detectors front-end electronics use an unified architecture based on six similar crates that each host up to 20 Front-End Boards (FEB) and one SuperNemo Control and ReadOut Board (SN_CROB).

The Calorimeter Front-End Board (FEB) is a 16 channels board, which performs the acquisition of the calorimeter channels. This FEB works on the principle of circular memory using a 40 MHz clock reference and a sample frequency between 1.28 and 3.2 GHz.

The Tracker FEB is a 108 channels board, it performs the acquisition of the tracker channels. The Tracker FEB is based on a specific time stamper ASIC dedicated to the time measurement of Geiger cells with a resolution of 12.5ns.

If a first trigger occurs in due time, the corresponding data are sent through the backplane from the Calorimeter and /or Tracker FEBs to the SN_CROB.

The SN_CROB board gathers the front-end data from the calorimeter or tracker FEBs and sends them through Ethernet link to the data acquisition (DAQ) system. It extracts the Trigger Primitive (TP) from the front-end data and sends them through serial link to the Trigger Board (SN_TB). Moreover SN_CROB distributes the clock, the trigger and the control signals for all the boards in a crate. It can also provide its own clock. On each SN_CROB, four Fe-PGA each receive the data from five FEBs and one Ctrl-PGA (the board driver) performs the actions which are not specific to a data channel and is in charge of copying and sending through the experiment's control system the data stored into the Fe-PGA for spying purpose.

With respect to trigger, we extract the TP from each Fe-PGA and send them to Ctrl-PGA. Then

from the Ctrl-PGA, we compute the TP and build the Crate Trigger Word (CTW) which contains informations about hit multiplicity, particle zoning and event identification. It is sent to the SN_TB through serial link.

Concerning data, they are extracted from each Fe-PGA and sent to Ctrl-PGA which then sends them to the DAQ through Gigabit Ethernet transceiver. The communication between FPGA is ensured by a dedicated protocol based on a parallel interface for byte transmission.

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Session Classification: Poster

Contribution ID: 159

Type: Oral

Development of Dedicated Front-end Electronics for Straw Tube Tracker in PANDA Experiment

Thursday, September 26, 2013 10:15 AM (25 minutes)

The design and measurements of front-end electronics for straw tubes tracker (STT) at PANDA experiment are presented. The challenges for front-end electronics are discussed and the proposed architecture comprising switched gain preamplifier, pole-zero cancellation circuit (PZC), variable peaking time shaper, ion tail cancellation circuit (TC) and baseline holder (BLH) is described. The front-end provides analogue amplitude output and leading edge discriminator (LED) output for time and time-over-threshold (ToT) measurements. The first prototype ASIC comprise four channels was fabricated in $0.35\ \mu\text{m}$ CMOS technology. The results of measurements on ion tail cancellation, gain, noise, time walk and jitter are presented.

Summary

The STT detector at the PANDA experiment needs a front-end electronics which can meet requirements of high speed, time resolution around 1 ns, amplitude measurement and low noise. For high event rate experiment the specificity of gaseous detectors requires to eliminate the long ion tail from the signal. In addition, to obtain high resolution the stabilisation of baseline level is needed. To fulfill the discussed requirements the front-end architecture comprising a switched gain preamplifier, a PZC, a second order variable peaking time shaper, a TC circuit and a BLH was developed. The front-end solution provides both the amplitude measurement and the timing and ToT information. The preamplifier works with resistive feedback in charge sensitive mode, its gain can be varied in the range between 0.5 and 2 mV/fC. The preamplifier is followed by PZC circuit and the first shaper stage. The peaking time of the shaper can be varied between 20 and 40 ns. The TC circuit following first shaper stage is designed as RC ladder providing two time constants used for the long ion tail cancellation. These time constants can be trimmed in wide range (3-43 and 17-512 ns) and thus can be matched to detectors with different gas mixtures. In addition, it is possible to switch off a part of TC responsible for one time constant or switch off the whole TC circuit and work with classic CR-RC² shaping. To stabilize baseline a BLH was designed. The BLH contains folded cascode OTA with slew rate limitation, followed by RC filter driving a current sink. To obtain high value of RC filter time constant ($\sim 1\ \mu\text{s}$ for default settings) an active resistor was used. To perform time measurement a fast LED with LVDS driver is placed after the last shaper stage. The first prototype was fabricated in two-poly four-metal $0.35\ \mu\text{m}$ CMOS technology. A number of measurements for different modes of operation were done both for test delta-like pulse and with signals from straw tubes. The measurements with delta-like pulse were done for CR-RC² configuration (with TC switched off) for the whole range of preamplifier gains and shaping times and for wide range of input capacitances (between 5 and 100 pF). The measured charge gain is in the range between 3.8 and 23 mV/fC for $C_{in} = 22\ \text{pF}$, and the obtained ENC is on the level ~ 2400 and 980 for lowest and highest charge gain respectively. The discriminator time walk is below 9 ns with jitter around 0.14 ns (for highest gain settings). The measurements with straw tubes show very good performance of TC circuit. Setting correctly the TC time constants an output pulse with quasis Gaussian shape lasting around 150 ns and without undershoot is obtained. To check the BLH performance various measurements at different supply voltage, temperature and input signal rates were done showing very good stability of the baseline.

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Session Classification: ASICs

Contribution ID: 160

Type: **Poster**

Development of the readout system for Triple-GEM detectors for the CMS forward muon upgrade

Tuesday, September 24, 2013 6:18 PM (1 minute)

For the LHC high luminosity phases new triple-GEM detectors should be installed in the CMS muon endcap spectrometer, together with a new readout system. The functional requirements on the system are to provide both triggering and tracking information. In addition the system will be designed to take full advantage of current generic developments introduced for the LHC upgrades: CERN GLIB boards host in micro-TCA crates, the Versatile Link with the GBT chipset, etc. In this contribution the physics goals, the hardware architectures and expected performance of the CMS GEM readout system, including preliminary timing resolution simulations will be presented.

Summary

In this contribution we will report on the progress of the design of the readout system being developed for triple-GEM detectors that should be installed in the CMS muon endcap system for the LHC high luminosity phases. The functional requirements on the system are to provide both triggering and tracking information. In addition the system will be designed to take full advantage of current generic developments introduced for the LHC upgrades. The current design is based on the use of CERN GLIB boards host in micro-TCA crates for the off-detector electronics and the Versatile Link with the GBT chipset to link the FE electronics to the GLIB boards. In this contribution we will describe the physics goals, the hardware architectures and report on the expected performance of the CMS GEM readout system, including preliminary timing resolution simulations.

In 2009, a dedicated CMS R&D program was launched to study the feasibility of using micro-pattern gaseous detectors (MPGD) for the instrumentation of the $|\eta| > 1.6$ region in the CMS muon endcap system. The proposed detector for CMS is a triple-GEM trapezoidal chamber, equipped with 1D readout, with dimensions (990x440-220) mm². Triple-GEM detectors can provide precision tracking and fast trigger information, contributing on one hand to provide missing redundancy in the high-eta region and on the other hand to the improvement of the CMS muon trigger.

The challenges for the readout system are numerous: the time resolution should be as good as 5ns, to unambiguously identify each LHC bunch crossing, the best spatial resolution, $\sim 100 \mu\text{m}$, should be ensured at the first level of the CMS trigger system which has a latency of 3.2 μs and the data acquisition should sustain a very high data throughput, of the order of 100 MB/s of trigger data per detector at high LHC luminosity.

The CMS GEM Collaboration has launched a complete R&D program to develop a new Front-End chip, which should be flexible enough to be used with various MPGDs, as well as a trigger and data acquisition system based on the most recent developments from the telecommunication industry (μ -TCA), in line with the other CMS upgrade projects. In this contribution we will report on the design and the expected performance of the CMS GEM readout system, including preliminary timing resolution simulations.

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Session Classification: Poster

Contribution ID: 162

Type: **Poster**

A Small-Footprint, Dual-Channel Optical Transmitter for the High-Luminosity LHC (HL-LHC) Experiments

Tuesday, September 24, 2013 5:37 PM (1 minute)

We present a small-footprint dual-channel optical transmitter module called MTx for the High-Luminosity LHC experiments. The MTx module consists of two separate commercial transmitter optical sub-assemblies (TOSAs) and a dual-channel laser driver ASIC. We have demonstrated that the module prototypes can operate at 10 Gbps using commercial 10 Gbps laser diode drivers. We are developing an 8 Gbps Vertical-Cavity Surface-Emitting Laser (VCSEL) driver ASIC to replace the commercial laser driver used in the current MTx prototypes and three prototype ASICs have been designed and tested. The design and testing results of the module and the ASIC are reported.

Summary

High-energy physics experiments have extensively used optical links, which provide many advantages including high bandwidth, long distance transmission, high density, low power consumption, and no ground loop. Small footprint is critical in designing front-end modules where the space is limited. In this paper, we present a small-footprint dual-channel optical transmitter module called MTx for the High-Luminosity LHC experiments.

The MTx module consists of two separate commercial transmitter optical sub-assemblies (TOSAs) and a dual-channel laser driver ASIC (or two separate commercial laser drivers in the prototype). We adopt the original idea of the small footprint versatile transceiver (VTRx) module developed by CERN. The electrical interface is a high-speed high-density surface-mount connector. The serializer ASIC is placed on the motherboard in the area underneath the laser drivers. The optical interface is a custom-designed plastic latch holding the two TOSAs and optical fibers. The latch used in the prototype is printed with a 3-D printer and the one used in the final design will be injection molded. Two 8-mm-high pluggable prototypes with LC connectors have been demonstrated. A 6-mm-high non-pluggable prototype without any connector is under development. With commercial laser diode drivers, we have demonstrated that the prototypes can operate at 10 Gbps. The commercial laser drivers will be replaced with a radiation-tolerant laser driver ASIC.

We are developing an 8 Gbps Vertical-Cavity Surface-Emitting Laser (VCSEL) driver ASIC to replace the commercial laser driver used in the current MTx prototypes. Three prototype ASICs have been designed and tested. The first prototype is a single-channel VCSEL driver. The modulation current and the biasing current are externally adjustable. The prototype provides the embedded inductive peaking with adjustable peaking strength. The prototype can operate error-free at 8 Gbps. The total power consumption is 215 mW (including the power consumption of the VCSEL). The prototype has been tested in X-rays (the maximum energy is 160 keV) up to the total ionizing dose required by the HL-LHC upgrade. The prototype has also been tested in a neutron beam with an energy spectrum close to the LHC background. No single event upset is observed with the fluence up to $1.8E11$ n/cm². The second prototype provides digital control interface I2C and is packaged in a QFN package. The third prototype has two channels with each channel operating at 8 Gbps. All prototypes are fabricated in a commercial 0.25-um Silicon-on-Sapphire (SoS) CMOS process. We present the design and testing results of the first two prototypes and the simulation results of the third prototype.

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Session Classification: Poster

Contribution ID: 163

Type: **Poster**

The 120Gbps VCSEL array based optical transmitter (ATx) development for the High-Luminosity LHC (HL-LHC) experiments

Wednesday, September 25, 2013 5:11 PM (1 minute)

The integration of VCSEL array and driving ASICs in a custom optical transmitter module (ATx) for operation in the detector front-end is demonstrated. The ATx provides 12 parallel channels with each channel operating at 10 Gbps. The assembly comprises a ceramic substrate with high-density wiring for electrical interface, OE components, and a micro-lens array with guiding structure for optical interface. Commercial driver is currently used on the demonstrator and will be replaced by a radiation tolerant driver. The complete module with ASIC shielded is to be irradiated under x-ray with total dose over 10Mrad.

Summary

The development of high-speed, low power, radiation-tolerant optical data links is critical for the LHC upgrade as well as other collider detector developments. A general trend is to leverage the rapid advancement in commercial optical transceivers, qualify a suitable form factor, maintain the optical/electrical interfaces and fabrication/assembly platform, and customize the components and materials to ensure radiation tolerance. VCSEL-based technology has been widely adopted by short-range data transmission links and parallel modules utilizing an array of VCSELs have also been commercialized. In this paper, we report the development of integrating a VCSEL array with a driving ASIC in a custom optical transmitter module (ATx).

The VCSEL array and driving ASIC in the custom transmitter module (ATx) is based on ceramic packaging technologies with high-density circuitries, single layer thick film with plated through holes and solder bumps. The ceramic substrate serves as a good heat spreader for stable laser operation. Low thermal coefficients of linear expansion of ceramic and optical connector resin are also beneficial to the reliability of the modules.

The light output of the VCSEL is collimated and deflected by 90 degree using array optics. The VCSEL and micro-lens is visually aligned and tacked down with epoxy. The distance from the VCSEL aperture to the optical plane of the lens is optimized with spacers. The fiber ribbon cable which clips onto the module, the Prizm cable, is also a commercially available standard component.

A commercial array driver has been electrically characterized using multi-channel data transmission with each channel operating at 10 Gbps, both in standard alone and I2C mode. This driver is currently used on the demonstrator and will be replaced by a radiation-tolerant driver. The micro-lens block and the connection elements are made from optically clear Polyetherimide (PEI) compound, and the structural resin is similar to the conventional MT ferrule. The complete module with driver ASICs shielded is to be irradiation under x-ray with total dose above 10 Mrad.

The 12-channel ATx module is designed to operate at 10 Gbps/ch with a 10E-12 bit error rate, indicating a potential of 120-Gbps aggregate throughputs. The ceramic carrier is to be submitted for fabrication in early May and the module will be assembled in July. Transmitter testing is designed to optimize the optical eye-diagram at 10 Gbps. Electrical transmission signal integrity and optical insertion loss will be evaluated, and the assembly challenges will be discussed.

The ATx front-end transmitter is intended to work with commercial parallel receivers such as micropod and lightable engines. System integration issues, especially power budget will be explored.

We describe the devices evaluated, the experimental set-up for multi-channel testing based on a transceiver enabled FPGA evaluation kit, and the analysis of performance compliant test.

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Session Classification: Poster

Contribution ID: 164

Type: Oral

An optical data transmission ASIC for the ATLAS liquid argon calorimeter upgrade

Thursday, September 26, 2013 10:15 AM (25 minutes)

We present several ASICs of optical data transmission for the ATLAS liquid argon calorimeter trigger upgrade. These ASICs include a two-channel serializer (LOCs2), a single-channel and a four-channel VCSEL driver (LOCld1 and LOCld4), each channel operating at 8 Gbps. The serializer ASIC implements a low-latency, low-overhead, quick-resynchronization interface chip (LOCic) between ADCs and serializers. These ASICs are designed and fabricated in a commercial 0.25- μm silicon-on-sapphire (SoS) CMOS technology, which is suitable for high energy physics front-end electronics applications. The designs and test results will be presented.

Summary

The ATLAS liquid argon calorimeter trigger upgrade requires high-speed, low-power and low-latency data transmission. The commercial serializer and laser driver do not work in the front-end radiation environment. Based on a commercial radiation-tolerant 0.25- μm SoS CMOS process, we have designed high-speed serializer and laser driver ASICs for the ATLAS ATLAS liquid argon calorimeter trigger upgrade.

LOCs2 is a two-channel serializer, each channel operating at 8-Gbps. LOCs2 consists of two 16:1 serializer channels. Each channel has a 16-bit parallel data input in LVDS logic and a serial data output in CML logic. The two channels share an LC-tank-based phased-locked loop (LC-PLL), which has been prototyped and tested. The tuning range of the LC-PLL has been slightly modified to match to the speed requirement of the serializer. The PLL loop bandwidth is programmable from 1.3 to 7.0 MHz. Post-layout simulations indicate that the deterministic jitter is about 15 ps (peak-to-peak) at 8 Gbps at nominal process corner and room temperature. The random jitter has been verified to be about 1.4 ps in previous prototype chip. The power consumption of LOCs2 is estimated to be 1.2 W. The first version was submitted in June, 2012. A bug in the divider chain of the PLL was found in the test. The second version was submitted in February, 2013. More test results of LOCs2 will be presented in the paper.

LOCs2 will implement a low-latency, low-overhead, quick-resynchronization interface chip (LOCic) between ADC and serializer. The data frame with 14% overhead provides 12-bit bunch crossing identification (BCID) information, fast resynchronization and strong error detection capability. The latency is less than 10 ns. LOCic is designed and will be submitted in October, 2013. It will be integrated into the serializer in the future. The firmware on the receiver side is implemented in an FPGA to verify the design logic and performance.

LOCld1 is a single-channel VCSEL driver and will be used in a low footprint dual-channel optical transmitter module called MTx. The LOCld1 core analog circuit has been tested with previous prototype chip. When LOCld1 drives a VCSEL, the total jitter is 30-ps at the bit error rate of $1\text{E-}12$ and the optical modulation amplitude is -1.3 dBm at 8-Gbps and room temperature. The modulation current, biasing current and shunt-peaking strength is programmable via I2C. To immune from the single event upsets (SEU), internal registers are protected with Triple Modular Redundancy (TMR). We adopt the HDL code of I2C module developed by CERN and slightly modified to adapt the foundry digital library.

LOCld4 is a four-channel VCSEL driver array to drive a four-channel VCSEL array with single-end outputs. LOCld4 or the future multiple-channel VCSEL driver array will be used in a VCSEL array based optical transmitter module. The test results of LOCld4 will be presented in the conference.

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Session Classification: Optoelectronics and Links

Track Classification: Opto

Contribution ID: 168

Type: Poster

Radiation-Hardened-By-Design Clocking Circuits in 0.13 μm CMOS Technology

Tuesday, September 24, 2013 5:07PM (1 minute)

We present single-event-hardened phase-locked loop for structured-ASIC and digital delay-locked loop for DDR2 memory interface applications. The PLL covers a frequency range from 12.5 MHz to 500 MHz with an RMS jitter of 4.7 pS. The DLL operates at 267 MHz and has a phase resolution of 60 pS. Designed in 0.13 μm CMOS technology, the PLL and the DLL are hardened against SEEs for charge injection of 250 fC. The PLL and the DLL consumes 17mW and 22mW of power under 1.5V power supply, respectively.

Summary

In this paper, we present single-event-hardened phase-locked loop for structured ASIC and digital delay-locked loop for DDR2 memory interface applications. The PLL and the DLL are designed in a 0.13- μm standard CMOS digital technology and are hardened against SEEs for charge injection of 250 fC

All of the blocks in the PLL are designed by using RHBD techniques to reduce single-event effects. Dual interlock cell flip-flop is used in designing the phase frequency detector, frequency divider, lock detector, and all other sequential logic blocks to eliminate single event upset and to minimize effect of single event transient on the PLL performance. The voltage-controlled oscillator is designed with two VCOs being cross-coupled to achieve quick recovery by compensating each other during SET. For the most vulnerable node of the PLL, the output of charge pump, a proposed charge compensation circuit is developed to compensate the SEE-induced charge in order to minimize the SEE impact on the PLL output jitter. In addition, a third-order loop filter is used to further purify the VCO control voltage. The entire PLL only uses normal transistors. It covers a frequency range from 12.5 MHz to 500 MHz with an RMS random jitter of 4.7pS. The PLL consumes 17mW of power under 1.5V power supply and occupies an area of 0.55mm².

The DLL is designed using a dual-loop structure which includes a coarse tuning loop and a fine tuning loop. In the DLL operation, the coarse tuning loop is first launched and is used to adjust a multiplexer-based digital controlled delay line (DCDL) until the phase difference between the output clock and the reference clock is within one multiplexer delay. The phase detection is protected by TMR. The multiplexer-based DCDL allows thermometer coding with error correction to protect the loop digital integrator from SEEs. The ECC logic itself, on the other hand, is protected by TMR. After the coarse tuning process, the fine tuning loop takes over the locking operation. It adjusts a phase interpolator to reduce the phase difference. The phase interpolator achieves a phase resolution of 60 ps. The phase detector and the digital integrator in the fine tuning loop operate in a similar manner as those in the coarse tuning loop and are also protected by ECC and TMR. In addition, a duty cycle corrector (DCC) is designed in the DLL to satisfy the DDR memory interface requirement. The DCC can self-counteract the SEEs by properly setting the delay components inside the duty-cycle adjustor circuit. The DLL operates at 267 MHz with a 1.5 V supply and consumes 22 mW of power. The DLL completes the locking process within 100 ps and achieves a phase resolution of 60 ps.

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Session Classification: Poster

Track Classification: ASICs

Contribution ID: 169

Type: Poster

The upgrade of the LHCb calorimeter

Wednesday, September 25, 2013 6:09 PM (1 minute)

The LHCb collaboration foresees a major upgrade of the detector for the high luminosity run that should take place after 2018. Apart from the increase of the instantaneous luminosity at the interaction point of the experiment, one of the major ingredients of this upgrade is a full readout at 40MHz of the sub-detectors and the acquisition of the data by a large farm of PC. The trigger will be done by this farm and should increase the overall trigger efficiency with respect to the current detector, especially in hadronic B meson decays. A general overview of the modifications foreseen to the calorimeter system and the integration of the electromagnetic and hadronic calorimeters in this new scheme will be described.

Summary

The LHCb detector is located on the ring of the LHC accelerator at CERN. The fields of research of the collaboration are CP violation, charm physics and rare decays of the B meson. More than 3fb^{-1} have been recorded since the LHC start-up, mainly in 2011 and 2012. The data quality permitted to make important measurements. The B_s meson decay in a pair of muons and other new decays of the B_s have been observed, the B_c mass has been measured with the best precision ever, etc. The performances of the detector are very satisfactory although the beam conditions have been far more aggressive than what was foreseen during the design period. The pile-up was roughly 1.7 in 2012, in spite of the expected nominal conditions foreseen to be 0.4 during the installation of the detector. The confidence of the collaboration in the detector justified those conditions, the gain in statistics being larger than the relative degradation of the data quality due to the higher number of collisions per crossing.

Since a few years, the upgrade of the LHCb detector is being prepared in order to improve the measurements in major areas of flavor physics and to reach ultimately the theoretical uncertainties in several fields. The upgrade will take place during the long shut-down of 2018 (LS2) and should permit to increase the instantaneous luminosity up to $2 \times 10^{33} \text{cm}^{-2} \cdot \text{s}^{-1}$. All the sub-detectors are affected by this upgrade. The pile-up leads to some drastic modifications of the tracking and particle identification systems. But, the most important modification concerns the first hardware trigger (L0) which will be removed. A pure software trigger, more efficient and more flexible, will remain. The suppression of the L0 implies that each sub-detector sends its data at 40MHz to the computer farm on which the trigger program is running. Estimations of the impact of the software trigger (not considering the increase of luminosity) show that the event yield should be more than doubled in B meson hadronic decays (the improvement could be larger for high multiplicity final states with up to 6 charged particles), after the suppression of the present hardware trigger.

The first level trigger will disappear, but part of its electronics can be re-used and adapted in order to reduce the bandwidth at the input of the PC farm. The purpose here is not to limit the bandwidth systematically at a fixed rate like the L0 does, but to reduce the bandwidth between 1 and 40 MHz, depending on the needs and altogether to enrich the sample. The reasons for such a Low Level Trigger (LLT) are a possible staggering of the size of the PC farm at LHC start-up or an occasional problem on the farm.

The calorimeter system of LHCb will evolve by reducing its complexity, the present scintillating pad detector and the preshower will be removed, their disappearance being compensated by the

future software trigger and the improved tracking system. The module performances can be affected by radiations. Hence, some of the cells in the inner region (the closest to the beam pipe) may be replaced during LS2. The calorimeter of LHCb, like the other sub-detectors should adapt its electronics (common to the electromagnetic and hadronic calorimeters) to the new running conditions of the upgrade. The consequences of the upgrade for the electronics are: the readout of the data is done at 40MHz ; the gain of the PMT will be reduced by a factor 5 in order to keep them alive during the high luminosity run, this reduction is compensated by an increase of the gain of the electronics (without increase of the noise with respect to the present system) ; the calorimeter implementation of the first level trigger will be adapted to the new low level trigger. This implies the design of a new front-end electronics. A fraction of the existing system will be kept: the crates, the backplanes, some of the power supplies. The front-end and control boards will be removed and the architecture will be revised. The architecture will consist in acquiring 32 PMT per front-end board. The analog electronics should be made either from an ASIC component or a system based on "commercial-off-the-shelf" (COTS) components. The shaping and integration of the signal in the two concurrent techniques are very different but give comparable performances. After the sampling of the output of the analog part of the front-end electronics, FPGA will be used to perform several operations : baseline subtraction, calibration of the signal for the low level trigger, event building, \dots The output bandwidth of each front-end board will reach 20 Gbits/s. 5 Optical links driven by GBT components, designed at CERN, are used: 4 for the data acquisition path and 1 to send the low level trigger information to the counting room. A front-end crate will contain up to 16 boards, the middle slot of each crate being filled by a control board. This card receives from the counting room the clock, the slow control signals and the fast (synchronous) commands of the experiment and propagates them to the backplane and finally to the front-end boards. The control board will receive or emit the signals (slow control, commands, clock) through a bi-directional link based on the GBT system.\

One of the particularity of the calorimeter electronics is its location: on the gentry which is just above the calorimeter itself. Radiation levels in this region are high and extra safety precautions are essential to protect the electronics against the cumulated dose and the single event effects. Commercial components should be tested in beam in order to guarantee their usage in such conditions; the ASIC is designed with specific conception techniques; flash-based FPGA will be used in the digital part of the electronics, etc\ldots \

Prototypes for the analog part (both ASIC and COTS) and the digital part exist. They have been tested with a spare ECAL module in November 2012 at CERN in an electron beam. The performances obtained from the data are close to the expected ones and a few modifications are foreseen in order to obtain a fully satisfactory design. \

Peripheral systems permit to follow continuously the performances or to control the functioning of the calorimeter. These include the electronics providing high-voltage to the photo-multipliers, the pulsing system for the LED or the radioactive source based calibration of the hadronic calorimeter. A fraction of it can be kept as is or simply adapted in order to be able to receive (like the new control board described above) its slow control or clock signals and commands from the LHCb time and fast control system, through the GBT driven optical links.\

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Session Classification: Poster

Contribution ID: 170

Type: **Oral**

The Alice CTP upgrade

Wednesday, September 25, 2013 10:15 AM (25 minutes)

After three years of successful operation of Alice Central Trigger Processor (CTP) system for proton-proton, Pb-Pb and p-Pb collisions, the Alice CTP is going to be upgraded with a new L0 board in order to improve the performance of the Alice trigger system. The new L0 board will include several new features: an additional trigger level “LM”, which will precede the L0 trigger and will improve efficiency of data taking for the Transition Radiation Detector (TRD); a new 10G Ethernet link for CTP readout and control; an extension of the number of clusters and an extension of functionality for classes. Information for the classes with different BC masks will be registered in counters at each trigger level. In addition to these changes, which will come into effect in 2014 at the end of “Long Shutdown 1”(LS1), the first ideas for a CTP upgrade after “Long Shutdown 2” (LS2) in 2018 will also be presented.

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Session Classification: Trigger

Contribution ID: 174

Type: **Poster**

The CMS Global Muon Trigger upgrade

Wednesday, September 25, 2013 6:22 PM (1 minute)

To continue triggering with the current performance in the LHC Run 2 the Global Muon Trigger (GMT) of the CMS experiment will be reimplemented in a Virtex-7 card utilizing the uTCA architecture. The thus available high-capacity input as well as increased logic could be used to migrate the final sorting stage of each subsystem to the GMT. Additionally the GMT will calculate a muon's isolation using energy information received from the calorimeter trigger which will be propagated to the Global Trigger.

A summary of the current status of the future GMT's development will be given.

Summary

The Level-1 Trigger of the CMS experiment is responsible for reducing the rate of events to be read out from 40 MHz (the bunch crossing frequency) to 100 kHz, which will be then further reduced by the High-Level Trigger. A key component of the Level-1 Trigger is the Global Muon Trigger (GMT). It receives data from the regional muon triggers, which are processed and merged to produce muon candidates. These candidates are checked for so-called ghosts (i.e. two tracks from different subsystems corresponding to the same particle), merged appropriately, and then sorted in two stages before a set of best muons is finally sent to the Global Trigger (GT).

The upgrade of the LHC for Run 2 will require the L1 Trigger to cope with higher multiplicities due to the increased luminosity of the accelerator. This will require the GMT to increase the number of muons sent to the GT from currently four to eight as well as increase the resolution of the muon information. Furthermore the complete system will be upgraded to use high-bandwidth optical links as well as powerful FPGAs. Additionally, a new track finder dedicated to the overlap region shared between endcaps and barrel will be introduced, augmenting the barrel and endcap track finders and providing additional inputs to the GMT.

To comply with these requirements the upgraded GMT will be implemented in a Virtex-7-based card within the uTCA architecture. Currently the MP7 card developed by Imperial College is being targeted which will offer 72 input and 72 output links at 10 Gb/s. The thus available high-capacity inputs as well as increased logic will allow to move the final sorting stage of each subsystem to the GMT. This will mean 36 muons to be received from each of the three track finders which will require half the available input bandwidth. Initially the sorting would still be done separately for each subsystem, however in the future it may be possible to implement more ambitious algorithms if these improve the GMT's performance and resources permit it. An immediate benefit of the integration of the final sorters into the GMT is the possibility of doing ghost-busting between the track finders' muons at an earlier stage, thus reducing the probability of replacing a true muon with a ghost that will only later be canceled. Additionally the GMT will be able to calculate a muon's isolation using energy information obtained via optical links from the calorimeter trigger. The isolation information will then be propagated to the GT together with the muons' other information. As the future GMT should be able to flexibly adapt to changing physics requirements, a further requirement for its development is the provision of significant spare logic capacity. If the need arises the GMT can in this way be reconfigured to provide extended functionality without large changes to the hardware.

We report on design studies and the current status of the firmware implementation.

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Session Classification: Poster

Contribution ID: 177

Type: **Oral**

A Real-time Histogramming Unit for Luminosity and Beam Background Measurements for each Bunch Crossing at the CMS Experiment

Thursday, September 26, 2013 4:05 PM (25 minutes)

The Real-time Histogramming Unit (RHU) is a VME board for sampling and processing discriminated signals from detectors in real time and free of dead-time. The RHU is used at the CMS experiment to measure the arrival time of signals from the BCM1F detectors relative to the orbit trigger of the LHC at CERN. The RHU incorporates a FPGA, 21MBit memory and an embedded Linux system for readout. For each input channel a histogram is produced by the FPGA algorithm in real time that contains the hits per bunch over several orbits. A postmortem buffer can be used for data analysis after a beam dump.

Summary

The Real-time Histogramming Unit (RHU) is a VME board for sampling and processing discriminated signals from detectors in real time and sending data via network. The RHU is used at the CMS experiment to measure the time of signals from the BCM1F detectors relative to the orbit trigger of the LHC. The detectors are installed close to the interaction point inside the CMS detector to measure both collision products and beam halo. The RHU incorporates a FPGA with 5MBit internal memory, 16MBit external memory and a single board computer (SBC). The FPGA of the RHU reads out the detector channels and samples the hits with a frequency of 160MHz, synchronous to the LHC bunch clock. For each channel a histogram is produced in real time that contains the hits as a function of time collected over several orbits mapped on the time of an orbit. The histograms have a binning of 6.25ns and contain 14256 bins. The external memory is used to store the last 50 orbits of sampling data in a ring buffer. When a beam dump occurs, the RHU stops sampling and the postmortem data can be read out for analysis. Every 2048 orbits, the histogram buffers are read out via the Linux based SBC and are transferred via network to the Luminosity DAQ. To avoid dead time, the histogram buffers are implemented as a dual buffer system and sampling continues while software reads out the data. The SBC is connected via a static memory interface to the FPGA for read out and has a bandwidth of 20MByte/sec. The SBC incorporates a 32Bit ARM926 Core at 400MHz and 128MB of RAM. A Linux Kernel driver has been implemented to achieve full performance at the interrupt-based read out. In the user space, a TCP server waits for connections and sends the data to connected clients. A software framework has been developed to allow access to the data of the RHU via network and can be used with ROOT programs for data analysis. The framework uses shared memory to allow multiple clients on the same machine to reuse the network connection to the RHU device and to save bandwidth.

Results on the performance of prototypes used in the last running period are presented.

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Session Classification: Programmable logic, design tools and methods

Contribution ID: 178

Type: Oral

The Front-End Hybrid for the ATLAS HL-LHC Silicon Strip Tracker

Friday, September 27, 2013 11:05 AM (25 minutes)

For the HL-LHC, ATLAS will install a new all-silicon tracking system. The strip part will comprise five barrel layers and seven end caps on each side. The detectors will be connected to highly-integrated low-mass front-end electronic hybrids with custom-made ASICs in 130nm technology. The hybrids are flexible PCB four-layer copper polyimide constructions. They are designed and populated at the Universities involved, while the flex PCB is produced in industry. This presentation will describe the evolution of hybrid designs for the barrel and endcap, discuss their electrical performance, and present results from reading out prototype modules made with the hybrids.

Summary

The Large-Hadron-Collider (LHC) will undergo a major upgrade to the High Luminosity LHC (HL-LHC), which is designed to deliver of order five times the LHC nominal instantaneous luminosity along with luminosity leveling. The final goal is to extend the data set to 3000 fb⁻¹ by around 2030. The challenge of coping with HL-LHC instantaneous and integrated luminosity, along with the associated radiation levels, requires major changes to the ATLAS detector. The designs are developing rapidly for an all-new inner-tracker, significant upgrades in the calorimeter and muon systems, as well as improved triggers and data acquisition.

This submission is connected to the HL-LHC upgrade of the ATLAS Inner Tracker (ITK), which consists of replacing the entire current Inner Detector (silicon pixels, silicon strips and transition radiation tracker) with a completely new silicon-only system. This new ITK will be made from several pixel and strip layers, and both detectors and read-out electronics have to be designed to withstand the extreme radiation environment in close proximity to the HL-LHC interaction point. This broadly speaking means an order of magnitude higher radiation hardness than the existing ID. At the same time, the radiation length should be kept to the level of the present system or below in order to conserve the physics performance of ATLAS. In the current planning, the pixel system involves four barrel layers and six disks on each side for a total pixel area of 7m² and 400 million channels. The strip system will contain five barrel layers and seven end-cap disks, covering 200m² of silicon and 45 million channels.

This presentation concentrates on the front-end electronic hybrids for the silicon strip tracking system. In order to minimize the mass, the hybrids, realized as flexible PCB with a four-layer copper polyimide buildup, are characterized by a very high integration density. The development of the hybrid is an evolutionary process closely linked to the development of the read-out CMOS ASIC (the ATLAS Binary Chip or ABC), and the strip detectors to be read out. The present hybrids employ the 250nm version of the ASIC, derived from the ABC (though in DMIL technology) running in today's ATLAS strip tracker. A 130nm version has been designed and will be produced during this year, with the matching hybrids also currently under design. In our presentation, will be describe the detailed design of the various hybrids for barrel and endcap detectors. The endcap region has added complications due to its wedge-shaped geometry, requiring around ten different hybrid designs with a different layout and varying numbers of ASICs. We will show our experience with producing the PCBs in industry and the process of populating them with active components in-house. We will also show the electrical performance with a number of powering, grounding,

shielding and read-out options. In addition, we will discuss lessons learned along the way, and present results from testing prototype silicon detector modules made by connecting several designs of ATLAS HL-LHC prototype detectors with our hybrids.

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Session Classification: TOPICAL (Packaging & High Density Hybrids)

Contribution ID: 179

Type: **Poster**

ATLAS Diamond Beam Monitor

Wednesday, September 25, 2013 6:02 PM (1 minute)

The Diamond Beam Monitor (DBM) is a pCVD diamond pixel tracker for detecting high-energy charged particles. It is planned to be installed in the ATLAS experiment at CERN for the luminosity measurements. In this talk, the overview of the DBM system and the operation of the diamond pixel sensors are described.

Summary

Accelerator luminosity is a measure of the number of particles that pass through a given area each second multiplied by the opacity of the detector. It is one of the most important parameters for the physics analysis of the particle collisions. It is measured by special detector systems inside the particle detectors. In ATLAS experiment at the Large Hadron Collider (CERN), this system is called the Beam Conditions Monitor (BCM), a pCVD pad diamond detector.

The Large Hadron Collider at CERN has been running with the energy of 8 TeV and it is planned to increase to 14 TeV in 2015, after the next long shutdown. Current instantaneous luminosity is at a few 10^{33} cm⁻²s⁻¹ and is planned to increase by a factor of 10 in the next five years. The average number of particle collisions per bunch crossing (every 25 ns) will increase from the current 20 to over 200. This might cause saturation of the current luminosity detectors. Hence, a new detector called the Diamond Beam Monitor (DBM) has been designed to account for the augmented number of collisions taking place at the ATLAS experiment. Diamond material was chosen because its properties after an irradiation don't change significantly, as opposed to silicon.

The DBM is a charged-particle detector. Its purpose is to monitor the bunch-by-bunch luminosity and bunch-by-bunch position of the beam spot. 8 telescopes, each housing 3 consecutive pixel modules, are placed approximately 1 m from the collision point in the high-eta region of approximately 3.5. Every time a particle traverses a sensor plane, a hit is recorded in the corresponding pixel. The telescope-like positioning of the pixel sensors allows to track the particle paths while traversing the sensor planes. The DBM will calculate the luminosity by counting the number of particle tracks. It will be able to distinguish whether a particle came from the collision point or from some other place inside the detector (beam halo), and choose only the relevant hits/tracks for the luminosity calculation.

The FE-I4 ASIC front-end chip is used for the front-end electronics. Its integrated circuit contains readout circuitry for 26,880 hybrid pixels arranged in 80 columns on 250 um pitch by 336 rows on 50 um pitch. It operates at 40 MHz with a 25 ns acquisition window and is hence able to correlate hits/tracks with their corresponding bunch count.

CVD diamond has been chosen as the sensor material due to its high radiation hardness, negligible noise and fast signal response. Only polycrystalline diamonds are commercially available in the required sizes (21 mm x 18 mm, 500 um thickness).

After extensive processing, the diamonds are bump-bonded to the front-end chip. The modules are then wire-bonded to the PCB and installed in the telescope mechanics.

In this talk, the overall system and the preliminary detector test results will be presented. Then, the QA procedure and the installation status will be given.

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Session Classification: Poster

Contribution ID: 180

Type: **Poster**

Digital Column Readout Architectures for Hybrid Pixel Detector Readout Chips

Wednesday, September 25, 2013 4:36 PM (1 minute)

In this paper, two digital column architectures suitable for sparse readout of data from a pixel matrix in trigger-less applications are presented. Each architecture reads out a pixel matrix of 256x256 pixels with a pixel pitch of 55um.

The first architecture has been implemented in the Timepix3 chip, and this is presented together with initial measurements. Simulation results and measured data are compared.

The second architecture has been designed for Velopix, a readout chip planned for the LHCb upgrade. Unlike Timepix3, this has to be tolerant to radiation-induced single-event effects.

Results from post-layout simulations are shown with the detailed circuit architectures.

Summary

In this paper, column readout architectures focused on pixel detector readout chips with 65,536 pixels of 55 um x 55 um, suitable for continuous, sparse readout without trigger signal are presented. A sparse readout architecture reads only the pixels which contain event information, and continuous readout keeps pixels sensitive at all times with only a small readout related dead time. Operation without trigger requires reading out all hit information with no event-filtering by an external signal.

Timepix3 [1] was fabricated in 130 nm CMOS in spring 2013. It has been designed as a general purpose pixel detector readout chip targeted for many applications. The double column readout architecture in Timepix3 has been implemented using a low-power (high Vt), high-density (350 kgates/mm²), custom-made CMOS standard cell library. The architecture has been designed by localising critical timing paths and making global communication asynchronous. This flexibility allows clocking the periphery of the chip with a different frequency (up to 80 MHz) than the pixel matrix (up to 40 MHz). One readout column consists of two pixel columns abutted together. Locally in a column, the readout logic is shared between a region of 2x4 pixels (a super-pixel). One double column delivers 2 Mhits/s from a pixel matrix to the periphery.

Each column uses a two-stage token ring arbitration with 8 token stations per super pixel and 64 stations per double column. The token is fully synchronous within a column. Data is transported from pixels to End-of-Column using a 2-phase handshake protocol over 4 handshake cycles. In Timepix3, event information is encapsulated into a 48-bit pixel packet containing a 14-bit coarse time (40 MHz), a 10-bit time-over-threshold measurement and a 4-bit fine time (640 MHz) information in addition to a 16-bit pixel address. For characterising the chip, a custom test system has been constructed based on programmable logic. Initial measurements of the efficiency of the Timepix3 architecture are presented.

Velopix is targeted specifically for the LHCb upgrade [2] and a fully synchronous design has been chosen. Local pixel logic has been implemented using high-density cells and global communication is driven by stronger cells from a commercial library. The column architecture has been designed for maximum peak rate of 8.8 Mhits/s per super pixel column. The architecture has been protected against single-event-upsets by triplicating on-pixel configuration registers, state machine registers and FIFO pointers.

Locally in a column, the readout logic is shared by a super-pixel of 4x4 pixels. A data encoding scheme has been implemented in this region to share coarse time and address information with a cluster of hits formed by the same track. Particle hits create clusters with an average size of 2.2

pixels and a reduction of over 25% of data volume can be achieved using this encoding scheme compared to reading out individual pixels. The format has been optimised to simplify decoding at the next level of electronics where the high data rates result in complex algorithms for event-reconstruction.

For future work, the characterization of Timepix3 readout architecture will continue. Implementation of Velopix will proceed aiming for a maximum data rate of about 17 Gbit/s/chip.

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Session Classification: Poster

Contribution ID: 183

Type: **Poster**

A new approach to interfacing on-detector electronics

Tuesday, September 24, 2013 6:19PM (1 minute)

The current off-chamber readout chain in the ATLAS experiment consists of sub-detector specific ReadOut Drivers (RODs), typically 9U VME cards, which receive data from a number of front-end links. The RODs build event fragments and forward these via point-to-point links, the Read-Out Links (ROLs) to the ReadOut System (ROS). The functionality of the RODs, not only consisting of fragment building but also of the associated error handling and for some subdetectors processing of the event data and also of support for calibration, is implemented in FPGAs and DSPs. For the Readout of new muon detectors to be installed during LS2 and for the Readout of all detectors after LS3 a new approach is foreseen, in which as much as possible functionality is moved to software. A similar system has been proposed for the LHCb experiment electronics upgrade in LS2. In this paper we present the new approach. We foresee that first results of tests can also be presented.

Summary

A new approach to interfacing to on-detector electronics

The upgrade of the LHC planned during LS3 (~2022) will necessitate major changes in the ATLAS trigger/DAQ system. The current first-level trigger will be augmented with a track trigger and be subdivided into two levels: an L0 trigger on the basis of calorimeter and muon detector with an accept rate of at maximum 500 kHz and an L1 trigger also making use of tracking detector data with an accept rate currently foreseen to be at maximum 200 kHz. The ATLAS detector will need to be read out at the new L1 accept rate, which currently is at maximum 100 kHz. On-detector electronics of the calorimeters and muon detectors, apart from the “small wheels”, will be completely or to a large extent be replaced, while a complete new inner detector with associated on-detector electronics will be installed. All detector systems are foreseen to be read out via GBT links, either directly connected to the on-chamber electronics, or via off-detector pre-processors for the calorimeters. New muon detector “small wheels” will be installed already during LS2. The readout of the detectors (sTGCs and MicroMegas detectors) will be done with GBT links and the organisation of the off-chamber readout will be similar to the organisation foreseen for post-LS3 running. Also the

The current off-chamber readout chain consists of sub-detector specific ReadOut Drivers (RODs), typically 9U VME cards, which receive data from a number of front-end links. The RODs build event fragments and forward these via point-to-point links, the Read-Out Links (ROLs) to the ReadOut System (ROS). Here the data is buffered until explicitly deleted, either after successful event building or after a reject by the second-level trigger. The functionality of the RODs, not only consisting of fragment building but also of the associated error handling and for some subdetectors processing of the event data and also of support for calibration, is implemented in FPGAs and DSPs.

The evolution of general purpose processors allows to implement ROD functionality now implemented in FPGAs in software, and further evolution of the technology can be expected at the time scale of LS2 and LS3. Also further evolution of network technology is to be expected, 40 Gb/s and 100 Gb/s Ethernet links for example at acceptable cost are on the horizon, allowing to concentrate the data from tens of GBT links on a single network link.

In view of this and in view of the desire to keep any special-purpose off detector electronics as simple and subdetector independent as possible a new readout architecture has been defined in

which the ROD functionality is implemented as much as possible in software. The equivalent of the current ROD system is foreseen to be implemented as a combination of dedicated electronics interfacing to the GBT links and of server nodes receiving data from the dedicated electronics via a local area network. The dedicated electronics has been given the name FELIX (Front End LInk eXchange). The task of FELIX is not only to forward event data, but also to forward L1 and possibly L0 trigger information, as received from the TTC or its successor, to the on-chamber electronics, and to provide support for the communication of the Detector Control System (DCS) via GBT links with on-chamber electronics and on-chamber sensors. The latter functionality demands continuous running of FELIX and support for this type of communication. Handling of data received via the GBT links should essentially consist of forwarding the data to the server nodes via the general purpose network based on routing tables loaded in the FELIX system. A similar system has been proposed for the LHCb experiment electronics upgrade in LS2. Protocol definitions and implementations will be useful for and be applicable to both systems.

In this paper we present the new approach as outlined in this summary. We foresee that first results of tests can also be presented.

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Session Classification: Poster

Contribution ID: 184

Type: Oral

A 20 mW, 4.8 Gbit/sec, SEU robust serializer in 65nm for read-out of data from LHC experiments

Tuesday, September 24, 2013 11:35 AM (25 minutes)

The availability of a sub 1-W SerDes for future LHC read-out systems is of paramount importance. This work relates to the design of two alternative architectures for the critical serializer block within a SerDes with the objective of achieving a power consumption of less than 30 mW at the operating speed of 4.8 Gbit/sec. Two alternative architectures are implemented using a commercial 65nm LP-CMOS technology. The architectures used are a “simple-TMR” and a “code-protected” one, and are meant to investigate different strategies against SEU effects. While using the same technology and flip-flops, the simple-TMR architecture results in a consumption of 30 mW, the code-protected one of 19 mW, which are better than 1/4 of the power used in state-of-the-art rad-hard serializers. The robustness to SEU effects is also presented.

Summary

The higher beam luminosity at the HL-LHC will generate higher detector data rates. The 130nm CMOS 4.8 Gbit/s gigabit transceiver (GBT) currently developed at CERN provides a radiation robust solution for the communications between LHC detectors and the control rooms.

In order to provide lower power data links, a new SerDes called low power GBT (LPGBT) will be realized with a 65 nm technology using a 1.2 V supply. The aim of this new version is to implement the same transmission protocol used in the GBT with a power reduction of a factor of four.

The two circuits presented here are designed as possible solutions for the critical serializer function in the LPGBT. Both of them use an architecture working at full data-rate and are based on a 120 bit shift register to serialize data and a “load generator” logic to load the new data in parallel to transmission. These options aim at simplifying the circuitry used in the previous version of the serializer and to reduce the power consumption.

Operation at 4.8 Gbit/s requires the use of dynamic true single phase clock flip flops (TSPC). To avoid using a regular binary counter in the load circuit, which is difficult to design at this speed, a linear feedback shift register is instead applied.

To cope with the total ionizing dose expected for this application (100 MRad/10 years), previous studies have shown that the smallest and fastest transistors available in the technology can not be used and that the minimum transistor width required is 300nm.

The first serializer (“simple-TMR”) developed uses a triple module redundancy scheme to assure single event upsets (SEU) robustness through masking. Hence, three different shift registers work in parallel with voted outputs and each register has a dedicated load generator logic.

The second serializer (“code-protected”) takes advantage of the Reed-Solomon code used in the GBT forward error correction (FEC) scheme. This code is designed to correct up to four corrupted 4-bit symbols per received word. The logic providing the load signals to the serializer takes advantage of this data structure to minimize the number of flip-flops that have to work at high speed while maintaining the robustness of the code. It introduces a novel way to use coding by protecting not only data from transmission errors but also the control logic.

The two serializers are included in a 3 mm x 1 mm test chip which was characterized for pre-irradiation functionality and electrical characteristics. The “simple-TMR” serializer occupies an area of 7900 μm^2 and the “code-protected” serializer occupies 3900 μm^2 . Both of them were func-

tionally tested at 4.8 Gbit/s showing a correct behaviour and power consumption respectively of 30 mW and 19 mW. The maximum speed achieved during tests was 5.6 Gbit/s for both serializers. A dedicate custom PCB was developed to test and characterized the chip, the test bench is completed with the use of a JBERT or GLIB card. In addition, the chip was irradiated at the Louvain-la-Neuve Heavy Ion Irradiation Facility (HIF) and the SEU robustness characteristics are also presented here.

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Session Classification: ASICs

Contribution ID: 185

Type: Oral

Monolithic Active Pixel Sensor Development for the Upgrade of the ALICE Inner Tracking System

Tuesday, September 24, 2013 4:05 PM (25 minutes)

ALICE plans an upgrade of its Inner Tracking System for 2018. The development of a monolithic active pixel sensor for this upgrade is described. The TowerJazz 180 nm CMOS imaging Sensor process has been chosen as it is possible to use full CMOS in the pixel due to the offering of a deep pwell and also to use different starting materials.

Several prototypes have already been designed, submitted for fabrication and some of them tested with X-ray sources and particles in a beam. Radiation tolerance up to the ALICE requirements has also been verified.

Summary

For the upgrade of the Inner Tracking System [1] of ALICE at CERN a monolithic active pixel sensor is under development. R&D will be pursued during 2013-2014, with a full conceptual demonstration towards the end of 2013 and a production-ready prototype towards the end of 2014. The TowerJazz 180 nm CMOS imaging Sensor process [2] has been chosen as it is possible to use full CMOS in the pixel due to the offering of a deep pwell and also different starting materials.

A pixel size of about $20 \times 20 \mu\text{m}^2$ is targeted. To limit material budget power consumption should not exceed 300 mW/cm^2 , but a reduction below 100 mW/cm^2 would really be beneficial. Power is consumed in the sensor chip in the analog and digital circuitry, and also to transmit the data off-chip.

Analog power consumption is determined by the collected charge over capacitance (Q/C) ratio, requiring pixel sensor optimization. An early prototype implemented on an $18 \mu\text{m}$ thick $>1 \text{ k}\Omega\text{cm}$ epitaxial layer showed that changing the reset voltage of the detecting diode over a $\sim 1 \text{ V}$ range drastically affects this Q/C ratio. A new prototype allowing reverse substrate bias, similar to earlier ones in another technology [3], was submitted and measured: reverse substrate bias reduces input capacitance and average cluster size, and increases efficiency for a certain charge threshold. Analysis showed that further sensor optimization could be done, both through design but also using different starting materials. An improved test chip has been submitted in an engineering run early April with a split on starting material. A prototype with a $\sim 40 \text{ nW}$ in-pixel binary front-end circuit was also included.

Digital power consumption depends on the on-chip architecture and also on cluster size. Apart from the traditional rolling shutter, architectures based on a low-power in-pixel binary front-end like the one mentioned before are investigated to minimize the digital power consumption. In a first architecture, a priority encoder circuit provides the address of the first hit pixel in a sector, and subsequently resets it, so that during the next clock cycle the address of the next hit pixel is made available. This continues until all hits in the sector have been read out. Power is minimized as power is consumed only if hits are present. Another architecture [4] tries to reduce power by reducing the number of signals to be treated. One example yields good reconstruction results for the outer layers and reduces the data from N^2 pixels to $4N$ signals. Prototype circuits for both architectures were also included in the April engineering run.

If the aforementioned low-power front end in combination with one of the above architectures is successful, data transmission may very well be the dominant power contributor: about 2 Gbit/s is required for a $1.5 \times 3 \text{ cm}^2$ pixel sensor.

Measurements with X-ray sources and particles in a beam will be presented. Radiation tolerance up to the modest ALICE requirements (Total Ionizing Dose < 700 kRad, Non-Ionizing Energy Loss < 1013 neq/cm²) has also been verified.

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Session Classification: ASICs

Contribution ID: 187

Type: **Poster**

Development of Precision Time-Of-Flight Electronics for LHCb TORCH

Tuesday, September 24, 2013 6:20 PM (1 minute)

The TORCH detector is proposed for the low-momentum particle identification upgrade of the LHCb experiment. It combines Time-Of-Flight and Cherenkov techniques to achieve positive $\pi/K/p$ separation up to 10GeV/c. This requires a timing resolution of 70ps for single photons. This paper will report on the electronics developed for such measurements, using commercial Micro Channel Plate devices and custom ASICs (NINO and HPTDC). The intrinsic timing resolution of the electronics measured with electrical test pulses is 40ps. With the photon detector and Cherenkov light, a resolution of 130ps has been recorded in a test beam.

Summary

The TORCH detector is proposed for the low-momentum particle identification upgrade of the LHCb experiment. In this detector, Time-Of-Flight and Cherenkov techniques are combined to achieve positive $\pi/K/p$ separation up to 10GeV/c. This requires a timing resolution of 70ps for single photons.

Currently, we use an 8x8-channel Planacon Micro Channel Plate (MCP) photon detector. The outputs of the MCP are measured by custom electronics that consists of four Front End boards and a Giga-bit Ethernet-based readout/ slow control system. Each Front End board is equipped with two 8-channel fast amplifiers/discriminators ASICs (NINO), two time to digital convertor ASICs (HPTDC) and a Spartan 3AN FPGA. The NINO chips amplify the output signals from the MCP and discriminate at a threshold defined through a detector control system. In order to suit the input requirement of the HPTDCs, the outputs are converted to LVDS signals through external discrete components. The configurations of the HPTDCs are uploaded by a stand-alone JTAG programmer. The HPTDCs are intended to run in Very High Resolution Mode to offer a 25ps resolution, therefore, only 8 of 32 channels are used on each chip. The HPTDCs are read out and throttled by the on-board FPGA. The outputs are buffered on the FPGA and then transferred to a computer via the readout system. The HPTDCs require low jitter clocks to provide an accurate timing measurement. Users can select between an on-board 40MHz clock and an external clock; the selected clock is then fanned out by a low jitter device (SY89832), into the HPTDCs and the FPGA. The external trigger signal is also fanned out in the same way. The Giga-bit Ethernet-based readout/ detector control system has been developed. Three versions of firmware have been written for production tests, laboratory tests and beam tests. Labview-based DAQ software has also been developed to provide basic data transfer, online monitoring and control functions.

The intrinsic timing resolution of the electronics has been measured by injecting two separate pulses into a test channel with an Agilent 81110A generator. The difference of the two leading edges is measured and a Gaussian fit shows a timing resolution of 40ps. A beam test has been carried out at CERN using an MCP as described earlier in a low-intensity muon beam. Two 8mmx8mm borosilicate bars were coupled to the MCP to produce Cherenkov photons from the incident particles. Time differences were measured against a reference signal provided by a borosilicate bar coupled to a single-channel MCP read out with commercial electronics. The measured timing resolution is of order 130ps.

Possible improvements have been identified. This includes designing a 64-channel system based

on 32-channel NINO chips to offer a higher channel density for future MCPs. Implementing Integral Nonlinearity (INL) corrections on the HPTDC chips to provide better timing resolution is also underway.

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Session Classification: Poster

Contribution ID: 188

Type: Poster

Characterization results and first applications of KLauS - an ASIC for SiPM charge and fast discrimination readout

Wednesday, September 25, 2013 4:38 PM (1 minute)

KLauS is an ASIC produced in the AMS 350nm SiGe process to read out the charge signals from silicon photomultipliers.

Developed as an analog frontend for future calorimeters with high granularity as pursued by the AHCAL concept in the CALICE collaboration, the ASIC is designed to measure the charge signal of the sensors in a large dynamic range and with a high precision.

In order to compensate bias and temperature fluctuations of each sensor individually, an 8-bit DAC to tune the voltage at the input terminal within a range of 2V is implemented.

Using an integrated fast comparator with low jitter, the time information can be measured with sub-nanosecond resolution.

The low power consumption of the ASIC can be further decreased using power gating techniques. Future versions of KLauS are under development and will incorporate an ADC with a resolution of up to 12 bit and blocks for digital data transmission.

Most recent characterization results for the KLauS chip are presented as well as results from a KLauS-based test setup developed for mass characterisation of scintillator tiles used in the AHCAL test beam program.

Summary

KLauS is an analog ASIC for current mode charge read out of silicon photomultipliers.

The 12 channel test chip aims at providing a readout system of scintillating tiles with silicon photomultipliers,

integrated within a calorimetry system for a future linear collider experiment.

The AHCAL concept developed within the CALICE collaboration plans to build such a system, which is using scintillating tiles, silicon photomultipliers and integrated electronics in a sandwich calorimeter.

One of the main constraints in such a system is the very low allowable power consumption of the electronics.

The special feedback scheme of the KLauS input stage offers a low power consumption, which can be decreased using power gating techniques.

Using this technique the total power consumption is decreased to 25uW per channel for the nominal ILC bunch crossing scheme.

The topology of the input stage is a current conveyor specialized for the ASICs powergating capabilities, allowing a very low input impedance for the channels,

thus most of the signal charge can be collected by the later integration stage.

This yields a high signal to noise ratio even for low gain silicon photomultipliers.

The input stage topology allows the voltage at the input terminal to be adjusted to compensate for variations

in the operating voltage of the silicon photomultipliers due to sensor production or temperature fluctuations.

Each of the 12 channels of the ASIC includes an 8-bit DAC to tune the input terminal voltage within 2V at an INL smaller than 2%,

with a resolution of approximately 10mV per LSB. The terminal voltage in power pulsing mode varies less than 20mV

when comparing the 'on' and 'off' state of the chip, keeping the sensors in a stable condition at all times.

The measured current is integrated in the later integration stage and then converted to a pulse height signal using an active shaper with adjustable time constant and no undershoot. This makes precise charge measurements possible, even for dark count rates in the order of several MHz as commonly seen in 3x3mm² Silicon Photomultipliers.

A discrete gain switching unit allows a dynamic range of more than 200pC for large area SiPMs. The equivalent noise charge generated by the electronics was determined to be 25000 e⁻ at an input capacitance of 40pF,

allowing a precise estimation of the sensor gain using single photon spectra. For a Hamamatsu S11028-025 MPPC, the signal to noise ratio was measured to be larger than 8 for a single pixel signal, dominated by the MPPC intrinsic signal fluctuations as SiPM excess noise and dark count pileup contributions. The ASIC contributes about 12.5% to the total noise.

In order to develop a full readout system in a mixed mode ASIC, an ADC with a pipelined capacitor switching structure is being developed.

For normal physics mode operation, a resolution of 8 bits seems sufficient due to the large Landau fluctuations in the expected signals.

For measurements of the time information and calibration of the SiPM gain a higher resolution will be used (10 bits and 12 bits, respectively).

Together with a peak sensing unit, the ADC will be capable of measuring events with a rate of 1-3 MHz. This leads to a minimum of analog memory cells

prior to the conversion stages. The submission of a mini-ASIC to test the ADC is planned for the end of 2013.

The CALICE collaboration is running an extensive test beam program, for which scintillator tiles have to be characterized and validated for functionality. The properties of KLauS, especially the high signal to noise ratio and the pileup compensating shaper, make the ASIC very suited to test the characteristics of the scintillating tiles. A prototype setup using the KLauS ASIC has been set up, allowing semi-automated characterisation of 12 tiles in parallel. A fully automated system is being commissioned.

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Session Classification: Poster

Contribution ID: **189**Type: **Poster**

The AMC13XG: A New Generation Clock/Timing/DAQ Module for CMS MicroTCA

Wednesday, September 25, 2013 6:05 PM (1 minute)

The AMC13 provides clock, timing and DAQ service for many subdetectors and central systems in the upgraded CMS detector. This year we have developed an upgraded module, the AMC13XG, which supports 10 gigabit optical fiber and backplane interfaces. Many of these modules are now being installed in the CMS experiment during the current LHC shutdown. We describe the implementation using Xilinx Kintex-7 FPGAs, commissioning, production testing and integration in the CMS HCAL and other subsystems.

Summary

The AMC13XG is constructed of a 3-board assembly. The tongue 1 board houses the front-panel optics in a quad SFP+ cage, provides a 1 GbE interface for configuration and control, and acquires DAQ data from AMC cards over the MicroTCA backplane. Most functions are implemented in a Xilinx Kintex XC7K325T FPGA in a 900 pin BGA package. This device was chosen because it supports 16 high-speed (up to 12.5 Gb/s) serial links and about 325,000 logic cells and is relatively inexpensive. By comparison, the XC6VLX130T used in the first generation AMC13 had about 130,000 logic cells and up to 6.6 Gb/s serial links. The use of 10 Gb/s links required a complete PCB redesign, including the selection of a particular high speed PCB base material rather than the typical FR-4. Other changes to the tongue 1 board include the upgrade of the on-board memory to DD3 with 512 MB capacity and 6.4 GB/s throughput. In principle the AMC13XG can support a DAQ throughput approaching 3 GB/s with all 3 front-panel links operating at 10 Gb/s.

The tongue 2 board houses a Xilinx Spartan XC6SLX25T FPGA, an Atmel AVR32 microcontroller and most of the low-jitter clock fanout circuitry. The Spartan FPGA provides housekeeping functions including a flexible interface for download and programming of firmware into an SPI flash memory and management of IP and MAC address setting. In addition the Spartan FPGA distributes timing and trigger signals to AMC modules via the MicroTCA backplane. The AVR32 microcontroller implements a MicroTCA Module Management Controller (MMC) using firmware produced by our Wisconsin colleagues. It provides for configuration management, control and monitoring of module operation. This MMC extends the MicroTCA standard to provide many additional features valuable for CMS, including readout of up to 16 analog sensors, power supply status inputs, multi-stage power enable and others.

The tongue 3 board shipped with the AMC13XG is a simple two-layer board which provides access to JTAG and console signals for initial programming and debug. The AMC13XG is customized for various applications by installing a new tongue 3 board with can accommodate

for example discrete I/O for clock/control or a crosspoint switch for trigger applications. Power and GPIO signals are provided on a connector to tongue 3 for this purpose.

We present the new AMC13XG design, production testing, customization and commissioning in the ongoing CMS upgrade project.

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Session Classification: Poster

Contribution ID: 190

Type: Oral

Gamma Irradiation of Minimal Latency Hollow-Core Photonic Bandgap Fibres

Thursday, September 26, 2013 11:35 AM (25 minutes)

Hollow-core photonic-bandgap fibres (HC-PBGFs) offer many advantages over conventional fibres, such as low latency and radiation hardness; properties that make HC-PBGFs interesting for the HEP community. This contribution presents the results of gamma irradiation tests carried out using a new type of HC-PBGFs that combines low enough attenuation over distances that are reasonable for HEP applications together with a transmission bandwidth that covers the 1550nm region. The HC-PBGF showed two orders of magnitude lower radiation induced attenuation than a conventional single-mode fibre during a 67.5h exposure to gamma-rays, resulting in an RIA of 2dB/km at an accumulated dose of 1MGy.

Summary

Radiation hardness is one of the primary concerns when designing optical data transmission links for HEP applications. As a part of the link, optical fibres must withstand high radiation levels. Radiation tolerance grades for the High Luminosity LHC are 10kGy for calorimeter-grade and 500kGy for tracker-grade applications. These radiation levels cause significant darkening in a conventional glass core optical fibre, where radiation creates light absorbing defects, colour centres, into the core material. In a hollow-core photonic-bandgap fibre (HC-PBGF) more than 99.8% of the light is confined in a radiation-insensitive air filled core using a surrounding regular lattice structure. Also, in an air filled core the propagation of light is almost 50% faster than in a glass core. Due to the low latency HC-PBGFs could replace electrical links, and provide all the advantages of optical data transmission, in places where the latency of conventional optical fibres has been a limitation. These properties make HC-PBGFs very interesting for the HEP community.

We used two HC-PBGF samples (lengths 201m and 243m) together with a standard fibre (255m, Corning SMF28e+). The HC-PBGF samples were produced at the Optoelectronics Research Centre at the University of Southampton using a two-stage stack-and-draw method, where 19-cells of material were omitted from the microstructured cladding generating a hollow core 26µm in diameter. These HC-PBGFs have 160nm transmission bandwidth around a wavelength of 1550nm. The samples were pigtailed using single-mode fibres and FC/APC connectors and spooled around plastic (POM-H) bobbins. The samples were irradiated with a dose rate of 12.2kGy/h to 15.0kGy/h for 67.5h resulting in a total dose close to 1MGy, which is compatible with the dose expected in HL-LHC inner detectors. A super luminescent diode (SLED) was used to illuminate all samples. The optical spectra and optical powers were measured in fixed time intervals (1-3min). After the irradiation the recovery process was observed for several weeks, and additional time of flight measurements and transmission tests were carried out.

After the total dose of 1MGy, the radiation induced attenuation (RIA) in the HC-PBGF was only around 2dB/km, two orders of magnitude better than in the SMF. In fact, the SMF sample became practically opaque (200dB/km) during the irradiation. The RIA of the HC-PBGF is even one order of magnitude better than in a special radiation hard optical fibre, if we compare the results with earlier studies. Almost no change was observed in the optical transmission spectrum of HC-PBGF; only a minor increase in attenuation was present in limited regions of the spectrum. Post-irradiation time of flight measurements using picosecond optical pulses confirmed that the signals propagate in HC-PBGF samples at close to (>99%) the speed of light in vacuum. High-speed transmission tests up to data-rates of 10Gbps resulted in good quality eye diagrams, which were comparable

with non-irradiated SMF eye diagrams.

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Session Classification: Optoelectronics and Links

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Type: **Poster**

Evaluation of 400m, 5Gbit Versatile Link lengths over OM3 and OM4 fibres for the LHCb upgrade

Wednesday, September 25, 2013 5:10 PM (1 minute)

The LHCb experiment will upgrade its DAQ system to a trigger less, 40MHz read-out after LS2. To be able to process the approximately 40Tbit/s of data we will require a massive computing farm. This computing farm can not be installed underground, in the vicinity of the detector anymore due to the enormous power and cooling requirements. An affordable data transport solution has to be found to carry the data from the detector to the new data center on the surface. The distance to cover is estimated to be between 300 and 400 meters. We evaluated the feasibility of using the 5Gbit/s Versatile Link to cover the full distance over OM3 and OM4 quality fibres and will present our results.

Summary

Since LHCb will have to install their new computing center on the surface instead of the underground cavern, next to the detector, we will have to come up with a solution of transporting 40Tbit/s to the surface based data center, which is approximately 400m away from the detector. We have looked at several commercial, high speed interconnects, but all current solutions are prohibitively expensive at these distances. Further, all future solutions like 100 Gbit Ethernet or Infiniband will reach even shorter distances and would require expensive LR optics components.

The Versatile Link offers a way out of this dilemma. It was originally developed as a low mass, low power link that can handle the radiation levels and data rates of LHC's particle detectors. To be able to cope with radiation, the link runs at a relatively low speed of 5 Gbit/s. Since the extinction ratio and optical launch power of the Versatile Link are comparable to other commercial SR based optics, this should at the same time allow longer distances than commercial links.

There are of course several questions that need to be answered before this system can be deployed on a large scale. The link length is at the limit of the specification for 10Gbit over OM4. The closest commercial link would be 4Gbit fibre channel, which is also rated at 400m over OM4. Additionally this mode of operation was not the original intent of the Versatile Link, which is supposed to connect the LHC detectors to relatively close by network translators.

We decided to test several different fibres of different manufacturers to see if this approach is possible. We also tested if OM3 is a viable candidate for 5 Gbit/s link speeds. We will present the results of our investigation and show that it is indeed possible to use the Versatile Link in a long distance setup over OM4 as well as OM3.

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Session Classification: Poster

Contribution ID: 193

Type: Oral

System-level Testing of the Versatile Link Components

Thursday, September 26, 2013 12:00 PM (25 minutes)

During the first upgrade phase of the Large Hadron Collider experiments, high-speed optical links will be deployed to achieve the bandwidth needed to exploit the increasing luminosity and to allow data acquisition at higher rates. The Versatile Transceiver (VTRx) and Versatile Twin Transmitter (VTTx) modules are in their final development phase before production. They support different link architectures and offer compatibility with either single-mode or multi-mode fibre plants. This paper describes the supported link configurations and presents the system-level testing of the VTRx and VTTx front-end modules with various commercial-off-the-shelf back-end components.

Summary

The Large Hadron Collider (LHC) will be upgraded in multiple phases in order to achieve higher luminosity and to improve its physics performance. These periods offer unique opportunities for LHC experiments to perform the necessary maintenance and upgrade tasks allowing them to follow the evolution of the accelerator. As part of their upgrade programme, some detectors will deploy high-speed optical links during Long Shutdown 2 (2017-2018) to deal with the increasing data volume and higher trigger rate. To satisfy the bandwidth requirements and to cope with the on-detector radiation levels, the Versatile Link common project proposes link architectures based on radiation-resistant, low-mass and low-power front-end components, the Versatile Transceiver (VTRx) and the Versatile Twin Transmitter (VTTx) modules together with commercial-off-the-shelf (COTS) back-end components. The choice of these components depends on the architecture of the readout system as well as on the fibre plant (single-mode or multi-mode) already present in the experiments.

To support single-channel bidirectional as well as multi-channel unidirectional link architectures we have identified and tested COTS back-end devices that meet the Versatile Link system requirements. These candidate components are recommended for new optical systems designed to be compatible with the Versatile Link specifications. To verify the interoperability between existing VTRx/VTTx flavours and the selected COTS components, system-level tests have been performed. Apart from demonstrating feasibility, these tests were used to explore various options (e.g. optical cable type and length) and to quantify any incurred penalty on the link performance. They also allowed to measure parameters which are often not specified in device data sheets (due to the fact that the link may operate at a non-standard bit rate, e.g. 4.8 Gbit/s) or go beyond the original Versatile Link specifications. Finally, these tests enabled us to validate/verify optical link budget calculations carried out using parameters from the system specifications.

The paper will describe test systems based on high-end bench-top instruments and FPGA-based development platforms. We will present the results obtained from production-grade VTRx and VTTx devices linked with different back-end components.

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Presenter: SOOS, Csaba (CERN)

Session Classification: Optoelectronics and Links

Contribution ID: 194

Type: **Poster**

Neutron Irradiation of Optoelectronic Components for HL-LHC Data Transmission Links

Tuesday, September 24, 2013 5:38 PM (1 minute)

We report on the results of a radiation test carried out using 20 MeV neutrons on optoelectronic components, such as multi-channel transmitters and Si photonics building blocks, for use in future data transmission links by experiments at the High-Luminosity LHC.

Summary

The upgrade from LHC to High-Luminosity LHC will increase the luminosity of the LHC by a factor of 5-10; thus imposing even more stringent requirements on the optoelectronic components used in the front-ends of data-transmission links at the HL-LHC. Not only must they operate in harsher radiation environments, but they must also cope with the increase in data-rates. Components with lower power consumption, higher-speeds, and smaller sizes than those currently used in the optical links installed at the LHC are being investigated as possible candidates for HL-LHC data transmission links. In this paper we investigate the radiation tolerance of devices from two different “families” of technologies which fulfill these criteria: multi-channel transmitters and devices which can form the building blocks of a Si-photonics optical link.

The multi-channel transmitters tested consisted of a 12-channel InGaAs VCSEL array and a 4-wavelength Coarse-Wavelength-Division-Multiplexing (CWDM) module based on VCSELs. InGaAs lasers are a new material which we have not previously exposed to radiation testing, and are of interest because of their high reliability and efficiency, and their low power consumption. CWDM modules are interesting candidates for future optical links because they allow the transmission of multiple wavelengths over a single optical fibre which could allow us to increase the fibre-bandwidth of the currently installed fibre plants. The building blocks of a Si-photonics link tested were hybrid silicon lasers (Edge Emitting Lasers (EELs) built from type III-V semiconductor material on an SOI waveguide), SiGe photodiodes, and Si-based Mach-Zehnder Interferometer (MZI) modulators. The integration of these building blocks into a silicon-photonics link that could generate, modulate, process and detect light signals - all in a small Si-based package - would provide front-end components which are perfectly suited for HL-LHC applications.

The devices were irradiated with a 20 MeV neutron for 24 hrs at the University Cyclotron in Louvain-La-Neuve, Belgium and received a total fluence of $1.7-7.2 \times 10^{15}$ n/cm² depending on their position relative to the target. The static performance of the devices was monitored during the test and their recovery was monitored for ~350 hrs after the end of the irradiation period. A decrease in the slope efficiency and an increase in threshold current was observed in the lasers, while an increase in leakage current and a decrease in responsivity was observed in the photodiodes. The hybrid silicon lasers were observed to stop lasing before a fluence of 1×10^{14} and therefore are not suitable for operation in the harshest radiation environments of the experiments (e.g. tracker-type applications). The SiGe photodiodes exhibited a smaller relative increase in dark current compared to InGaAs devices also tested. Finally the the leakage and forward current of the modulators was found to increase during the irradiation period.

This paper will present the results from this radiation test, and examine the effect of the radiation on the performance of the silicon-based modulators and photodiodes in more detail, and will conclude by presenting the potential HL-LHC applications for these types of devices.

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Presenter: SEIF EL NASR, Sarah (University of Bristol (GB))

Session Classification: Poster

Contribution ID: 198

Type: Oral

Integration Design Issues in HEP Experiments

Wednesday, September 25, 2013 3:15 PM (25 minutes)

The global design process of high-energy physics experiments typically follows three overlapping stages consisting of detector modeling, detector integration and services implementation phases.

This process sometimes results in unexpected interactions between subsystems. At the CMS experiment at CERN we have had over two years of operational experience during which time we have observed several instances of unexpected behavior attributable to the complexity of detector integration design.

This presentation will examine the mechanisms and consequences of these behaviors, as well as considering their origins in the three level design process common to such experiments.

Summary

The global design process of high-energy physics experiments typically follows three overlapping stages consisting of detector modeling, detector integration and services implementation phases.

The detector modeling phase consists of successive optimizations of physics performance using Monte Carlo simulation. Based on a set of target processes, subdetector assemblies are added and modified until an acceptable cost to performance ratio of the complete detector is achieved, at which point the global design of the detector is fixed. Rarely are the practical details of detector construction addressed at this stage.

The inevitable conflicts arising from competing subdetector requirements are addressed during the detector integration phase, at which point issues such as cable routing, power dissipation and interaction between subdetectors result in design changes which often affect the subdetectors themselves and result in a further cycle of detector simulation.

Detector services can be explicit, such as detector readout, electrical power, cooling, safety systems and radiation shielding. They can also be implicit, such as mechanical support, maintenance access and lighting, which are not immediately obvious as part of the detector design and are often added late in the construction phases of an experiment.

Provision of the necessary services is implemented in part by subdetector groups and also by central support teams that provide services for several experiments at the same time. The design personnel for these systems are typically familiar with industrial systems and not with the special sensitivities of high-energy physics detectors. The resulting systems are designed for a contemporary industrial environment, often independently from the design process of the detector.

In addition, service requirements at the subdetector level are frequently specified in terms not directly addressable by support crews, such as detector temperature limits rather than coolant flow rate, which can result in the need for system modifications during the installation phase.

It should come as no surprise that such a design process sometimes results in unexpected interactions between subsystems. From a practical point of view, the organizational aspects of HEP detectors and laboratories are sufficiently complicated that achieving tighter integration between design teams remains a distant goal, so the detector commissioning and operation phases are marked by iterations of emerging design issues and subsequent modifications to the detector design.

At the CMS experiment at CERN we have had over two years of operational experience during which time we have observed several instances of unexpected behavior attributable to the complexity of detector integration design, issues that could be expected in any detector of comparable

scale.

This presentation will examine the mechanisms and consequences of these behaviors, as well as considering their origins in the three level design process common to such experiments. There are common features in the issues we have observed so far which can guide diagnostic methods and serve as a benefit of experience.

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Presenter: LUSIN, Sergei (University of Wisconsin (US))

Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Contribution ID: 199

Type: **Poster**

A Fast UV-LED QRdriver for Calibration System for SiPM Based Scintillator HCAL Detector

Tuesday, September 24, 2013 5:39PM (1 minute)

We report on electronic design of new calibration and monitoring system developed for the scintillator tiles calorimeter (AHCAL) for the ILC. System is based on original fast (3 ns pulsewidth) and precise LED driver called QMB. LED driver uses unique Quasi-Resonant circuit with embedded toroidal inductor. The QR-LED driver creates sinusoidal pulse to drive the LED. It has high dynamic range of precise a few nanosecond pulses. This sinus waveform significantly reduced EMC problems in the detector. System of one UV-LED can illuminates 72 scintillating tiles with SiPM using notched fibres. The system is flexible to all necessary task monitoring and calibration of SiPM detector.

Summary

The system based on QR-LED driver is flexible to all necessary task monitoring and calibration of SiPM detector. It has high dynamic range of precise a few nanosecond pulses. Low intensity LED pulses are needed to obtain nice SiPM single photoelectron spectra. A routine monitoring of all SiPMs during test beam operations is achieved with mid-range a fixed-intensity light pulse. The full SiPM response function is cross-checked by varying the light intensity from zero to the saturation level. In calibration systems we developed, we concentrate especially on the aspect a high dynamic range of precise a few nanosecond pulses. Calibration system has been tested with 2.2m long slab of engineering AHCAL prototype uses 864 SiPM embedded in 3 by 3cm scintillator tiles and represents a part of the biggest planned detector using SiPMs. During last two years, we developed the distribution of UV flashes to scintillator tiles. Instead of using one fiber for each tile, a series of notches cut on a single optical fiber illuminates a row of tiles below the fiber. The challenge is to make the light flashes equal with the same amount of light for each tile. We achieved the spread of light better than 20%.

We can get a nice single photoelectron spectra taken by SiPM illuminated by UV LED at QMB1. The SiPM response of quasi-resonant UV LED driver and the light distribution system to the low intensity light will be discussed at presentation. We can conclude that the system meets requirements for the calibration of the engineering hadron calorimeter prototype [2]. We also performed measurements of the amplitude dependence of the QRLED driver on the intensity of the magnetic field in the range 0 –4 T. The strength of the magnetic field is close to the field in the future ILD detector. We conclude that the relative change of the amplitude of the QRLED driver with embedded toroidal inductor do not exceed level of -3 per mille at 1 Tesla change. If we assume that the relative time stability of the magnetic field of the ILD solenoid will be at the level of 5E-4, then the amplitude time stability of the calibration light is better than 2E-6.

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Session Classification: Poster

Contribution ID: 200

Type: **Poster**

NaNet: a flexible and configurable low-latency NIC for real-time trigger systems based on GPUs.

Tuesday, September 24, 2013 6:28 PM (1 minute)

The adoption of GPUs in the low level trigger systems is currently being investigated in several HEP experiments.

While GPUs show a deterministic behaviour in performing computational tasks, data communication is the main source of fluctuations in the response time of such systems. We designed NaNet, a FPGA-based NIC supporting 1/10GbE links and the custom 34 Gbps APElink channel.

The design has GPUDirect RDMA capabilities, i.e. is able to inject the input data stream directly into the Fermi/Kepler class GPU(s) memory, and features a network stack protocol offloading engine.

We will provide a detailed description of the NaNet hardware modular architecture and a comparative performance analysis on the NA62 RICH detector GPU-based L0 trigger case study using the NaNet board and a commodity GbE NIC.

Figures of merit for the system when using the APElink and 10GbE links will also be provided.

Summary

The adoption of GPUs in the low level trigger systems is currently being investigated in several HEP experiments.

In this context the main issue to be taken into account is the strict real-time requisite typical of such systems.

While GPUs show a deterministic behaviour in performing computational tasks once data are available to be processed in their own internal memories, when the low level trigger system is considered as a whole, it becomes soon evident that input data transfer from the detector readout system is the main source of fluctuations in the trigger response time.

Our approach to this problem is twofold.

First, we designed a NIC capable of injecting readout data directly from the links into the memories of Nvidia Fermi and Kepler class GPUs without any intermediate buffering or CPU operation, reducing data transfer latency and its fluctuations (GPUDirect RDMA being the commercial name for this feature).

Second, we offloaded the CPU from the network stack protocol management, implementing a dedicated engine in the NIC, to further reduce latency and avoid possible OS jitter effects.

We implemented these two features in the NaNet FPGA-based NIC: the first was inherited from the development of the APEnet+ 3D HPC dedicated NIC, the second was realized adapting and integrating an open core developed by the FPGA vendor.

NaNet is flexible, supporting three different link technologies, namely GbE (1000BASE-T and 1000BASE-X), 10 GbE (10BASE-X) and the custom APElink channel implemented with 4 bonded LVDS lanes over QSFP+ cables and capable of 34 Gbps raw data bandwidth.

Beside this, being an FPGA based design, NaNet logic can be effectively tailored to different usage scenarios by adding dedicated custom logic blocks, e.g. performing compression or reshuffling on the data stream.

NaNet is currently being used in a pilot project within the CERN NA62 experiment aiming at the investigation of GPUs usage in the central Level 0 trigger processor.

We will provide a detailed description of the NaNet hardware modular architecture and a comparative performance analysis on the NA62 RICH detector GPU-based Level 0 trigger case study using the NaNet board and a commodity GbE NIC.

Figures of merit for the system when using the APElink and 10 GbE links will also be provided, along with an outline of future project developments.

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Presenter: LONARDO, Alessandro (Universita e INFN, Roma I (IT))

Session Classification: Poster

Contribution ID: **201**Type: **Poster**

Versatile Transceiver and Transmitter Production Status

Wednesday, September 25, 2013 5:12PM (1 minute)

Production of the Versatile transceiver and twin transmitter modules for use in the readout and control systems of upgrading LHC detector systems is starting. We review the performance of the prototypes produced so far and show that the modules are ready for production. We outline the commercial actions being taken to procure parts and assemblies and show the production plan for delivering known good parts in the various flavours required for the upgrade projects that will be using them.

Summary

The Versatile Link project aims to provide a multi-gigabit per second optical physical data transmission layer for the readout and control of High Luminosity LHC (HL-LHC) experiments. A point-to-point bidirectional system architecture is proposed. The front-end component that will enable the configuration of any of the Versatile Link's supported architectures is either a bi-directional module composed of both optical transmitter and receiver –the Versatile Transceiver (VTRx); or a twin transmitter for uni-directional applications (VTTx). Both SingleMode (SM) and MultiMode (MM) flavours of the VTRx and a MM VTTx have been developed to support the various types of installed fibre-plant in the LHC experiments.

Functional prototypes of all three module variants have been successfully designed, built, and tested in the laboratory. The latest generation include final versions of the laser driver and TIA/LA receiving amplifier married to a set of shortlisted lasers and photodiodes suitable for the three module variants. The newly finalized mechanical assembly including a custom-designed plastic connector latch has also been included in the assemblies that will be shown. The final prototypes have been fully evaluated for functionality and operation across the full operating temperature range. The results obtained will show that the design is sufficiently mature to go into mass production.

The overall required quantities of the different module variants will be reviewed and details will be given on how this requirement is split between the different upgrade projects. We will outline the procurement, production, and testing strategy for each module type and conclude with the overall timeline of the production.

Author: TROSKA, Jan (CERN)

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Presenter: TROSKA, Jan (CERN)

Session Classification: Poster

Contribution ID: 203

Type: Oral

PETA4 - A Multi Channel TDC/ADC ASIC for SiPM Readout

Thursday, September 26, 2013 2:50 PM (25 minutes)

We present a multi channel ASIC developed mainly for the readout of Silicon Photomultipliers. Each of the 36 channels contains a single ended and a differential frontend, self triggered hit detection and time stamping with 50ps bin width, signal integration, digitization and a common fast serial readout. Several additional features like neighbor triggering or fast self-abort for noise hits or insufficient amplitude are included. The chip uses bump bonding and requires very few external components so that very compact modules can be constructed.

Summary

The PETA4 ASIC is the latest member of a family of chips targeted mainly at the readout of Silicon Photomultipliers in PET, with possible use in other detector applications.

PETA4 houses 36 channels on a 5x5mm² die and is fabricated in the UMC 180nm technology. It uses bump bonds with a convenient pitch of ~270um to allow the construction of very compact modules at moderate substrate cost. The chip requires nearly no external components by integrating everything (PLL loop filter, bandgap reference, bias DACs,...) on chip. Power consumption is <40mW per channel, depending on digital speed and bias settings.

Every channel has two independent frontends: An established differential amplifier which has shown to be insensitive to pickup in the target application of PET/MRI, and a single ended frontend with very low input impedance ($Z_{in} \sim 7 \text{ Ohms}$) for high channel count operation. A fast discriminator with tunable threshold and a noise of <300uV self-triggers time stamping with a bin width of 50ps as well as an integrator with programmable integration time. The amplitude signal is converted by a ~9 Bit SAR ADC. After conversion, events with sufficient amplitude are queued for serial readout.

The previous chip version PETA3 has achieved a CRT time resolution of ~200ps when reading out scintillation light from a 3x3x5mm³ LYSO crystal coupled at room temperature to a 3x3mm² SiPM from FBK. Energy resolution for LYSO is ~12.5%. LYSO Crystals of 1.3mm size could be clearly identified with SiPMs of 4x4mm² when using a light spreader.

The architecture of PETA4 and its performance in the lab and with SiPMs will be presented.

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Presenter: SACCO, Ilaria

Session Classification: ASICs

Contribution ID: 204

Type: Oral

Microfabricated silicon on-detector cooling systems

Friday, September 27, 2013 9:45 AM (25 minutes)

Microfabrication technologies are being investigated by the PH/DT group at CERN for optimized, localized on-detector cooling solutions for silicon tracking systems.

Silicon microchannel cooling has been selected for the active thermal management of the NA62 GTK pixel detectors. 130 μm thick silicon plates with embedded microchannels, in which the radiation hard liquid C6F14 flows, are thermally interfaced to the backside of the FE chips. This technology has been demonstrated to be advantageous in terms of cooling efficiency, material reduction and suppression of any CTE mismatch problem.

Following this first successful application, further studies have been launched on two-phase flow for the upgrades of the ALICE ITS and the LHCb VeLo detectors.

Summary

Novel on-detector cooling systems with very low material budget, of the order of 0.1% X0, are being developed by the PH/DT group at CERN. They consist of silicon wafers in which microchannels are etched and closed by bonding another wafer, and placed in direct contact with the sensors and FE electronics.

When designing cooling systems for HEP detectors three issues have to be addressed: (i) the material budget should be reduced, (ii) for a given material budget the cooling power should be enhanced and (iii) the temperature difference between heat source and heat sink should be minimized. Microfluidics is a good candidate for addressing the first two issues given the high heat transfer coefficient in laminar flows which is inversely proportional to the size of the channel. The natural minimization of material and thermal barriers between the heat source and the cooling fluid effectively addresses the third issue.

Three application cases are presented with quite different operational modes, specifications and constraints.

NA62-GTK - The first one, which has been selected by the NA62 collaboration for the cooling of their GTK pixel detectors, is optimized for single-phase liquid flow in 150 parallel silicon microchannels of a radiation hard coolant (C6F14) to dissipate the total power produced by the read-out chips (about 48 W per station) and to keep the sensor at a temperature of about -20°C with a maximum temperature difference of the order of 6°C . Six modules from a pre-production run with the final configuration have been delivered at CERN by an external supplier.

LHCb VeLo - The second case is studied in the context of the upgrade programme of LHCb. The upgraded detector modules of the VeLo detector will be placed only few mm away from the LHC beam and will be subject to very intense radiation levels. To be robust against radiation damage the sensors should be maintained at a temperature below -20°C . The active electronics of the detector modules is expected to dissipate about 2 W/cm² over a surface of 2.8×4.2 cm² per each half of the 42 detecting planes, with a total estimated power dissipation in the detector volume close to 2 kW. The present cooling configuration relies on evaporative CO₂ in metal pipes connected to the modules periphery by thermal ledges. The approach for the upgrade is to integrate the microchannel cooling together with two-phase CO₂ as the coolant. 400 μm thick silicon microchannel prototypes have been fabricated and successfully tested at temperatures down to -30°C and pressure greater than 160 bars.

ALICE ITS - The third case presented is being considered for the upgrade of the ALICE ITS. In

order to minimize the material budget contribution of the cooling system, a silicon frame with embedded microchannels has been developed. This design eliminates any material contribution in the detection region while keeping all the efficiency advantages linked to microchannel cooling for the thermal management of the on-detector electronics.

Tests have shown that such silicon frames with evaporative C4F10 are able to remove the power dissipated by the FE chips (of the order of 0.3 W/cm²) while maintaining the sensor below 30°C with a maximum temperature gradient over the sensor area of 5°C.

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Presenter: MAPELLI, Alessandro (CERN)

Session Classification: TOPICAL (Packaging & High Density Hybrids)

Contribution ID: 205

Type: Oral

Performance of capacitively coupled active pixel sensors in 180 nm HV CMOS technology after irradiation to HL-LHC fluences

Wednesday, September 25, 2013 12:00 PM (25 minutes)

We explore the concept of using a deep-submicron HV CMOS process to produce a drop-in replacement for traditional radiation-hard silicon sensors. Such active sensors contain simple circuits, e.g. amplifiers and discriminators, but still require a traditional (pixel or strip) readout chip. This approach yields most advantages of MAPS (improved resolution, reduced cost and material budget, etc.), without the complication of full integration on a single chip.

After outlining the basic design of the HV2FEI4 test ASIC, results after irradiation with protons, x-rays and neutrons up to $1e16$ neq/cm² or 100MRad will be presented. Subsequently, design changes towards the optimised HV2FEI4_v2 are discussed and first irradiation results are shown before elaborating on future plans and general prospects of active sensors within ATLAS.

Summary

Deep-submicron HV CMOS processes feature moderate bulk resistivity and HV capability and are therefore good candidates for drift-based radiation-hard monolithic active pixel sensors (MAPS). It is possible to apply 60-100V of bias voltage leading to a depletion depth of ~10-20 μm . Thanks to the high electric field, charge collection is fast and nearly insensitive to radiation-induced trapping. Due to the dopant concentration, the depletion voltage is stable up to ~ $1E16$ neq/cm².

We explore the concept of using such a HV CMOS process to produce active sensors that contain simple circuits to amplify and discriminate the signal. A traditional readout chip is still needed to receive and organize the data from the active sensor and handle high-level functionality such as trigger management. We test our devices with the ATLAS FE-I4 pixel readout chip and the LHCb Beetle strip readout chips. Either strip-like or pixel-like readout can be selected on the same device. The active sensor approach offers many advantages with respect to standard silicon sensors: fabrication in fully commercial CMOS processes costs less than traditional diode sensors, aggressive thinning is resulting in much lower mass, bias voltage and operation temperature requirements are favourable. From a practical perspective, maintaining the traditional separation between sensing and processing functions lowers development cost and makes use of existing infrastructure.

To explore the performance and radiation hardness of active sensors, the HV2FEI4 ASIC was produced in the AMS H18 process. It is compatible with the pixel and strip readout chips mentioned above and features a matrix of 60 by 24 pixels with a pixel cell size of 33 by 125 μm . Thanks to relying on active circuits, capacitive coupling to the pixel readout chip is straightforward and is explored with HV2FEI4 chips glued to FE-I4s. The option to replace the expensive and time-consuming bump-bonding by gluing will significantly lower the cost of future large-scale Pixel Detector upgrades and enable the instrumentation of larger areas with pixel detectors.

The HV2FEI4 pixels are combined to match the readout multiplicity of the respective chips: for the pixel readout, three HV-CMOS pixels are multiplexed onto one FE-I4 pixel such that the hit pixels are encoded by the pulse height. In this way, the position resolution of the HV-CMOS sensor can be significantly better than the granularity of the readout chip suggests. For the strip readout, the pixel cells are combined to form virtual strips. Here, the z-position of the hit is encoded via the discriminator's pulse height and can be evaluated by analogue strip readout electronics like the Beetle chip.

The presentation will give an overview of the characterization results of the HV2FEI4 chip after

irradiation with protons, x-rays and neutrons to $1e16$ neq/cm² or 100MRad. While assemblies with the FE-I4 readout chips still worked even after the highest fluences, there were strong effects from ionizing dose which can be attributed to the (deliberately used) standard (rad-soft) design. As a consequence, a refined, more rad-hard design (the HV2FEI4_v2) was produced and first irradiation results will be presented. Finally, future prospects of active sensors within the ATLAS Upgrade plans will be discussed.

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Presenter: FEIGL, Simon (CERN)

Session Classification: Radiation Tolerant Components and Systems

Contribution ID: 209

Type: Poster

Test Results of the first 3D-IC Prototype Chip Developed in the Framework of HL-SLHC/ATLAS Hybrid Pixel Upgrade

Tuesday, September 24, 2013 5:10 PM (1 minute)

To face new challenges brought by the upgrades of the Large Hadron Collider at CERN and of ATLAS pixels detector, for which high spatial resolution, very good signal to noise ratio and high radiation hardness are needed, 3D Integrated Technologies are investigated. Commercial offers of such technologies are only very few and the 3D designer's choice is as a consequence strongly constrained. We present here the test results of the first 3D prototype chip developed in the GlobalFoundries 130 nm chips processed by the Tezzaron Company, submitted within the 3D-IC consortium for which a reliable qualification program was developed. Reliability and influence on the integrated devices behavior of Bond Interface (BI) and Through Silicon Via (TSV) connections, both needed for the 3D integration process, has also been addressed by the tests.

Summary

A major upgrade of the ATLAS pixel detectors in the innermost layers is required for HL-LHC on a 10-year timescale. The detector should operate with luminosity of $L = 1035 \text{ cm}^{-2} \text{ s}^{-1}$, which is ten times higher than the nominal LHC luminosity. For the pixel B-layer at 3.5 cm radius this will correspond to a major increase in occupancy and to a total fluence of $2 \times 10^{16} \text{ cm}^{-2}$ of 1 MeV neutron equivalent. The improvement in the segmentation of the pixel detectors will then be critical for the success of the upgrade. The ATLAS pixel collaboration has started R&D work to use the latest advances in high density and 3D electronics technology in order to develop a new FE chip (FE-TC4). In addition to IC design, an important part of the work consists in radiation testing.

The basic idea of the FE-TC4 is to split the existing FE-I4 baseline pixel into two tiers (floors): The first tier with analog part and corresponding controls and the second tier with remaining digital part. The aim is to reduce the pixel size in longitudinal direction by a factor of two to reach a pixel size of 50×125 microns, while at the same time increasing the digital memory per pixel. The chip size is 19×20 mm and will have a rate capability and radiation tolerance appropriate for SLHC pixels.

The 3D FE-TC4_P1 demonstrator chips, which have a small pixel matrix of 61×14 pixels of the size $50 \mu\text{m} \times 166 \mu\text{m}$ and additional 3D test purpose chips were produced in March 2010 in the first multi-project Tezzaron-GlobalFoundries run.

In a first step, we received each individual tier on February 2011 and tested them separately. We have showed that the 3D process did not modify the electrical performances and the radiation hardness of the dies.

In a second step, we received the last batch of 3D assemblies FE-TC4_P1 chips during the summer 2012, and tested them, showing a very good communication between tiers, despite a very bad yield. The 3D test chips have also been tested to qualify the interconnection technology. These chips have high number of daisy chained interconnections (both BIs and TSVs) and test transistors placed at different distance from the TSV.

The next step should be the test of the chip after bump-bonding to a silicon sensor in order to test the compatibility and yield after bump-bonding. Another important issue to address is the possibility to wire-bond on a very thin tier, up to the sensitive area of the second tier.

Author: PANGAUD, Patrick (Centre National de la Recherche Scientifique (FR))

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Presenter: PANGAUD, Patrick (Centre National de la Recherche Scientifique (FR))

Session Classification: Poster

Contribution ID: 218

Type: **Oral**

Carbon nanotubes and graphene nanoribbons for future IC interconnect technology

Monday, September 23, 2013 5:00 PM (45 minutes)

Given their physical limits, conventional materials such as copper are expected to fail in meeting many of the requirements for future nanoscale IC interconnects. Due to their outstanding electrical, thermal and mechanical properties, Carbon Nanotubes (CNTs) or Graphene Nano-Ribbons (GNRs) are proposed as innovative interconnect materials.

This presentation will first discuss the first examples of real-world successful integration between such interconnects and CMOS technologies. Then, a simple transmission line model will be presented, to describe the electrical propagation along CNT or GNR interconnects, derived from a semi-classical electrodynamical model. Referring to the nanointerconnects predicted for the 22nm and 16 nm technology at chip and package level, a performance comparison will be carried out between copper, CNT, GNR and hybrid solutions.

Author: MAFFUCCI, Antonio

Presenter: MAFFUCCI, Antonio (University of Cassino and Southern Lazio)

Session Classification: Opening 2

Contribution ID: 219

Type: **Oral**

The First Long Shutdown (LS1) and future upgrades of the LHC machine

Monday, September 23, 2013 5:45 PM (45 minutes)

The LHC has been delivering data to the physics experiments since the first collisions in 2009. The first long shutdown (LS1), which started on 14 February 2013, was triggered by the need to consolidate the magnet interconnections so as to allow the LHC to operate at the design energy of 14 TeV in the centre-of-mass for proton–proton collisions. It has now become a major shutdown that, in addition, includes other repairs, consolidation, upgrades and cabling across the whole accelerator complex and the associated experimental facilities.

LHC physics will resume in early 2015 while the other injectors and experimental areas of CERN will resume their operation in the second half of 2014.

The presentation first will describe the main activities of the LS1 and the operation strategy up to the LS2. Then, it will give the plans for the full exploitation of the LHC in line with the Update of the European Strategy for Particle Physics.

Presenter: BORDRY, Frederick (CERN)

Session Classification: Opening 2

Contribution ID: 221

Type: **Oral**

The Design of the Alphasat Payload Processor - Advancing Space Electronics!

Tuesday, September 24, 2013 9:00 AM (45 minutes)

Alphasat is the most sophisticated and largest European telecommunication satellite ever built allowing Inmarsat to offer flexible communications to maritime, aeronautical and other mobile customers. Alphasat supports over 400 spot beams processing more than 750 simultaneous channels in L-band.

This presentation will share some of the key technical challenges encountered during the design of the Alphasat Payload Processor - many of the technologies used on this project simply did not exist when the original proposal was drafted.

The beamforming DSP provides unprecedented flexibility and operational capability in terms of routing, channelization and combining channels to the desired beam.

Presenter: BEDI, Rajan

Session Classification: Plenary 1

Contribution ID: 222

Type: **Oral**

Mismatch in deep-submicron and the consequences for analog designs

Tuesday, September 24, 2013 2:00 PM (45 minutes)

Bandwidth, accuracy and power are the main parameters that connect the world of technology and sensor physics to the digital systems-on-silicon and advanced signal processing. Bandwidth is associated with drive strength, lithography node, and available current. Accuracy relates to static device properties such as device mismatch. Bandwidth and accuracy tend to pose opposing demands on technologies.

In this talk a short description of device mismatch is given, the technology trends for mismatch are examined as well as consequences for analog circuitry. As dimensions shrink down to the 22 nanometer level, the impact of these limits becomes more severe and more effort and power are needed to mitigate the problems.

Often a smart interaction with the system allows overcoming performance loss. In some systems calibration is an option, however cost and power budgets require that the designer optimally uses the available opportunities of the devices and technology.

Presenter: PELGROM, Marcel

Session Classification: Plenary 2

Contribution ID: 223

Type: **Oral**

Continuous-Time Analog Filter Design in CMOS Nanoscale Era

Wednesday, September 25, 2013 9:00 AM (45 minutes)

The CMOS nanometer technologies represent a key opportunity for performance improvements, in terms of signal processing quality, power and area, but at the same time is an exciting challenge for analog designers to face MOS second-order effects present in scaled technologies which strongly modifies transistor behavior and operations.

Innovative solutions will be presented to mitigate the problems of:

- biasing Active-RC structures (critical for low VDD-VTH)
- designing large bandwidth closed-loop (Active-RC) filter (critical for high-speed signals)
- reducing the input referred noise (critical for achieving the same DR at lower VDD and, then, lower signal amplitude)
- reducing the power consumption (critical for medium-linearity very high-speed applications)

Presenter: BASCHIROTTO, Andrea (University of Milan-Bicocca)

Session Classification: Plenary 3

Contribution ID: 224

Type: **Oral**

Chips developed at CERN in the framework of the Medipix3 Collaboration

Thursday, September 26, 2013 9:00 AM (45 minutes)

This contribution will review on-going ASIC developments taking place within the context of the Medipix3 Collaboration and also discuss a development aimed at a future CLIC vertex detector. We will begin with a description of the Medipix3RX ASIC and its innovative architecture. The measurement results and the lessons learned in the project will be covered in detail. We will discuss the novel aspects of the on-going and future developments (the Dosepix, Timepix3, Smallpix, and CLICpix prototype ASIC). This will also include discussion on hybrid pixel detector readout chip compatibility with Through Silicon Via technology (TSVs) and the exploration of more downscaled technologies.

Presenter: BALLABRIGA SUNE, Rafael (CERN)

Session Classification: Plenary 5

Contribution ID: 225

Type: **Oral**

Biologically-Inspired Massively-Parallel Computation

Thursday, September 26, 2013 2:00 PM (45 minutes)

The SpiNNaker (Spiking Neural Network Architecture) project aims to deliver a machine, ultimately incorporating a million ARM processors, optimised for running large-scale models of systems of spiking neurons running in biological real time. The major challenge in developing the machine has been to reproduce the very high levels of connectivity found in the brain; this has been achieved by using a very lightweight multicast packet-switched network that can carry very large numbers of very small packets, each carrying information about an individual neural spike.

Presenter: FURBER, Steve

Session Classification: Plenary 6

Contribution ID: 226

Type: **Oral**

3D Integration, from tool box to applications

Friday, September 27, 2013 9:00 AM (45 minutes)

After a tremendous technology modules development phase, 3D integration is now looking for the right use cases. Miniaturization and bandwidth needs are partially addressed by 2,5D heterogeneous interposers, but with limited impacts on competitiveness and cost. Disruptive 3DIC stacking is potentially offering unmatched performances and scalability in both niche and consumers markets but is facing difficult integration challenges in terms of signal integrity, thermal/mechanical managements and reliability. Specific applications oriented technological solutions are today required and will be reviewed in this talk. We will discuss how microelectronic for particle physics and imaging is about to become one of the main driver and recipient of 3D integration.

Presenter: LAMY, Yann (CEA- LETI)

Session Classification: Plenary 7

Contribution ID: 228

Type: **Oral**

Electronics for Particle Physics in Perugia

Monday, September 23, 2013 3:00 PM (45 minutes)

This presentation will try to give an overview of the electronics developments, related to the particle physics experiments, carried out in Perugia within the framework of a two decades collaboration between the INFN and the University of Perugia. In particular, will be addressed the recent and future activities in CMS, e.g. the future 65nm pixel chip read-out and the track/trigger system, the NA48 and NA62 trigger system, the AMS power supply system and the R&D activities related to 3D VLSI electronics and silicon on diamond devices.

Presenter: PASSERI, Daniele

Session Classification: Opening 1

Contribution ID: **229**

Type: **not specified**

Messages from our friends

Thursday, September 26, 2013 5:35 PM (15 minutes)

Presenter: JOOS, Markus (CERN)

Session Classification: xTCA Working Group

Contribution ID: 230

Type: **not specified**

Evaluation results from AC/DC converters for xTCA

Thursday, September 26, 2013 5:00 PM (15 minutes)

Presenter: BOBILLIER, Vincent (CERN)

Session Classification: xTCA Working Group

Contribution ID: 231

Type: **not specified**

Summary of evaluation results of xTCA equipment

Thursday, September 26, 2013 5:20 PM (15 minutes)

Presenter: DI COSMO, Matteo (Ministere des affaires etrangeres et europeennes (FR))

Session Classification: xTCA Working Group

Contribution ID: 232

Type: **not specified**

Update on the AMC13 project in CMS

Thursday, September 26, 2013 6:25 PM (15 minutes)

Presenter: HAZEN, Eric Shearer (Boston University (US))

Session Classification: xTCA Working Group

Contribution ID: 233

Type: **not specified**

ATCA developments for the ATLAS Tile Calorimeter upgrade

Thursday, September 26, 2013 5:50 PM (15 minutes)

Presenter: CARRIO ARGOS, Fernando (Universidad de Valencia (ES))

Session Classification: xTCA Working Group

Contribution ID: **234**

Type: **not specified**

SlinkXpress

Thursday, September 26, 2013 6:40 PM (10 minutes)

Presenter: RACZ, Attila (CERN)

Session Classification: xTCA Working Group

Contribution ID: 235

Type: **not specified**

Update on the ATCA/AMC readout cards for LHCb

Thursday, September 26, 2013 6:05 PM (20 minutes)

Presenter: CACHEMICHE, Jean-Pierre (Centre National de la Recherche Scientifique (FR))

Session Classification: xTCA Working Group

Contribution ID: 236

Type: **Oral**

What does it take to engineer and mass-produce a reliable parallel optics module...Or is it good enough to just have a good VCSEL and PIN array?

Wednesday, September 25, 2013 2:00 PM (45 minutes)

Parallel optics modules are complex hybrid solutions that incorporate chip design of the VCSEL and PIN arrays plus optics design of the lens; a packaging design to provide thermal management and environmental protection; and an electrical subassembly that includes the IC and firmware. All of this needs to be designed to operate reliably over a long lifetime at worse case conditions. This is proven out thru extensive qualification testing. Designing and producing this complex product for high volume production also requires unique testing capabilities and process development. This presentation will highlight the design aspects involved in the development and manufacture of high speed parallel optics module.

Presenter: FORNASARI, Marco (Avago Technologies)

Session Classification: Plenary 4

Contribution ID: 237

Type: **Oral**

Welcome from Director of INFN Perugia and Director of Department of Physics

Monday, September 23, 2013 2:40 PM (20 minutes)

Presenter: Prof. MANTOVANI, Giancarlo (INFN)

Session Classification: Welcome

Contribution ID: 238

Type: **Oral**

Welcome from the Local Organizing Committee

Monday, September 23, 2013 2:20 PM (20 minutes)

Presenter: BILEI, Gian Mario (Universita e INFN (IT))

Session Classification: Welcome

Contribution ID: **239**

Type: **Oral**

TWEPP Opening

Monday, September 23, 2013 2:00 PM (20 minutes)

Presenter: FARTHOUAT, Philippe (CERN)

Session Classification: Welcome

Contribution ID: 240

Type: **Oral**

Technology trends for customized analogue and digital circuit manufacturing including radiation hardness requirements

Monday, September 23, 2013 3:45 PM (45 minutes)

Technology development and applications for integrated circuit manufacturing are focusing on twofold areas, the 1st one going the aggressive trend of miniaturization, the 2nd going moderate in smaller feature sizes however with wide range of diversification and customization.

In the 2nd area challenges are in fields like integration of different technology platforms such as “CMOS combined with MEMS” or adding to conventional CMOS technologies special features, enabling dedicated applications and designs. This can be special added technology features for use of CMOS for imaging applications or for high voltage applications or for complex system-on-chips like secure IC or special sensor products.

Some application need to have the semiconductor technology being capable to sustain in harsh environment, this are for example high temperatures like in automotive or radiation hardness like in medical and aerospace.

Presenter: KAESMAIER, Rainer (Lfoundry)

Session Classification: Opening 1

Contribution ID: **241**

Type: **not specified**

Visit of the museum of wine and oil in Torgiano

Contribution ID: 242

Type: **not specified**

News on foundry access services via CERN

Thursday, September 26, 2013 5:00 PM (15 minutes)

Presenter: KLOUKINAS, Kostas (CERN)

Session Classification: Microelectronics User Group

Contribution ID: 243

Type: **not specified**

Status of CMOS 65nm technology access, distribution and IP blocks development

Thursday, September 26, 2013 5:15 PM (30 minutes)

Presenter: BONACINI, Sandro (CERN)

Session Classification: Microelectronics User Group

Contribution ID: 244

Type: **Oral**

Powering large FPGAs - ALTERA

Thursday, September 26, 2013 5:00 PM (15 minutes)

Presenter: CACHEMICHE, Jean-Pierre (Centre National de la Recherche Scientifique (FR))

Session Classification: Power Working Group

Contribution ID: 245

Type: **Oral**

GBT Project Status

Thursday, September 26, 2013 5:00 PM (15 minutes)

Presenter: TAVERNIER, Filip Francis (CERN)

Session Classification: Optoelectronics Working Group

Contribution ID: 246

Type: **Oral**

Powering large FPGAs - XILINX

Thursday, September 26, 2013 5:20 PM (15 minutes)

Presenter: ROSE, Andrew William (Imperial College Sci., Tech. & Med. (GB))

Session Classification: Power Working Group

Contribution ID: 247

Type: **Oral**

A reliability test system for production grade DC-DC modules

Thursday, September 26, 2013 5:40 PM (15 minutes)

Presenter: TROYANO PUJADAS, Isaac (CERN)

Session Classification: Power Working Group

Contribution ID: 248

Type: **not specified**

Discussion

Thursday, September 26, 2013 6:00 PM (1 hour)

Session Classification: Power Working Group

Contribution ID: **249**

Type: **not specified**

VTRx Project Status

Thursday, September 26, 2013 5:20 PM (15 minutes)

Presenter: Dr TROSKA, Jan (CERN)

Session Classification: Optoelectronics Working Group

Contribution ID: **250**

Type: **not specified**

LOC Project Status

Thursday, September 26, 2013 5:40 PM (15 minutes)

Presenter: YE, Jingbo (Southern Methodist University, Department of Physics)

Session Classification: Optoelectronics Working Group

Contribution ID: 251

Type: **not specified**

US-CDRD Opto Project Status

Thursday, September 26, 2013 6:00 PM (15 minutes)

Presenter: YE, Jingbo (Southern Methodist University, Department of Physics)

Session Classification: Optoelectronics Working Group

Contribution ID: 252

Type: **not specified**

Si-photonics at ANL

Thursday, September 26, 2013 6:20 PM (5 minutes)

Presenter: PARAMONOV, Alexander (Argonne National Laboratory (US))

Session Classification: Optoelectronics Working Group

Contribution ID: 253

Type: **not specified**

Si-photonics at CERN

Thursday, September 26, 2013 6:30 PM (15 minutes)

Presenter: SEIF EL NASR, Sarah (University of Bristol (GB))

Session Classification: Optoelectronics Working Group

Contribution ID: 254

Type: **not specified**

Open discussions

Thursday, September 26, 2013 5:45 PM (1h 15m)

Session Classification: Microelectronics User Group

Contribution ID: 255

Type: **not specified**

xTCA

Friday, September 27, 2013 11:55 AM (10 minutes)

Presenter: JOOS, Markus (CERN)

Session Classification: WG Summaries

Contribution ID: 256

Type: **not specified**

Optoelectronics Working Group Summary

Friday, September 27, 2013 12:05 PM (10 minutes)

Presenter: VASEY, Francois (CERN)

Session Classification: WG Summaries

Contribution ID: 257

Type: **not specified**

Microelectronics User Group Summary

Friday, September 27, 2013 12:15 PM (10 minutes)

Presenter: KLOUKINAS, Kostas (CERN)

Session Classification: WG Summaries

Contribution ID: 258

Type: **not specified**

Power Working Group Summary

Friday, September 27, 2013 12:25 PM (10 minutes)

Presenter: HANSEN, Magnus (CERN)

Session Classification: WG Summaries