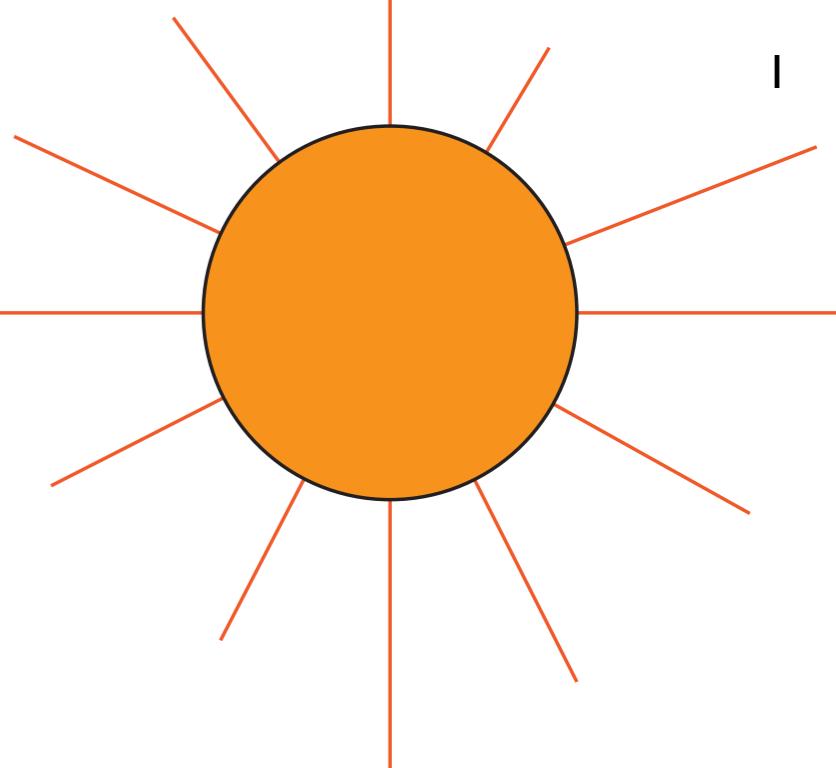


Characterization of COTS ADC radiation properties for ATLAS LAr calorimeter readout

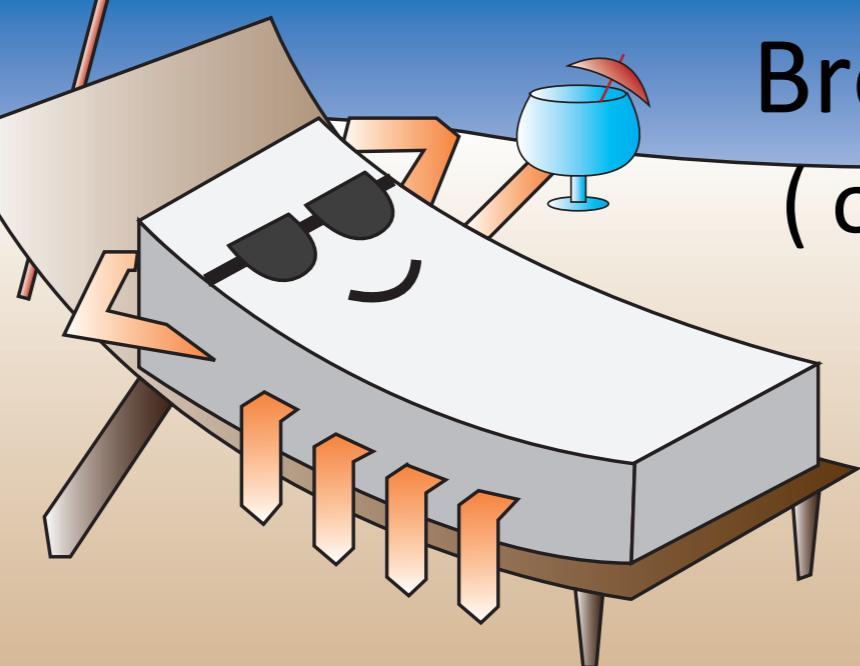
upgrade



Helio Takai

Physics Department

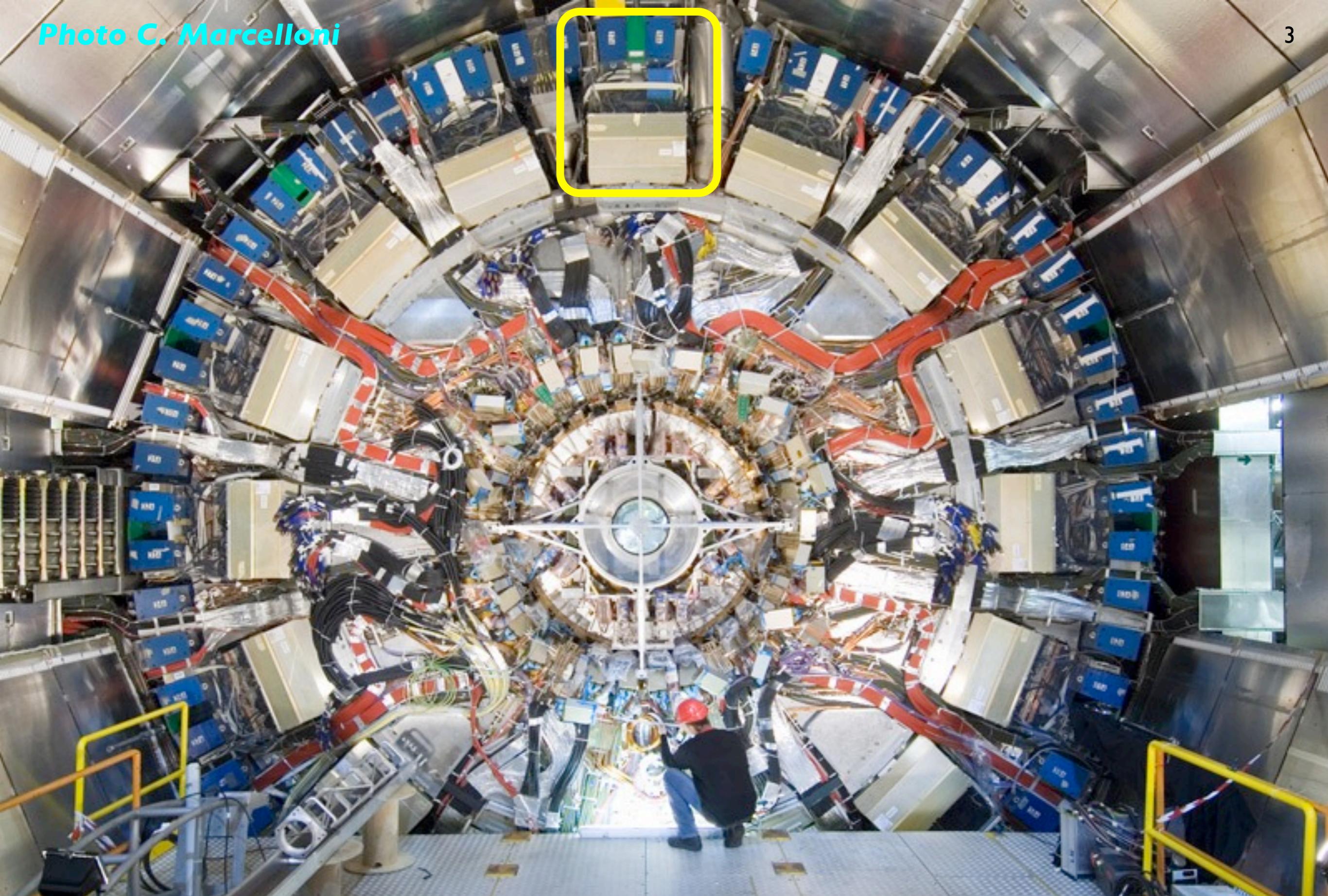
Brookhaven National Laboratory
(on behalf of the ATLAS liquid argon
calorimeter group)



Authors

Kai Chen, Hucheng Chen, Xueye Hu,
James Kierstead, Francesco Lanni,
Joseph Mead, Sergio Rescia, Hao Xu
and Helio Takai

Brookhaven National Laboratory



Can we use commercial components?

The Yin and Yang of COTS

Large number of design options.

Do they really fit my needs?

I can purchase a production lot

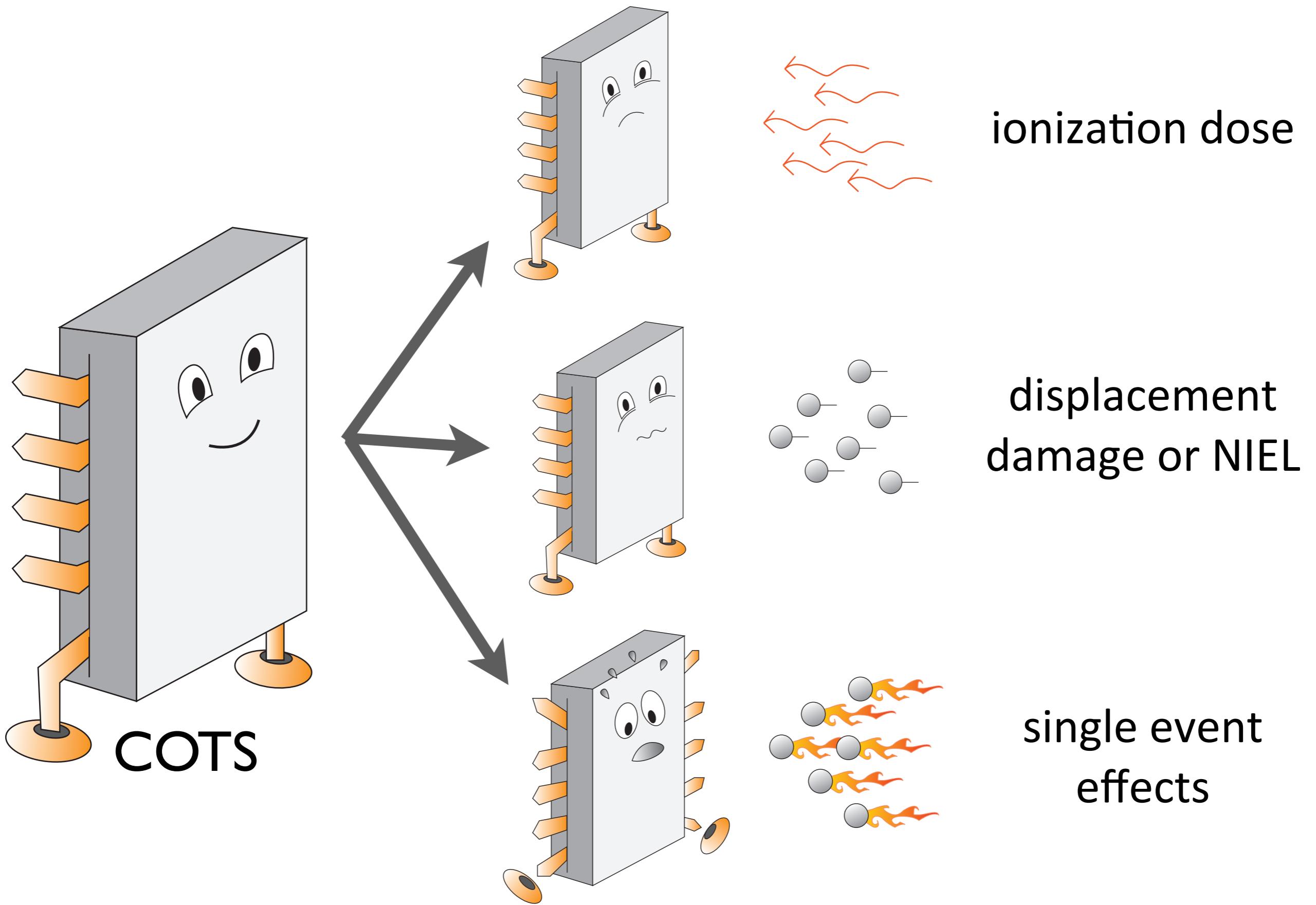
Parts become obsolete

Small feature size components are more radiation tolerant

Are they really radiation tolerant?

I can perform tests and qualify them for radiation

I worry about production variabilities



The Background in the Barrel LAr Crates

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The radiation background in the ATLAS Barrel electronics crates is composed of hadrons, electrons and photons produced in the last stages of the particle shower in the calorimeters itself.

	Simulation (fb^{-1})	Safety Factor	Test Target (3000 fb)
Ionizing Dose	3.0 rad	10	90 krad *
1 Mev eq. neutron **	2.0×10^9	2	1.2×10^{13} (1 Mev n)
Hadrons (>20 MeV)	2.84×10^8	2	2×10^{12} (>20 MeV)

* Enhanced Low Dose Rate Sensitivity (ELDRS)

** NIEL is not a concern for CMOS technology

Irradiation Facilities

Ionizing dose

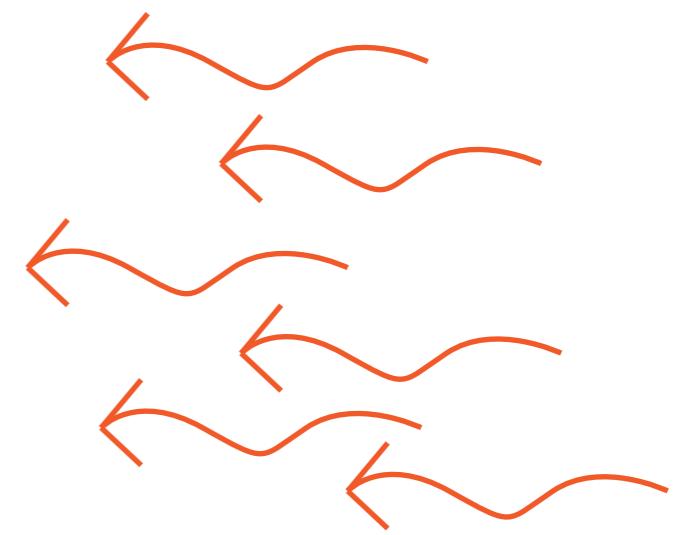
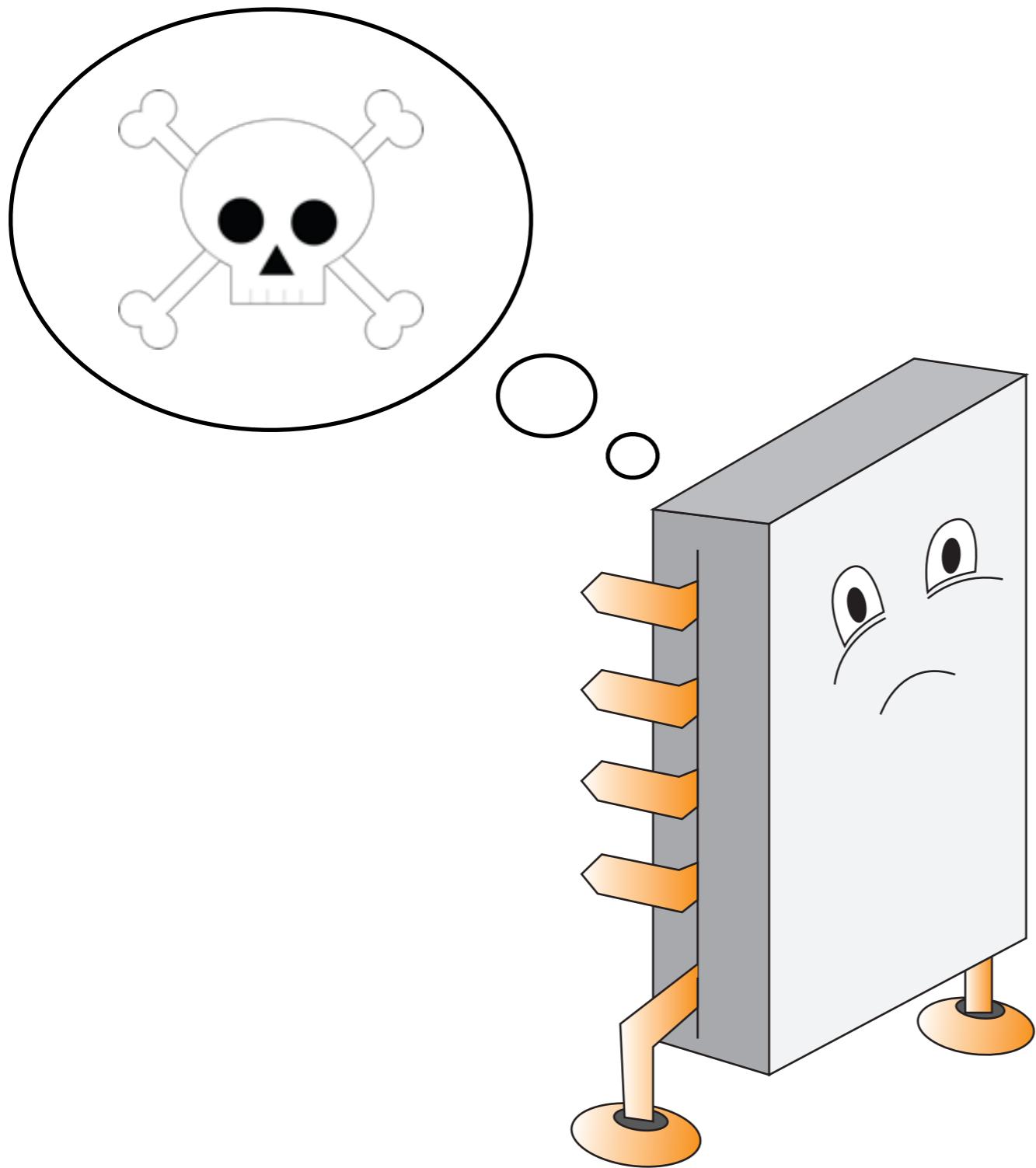
1. Solid State Gamma Irradiation Facility (BNL)

Single Event Effects

1. LANSCE WNR (Los Alamos, NM) - *neutrons (high energy)*
2. Mass General Hospital (Boston, MA) - *protons (216 MeV)*
3. IUCF (Bloomington, IN) - *protons (200 MeV)*
4. H4IRRAD (CERN) - *not available*
5. TSL at Uppsala, high energy neutrons and protons
6. 14 MeV neutron source @BNL

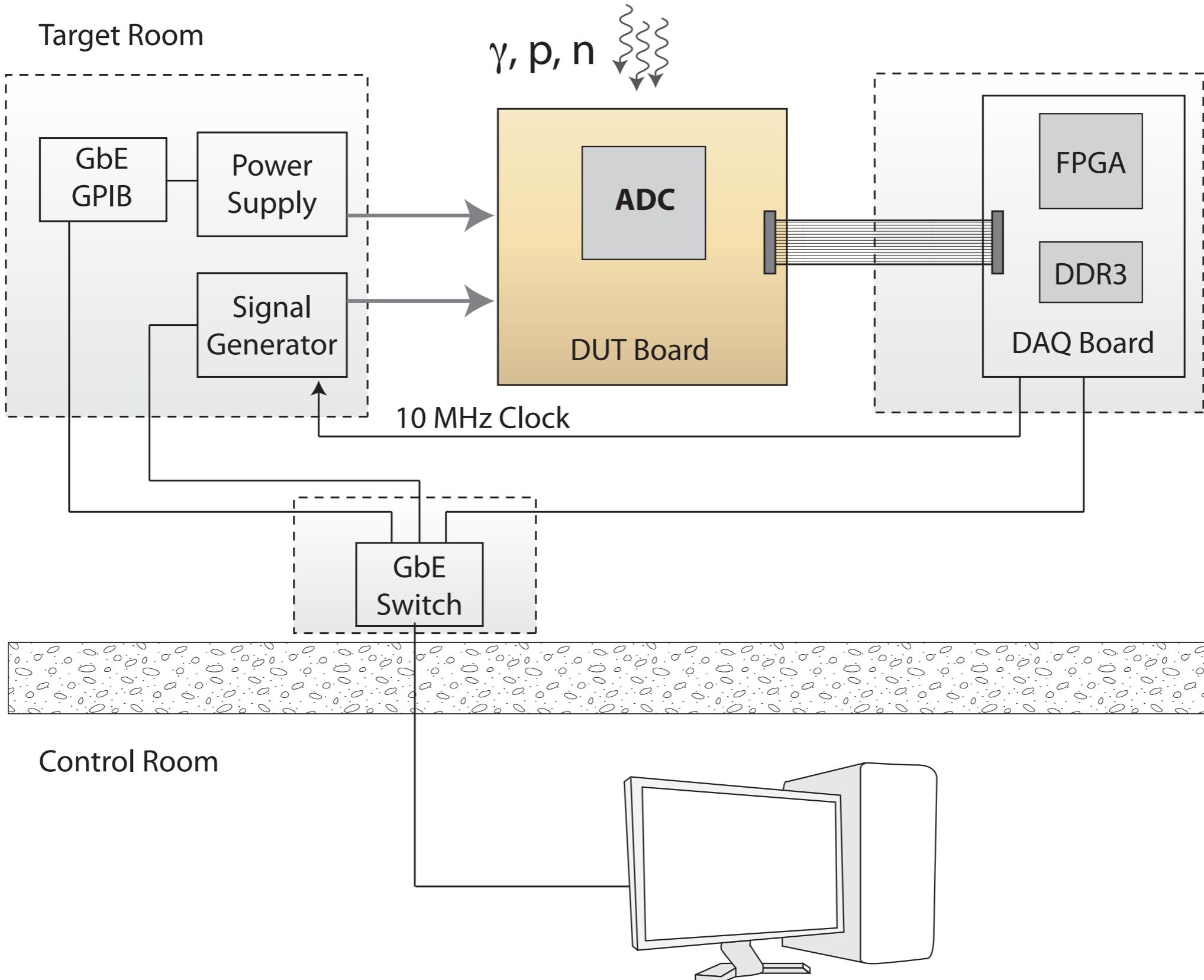
Displacement Damage

1. Reactor, UMASS at Lowell



Ionization Dose Effects

Experimental Setup

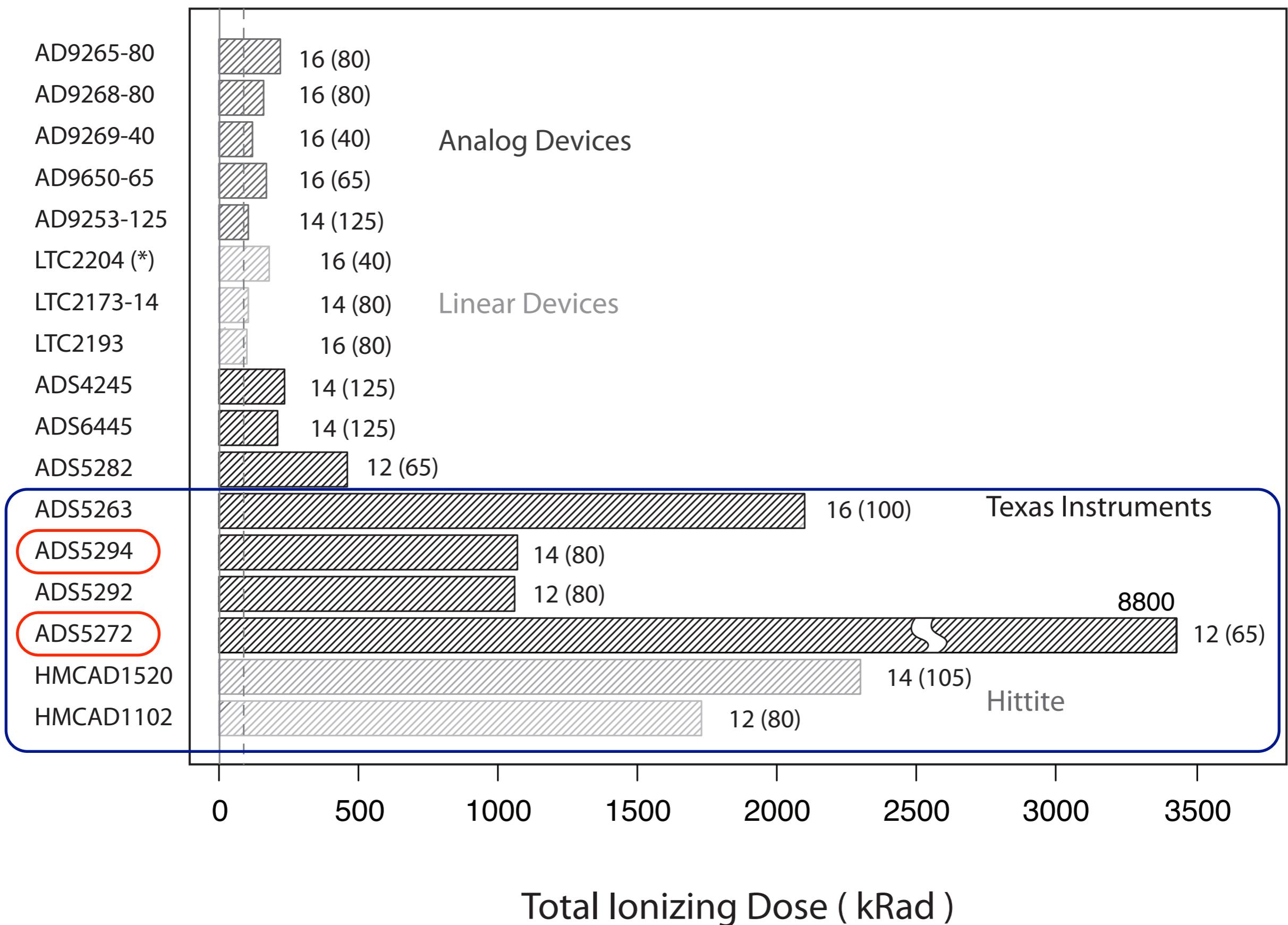


Setup used for TID and SEE studies

Total Ionizing Dose

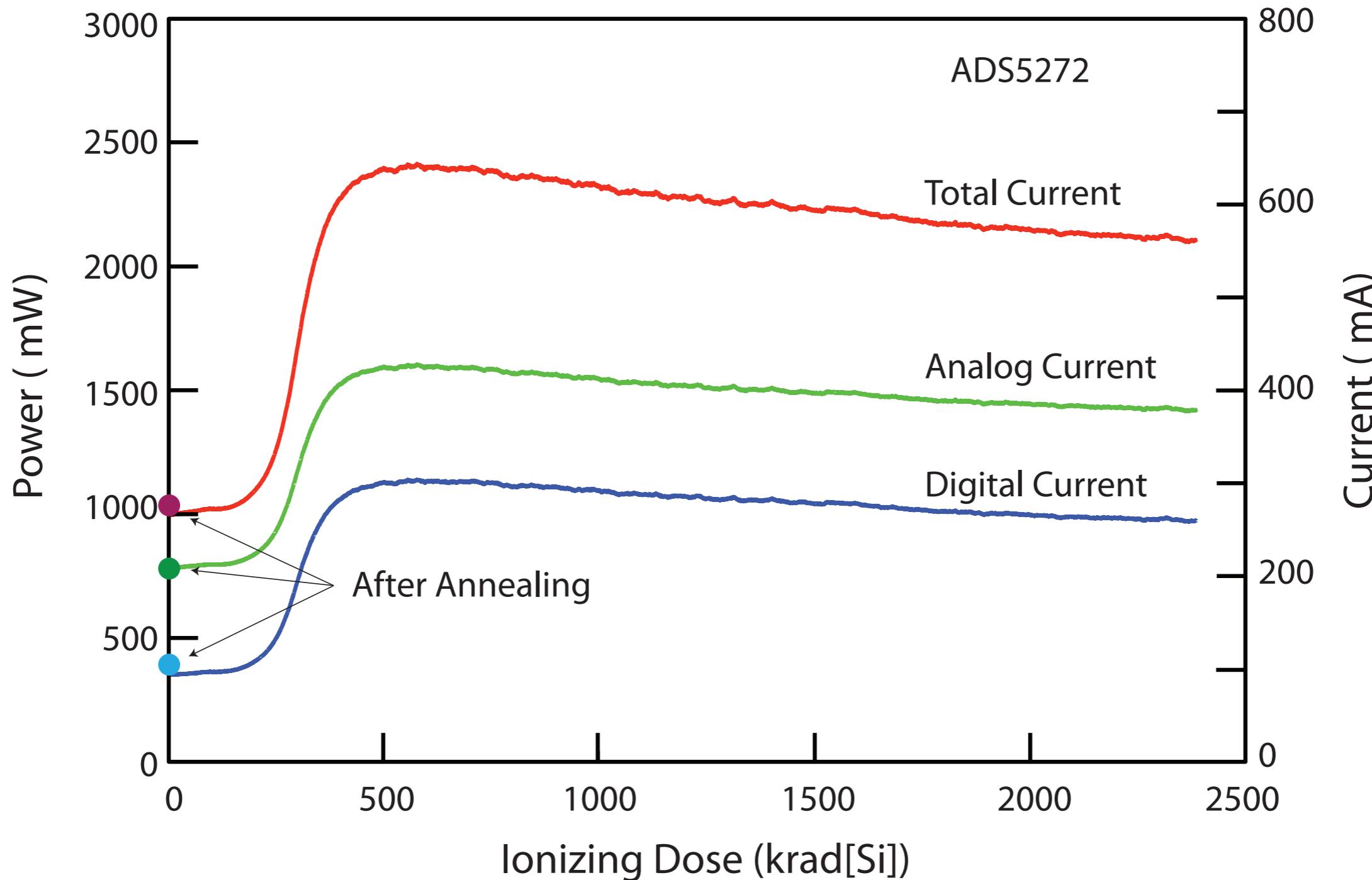
ADC	Dynamic Range [bit]	F [MHz]	Analog Input Span [V _{p-p}]	Channels per Chip	P _{total} per Channel [mW]	Feature Size (nm)	Vendor	TID [kRad(Si)]
AD9265-80	16	80	2	1	210	180	ADI	~220
AD9268-80	16	80	2	2	190	180	ADI	~160
AD9269-40	16	40	2	2	61	180	ADI	~120
AD9650-65	16	65	2.7	2	175	180	ADI	~170
AD9253-125	14	125	2	4	110	180	ADI	~105
LTC2204	16	40	2.25	1	480	350	Linear	~180
LTC2173-14	14	80	2	4	94	180	Linear	~105
LTC2193	16	80	2	2	125	180	Linear	~100
ADS4245	14	125	2	2	140	180	TI	~235
ADS6445	14	125	2	4	320	180	TI	~210
ADS5282	12	65	2	8	77	180	TI	~460
ADS5263	16	100	4	4	280	180	TI	~2100
ADS5294	14	80	2	8	77	180	TI	~1070
ADS5292	12	80	2	8	66	180	TI	~1060
ADS5272	12	65	2.03	8	125	180	TI	~8800
HMCAD1520	14	105	2	4	133	180	Hittite	~2300
HMCAD1102	12	80	2	8	59	180	Hittite	~1730

Total Ionizing Dose



Performance and Annealing

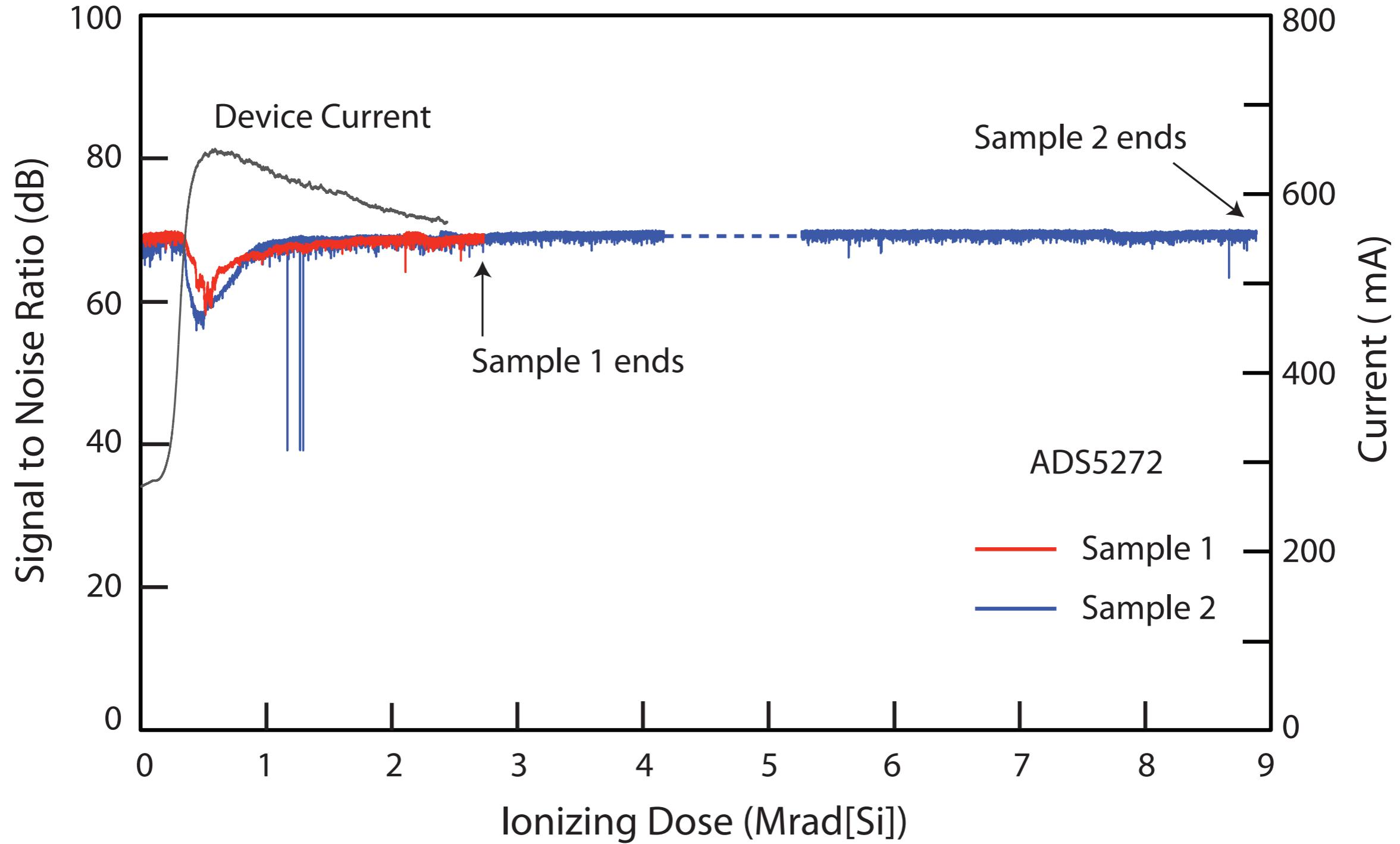
12



20 ADS5272 samples are now being tested following ATLAS guidelines. The first two samples show room temperature annealing.

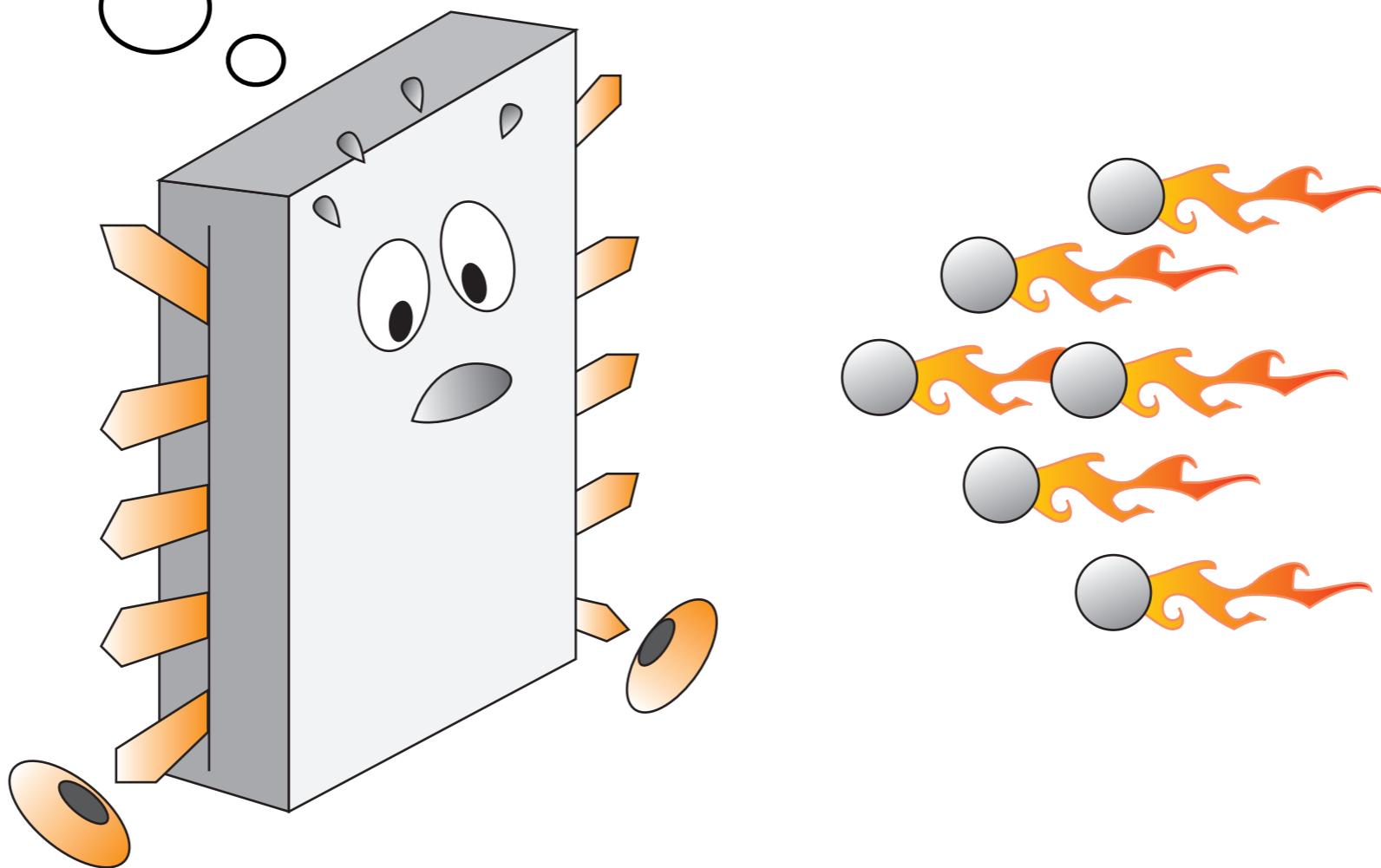
Performance and Annealing

13



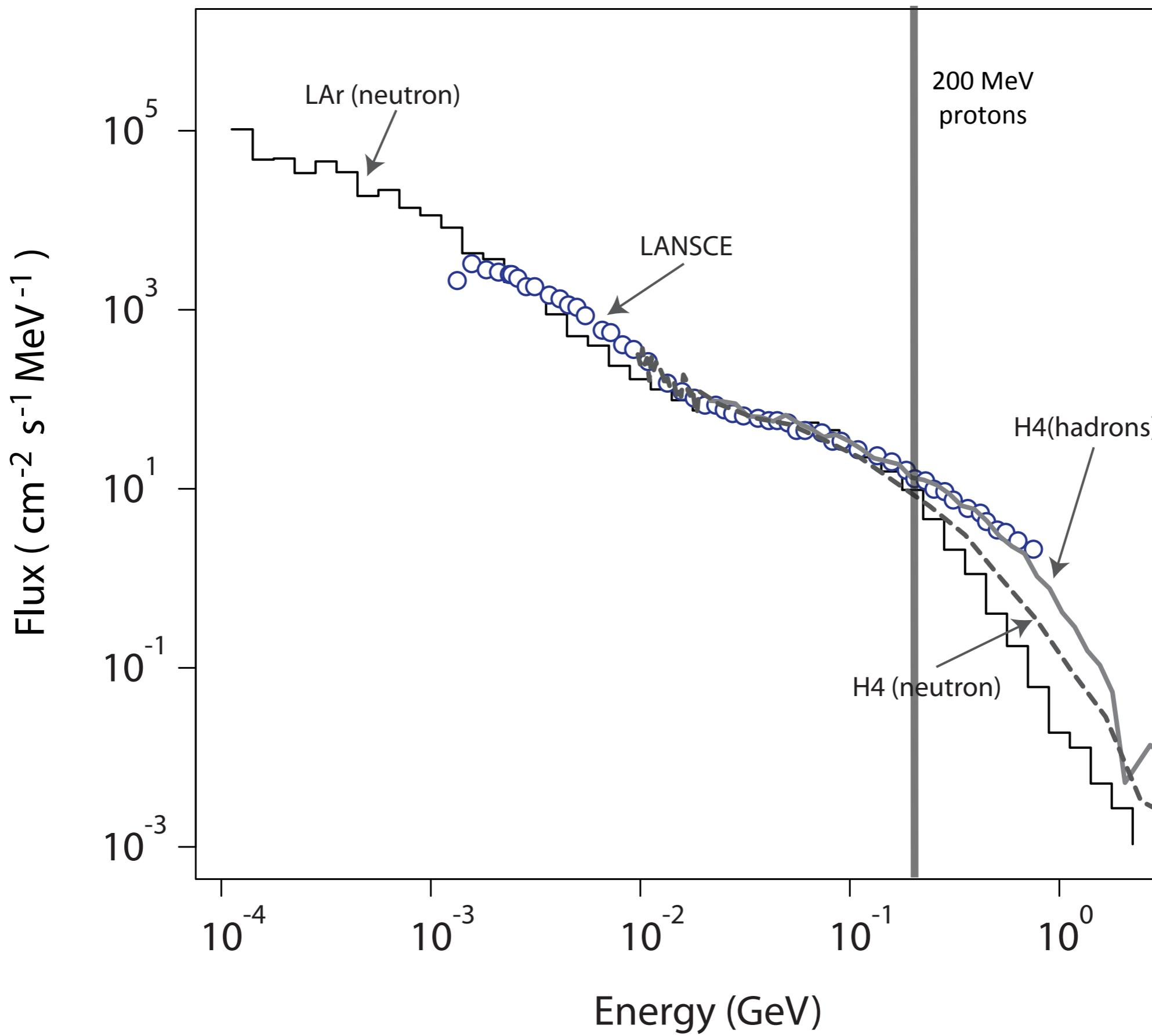
Signal to noise ratio as function of total ionizing dose for ADS5272

Latch Up?
SEFI?

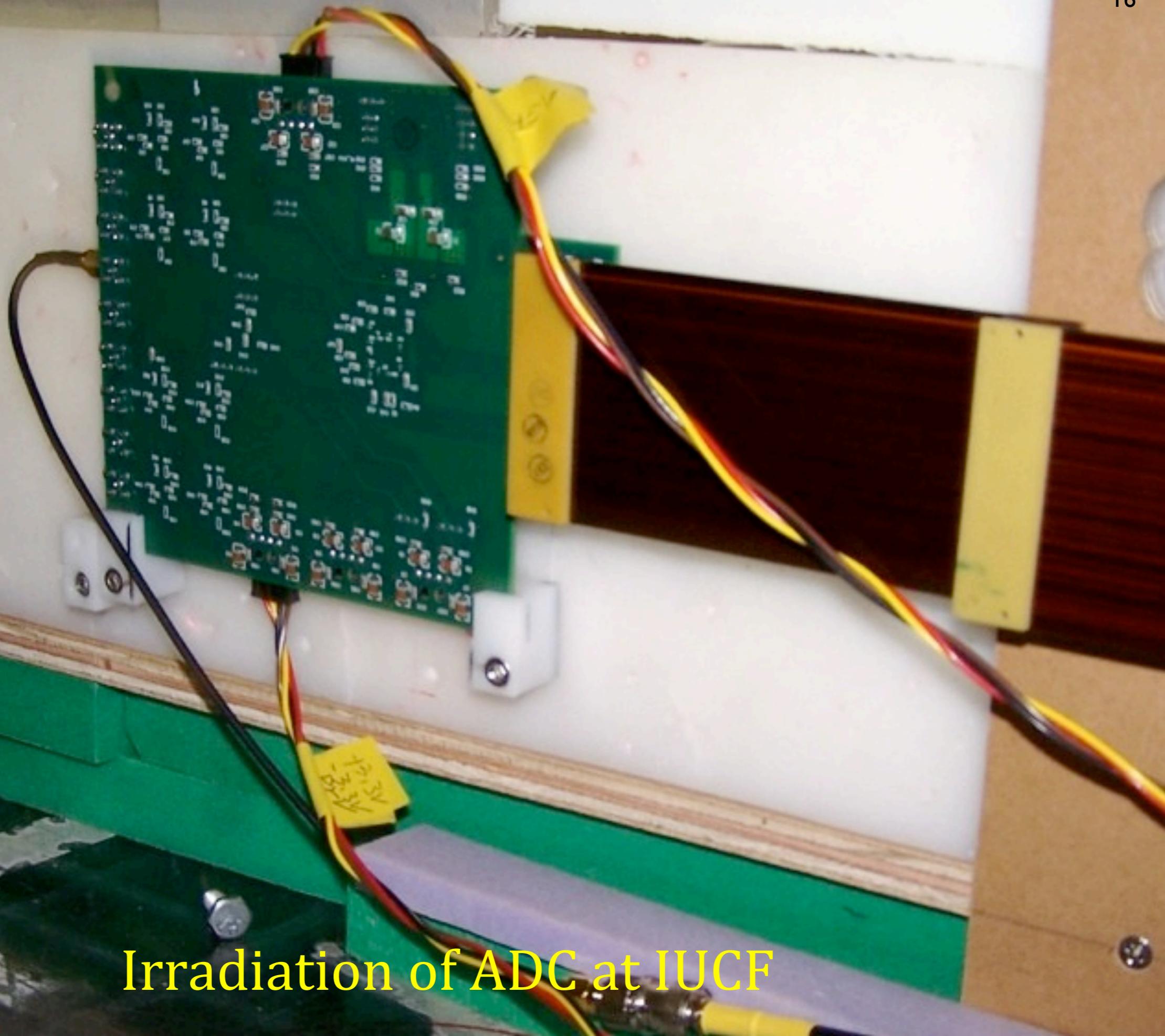


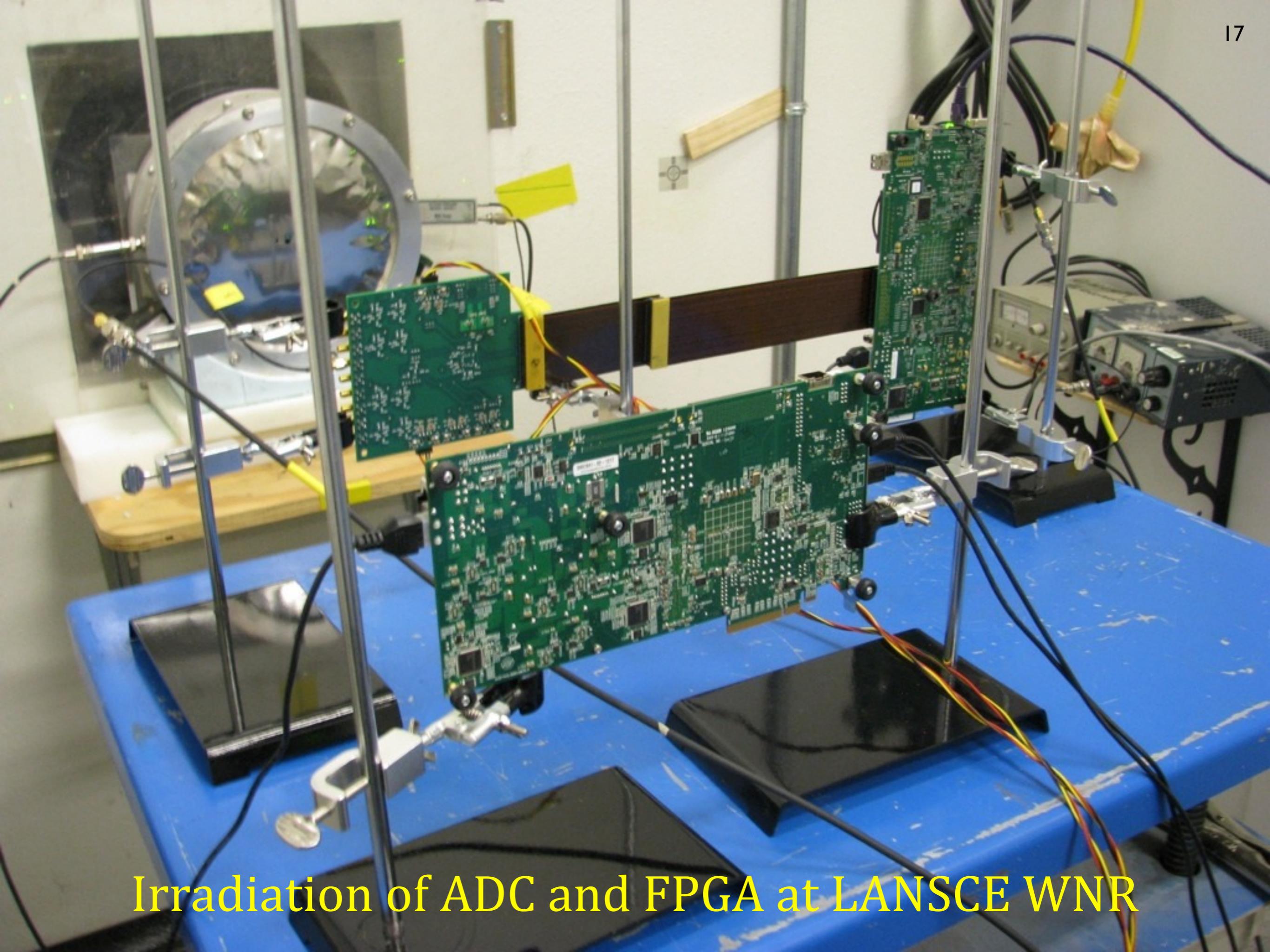
Single Event Effects

The Appropriateness of Test Facilities



Irradiation of ADC at IUCF

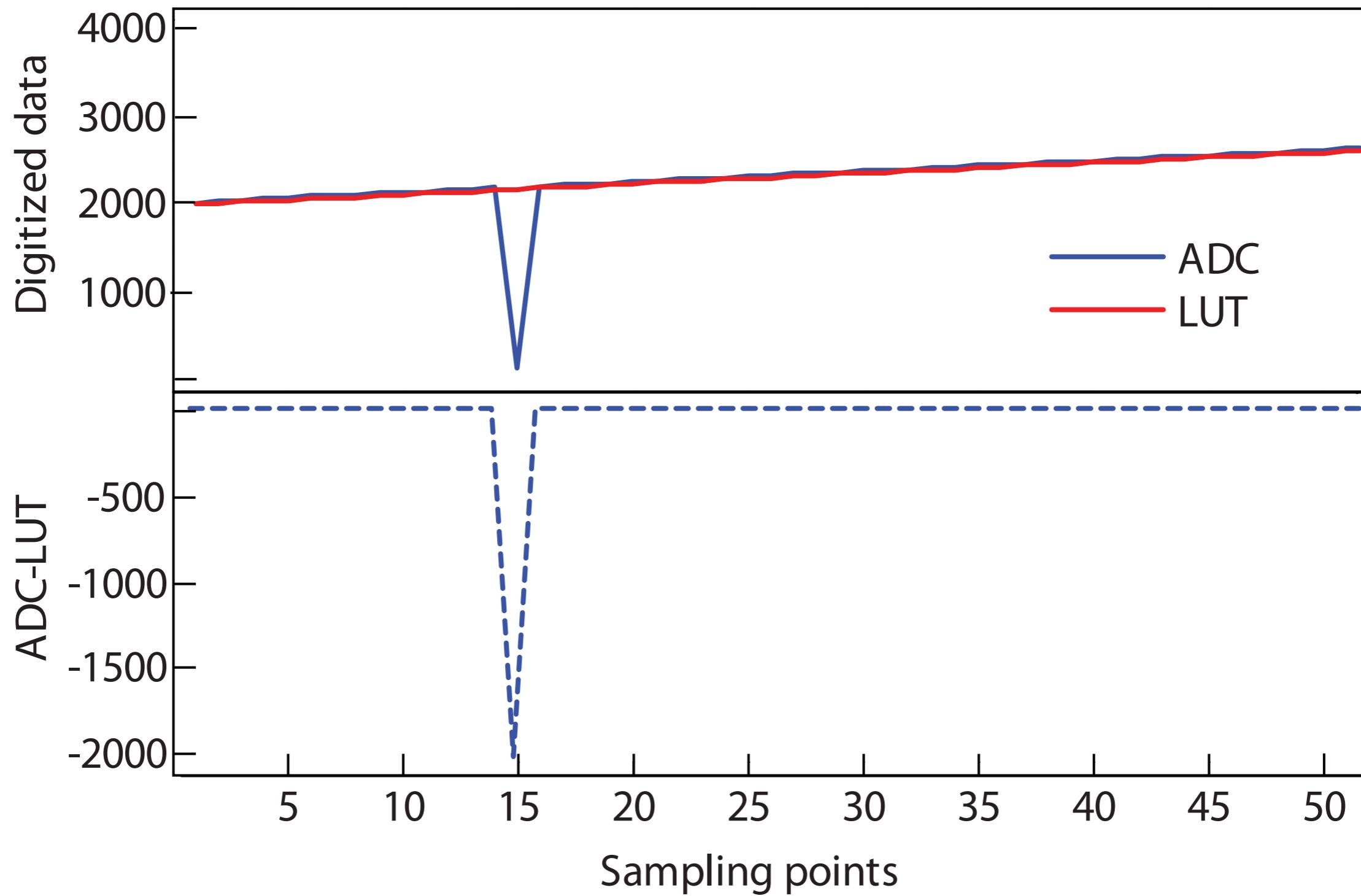




Irradiation of ADC and FPGA at LANSCE WNR

“Bit-Flip”

18



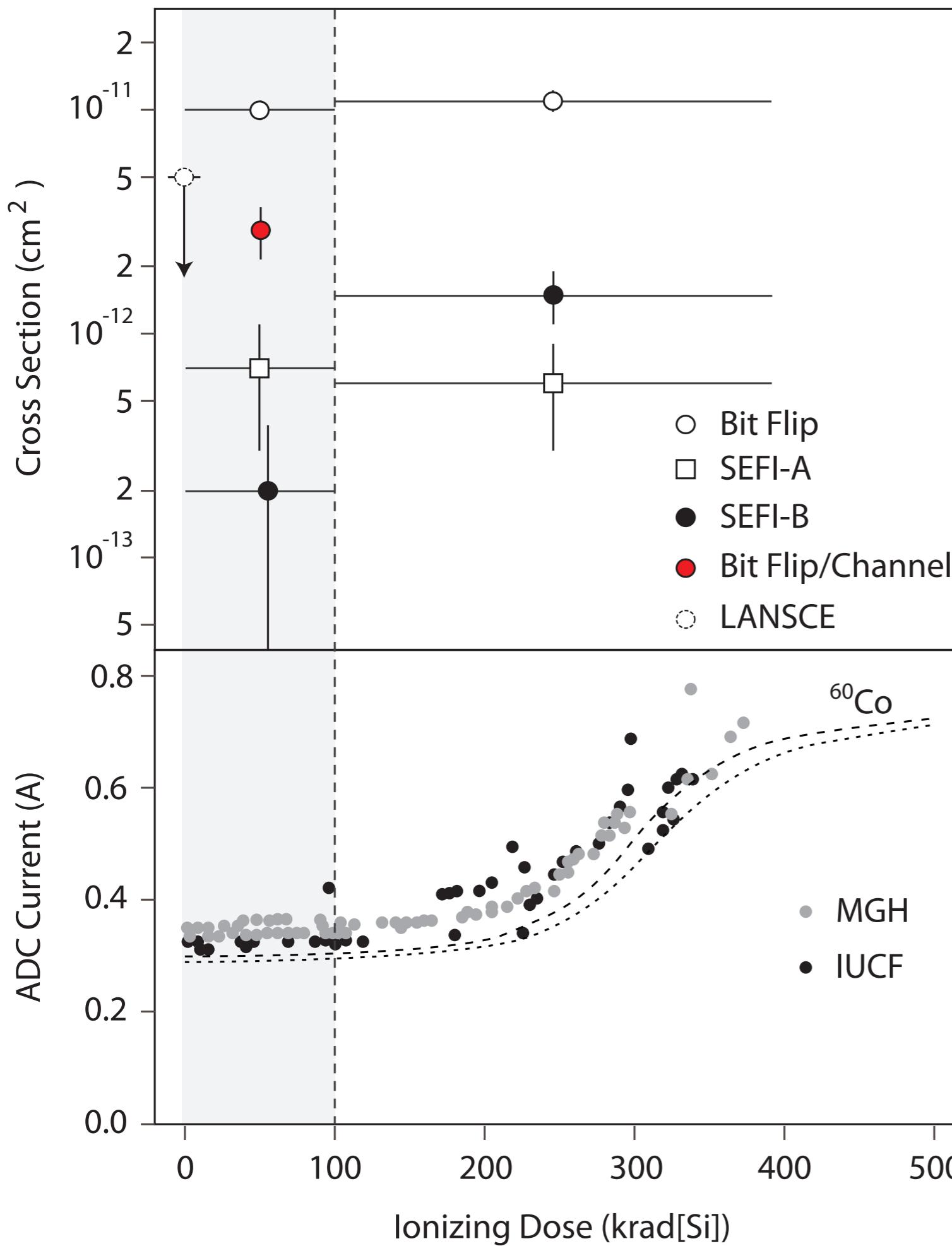
SEE cross sections¹⁹ for ADS5272

SEFI - Single Event Functional Interrupt.

SEFI-A: Can be reset by an external signal. Device recovers in 200 ns.

SEFI-B: Requires a Power Cycle.

*Quoted values are per device.
Each ADC digitizes 8 channels.*



Summary for ADS 5272 and ADS 5294

Quoted values are per device. Each ADC digitizes 8 channels.

SEE Measurement	ADS5272 (<100 kRad)	ADS5272 (>100 kRad)	ADS5294
SEFI A (cm^{-2})	$(0.7 \pm 0.4) \times 10^{-12}$	$(0.6 \pm 0.3) \times 10^{-12}$	$(7.4 \pm 1.2) \times 10^{-12}$
SEFI B (cm^{-2})	$(0.2 \pm 0.2) \times 10^{-12}$	$(1.5 \pm 0.4) \times 10^{-12}$	-
SEU ($cm^{-2} bit^{-1}$)	$(1.4 \pm 0.1) \times 10^{-12}$	$(1.6 \pm 0.1) \times 10^{-12}$	$(1.8 \pm 0.2) \times 10^{-11}$

ADS5272 - Identified SEU, and two types of SEFI. One that is recoverable via external reset and a second that requires a power cycle.

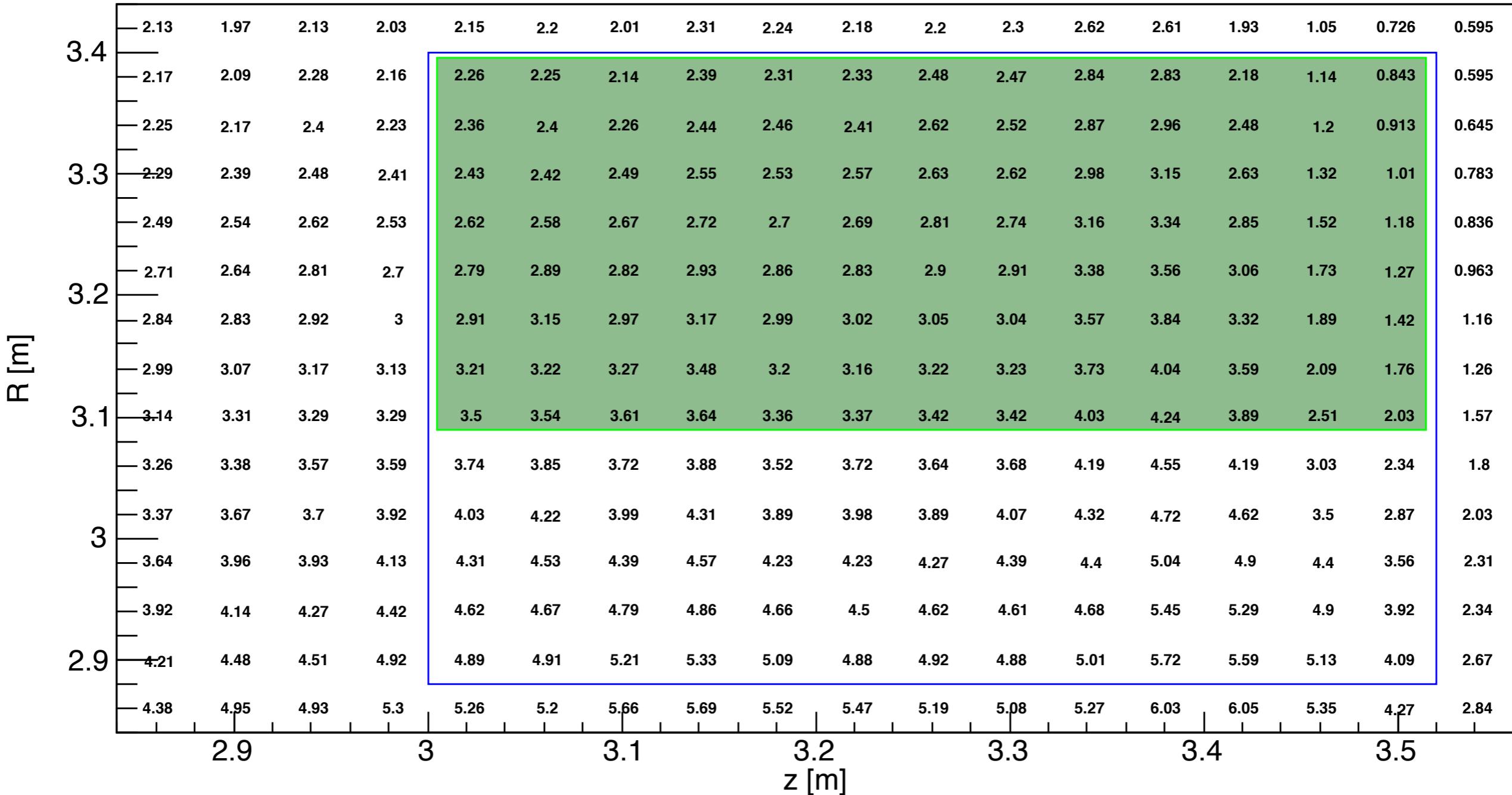
ADS5294 - There is no dependence on total dose for SEFI. SEFI requires reprogramming of three registers, that takes less than $5 \mu s$.

In both devices the probability of bit flip is independent of the bit position.

Rates and Mitigation

LAr EMB Front-End Crates: SEE fluence @ 14 TeV [$\times 10^8$ hadrons cm 2 /fb $^{-1}$]

Digital Section: $\langle \Phi \rangle = 2.84 \pm 0.59 / \Phi_{MAX} = 4.24 - SF=2$



Rates and Mitigation

For LAr barrel trigger boards in phase 2, the **SEFI-B rate** is:

$$\text{SEFI-B/h} = \frac{2 \cdot 2.84 \times 10^8 \cdot 2 \cdot 2 \times 10^{-13} \cdot 2500}{10 \text{ h}} \sim 0.5 \text{ /fill}$$

fluence
fb⁻¹

integrated
luminosity (fb)

number of
devices

safety
factor

one fill

cross
section

SEFI type A can be cleared issuing resets periodically during, e.g. gaps in the accelerator cycles ($f = 11 \text{ kHz}$).

Summary

- Qualification procedure for COTS ADC was established.
- Seventeen COTS ADCs were tested for their tolerance to ionizing dose. They all perform up to 100 krad, with six withstanding doses larger than 1 Mrad.
- Annealing tests reveal recovering to baseline even for larger doses. Controlled annealing tests is underway for 20 ADS5272 samples for ELDRS studies.
- ADS5272 and ADS5294 were selected for SEU tests. Bit Flips and SEFIs were observed and their cross sections measured.
- The ADS5272 has two types of SEFI. One type can be cleared by an external reset, and the second needs a power cycle.