TWEPP 2013 - Topical Workshop on Electronics for Particle Physics

Tuesday 24 September 2013

Poster: First Part (17:00 - 18:30)

-Conveners: Mitchell Franck Newcomer

time	[id] title	presenter
17:00	[4] Radiation hard programmable delay line for LHCb Calorimeter Upgrade	MAURICIO FERRE, Juan
17:01	[30] The CLARO-SiGe, a front-end ASIC for precise timing measurements at low power	GOTTI, Claudio
17:02	[52] Pixel chip architecture optimization based on a simplified statistical and analytical model	CONTI, Elia
17:03	[75] Development of variable frequency, power Phase-Locked Loop (PLL) in 130nm CMOS technology	FIRLEJ, Miroslaw
17:04	[96] Development of CMOS Pixel Sensor with digital pixel dedicated to future particle physics experiments	PHAM, Thanh Hung
17:05	[127] STiC - A Mixed Mode Silicon-Photomultiplier Readout ASIC for Time-of-Flight Applications	HARION, Tobias
17:06	[135] The Charge Pump PLL Clock Generator Designed for the 1.56 ns Bin Size Time-to-Digital Converter Pixel Array of Timepix3 Readout Chip	FU, Yunan
17:07	[168] Radiation-Hardened-By-Design Clocking Circuits in 0.13µm CMOS Technology	YOU, yang
17:10	[209] Test Results of the first 3D-IC Prototype Chip Developed in the Framework of HL-SLHC/ATLAS Hybrid Pixel Upgrade	PANGAUD, Patrick
17:21	[23] Common Read-Out Receiver Card for the ALICE Run2 Upgrade	ENGEL, Heiko
17:22	[151] FPGA-based, radiation-tolerant on-detector electronics for the upgrade of the LHCb Outer Tracker Detector	VINK, Wilco
17:23	[140] Use of FPGA Embedded Processors for Fast Cluster Reconstruction in the NA62 Liquid Krypton Electromagnetic Calorimeter	DE SIMONE, Nicola
17:34	[15] Metrics and Methods for TTC-PON System Characterization	KOLOTOUROS, Dimitrios Marios
17:35	[90] A New High-Speed Optical Transceiver For Data Transmission at the LHC Experiments	PARAMONOV, Alexander
17:36	[133] Optical Fibre at HL-LHC	HUFFMAN, Todd Brian
17:37	[162] A Small-Footprint, Dual-Channel Optical Transmitter for the High-Luminosity LHC (HL-LHC) Experiments	LIU, Chonghan
17:38	[194] Neutron Irradiation of Optoelectronic Components for HL-LHC Data Transmission Links	SEIF EL NASR, Sarah
17:39	[199] A Fast UV-LED QRdriver for Calibration System for SiPM Based Scintillator HCAL Detector	POLAK, Ivo
17:50	[67] Developments on DC/DC converters for the LHC experiment upgrades	LANZA, Agostino

17:51	[85] A DC-DC Conversion Powering Scheme for the CMS Phase-1 Pixel Upgrade	KARPINSKI, Waclaw
17:52	[45] Quality Assurance and Functionality Tests on Electrical Components during the ATLAS IBL Production	BASSALAT, Ahmed
18:00	[6] Single-event upset tests on the readout electronics for the pixel detectors of the PANDA experiment.	MAZZA, Giovanni
18:01	[83] Longevity of CMS ECAL Electronics	BARTOLONI, Alessandro
18:02	[132] Radiation tolerance tests of SRAM-based FPGAs for the possible usage in the readout electronics for the LHCb experiment.	FAERBER, Christian
18:11	[8] Acquisition and control command system for power pulsed detectors	MAGNIETTE, Frederic Bruno
18:12	[46] DEPFET active pixel sensors for the vertex detector of the Belle-II experiment	ESPERANTE PEREIRA, Daniel
18:13	[91] The management of large cabling campaigns during the Long Shutdown 1 of LHC.	MEROLI, Stefano
18:14	[92] An Ultra-Fast Data Acquisition System for Coherent Synchrotron Radiation with YBCO Terahertz Detectors	CASELLE, Michele
18:15	[120] The sROD Module for the ATLAS Tile Calorimeter Phase-2 Upgrade Demonstrator	MORENO, Pablo
18:16	[142] Front end strategy for the daq system of a Kinetic inductance detector	MARCHETTI, Dedalo
18:17	[156] The LHCb Muon Upgrade	CARDINI, Alessandro
18:18	[160] Development of the readout system for Triple-GEM detectors for the CMS forward muon upgrade	LENZI, Thomas
18:19	[183] A new approach to interfacing on-detector electronics	LEVINSON, Lorne
18:20	[187] Development of Precision Time-Of-Flight Electronics for LHCb TORCH	GAO, Rui
18:25	[1] Upgrade of the Muon Sorter in the Cathode Strip Chamber Level 1 Trigger System at CMS	MATVEEV, Mikhail
18:26	[110] A Full Mesh ATCA-based General Purpose Data Processing Board	OLSEN, Jamieson
18:27	[112] Development of a digital trigger system to identify recoil protons at COMPASS-II	GORZELLIK, Matthias
18:28	[200] NaNet: a flexible and configurable low-latency NIC for real-time trigger systems based on GPUs.	LONARDO, Alessandro

Wednesday 25 September 2013

Poster: Second part (16:35 - 18:30)

-Conveners: Mitchell Franck Newcomer

time	[id] title	presenter
16:35	[63] SALT - new silicon strip readout chip for the LHCb Upgrade	SWIENTEK, Krzysztof Piotr
16:36	[180] Digital Column Readout Architectures for Hybrid Pixel Detector Readout Chips	POIKELA, Tuomas Sakari
16:37	[7] The eCDR, a Radiation-Hard 40/80/160/320 Mbit/s CDR with internal VCO frequency calibration and 195 ps programmable phase resolution in 130 nm CMOS	TAVERNIER, Filip Francis
16:38	[188] Characterization results and first applications of KLauS - an ASIC for SiPM charge and fast discrimination readout	HARION, Tobias
16:39	[145] FEERIC, a very-front-end ASIC for the ALICE Muon Trigger Resistive Plate Chambers	MANEN, Samuel Pierre
16:41	[108] Prototype pixel detector in the SOI technology	KAPUSTA, Piotr
16:42	[102] Development of New Front-end Electronics for the Upgrade of the ATLAS Muon Drift Tube Chambers at High LHC Luminosity	SCHWEGLER, Philipp
16:43	[12] VIPRAM – 2D Prototype and 3D Design	HOFF, Jim
16:44	[55] Design and characterization of a GAPD pixel detector prototype for future particle trackers	VILELLA-FIGUERAS, Eva
16:55	[27] TRB3 264 Channel High Precision TDC Platform and Its Applications	NEISER, Andreas
16:58	[125] Design of a deterministic link initialization mechanism for serial LVDS interconnects	SCHATRAL, Sven
17:09	[106] The optical link system in the Upgrade project of the Drift Tubes electronics in CMS	DE REMIGIS, Paolo
17:10	[191] Evaluation of 400m, 5Gbit Versatile Link lengths over OM3 and OM4 fibres for the LHCb upgrade	SCHWEMMER, Rainer
17:11	[163] The 120Gbps VCSEL array based optical transmitter (ATx) development for the High-Luminosity LHC (HL-LHC) experiments	YE, Jingbo
17:12	[201] Versatile Transceiver and Transmitter Production Status	TROSKA, Jan
17:13	[109] DTCC, a Point-to-Point Link for Data, Trigger, Clock and Control over Copper or Fiber	TARAZONA MARTINEZ, Alfonso
17:24	[43] The high voltage power supplies of the CREAM experiement	ERAUD, Ludovic
17:25	[59] Pulsed power distribution for power supply isolation and remote 2-wire point-of-load regulation for the ATLAS Pixel Detector	HASIB, A A
17:36	[97] The new NA62 LKr readout: first tests and future perspectives	VENDITTI, Stefano
17:37	[101] System Level and Production Tests of the CMS HCAL QIE10	DRAKE, Gary
17:49	[11] Consolidation of the radiation tolerant programmable power supply cards for the LHC beam screen heaters	TRIKOUPIS, Nikolaos
17:51	[60] Single event upsets in the readout control FPGA of the ALICE TPC detector during the first LHC running period	ALME, Johan
18:01	[73] 10 Order of OF Magnitude Current Measurement Digitizers for the CERN Beam Loss Systems.	VIGANO, William

18:02	[179] ATLAS Diamond Beam Monitor	CERV, Matevz
18:03	[81] Mitigation of Radiation and EMI effects on the Vacuum Control System of LHC	PIGNY, Gregory
18:04	[119] Design of an FPGA-based embedded system for the ATLAS Tile Calorimeter front-end electronics test-bench	CARRIO ARGOS, Fernando
18:05	[189] The AMC13XG: A New Generation Clock/Timing/DAQ Module for CMS MicroTCA	HAZEN, Eric Shearer
18:06	[144] Simulation of ATLAS SCT module response to LHC beam loss scenarios	ROSE, Peyton
18:07	[148] The readout electronic of EUSO-Balloon experiment	CACERES, Thierry
18:08	[94] Performance evaluation of multiple (16 channels) sub-nanosecond TDC implemented in low-cost FPGA	KONSTANTINOU, Georgios
18:09	[169] The upgrade of the LHCb calorimeter	MAURICIO FERRE, Juan
18:20	[157] Common control and readout board for the Calorimeter and Tracker Front-end electronics of the SuperNEMO experiment.	CACERES, Thierry
18:21	[5] Simulation of the ATLAS sTGC trigger for the Phase-I new small wheel detector upgrade	CHAPMAN, Jay
18:22	[174] The CMS Global Muon Trigger upgrade	RABADY, Dinyar