EIROforum Science-Business WAMAS Workshop on Advanced Materials and surface

SESSION I - SURFACE SCIENCE: Part II

Polyimide anisotropic chemical etching

CERN TE/MPE/EM section

Summary

- Novel Polyimide etching process
  - description
- Applications
  - HDI circuits
  - GEMs
  - Embedded silicon circuits

Some well known brand names for Polyimide:
KAPTON from Dupont de Nemours
APICAL from KANEKA
UPILEX from UBE

Test description

Samples:

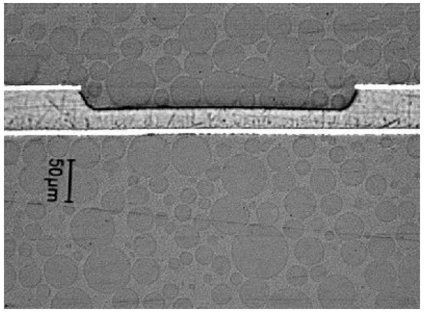
Polyimide 1 [5/50/5 um]
Polyimide 2 [5/25/5 um]
Polyimide 3 [5/25/0 um]
Polyimide 4 [25/25/25 um]

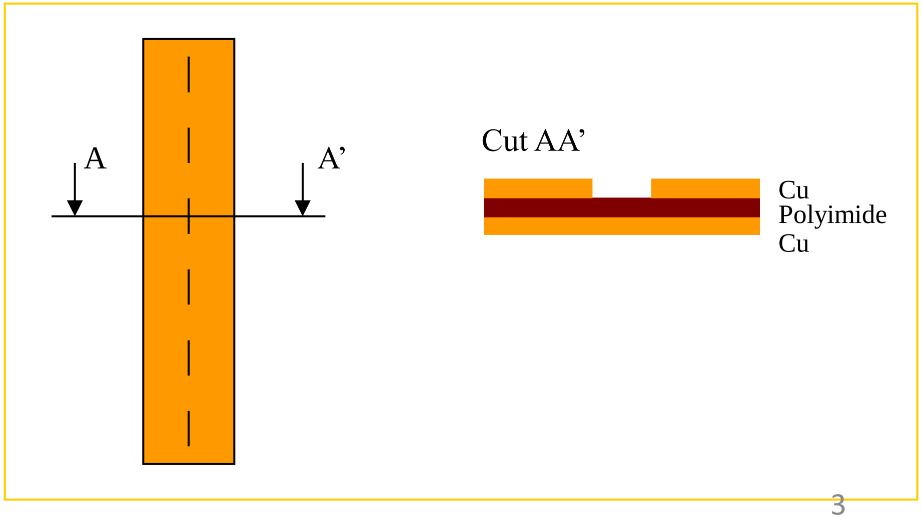
Strips used for measuring the Polyimide etching

Sample
10 cm x 1cm

Groove in Cu:
300um width

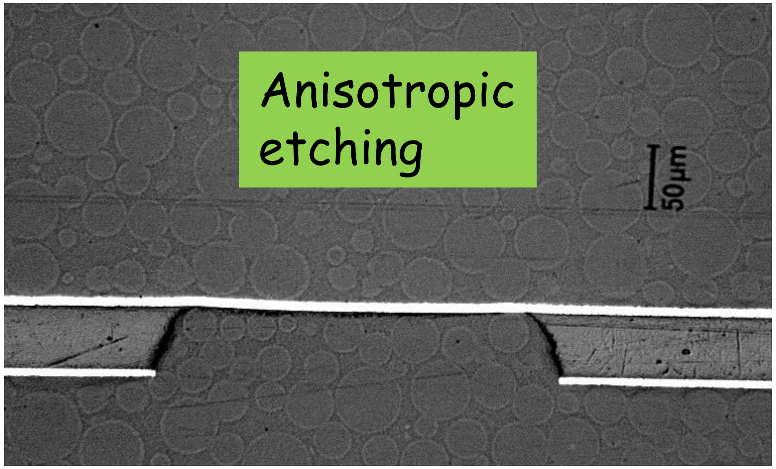
The etching of Polyimide is measured with micrographic pictures



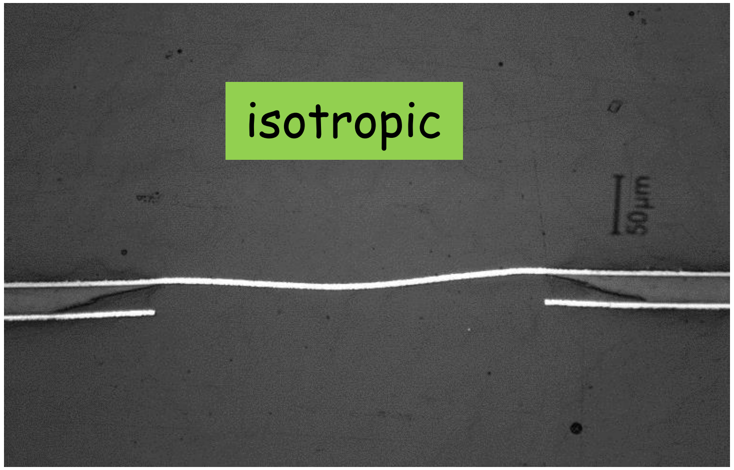


First results

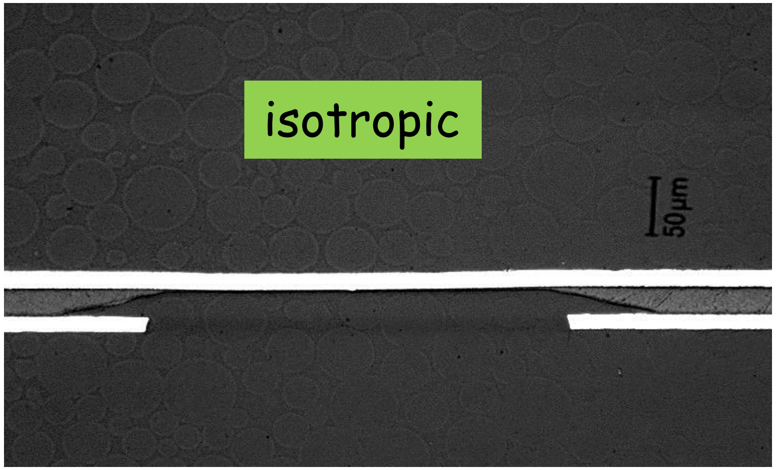
Polyimide 1 [5/50/5 um]



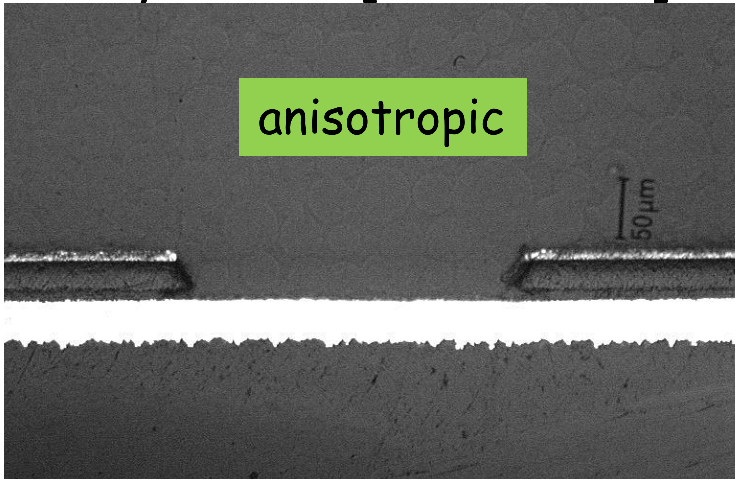
Polyimide 2 [5/25/5 um]



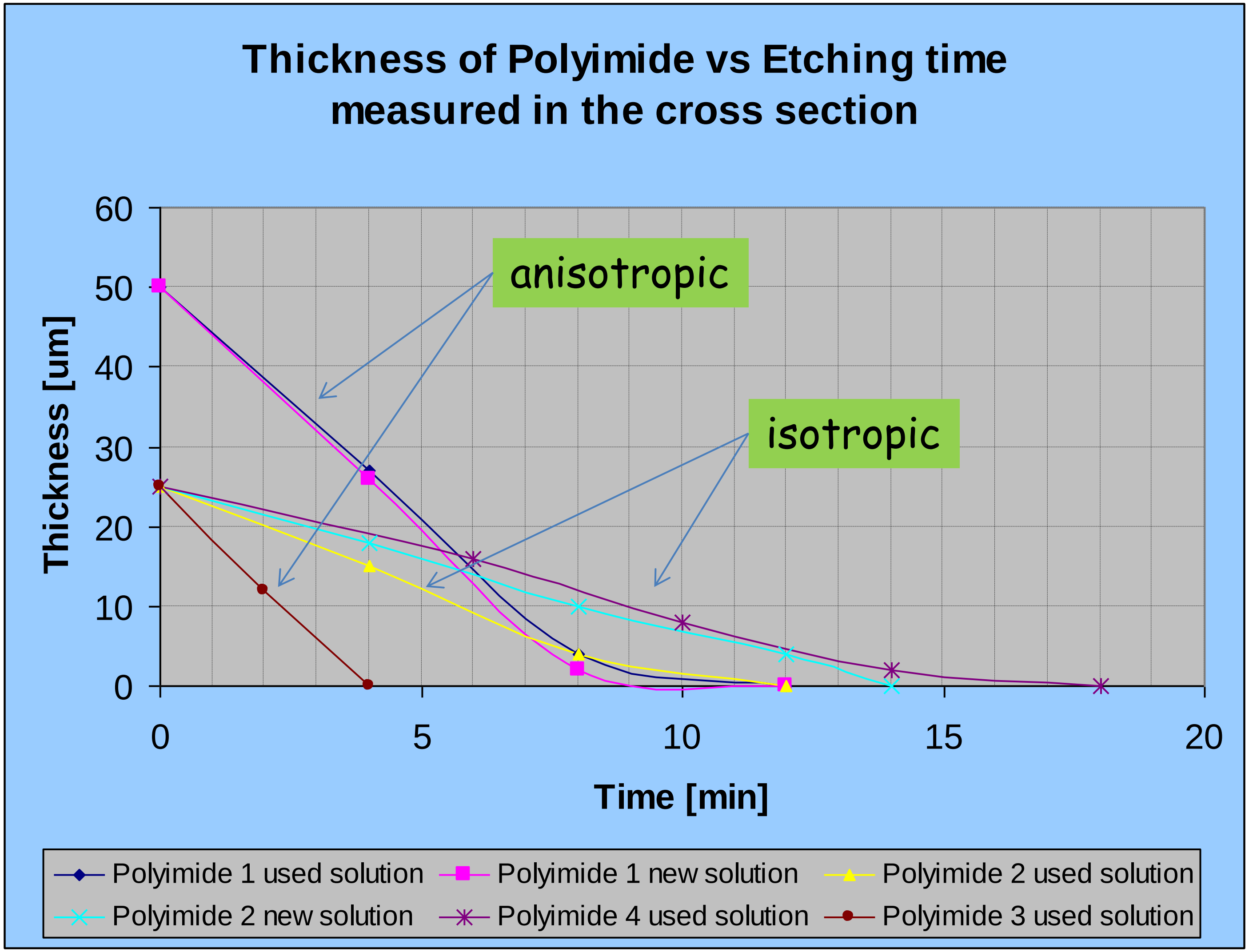
Polyimide 4 [25/25/25 um]



Polyimide 3 [5/25/0 um]

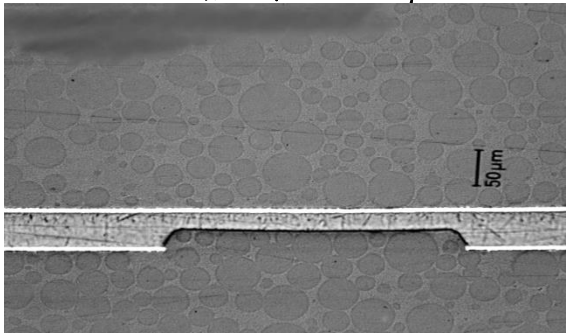


Polyimide etching

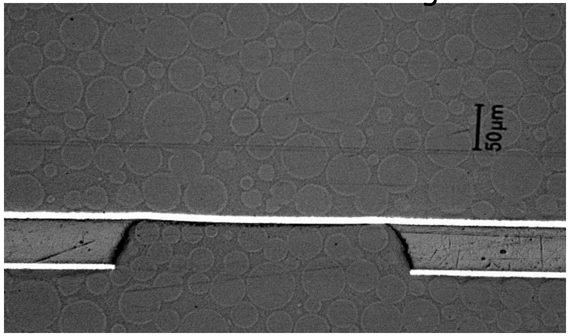


Most interesting sample : 1 [5/50/5 um]

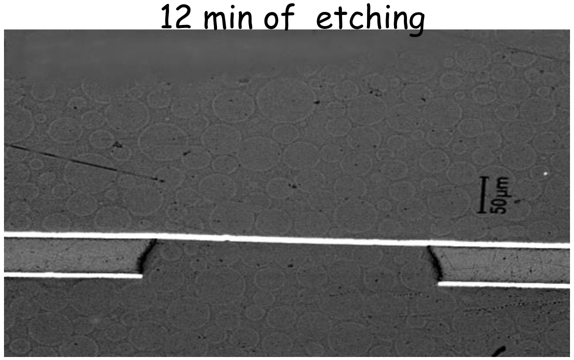
4 min of etching



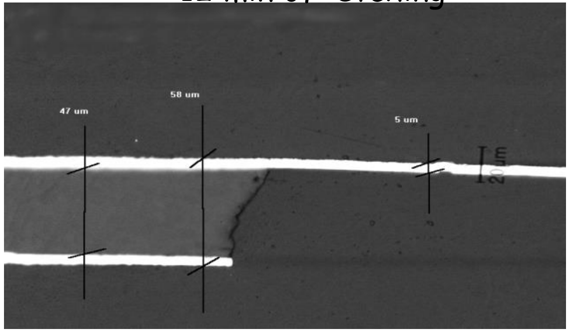
8 min of etching



12 min of etching



12 min of etching



Highly anisotropic etching
Micron level definition
Wide process window

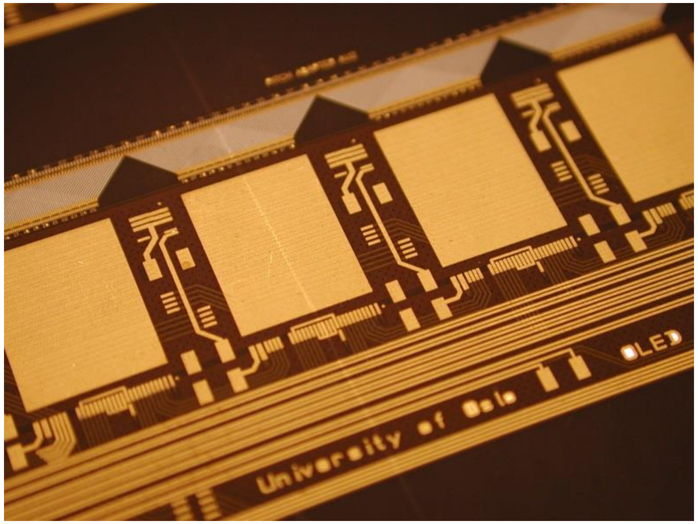
Equipment for PI etching

Polyimide etchant   Detergent   Water

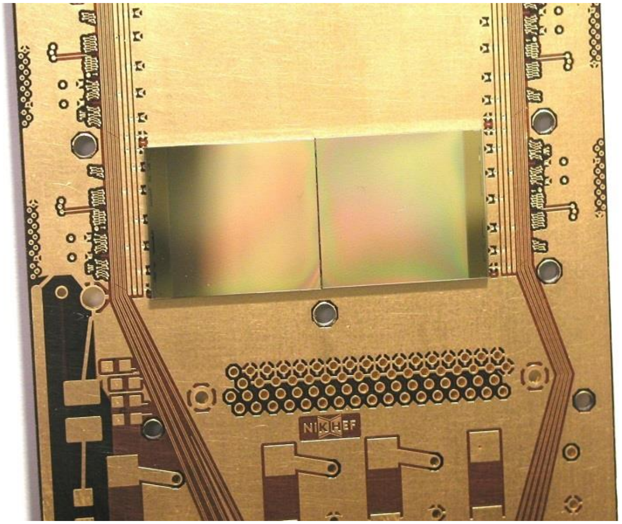
Summary

- Applications
  - HDI circuits
  - GEMs
  - Embedded silicon circuits

High Density Interconnect (HDI) circuits application

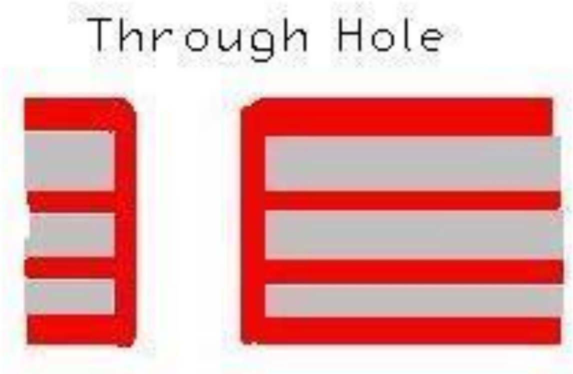


Atlas inner tracker front end module

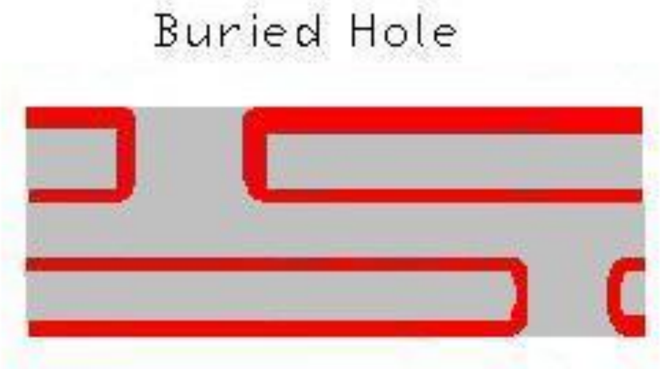


R&D Multi chip detector module

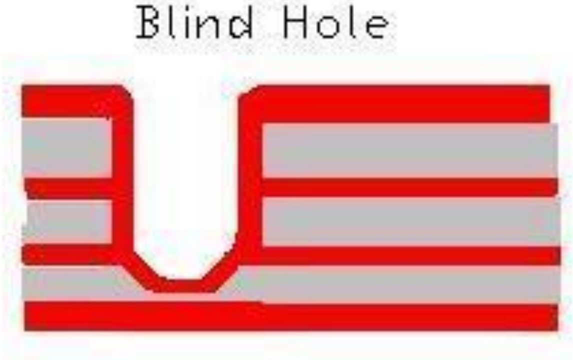
High density interconnections are limited by the PTH size (Plated Through Holes)



0.2 to 0.3mm min



0.2 to 0.3mm min



0.2 to 0.3mm min

15um min

HDI applications

High density circuits

Portable PCs
Mobile phones
Cameras

-High volume
-High R&D cost
-Mass production Driven
-Main players are defining machines & technologies

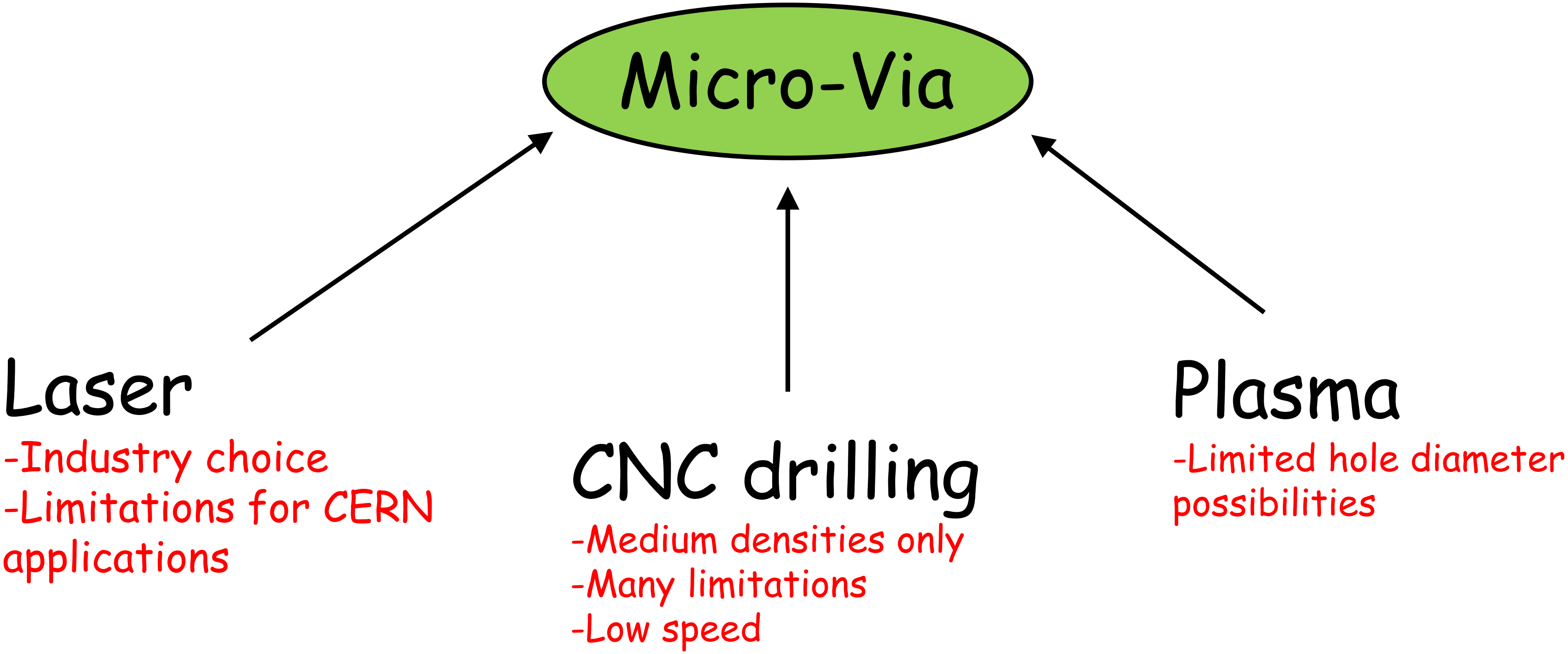
Industrial Applications

-Low to Medium volume
-Using High volume available techniques
-No R&D possible
-No possibility to influence main players choices

CERN inner tracker front end Electronics

-Low volume
-Very Special features
-CERN can't influence Main players choices

Micro-via processes existing in industry



Micro-Via

Laser

-Industry choice
-Limitations for CERN applications

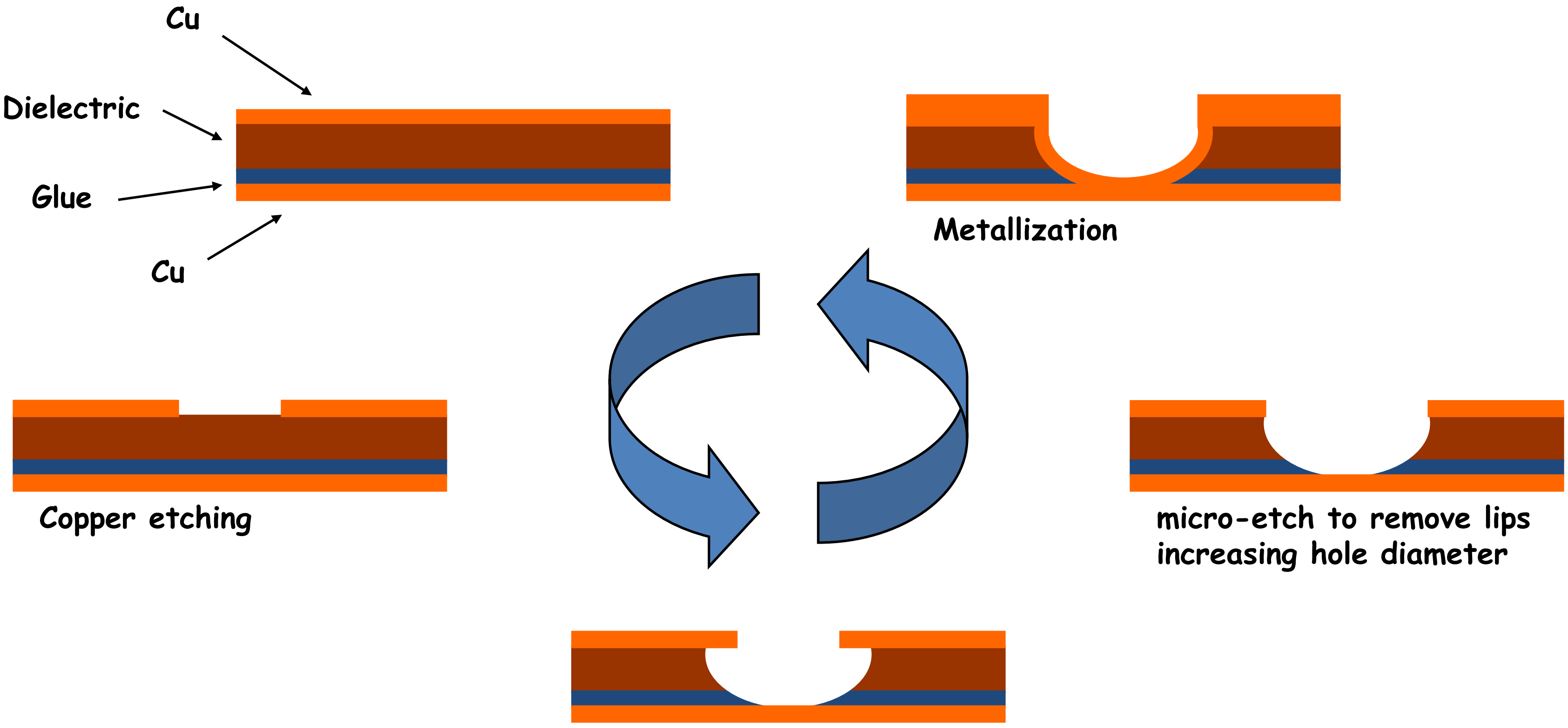
CNC drilling

-Medium densities only
-Many limitations
-Low speed

Plasma

-Limited hole diameter possibilities

Plasma



Metallization

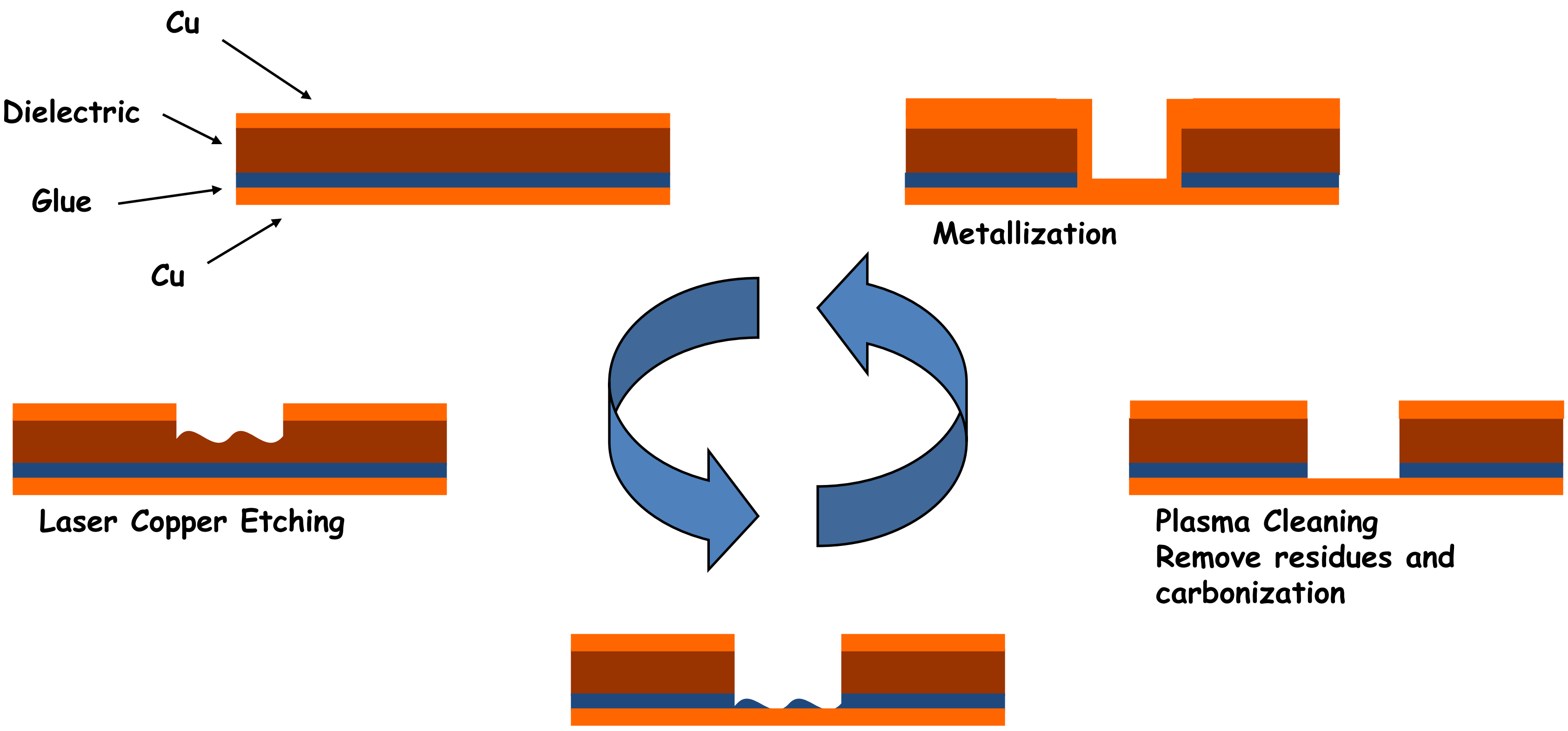
Copper etching

micro-etch to remove lips
increasing hole diameter

Plasma Etching
Highly Isotropic
Creating lips

Minimal Via diameter ≈ 120 um
At the edge of being considered as a micro-via

Laser (Industry preferred technique)



Laser Copper Etching

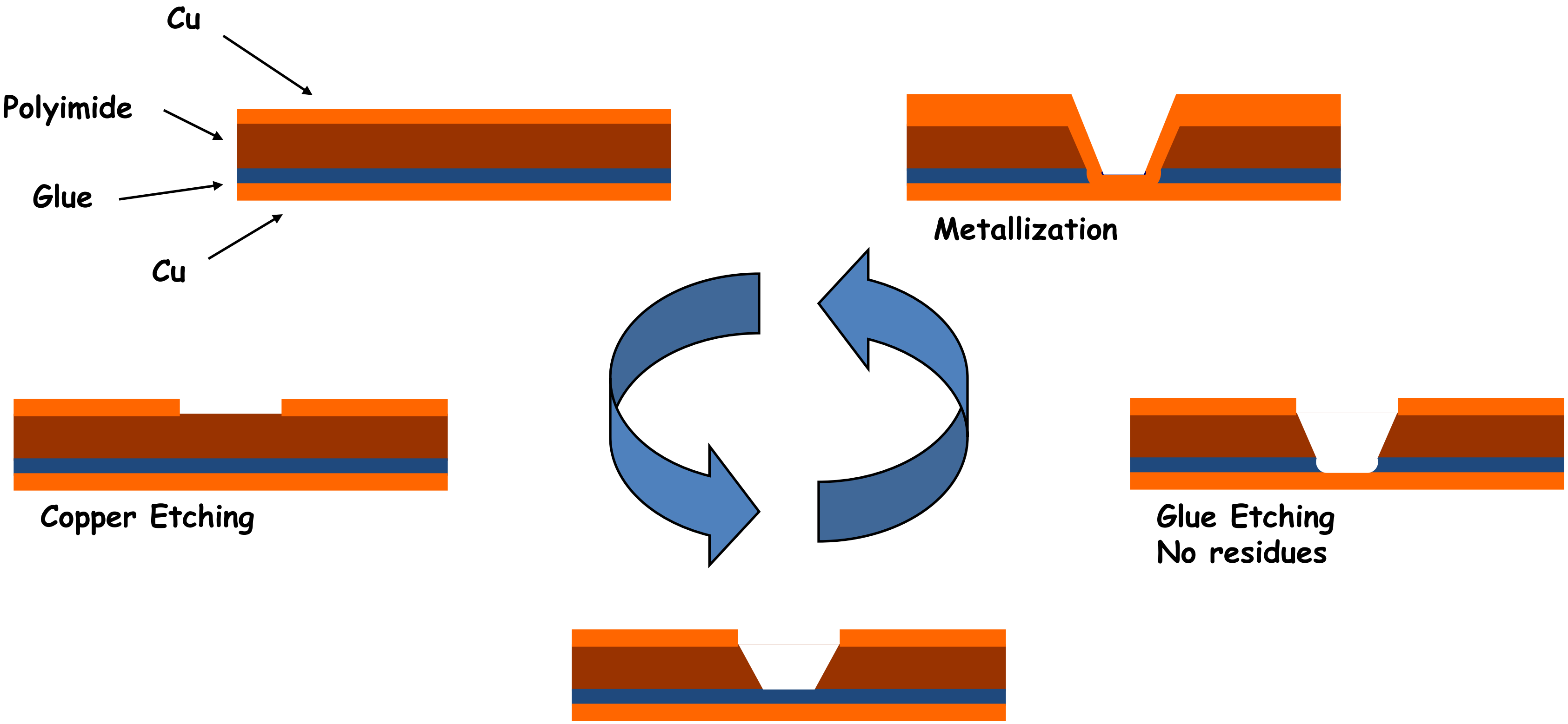
Dielectric Laser Ablation
Highly anisotropic
Can make the plating difficult
Needs thick metal to stop laser

Plasma Cleaning
Remove residues and
carbonization

Metallization

Minimal Via diameter ≈ 40 um

Chemical PI etching



Copper Etching

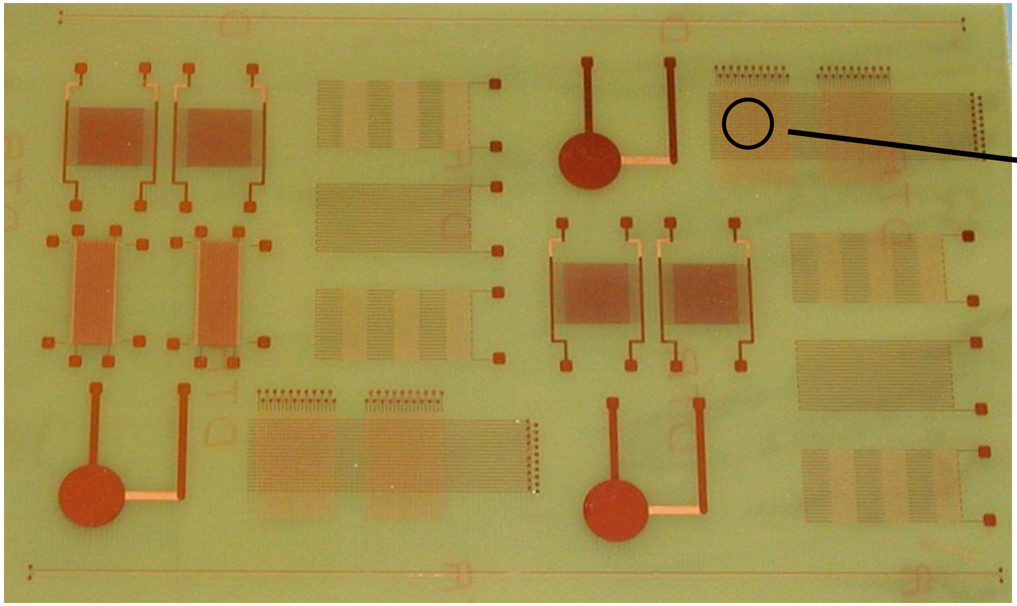
PI Etching
Anisotropic etching with an angle
No residues
Perfect for plating

Glue Etching
No residues

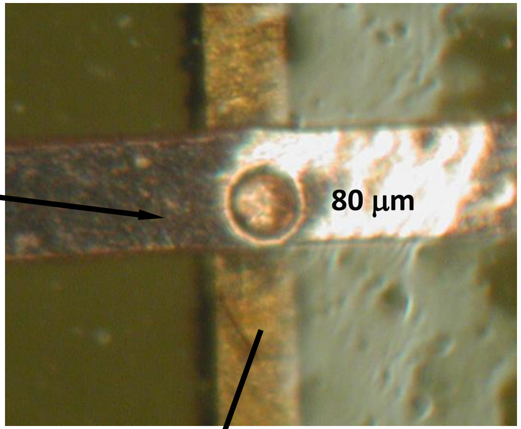
Metallization

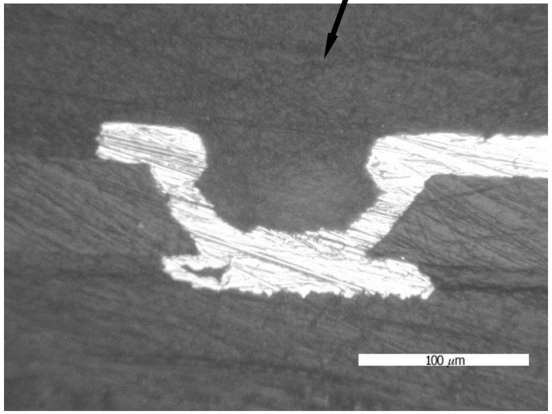
Minimal Via diameter ≈ 15 um

Chemical micro-via



Test board to qualify the technology

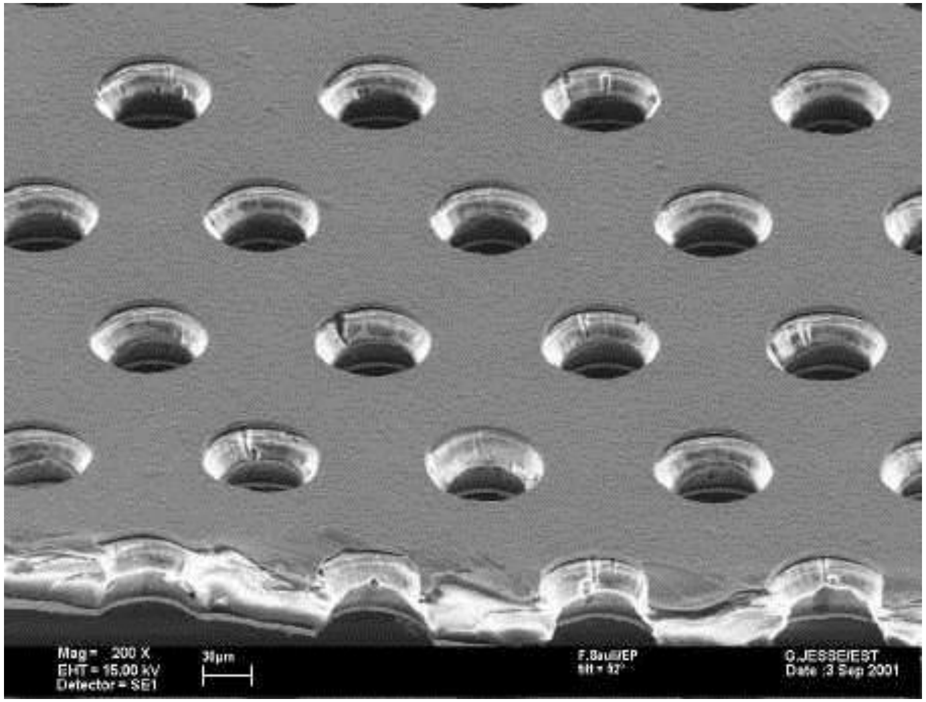




Why Chemical micro-via in HDI circuits:

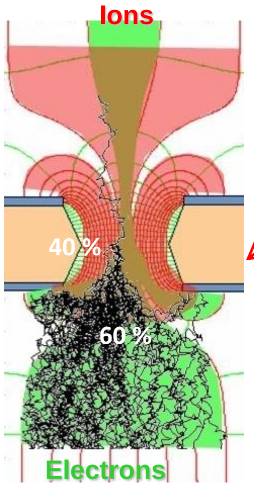
- Advantages
  - Highest connection density
  - Best hole definition
  - Low R&D cost
  - Low production equipment cost
    - CERN set up < 100 KCHF
    - laser + plasma > 800KCHf
  - Low maintenance cost
    - CERN set up→ chemistry cost
    - Laser → 10% of the equipment cost/year
- Disadvantages
  - Only Adhesive-less metal vacuum deposited cladded polyimide

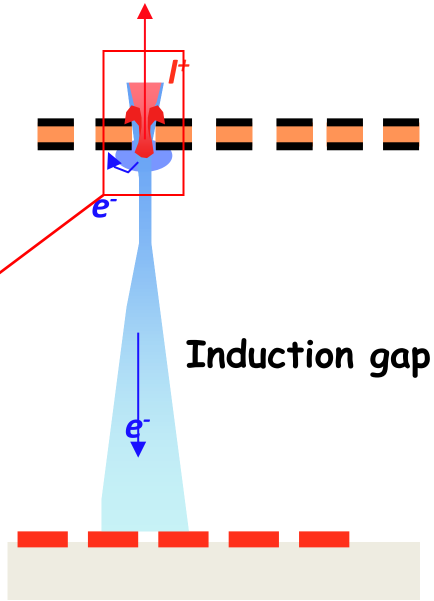
Gas electron multiplier (GEM) application

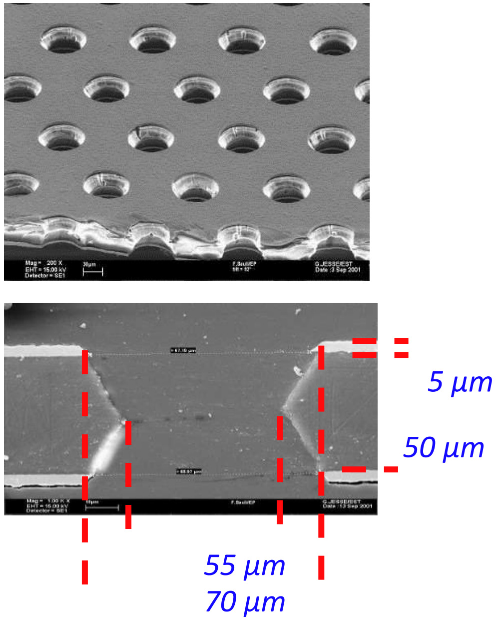


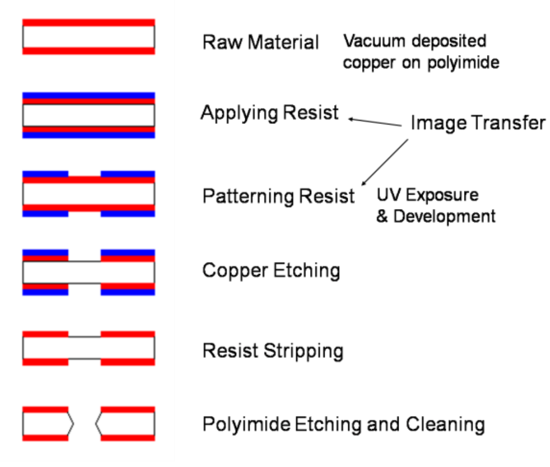
50um thick GEM SEM picture

GEM









Raw Material — Vacuum deposited copper on polyimide

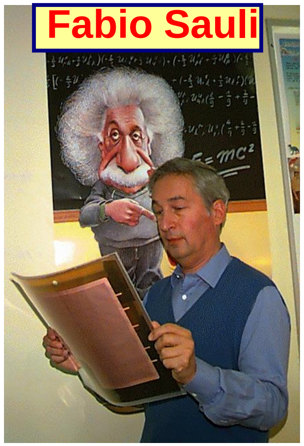
Applying Resist ← Image Transfer

Patterning Resist ← UV Exposure & Development

Copper Etching

Resist Stripping

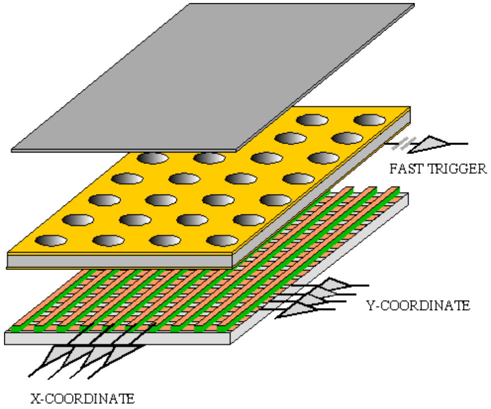
Polyimide Etching and Cleaning



Thin, metal coated polyimide foil perforated
with high density micron level accuracy holes pattern .

Electrons are collected on a patterned readout board.
A fast signal can be detected on the lower GEM electrode
for triggering or energy discrimination.
All readout electrodes are at ground potential.
Positive ions partially collected on the GEM electrodes.

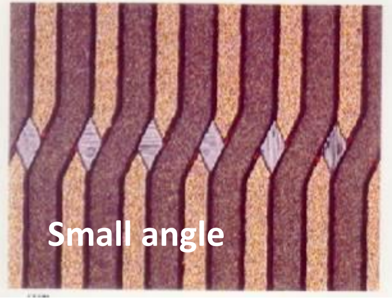
GEM detector

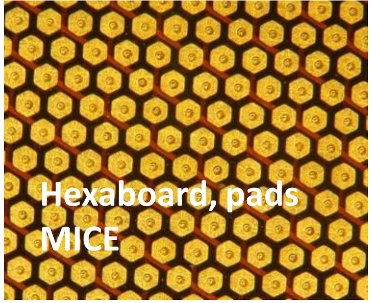


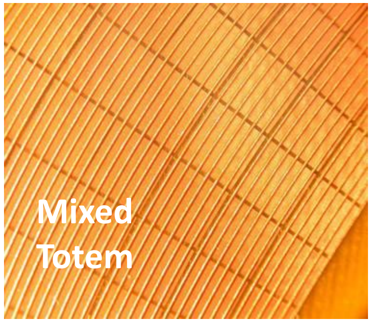
A. Bressan et al, Nucl. Instr. and Meth. A425(1999)254

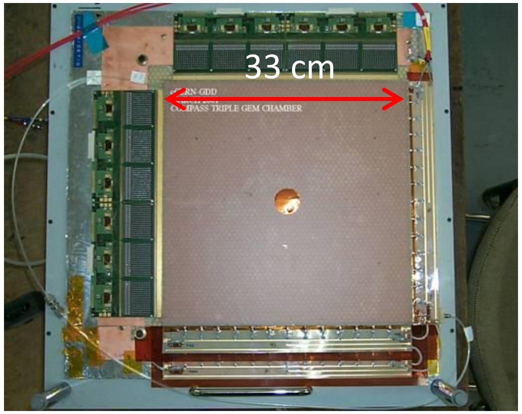
Full decoupling of the charge amplification structure from the charge collection board.

Both structures can be optimized independently !







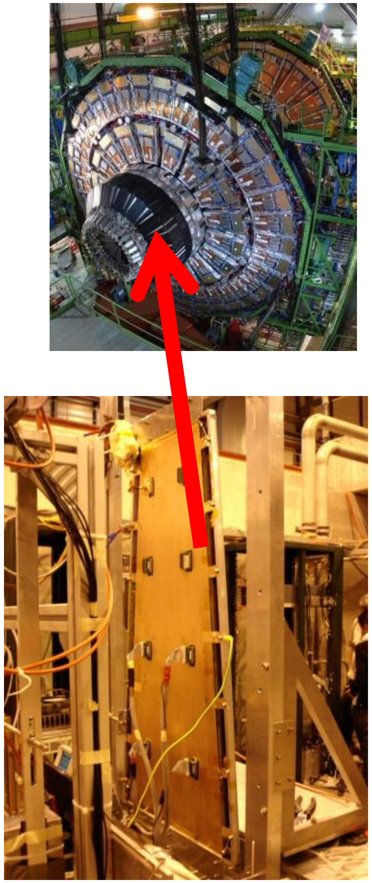


Compass

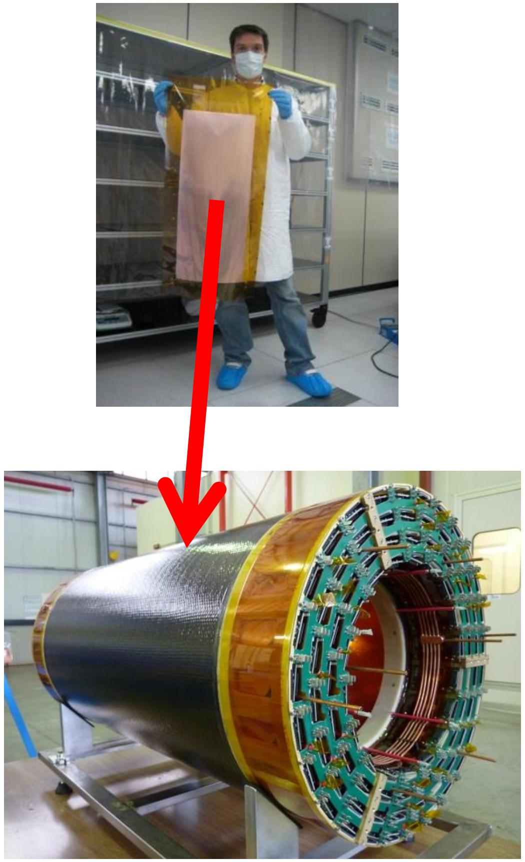
Totem

Both detectors use three GEM foils in cascade for amplification to reduce discharge probability by reducing field strength.

GEM detectors :planar & cylindrical



- GEM 1.1m x 500mm
- CMS GEM detector GE1/1



- KLOE – Cylindrical 3 GEM Detector
- GEM 800mm x 500mm
- Read-out 2D : 800mmx 500mm

Why Chemical micro-via in GEM ?

- One GEM needs up to 1x10^8 holes in a foil (1m x 0.5m)
- 8 min process with chemical process
- 138 hours with a modern laser (200Holes/sec).
  - And still hole shape and carbonisation problems
- Not possible with the other techniques.
  - Hole too large with plasma (min 120um)
  - 3 years to drill one foil with a CNC machine (1 hole/sec)

Embedded silicon circuits application

CERN needs special circuits near interaction points:

- -Low mass to avoid multiple scattering
- -Radiation hard , Long term reliability
- -High density of interconnection

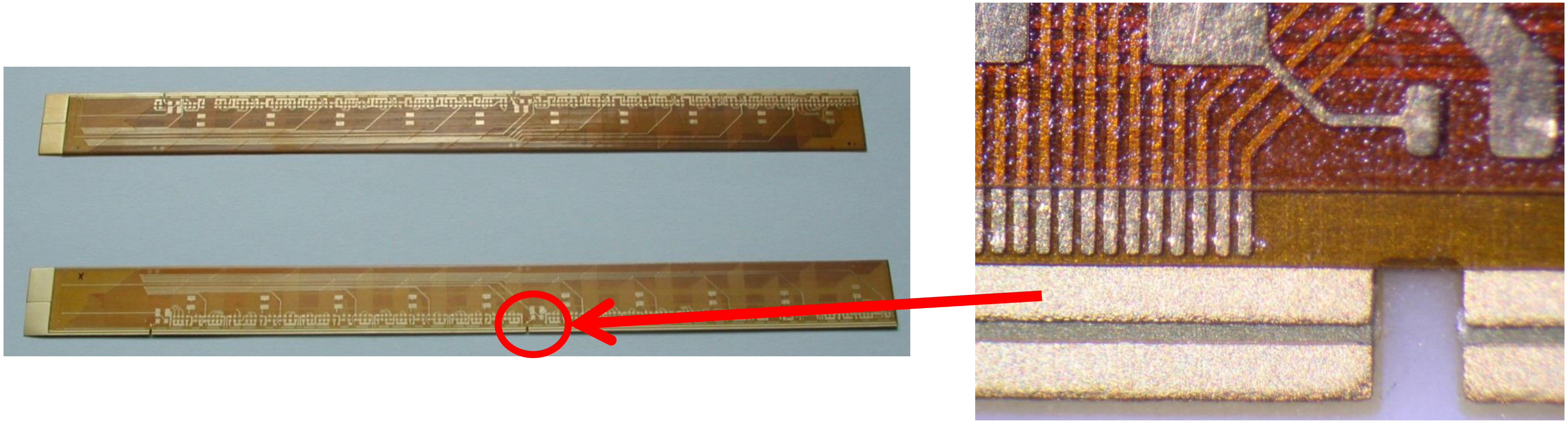
Ex: CMOS pixel detector embedded in Polyimide flex

Low mass aspect

Material	Radiation length [cm]	Density [gr/cc]	Resistivity [uohms*cm]
Gold	0.3	19.3	2.4
Copper	1.4	9.0	1.7
Aluminum	8.9	2.7	2.7
Glass epoxy	19.4		
Polyimide	29.0		
Beryllium	35.3	1.9	3.3

Copper is close to 6.5 times less transparent than aluminum
And aluminum has only 1.6 times the resistivity of copper
Polyimide is 1.5 times better than glass epoxy.

5 Al layers ALICE Pixel Bus



Via : 100um
5 Aluminum layers
10um Vacuum deposited aluminum for signals
50um laminated aluminum layer for power
100um line and 50um space
12um polyimide layers
Size 160mm x 16mm
Staircase shape on one side for bonding

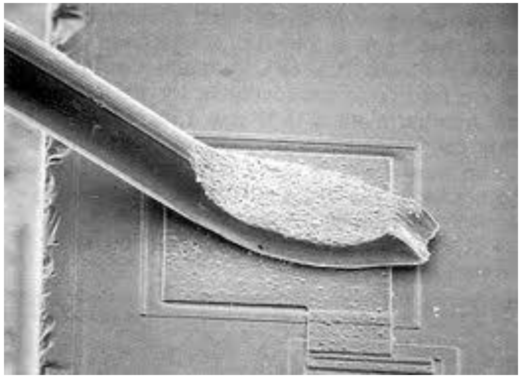
Full Aluminium circuit: Multiple scattering solved

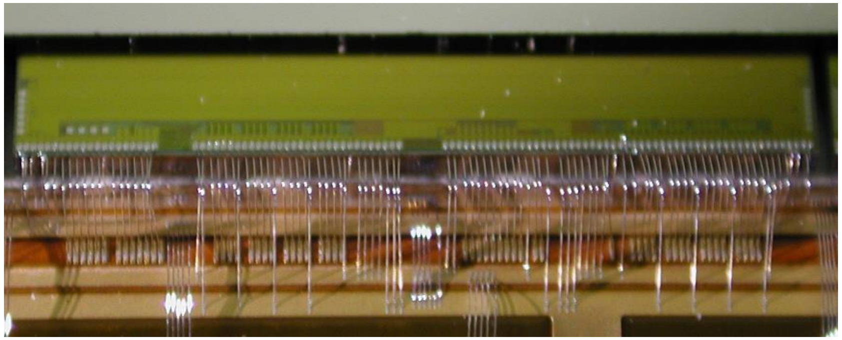
8 layer ATLAS IBL Al/Cu mixed multilayer

Via min : 300um
5 Copper signal layers
2 x50um laminated aluminum layer for power
70um line and 50um space
25um polyimide layers
Pure epoxy gluing
Size 400mm x 20mm
200 to 300 Mrad compatible

Only pure epoxy and PI: Radiation damage solved

Usual Chip to flex electrical connection technique: → wire bonding





2 to 3mm
Dead zone

Peripheral connection introducing dead zones
Needs mechanical and humidity protection (AL/Au glob top)

Conventional Bonding limits the density and needs protection.
Multiple scattering problem is solved
Radiation problem is solved

↓

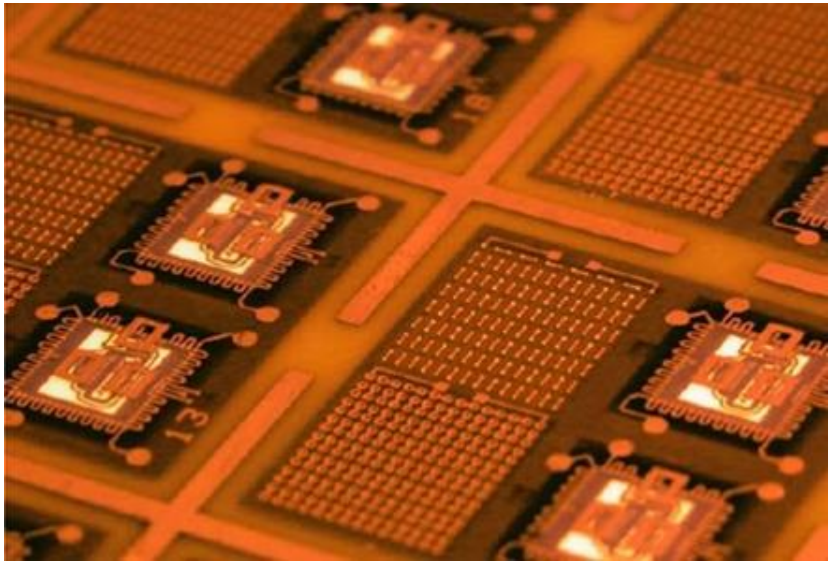
Embedding the silicon chip in a special HDI flex:

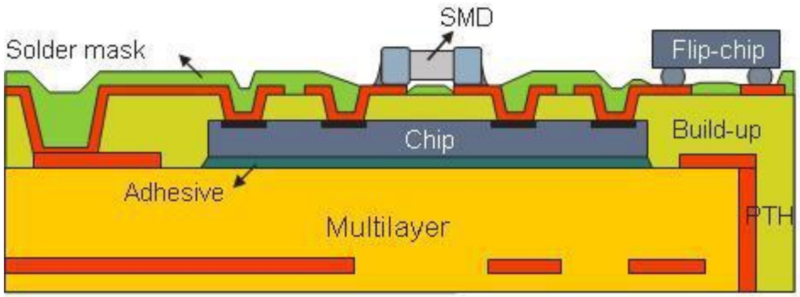
-Remove bonding and use micro-via for connections

-Use PI dielectric and epoxy glue for their resistance to radiations

-Use Aluminum tracks to limit multiple scattering

Embedded Chip situation in industry





Laser micro-via
100um via
Copper strips

Problems:

Thick copper pads on chip (15um) to avoid laser damage during drilling.

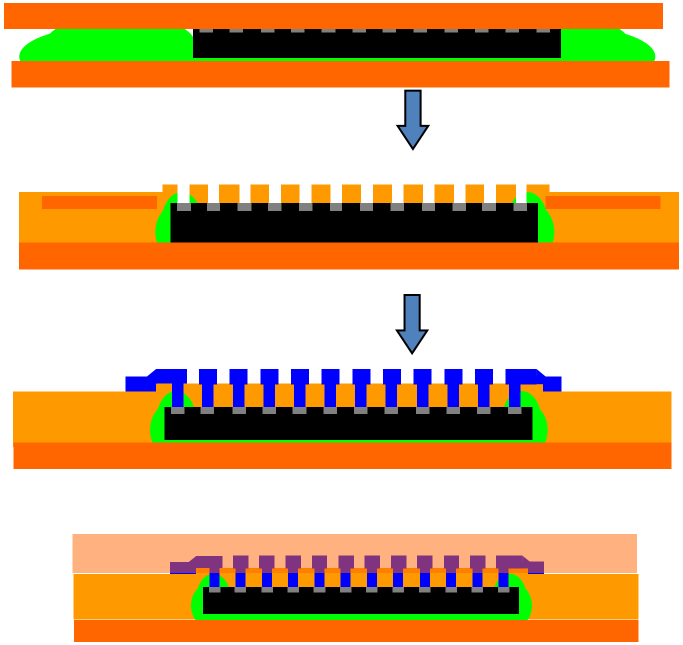
Wafer level post processing needed (large volume only).

Prohibitive R&D cost.

Only Copper system available in industry.

CERN needs Aluminum strips.

CERN chip embedding principle



Chip Gluing between two Polyimide foils

Standard aluminum pads on the chip

Creating via using chemical etching (40um)

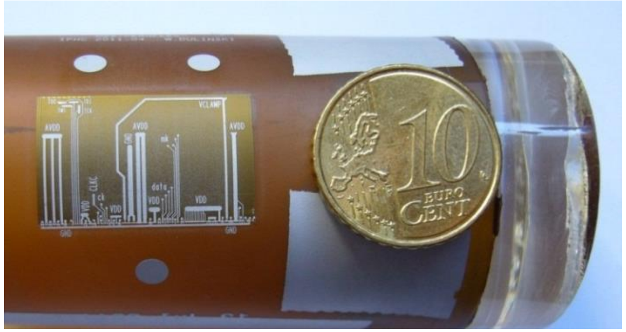
Metallization: Magnetron DC Al deposit (5-30 μm)

Lithography to pattern metal

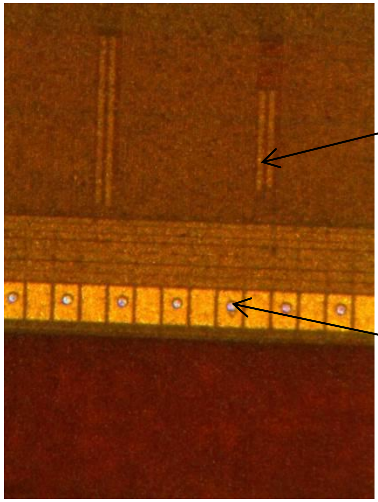
Gluing a new Polyimide layer etc…

- No possible damage of the chip during micro via creation
- No post processing of the chip needed The standard metal is sufficient

Example

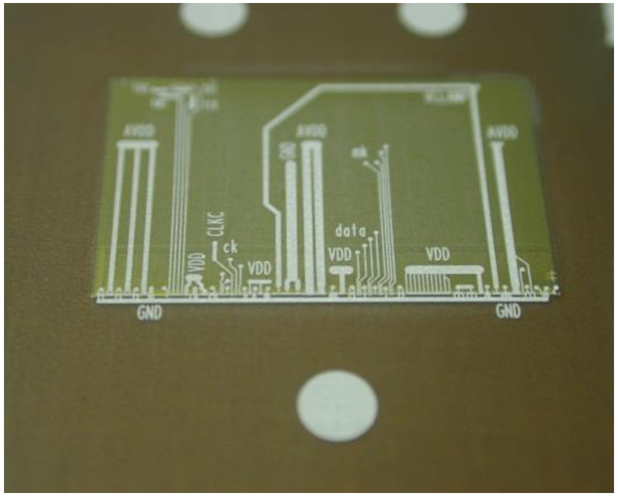


Solid state 50um silicon flexible sensor wrapped over cylindrical shape (R=20 mm)

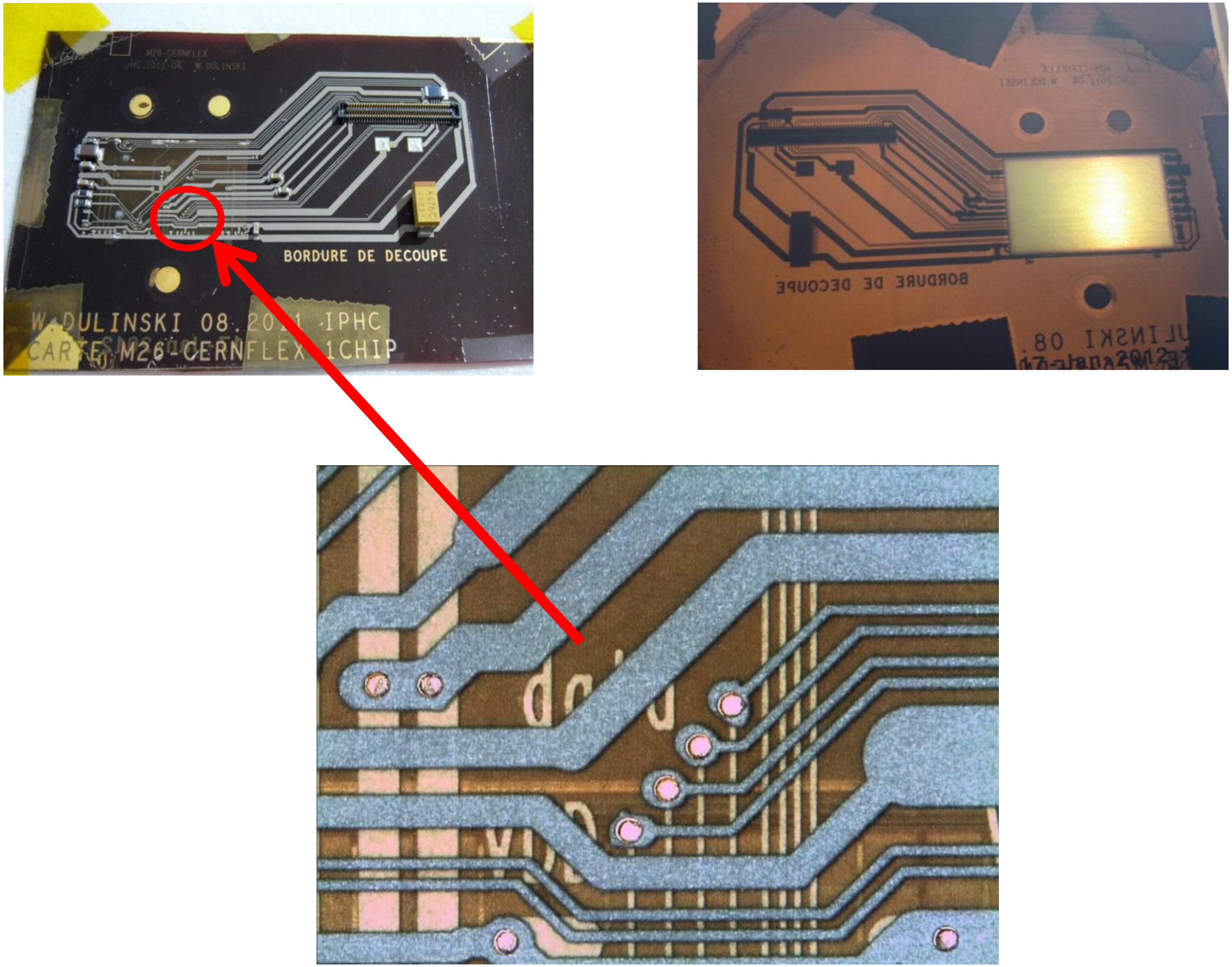


Solid state sensor embedded in Polyimide

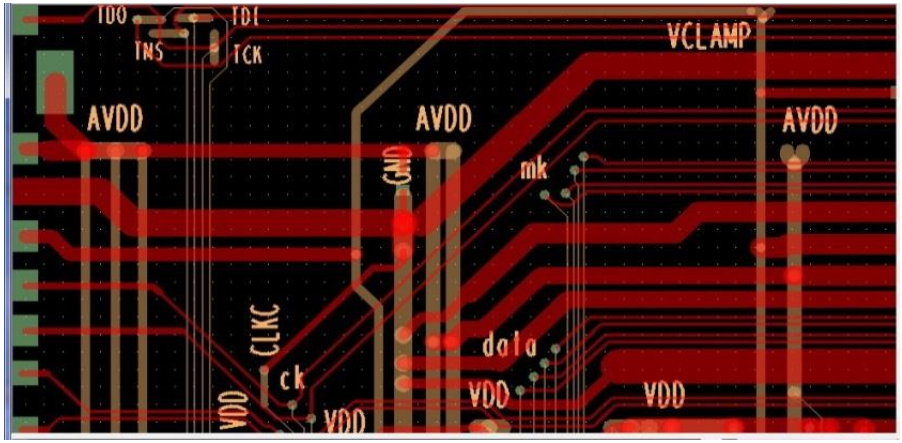
40um via
Before Al Plating
on 80um pads



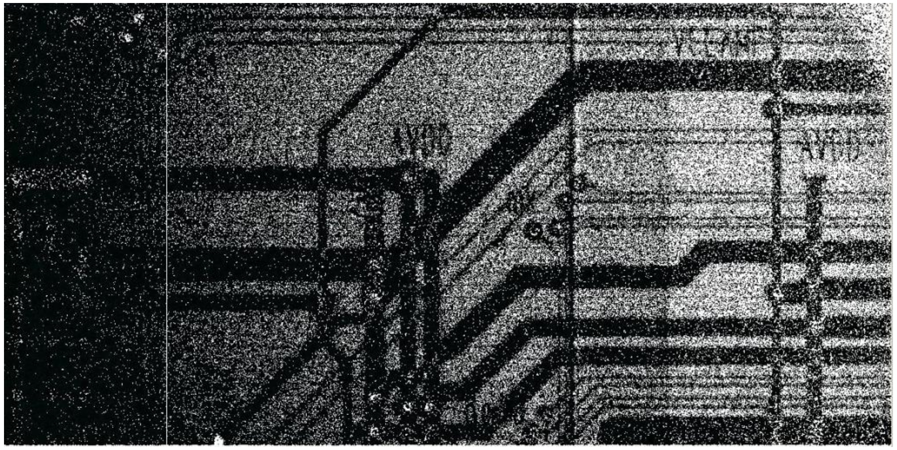
Same example with 2 aluminum layers



Auto-radiography test



Lithography details of interconnecting metal (two layers of ~10 μm thick Al) deposited on top of the pixel sensor



Auto-radiography of metal measured by pixel sensor itself using 5.9 keV Xrays (^{55}Fe)

Why Chemical Via with embedded chips:

- Advantages:
  - Low R&D cost
  - No chip post processing needed
  - Ultimate integration , no dead zones
  - PI Provides a mechanical and chemical protection
  - Low mass aluminium compatible
  - Rad hard
  - This technology closes the gap between integrated circuits and PCBs
- Disadvantages
  - No repair possible, inherent to Embedded technology

Conclusion

- The wet Polyimide etching is giving us a lot of possibilities (not all presented).
  - It as already triggered 4 patents
  - Close to 10 companies are already licensed for production
- Simple R&D set up and also good candidate for mass production.
- All the applications are not yet fully explored ex: microfluidic channels and embedded micro cooling structures.

Thank you