Software Interlock System

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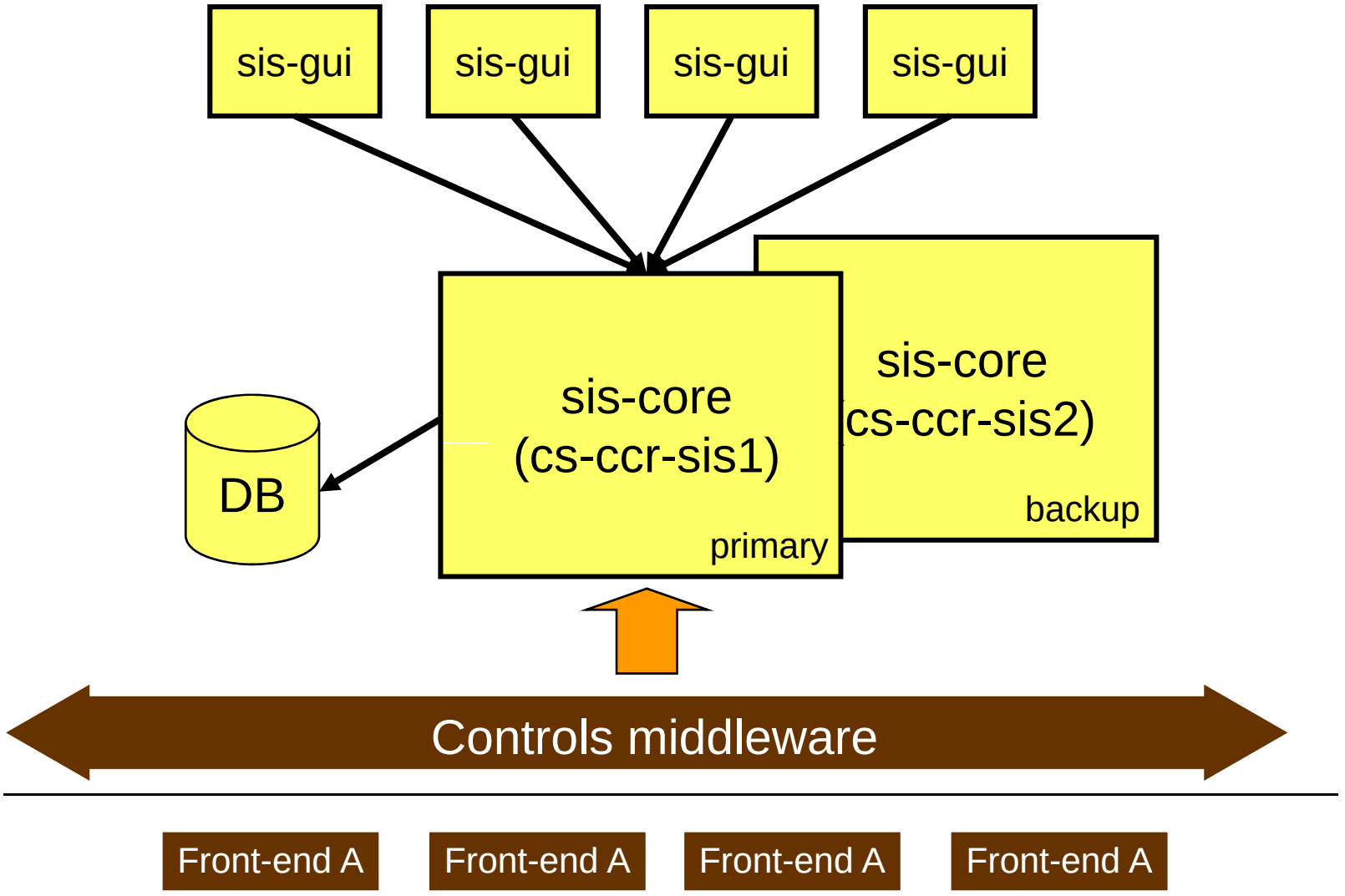
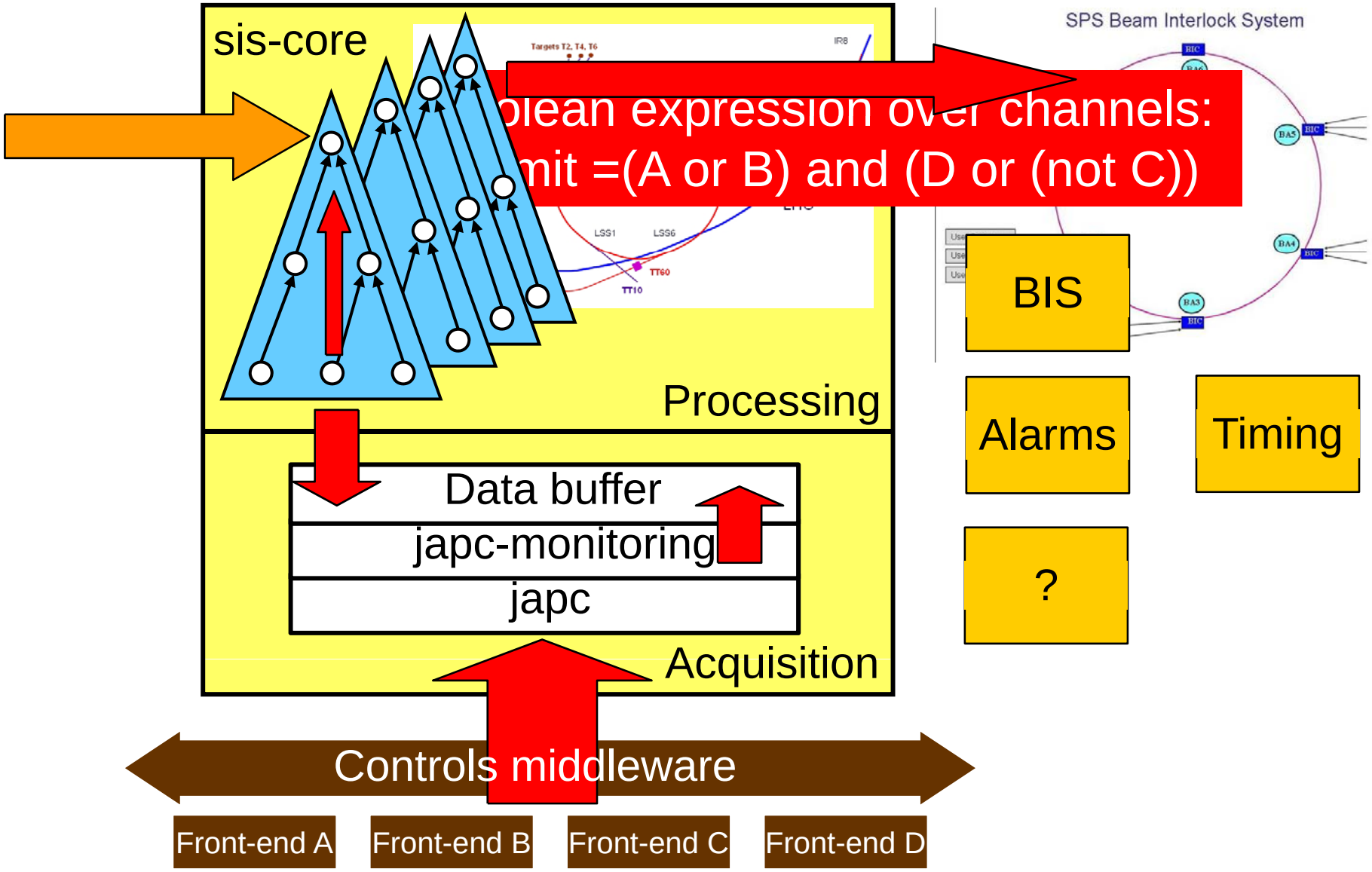
Overview

- The SIS system is a JAVA based software interlock kernel that is operational since 2007.
- Persons involved in OP :
  - J. Wenninger (project leader)
  - L. Pereira .
- Person involved in CO :J. Wozniak
- SIS acts on the beam through the SPS Beam Interlock Systems for the ring and for the LSS4 and LSS6 extraction. It also acts on the SPS MTG through dedicated inhibit signals.

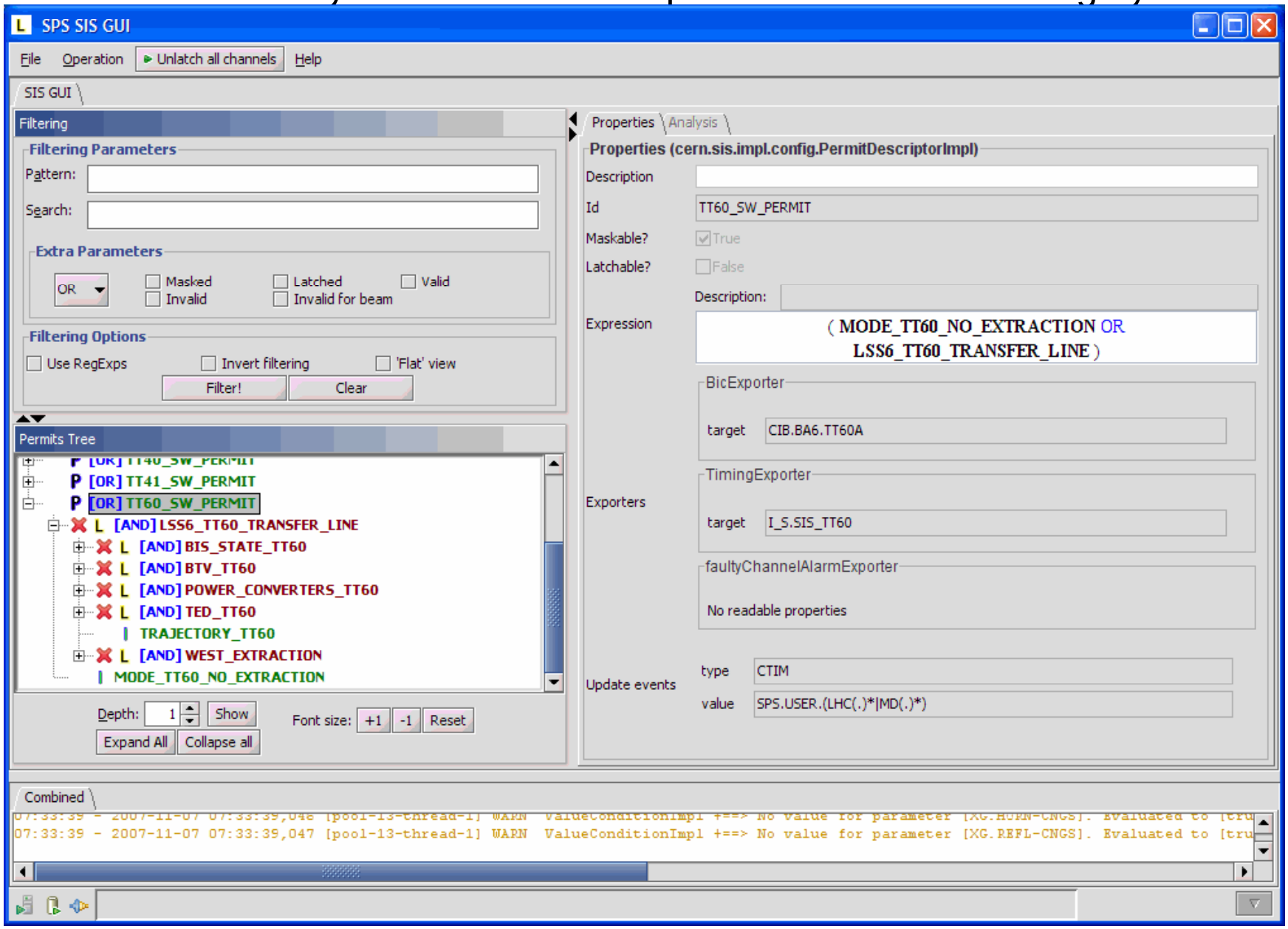
General Architecture Overview



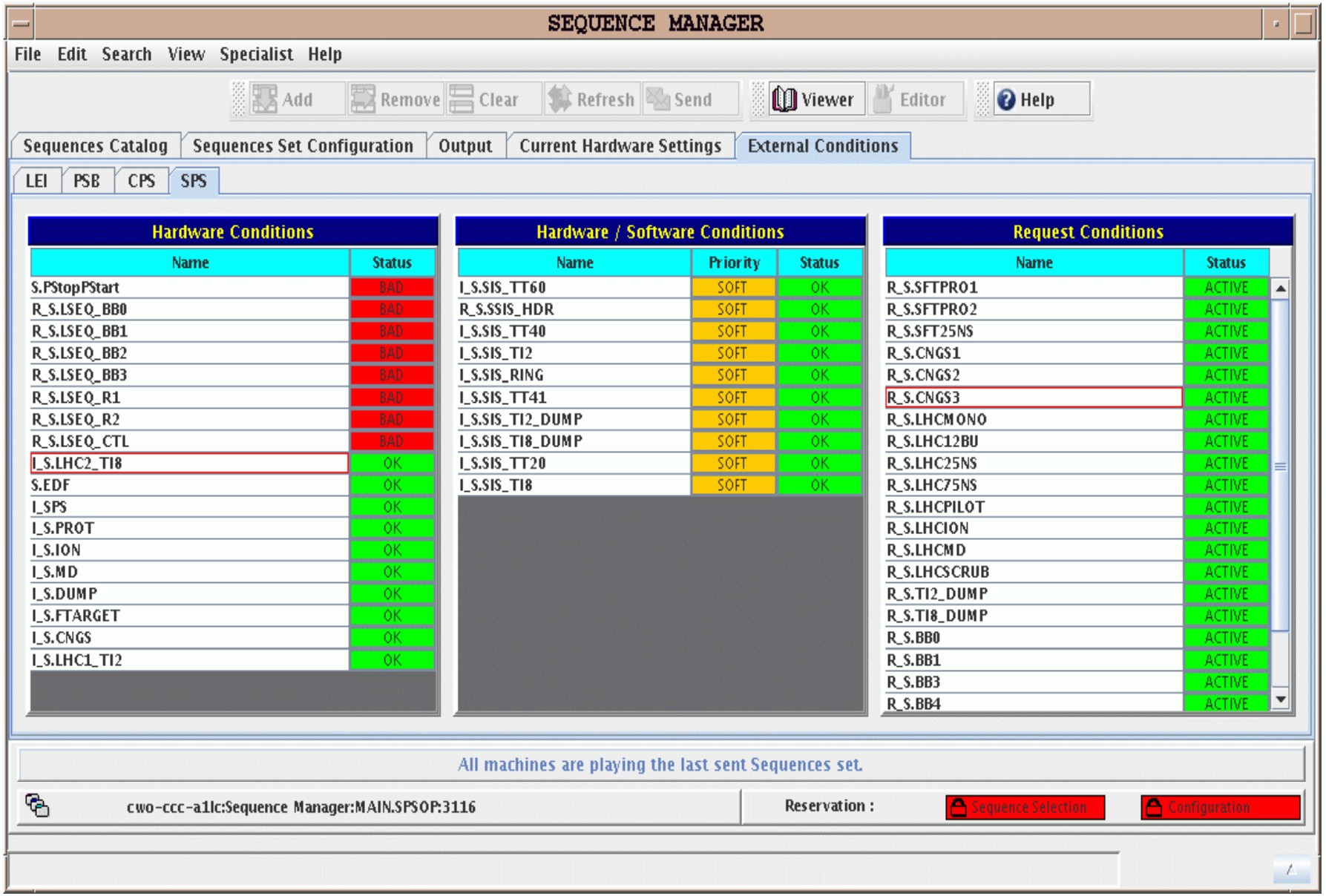
Flow of Control



The interlocks are organized in a tree structure. The top level signals are the summary states that are 'exported' to BIC and timing system

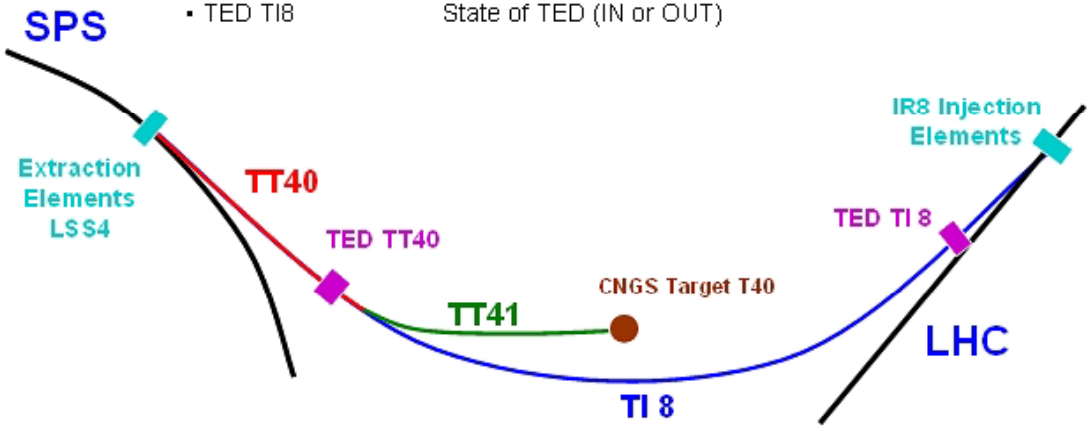


The status of the SIS inhibit signals at the SPS MTG are visible in the Sequence Manager in column Hardware/Software Conditions



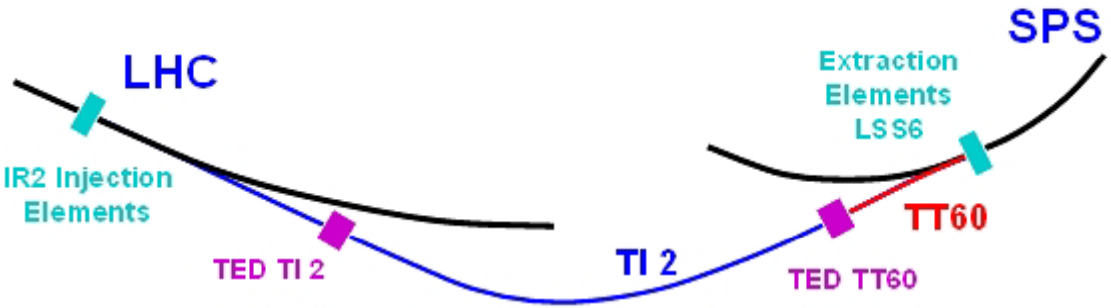
SPS LSS4 Extraction Area Permits :

- TT40 Extraction Elements LSS4 + TT40 transfer line
- TT41 TT41 transfer line + target T40 + secondary beam
- TI8 TI8 transfer line
- IR8-INJECTION LHC ring 2 injection region
- TED-TT40 State of TED (IN or OUT)
- TED TI8 State of TED (IN or OUT)



SPS LSS6 Extraction Area Permits :

- TT60 Extraction Elements LSS6 + TT60 transfer line
- TI2 TI2 transfer line
- IR2-INJECTION LHC ring 1 injection region
- TED-TT60 State of TED (IN or OUT)
- TED TI2 State of TED (IN or OUT)



S.I.S Core

- Operational for the SPS
  - Some improvements for next year
    - Beam stop reason ..
- Need a new server (+ spare) with a timing card connected to the LHC timing system
- SPS : States updated every cycle
- LHC : updated with a fixed clock (2 – 5 seconds period – to be defined) derived from the timing system clock
- LHC : acts on two injection BIC's + ring

SIS Interlocks foreseen

- Surveillance of all non HW-interlocked PC
  - around 1200 correctors
    - Injection inhibit
- COD settings and separation dipole currents (experiment protection)
    - Injection inhibit
- Integrated COD field for Dump safety
    - Dump beam

SIS Interlocks foreseen

- RF System
  - Surveillance of He levels
- Screens positions
- MCS
  - Check BLM settings etc
    - Verify consistency database and front-end setting
    - Frequency to be defined…

SIS Interlocks

- SIS is a “ fourre-tout” for interlocks that are not in HW
- Many ideas – not much very detailed

SIS Plans

- Preparation of configuration files & JAVA classes during shutdown (XML files)
- Tests during checkout for non-beam related tests (that are defined)
- Many tests need dedicated time during beam – possibly pre-tested
- Server on test environment (no timing export, no action on BIC's)

Questions & Comments