

# Software Interlock System

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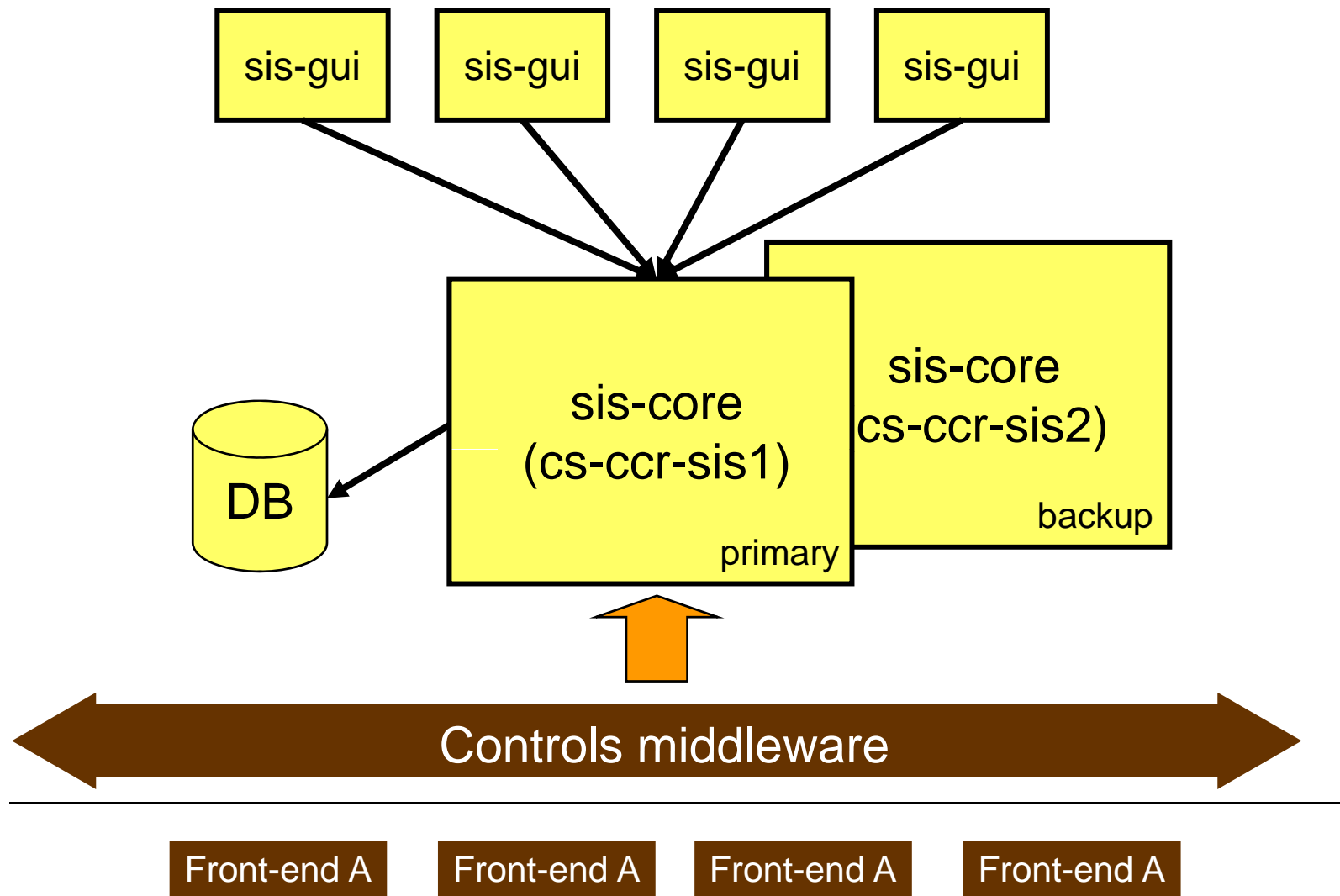
Pereira L.

# Overview

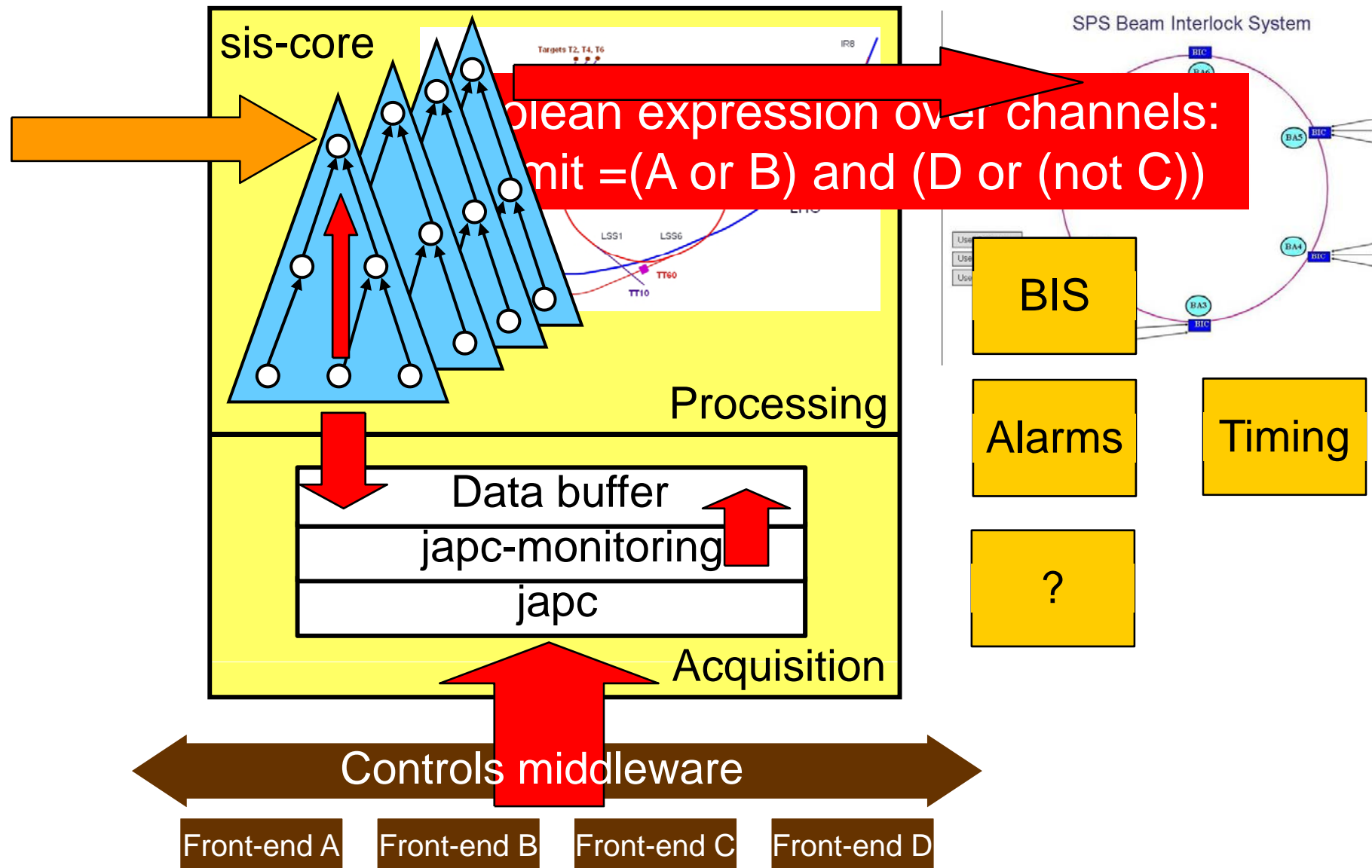
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- The SIS system is a JAVA based software interlock kernel that is operational since 2007.
- Persons involved in OP :
  - J. Wenninger ( project leader)
  - L. Pereira .
- Person involved in CO :J. Wozniak
- SIS acts on the beam through the SPS Beam Interlock Systems for the ring and for the LSS4 and LSS6 extraction. It also acts on the SPS MTG through dedicated inhibit signals.

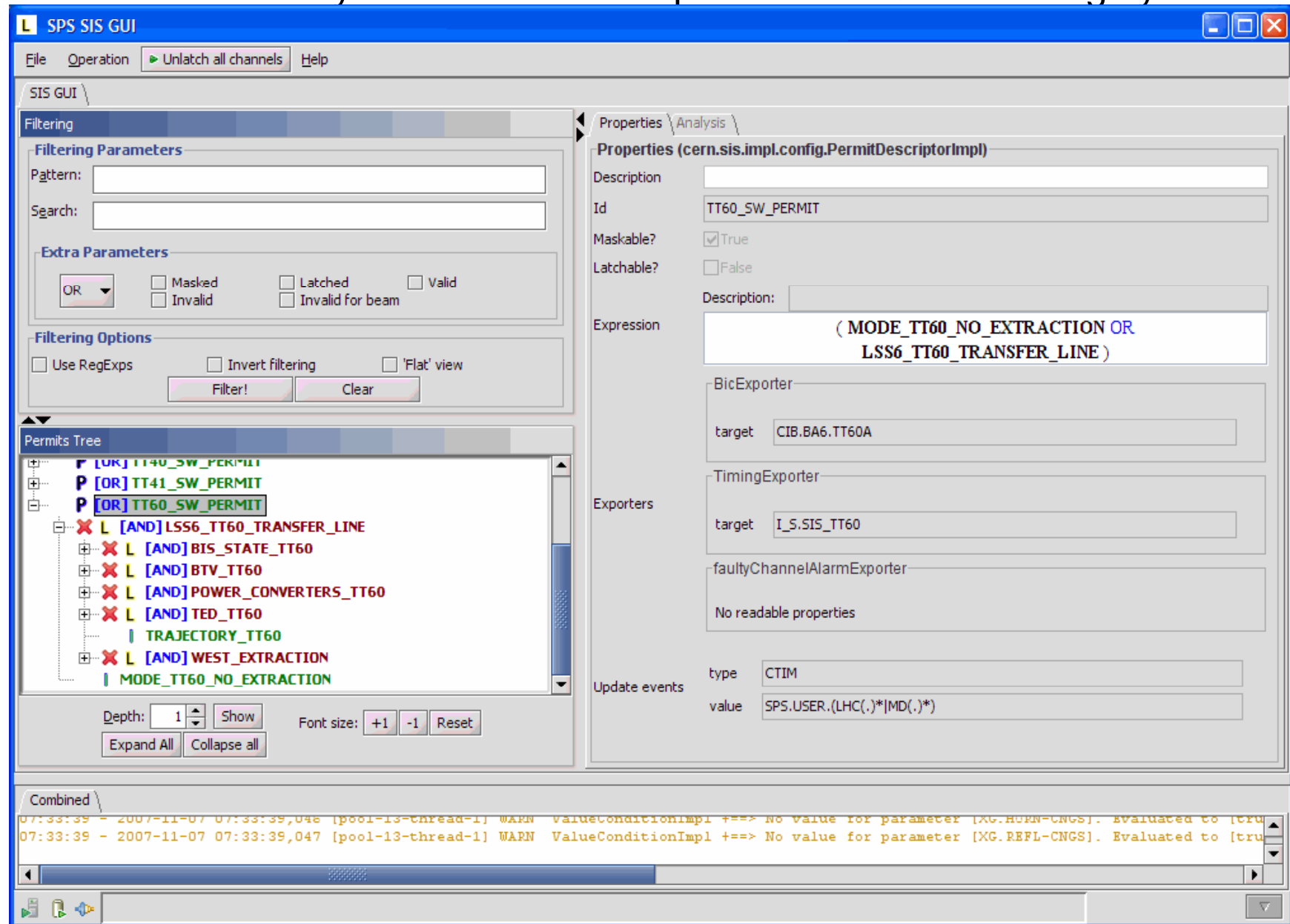
# General Architecture Overview



# Flow of Control



The interlocks are organized in a tree structure. The top level signals are the summary states that are 'exported' to BIC and timing system



The status of the SIS inhibit signals at the SPS MTG are visible in the Sequence Manager in column Hardware/Software Conditions

**SEQUENCE MANAGER**

File Edit Search View Specialist Help

Add Remove Clear Refresh Send Viewer Editor Help

Sequences Catalog Sequences Set Configuration Output Current Hardware Settings External Conditions

LEI PSB CPS SPS

Hardware Conditions		Hardware / Software Conditions			Request Conditions	
Name	Status	Name	Priority	Status	Name	Status
S.PStopPStart	BAD	I.S.SIS_TT60	SOFT	OK	R.S.SFTPRO1	ACTIVE
R.S.LSEQ_BB0	BAD	R.S.SIS_HDR	SOFT	OK	R.S.SFTPRO2	ACTIVE
R.S.LSEQ_BB1	BAD	I.S.SIS_TT40	SOFT	OK	R.S.SFT25NS	ACTIVE
R.S.LSEQ_BB2	BAD	I.S.SIS_TI2	SOFT	OK	R.S.CNGS1	ACTIVE
R.S.LSEQ_BB3	BAD	I.S.SIS_RING	SOFT	OK	R.S.CNGS2	ACTIVE
R.S.LSEQ_R1	BAD	I.S.SIS_TT41	SOFT	OK	R.S.CNGS3	ACTIVE
R.S.LSEQ_R2	BAD	I.S.SIS_TI2_DUMP	SOFT	OK	R.S.LHCMONO	ACTIVE
R.S.LSEQ_CTL	BAD	I.S.SIS_TI8_DUMP	SOFT	OK	R.S.LHC12BU	ACTIVE
I.S.LHC2_TI8	OK	I.S.SIS_TT20	SOFT	OK	R.S.LHC25NS	ACTIVE
S.EDF	OK	I.S.SIS_TI8	SOFT	OK	R.S.LHC75NS	ACTIVE
I.SPS	OK				R.S.LHCPILOT	ACTIVE
I.S.PROT	OK				R.S.LHCION	ACTIVE
I.S.ION	OK				R.S.LHCMD	ACTIVE
I.S.MD	OK				R.S.LHCSCRUB	ACTIVE
I.S.DUMP	OK				R.S.TI2_DUMP	ACTIVE
I.S.FTARGET	OK				R.S.TI8_DUMP	ACTIVE
I.S.CNGS	OK				R.S.BB0	ACTIVE
I.S.LHC1_TI2	OK				R.S.BB1	ACTIVE
					R.S.BB3	ACTIVE
					R.S.BB4	ACTIVE

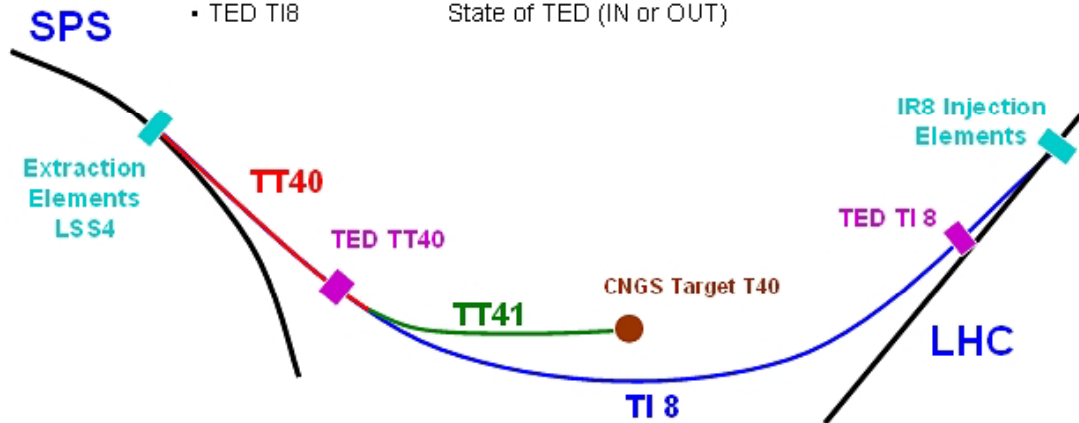
All machines are playing the last sent Sequences set.

cwo-ccc-a1lc:Sequence Manager:MAIN.SPSOP:3116

Reservation : Sequence Selection Configuration

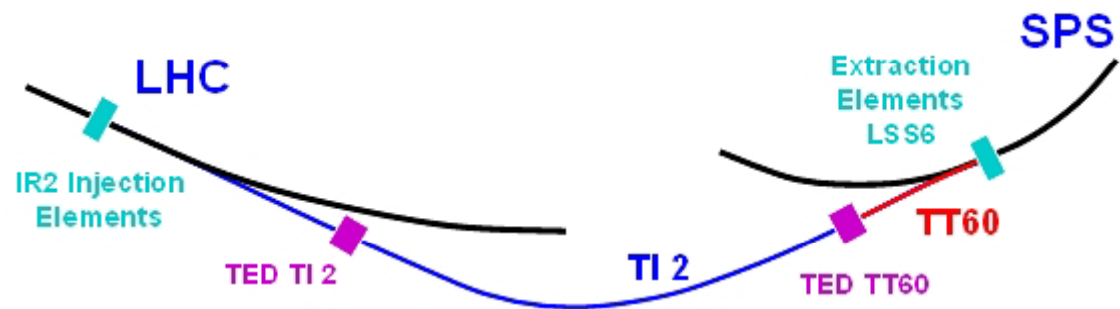
SPS LSS4 Extraction Area Permits :

- TT40                      Extraction Elements LSS4 + TT40 transfer line
- TT41                      TT41 transfer line + target T40 + secondary beam
- TI8                        TI8 transfer line
- IR8-INJECTION        LHC ring 2 injection region
- TED-TT40              State of TED (IN or OUT)
- TED TI8                State of TED (IN or OUT)



SPS LSS6 Extraction Area Permits :

- TT60                      Extraction Elements LSS6 + TT60 transfer line
- TI2                        TI2 transfer line
- IR2-INJECTION        LHC ring 1 injection region
- TED-TT60              State of TED (IN or OUT)
- TED TI2                State of TED (IN or OUT)



# S.I.S Core

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- Operational for the SPS
  - Some improvements for next year
    - ❖ Beam stop reason ..
- Need a new server ( + spare) with a timing card connected to the LHC timing system
- SPS : States updated every cycle
- LHC : updated with a fixed clock ( 2 – 5 seconds period – to be defined) derived from the timing system clock
- LHC : acts on two injection BIC's + ring



# SIS Interlocks foreseen

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- Surveillance of all non HW-interlocked PC
  - around 1200 correctors
    - ❖ Injection inhibit
- COD settings and separation dipole currents (experiment protection)
  - ❖ Injection inhibit
- Integrated COD field for Dump safety
  - ❖ Dump beam

# SIS Interlocks foreseen

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- RF System
  - Surveillance of He levels
- Screens positions
- MCS
  - Check BLM settings etc
    - ❖ Verify consistency database and front-end setting
    - ❖ Frequency to be defined...

# SIS Interlocks

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- SIS is a “fourre-tout” for interlocks that are not in HW
- Many ideas – not much very detailed

# SIS Plans

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- Preparation of configuration files & JAVA classes during shutdown ( XML files)
- Tests during checkout for non-beam related tests (that are defined )
- Many tests need dedicated time during beam – possibly pre-tested
- Server on test environment ( no timing export, no action on BIC's)



# Questions & Comments

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