LHC Timing

M. Albert

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Outline

- Introduction
- Status of LHC Central Timing
  - Hardware
  - Software
- Status of Beam Synchronous Timing (BST)
  - Hardware
  - Software
- Testing
- Conclusions

Central Timing

LHC timing is different compared to its injector chain

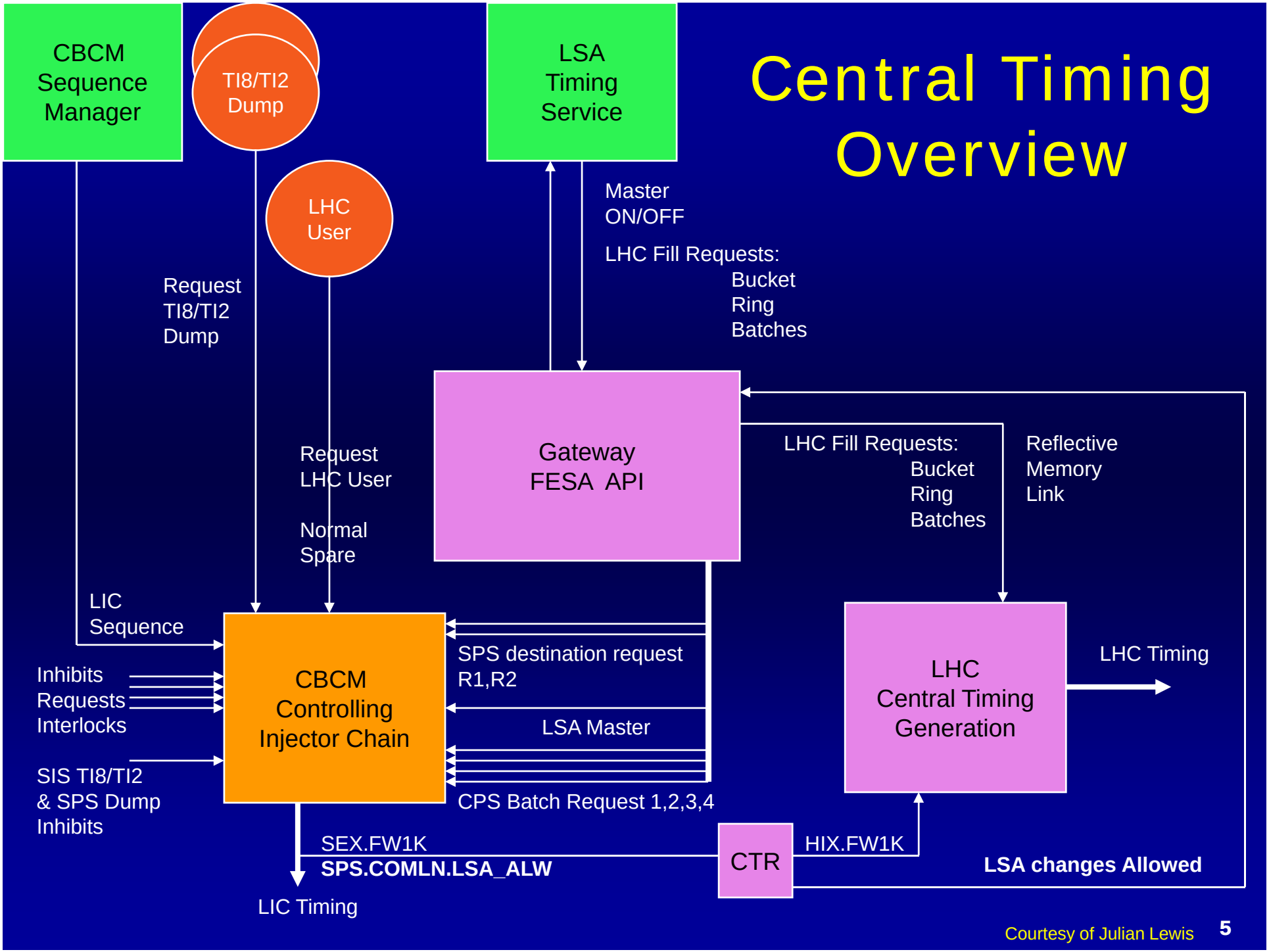
- Almost completely decoupled from injectors (like LEP)
- No cycles / supercycles, slow cycling machine, BUT
- Synchronisation of loosely coupled systems very important
- Events are linked to machine processes
  injection, ramp, squeeze, physics,... which are modelled as event tables
- Event tables:
  - list of events with name, delay, payload
  - loaded, unloaded, started, stopped, aborted under LSA control
  - played independently and concurrently (up to 16)
  - Run or loop n-times or forever on request (timing event)

like collection of CTG cards all driving the same GMT cable

Central Timing

- Asynchronous events (beam energy, intensity, SBF)
- Externally triggered events (injection warning, PM events)
- Telegram
  - Real time channel to broadcast machine information at 1Hz: modes, beam type, Energy, Intensity per ring, flags, ...
  - All information in the telegram is also sent out by events
- Distribution of safe beam parameters and flags
  - Safe beam flag (SBF)
  - Beam permit flag (BPF)
- UTC time reference for accurate timestamps
  - Provided by GPS
  - 25ns resolution
  - Jitter <= 1ns

Central Timing Overview



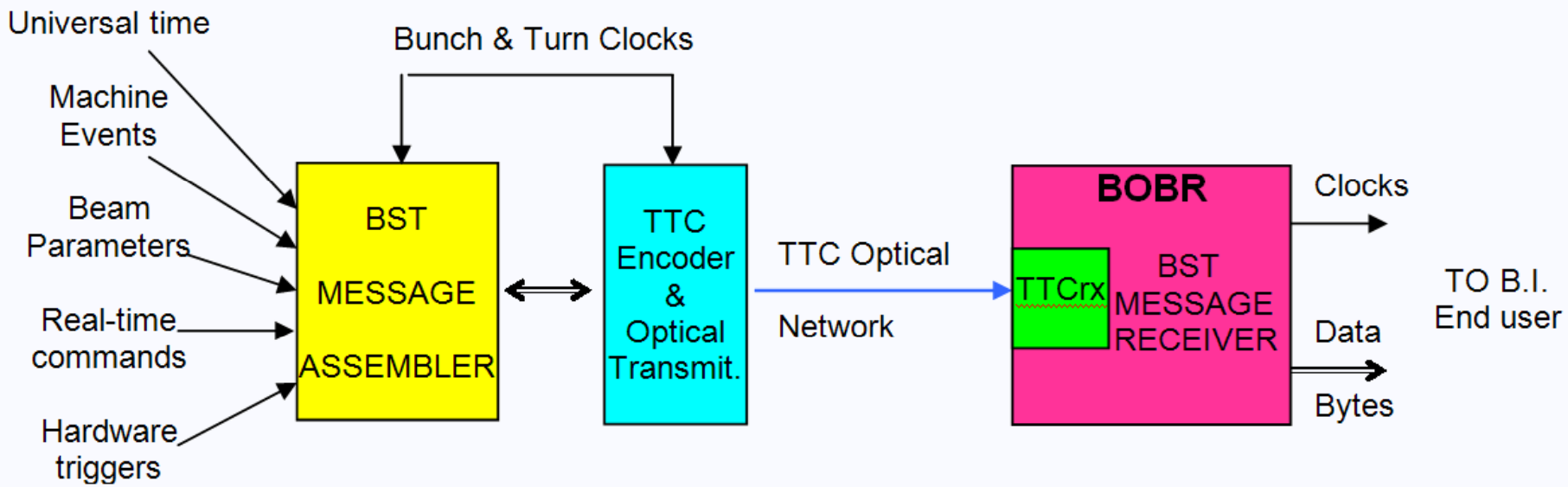
Courtesy of Julian Lewis

BST

- Means of supplying LHC-BI with two basic clocks :
  - 40Mhz bunch synchronous triggers
  - 11kHz LHC revolution frequency
- Components
  - BST master: broadcast of synchronisation signals & BST message
  - TTC system: signal encoding & transmission over optical fibre
  - Receiver (BOBR): recovers BST message and provides timing signals required to synchronize instrumentation
- BST message
  - mainly for beam instrumentation to trigger and correlate acquisitions (BPM 1000 turn, Q, etc.)
  - UTC time, turn count and BST status byte update each turn
  - contains current machine status and various LHC beam parameters (mode, E, I,...) ➔ of interest to LHC experiments

BST

Basic Architecture



Courtesy of J.J.Savioz

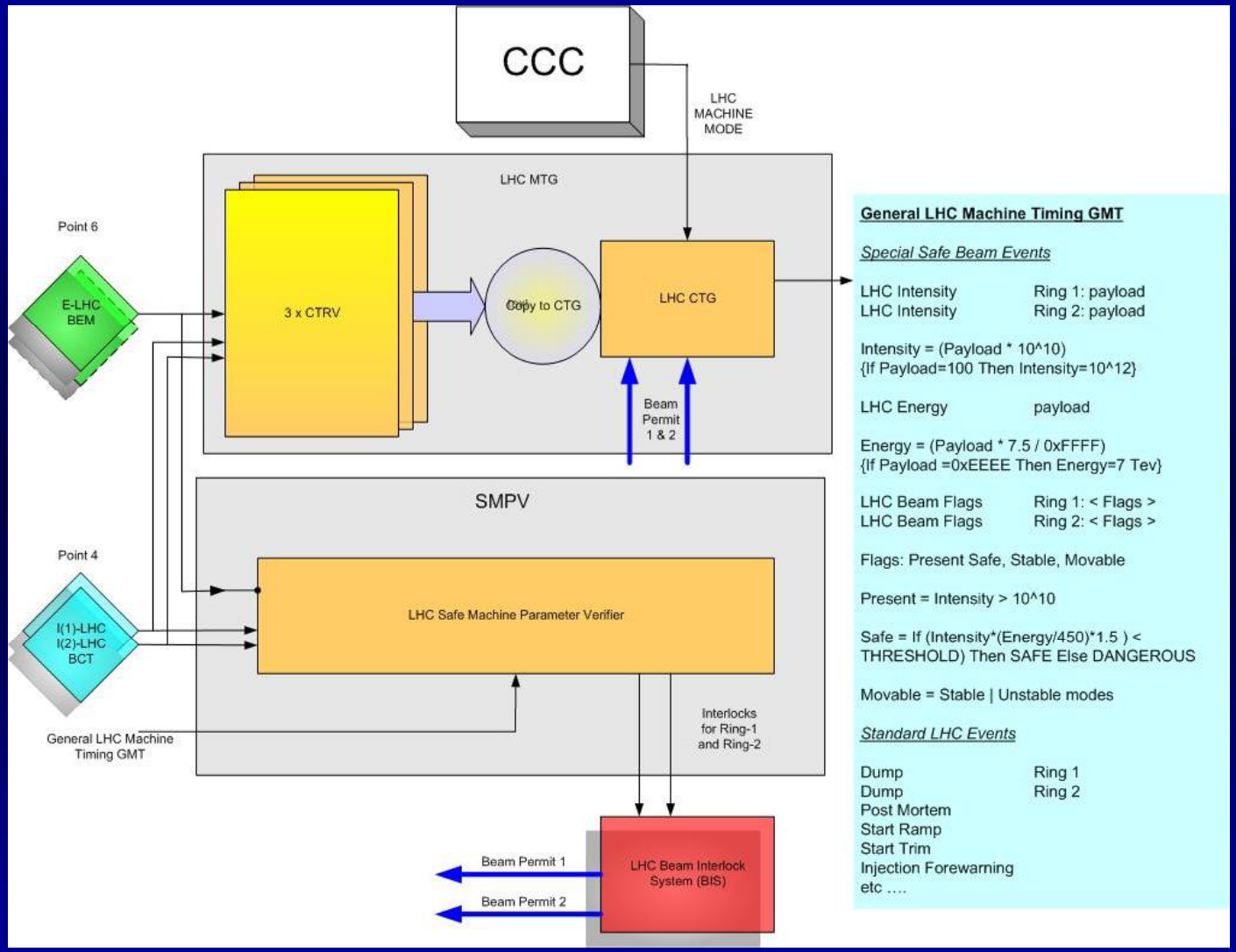
BST message assembler collects all data and commands to be transmitted via the TTC system on a given turn which is then transmitted by the BST master.

3 operational BST systems: B1, B2 and SPS with transfer lines

Central Timing – HW Status

- Timing Generators
  - 3 VME crates installed and working in CCR
  - 2 MTGS: CS-CCR-CTMLHCA, CS-CCR-CTMLHCB
    one acts as a hot-standby, manual switch for permutation
  - Gateway (FESA API): CS-CCR-CTMLHCGW
  - No connection to CBCM yet (external conditions)
- Timing Receiver cards (CTRI, CTRP, CTRV)
  - CTRI cards deployed to all WorldFIP gateways
  - For other equipment, deployment follows installation schedule
  - First functional tests are performed after installation
- Cables & Fibre optics, optical transmitters/receivers
  - All installed, except for experiments and collimators

Safe Machine Parameter Verification



SMPV module will be provided by AB/CO/MI, in the meantime it's simulated by software.

Central Timing – SW Status

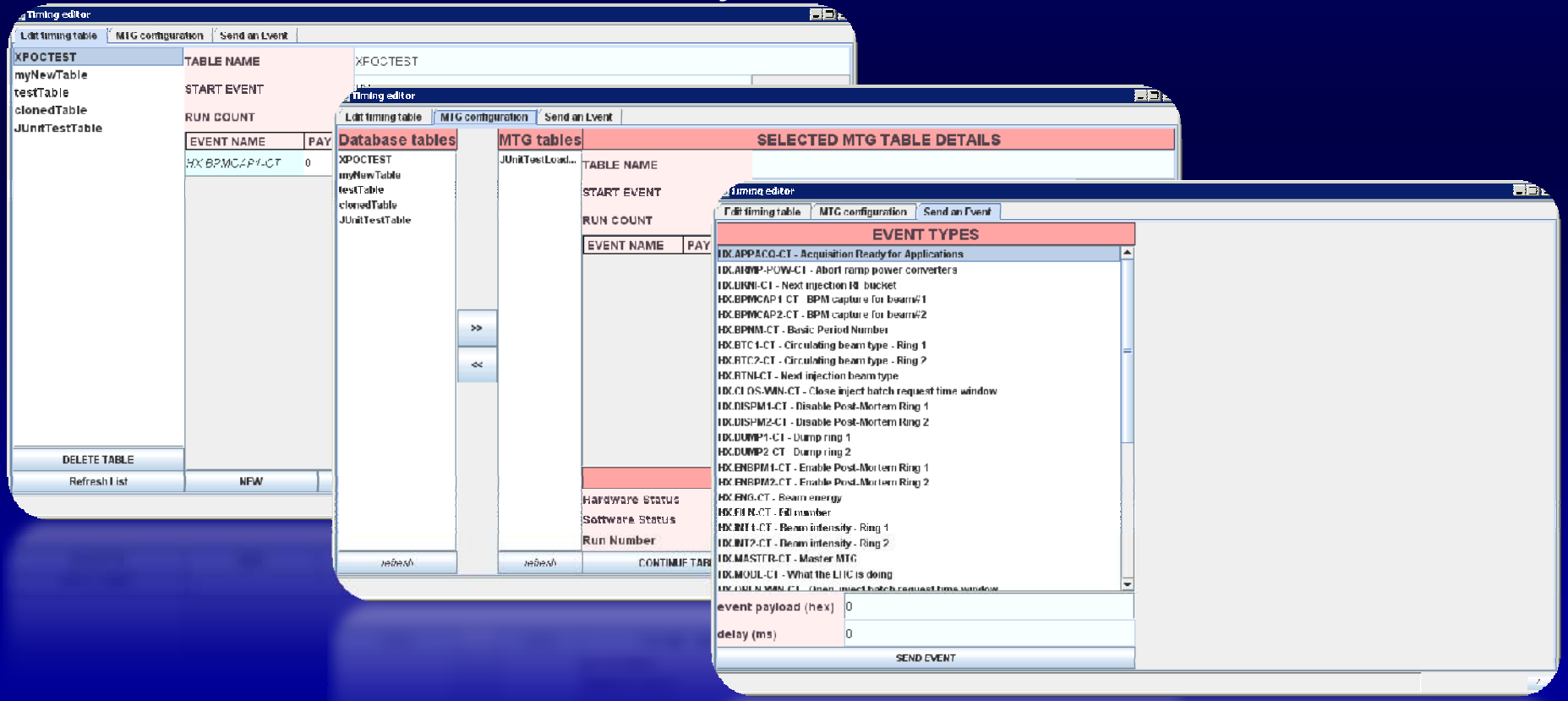
- Server Software:
  - CFV-CCR-CTMLHCGW runs 3 FESA classes
    - **LHCTM**: LHC Table Manager
      - event table manipulations
    - **LHCMTG**: Telegram
      - telegram manipulations
    - **LHCCTMON**: Diagnostics
      - Allows check of what timing table sends out
      - Still under development

Beware: All classes are still subject to modifications !

Central Timing – SW Status

Timing Editor application (by Delphine)

- Event table manipulations (load, unload, start, stop, abort)
- Issuing single events (already tested for PC ramps)
- Event tables have already been loaded/unloaded



Central Timing – SW Status

LHC Sequencer

- Communicates with CFV-CCR-CTMLHCGW to:
  - Take control over filling process (CBCM master)
  - Manage event tables (load, unload, start, stop, abort)
  - Issue events
- Tested so far:
  - Sending single events (power converter ramping)

CBCM Sequence Manager

- Integration of LHC logic into existing application
- Still under development
- No tests performed yet
- To be delivered in January 2008

BST – HW Status

- 3 BST master crate VME modules installed in CCR (B1, B2, SPS)
- BST receivers (BOBR) available, but not yet all (130 in total) installed

Beam Instrumentation

System	1	2	3	4	5	6	7	8
BPM	☑	☒	☒	☑	☑	☒	☒	☑
BLM	☑	☒	☒	☑	☒	☒	☒	☑
BCTFR				☑				
BCTFD						☒		
BWS				☒				
BSRL				☒				
BSRA				☒				
BRA	☒	☒			☒			☒
BQ				☒				

BST– SW Status

- Master FESA class still under development
- Receiver FESA class well advanced
  - FESA server with basic functionality ready to start diagnostics
  - Comparison tests between different locations
- Details will be published on LIDS (BDI sw website)
- Beam Synchronous Timing Expert Application
  allows monitoring & diagnostic of BOBR cards
  still under development…

  first version to be delivered for Dec ‘07

Timing - checks

System	GMT	BST	Check
Injection Kicker	yes	no	send event/verify reception
Dump Kicker	yes	no	send event/verify reception
PC	yes	no	send event/verify reception
RF	yes	no	send event/verify reception
BIS	yes	no	send event/verify reception
Collimators	yes	no	send event/verify reception
Vacuum	yes	no	send event/verify reception
Cryogenics	yes	no	send event/verify reception
BI	yes	yes	send event/verify reception
MPS	yes	no	send event/verify reception
Experiments	no	yes	verify reception

Timing checks per system could be prepared as subsequence for the LHC Sequencer and executed before each fill.

GMT tests

- Issuing events individually and check correct system response
- Generation of externally triggered events
  - Injection forewarning
  - Beam dump and PM events
- Execution of event tables
- All possible event table manipulations
- Concurrent execution of event tables (maximum)
- Dry run “Fill the LHC” to verify synchronisation with injectors

This may perhaps require some MD time after the startup of the injector chain.

BST tests

- Check BST masters
- Check BOBR
  issuing test byte from master and verifying correct reception
- BST Message checks
- AB-BDI-SW will provide a check routine to be launched from the LHC Sequencer

References

- Telegram: http://ab-dep-co-ht.web.cern.ch/ab-dep-co-ht/timing/Seq/tgm.htm
- Events: http://ab-dep-co-ht.web.cern.ch/ab-dep-co-ht/timing/Seq/mtgConfig.htm
- Documents:
  - The CERN LHC Central Timing, A Vertical Slice
    http://ics-web4.sns.ornl.gov/icalepcs07/FOAA03/FOAA03.PDF
  - “FILL THE LHC” A Use Case For The LHC Injector Chain
    https://edms.cern.ch/document/839438/1
  - BOBR
    AB-BDI Software section web page – LIDS

Conclusions

- Timing infrastructure is not yet fully available
- First BST tests could be performed end of this year
- First injector chain timing tests under sequencer control early next year
- Timing check procedures for fast and slow timing probably need to be executed regularly by the sequencer (before each fill ?).

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