Status of power approximation of *VELO algorithm TELL1*

K. Swientek

Department of Physics and Applied Computer Science
AGH University of Science and Technology

January 31, 2013

Simulation

- Cadence is a target platform for ASICs
- *VELO algorithm TELL1* was written in VHDL language
- Cadence specific troubles with VHDL
  - first larger VHDL design
  - VHDL libraries are treated in a specific way
- Waiting for Lozanna
  - missing module `ecs_ram_mux_cc`
  - hint needed – how to set inputs

Synthesis

- RTL Compiler – Cadence synthesis tool
- VHDL libraries are treated in specific way as in simulation
- Tri-state buffers necessary to make synthesis
- IBM 130nm standard cell library do not contain tri-state buffers
- Direct synthesis is impossible in the moment . . .
- Two ways to proceed
  - create fake tri-state buffers
  - extract processing algorithms form VHDL code (it seems that tri-state buffers are in control part)