AGH University of Science and Technology

Status of the Works on Silicon Strip Common ASIC at AGH-UST

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Outline

- Preliminary tests of 10-bit SAR in IBM 130 nm
- Design of front-end ASIC in IBM 130 nm
- Summary

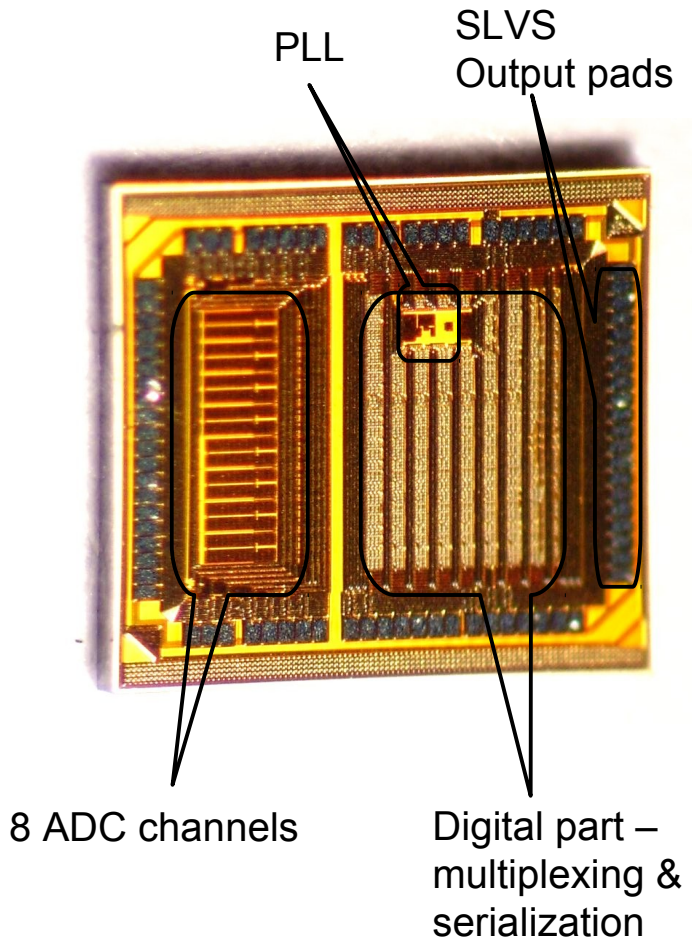
Prototypes under tests… 10-bit ADC, PLL, SLVS

Prototype of 10-bit ADC

- SAR ADC with segmented DAC
- Scalable frequency (up to ~50 MS/s) and power consumption
- 1-2mW at 40MS/s
- ~150um pitch

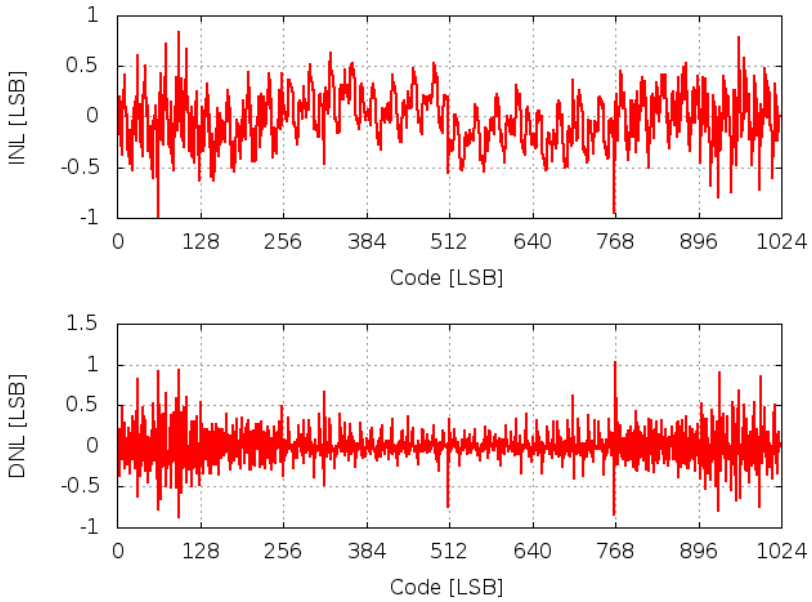
Prototype of PLL

- Type II PLL with 2nd order filter
- Scalable frequency&power
- Automatically switched VCO frequency range 8MHz – 3GHz
- VCO frequency division by 6, 8, 10 or 16
- Power consumption <2mW at 3GHz
- Jitter RMS<5ps

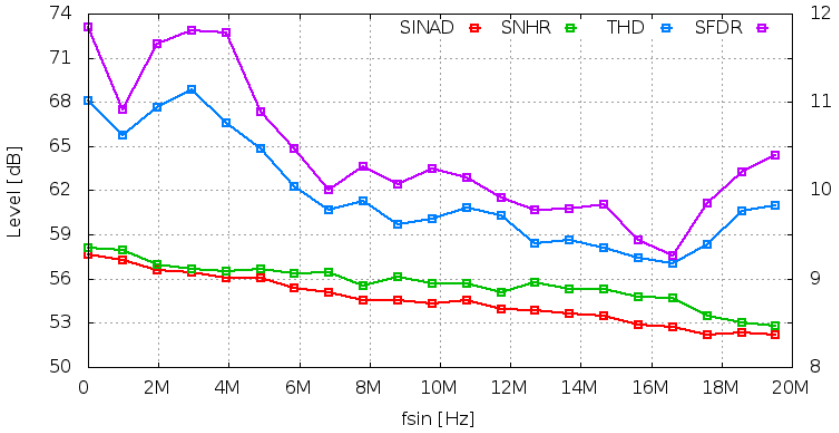


Preliminary measurements of 10-bit ADC Example measurements at 40Ms/S

Static measurements



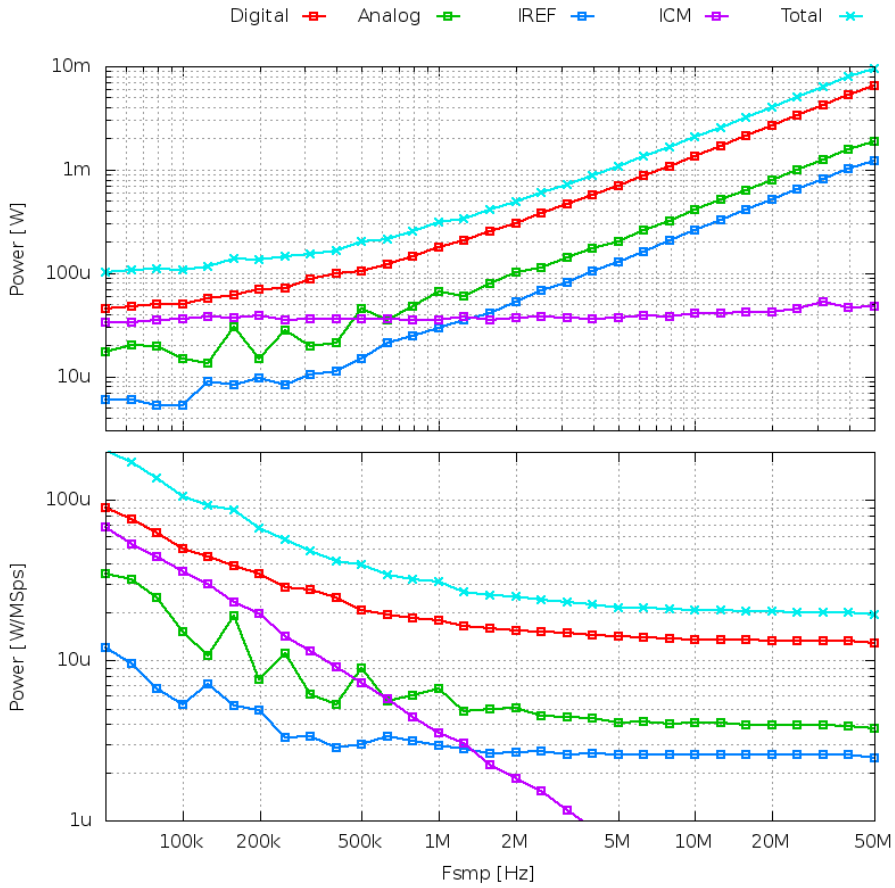
Dynamic measurements



- These results were obtained optimizing all parameters, and so are better than for default setting
- The main conclusion is that ADC works in the whole simulated frequency range
- The quantitive results will probably be worse than simulated (ENOB 8-9 bits ?)

Preliminary measurements of 10-bit ADC
- Power consumption vs sampling frequency
- Status of SLVS, PLL

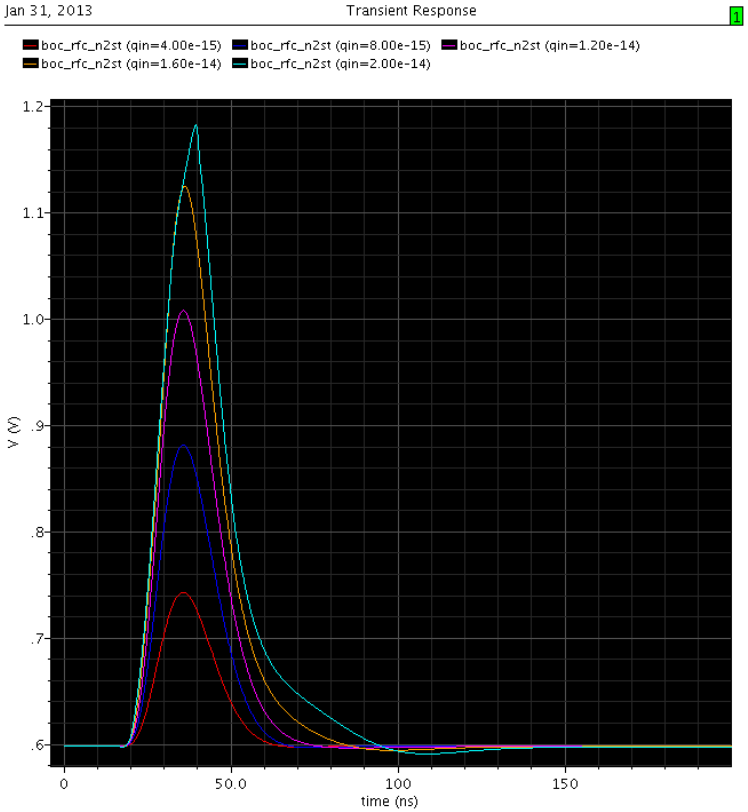
- Power measured for 8 ADC channels
- At 40Ms/S the consumption is about 1 mW per channel – in agreement with simulations



- SLVS interface used during ADC tests, so obviously working up to some hundred MHz. Dedicated tests not done yet
- PLL – it was verified that high frequency clock (up to ~1GHz) is generated. No quantitative info yet.

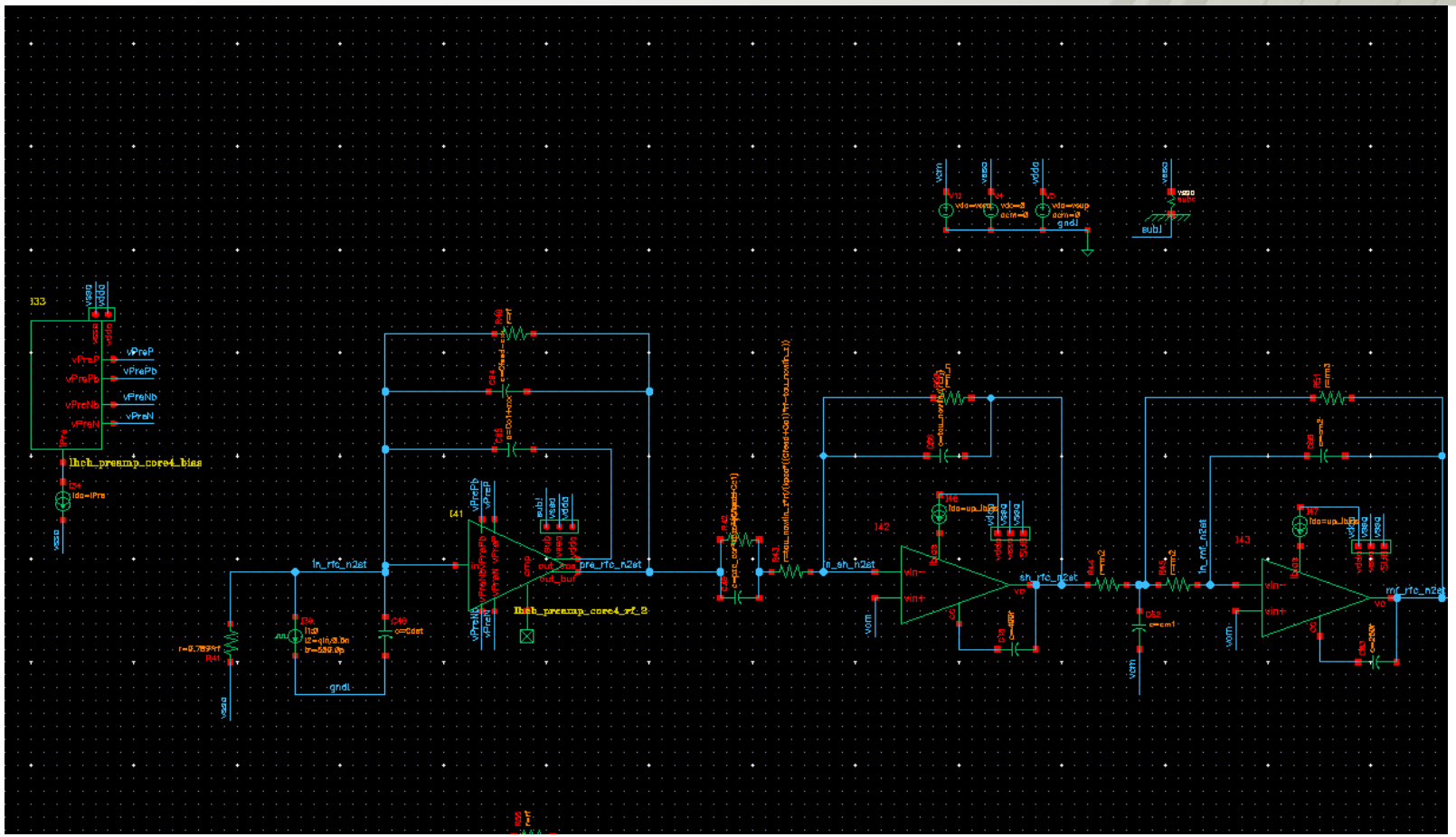
Front-end design Overview

- Design status:
  - People involved: M. Idzik, J. Moron, M. Firlej, T. Fiutowski
  - Cadence simulations: schematic - still to be complteted soon, layout - started week ago (by Monday size need to be sent to Kostas)



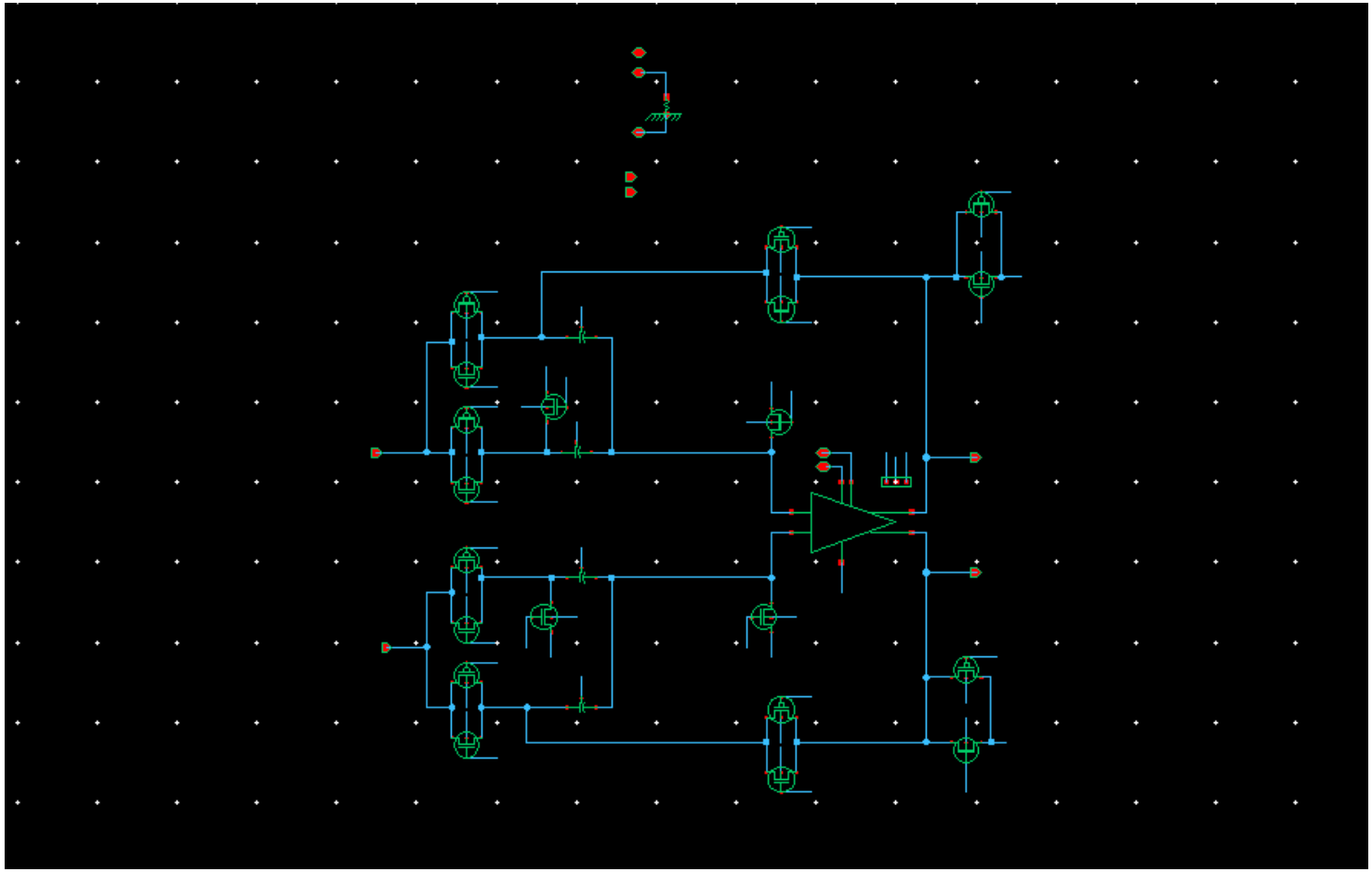
Example of single ended front-end output
For Qin 4fC - 20fC

Front-end architecture
Preamplifier & Shaper



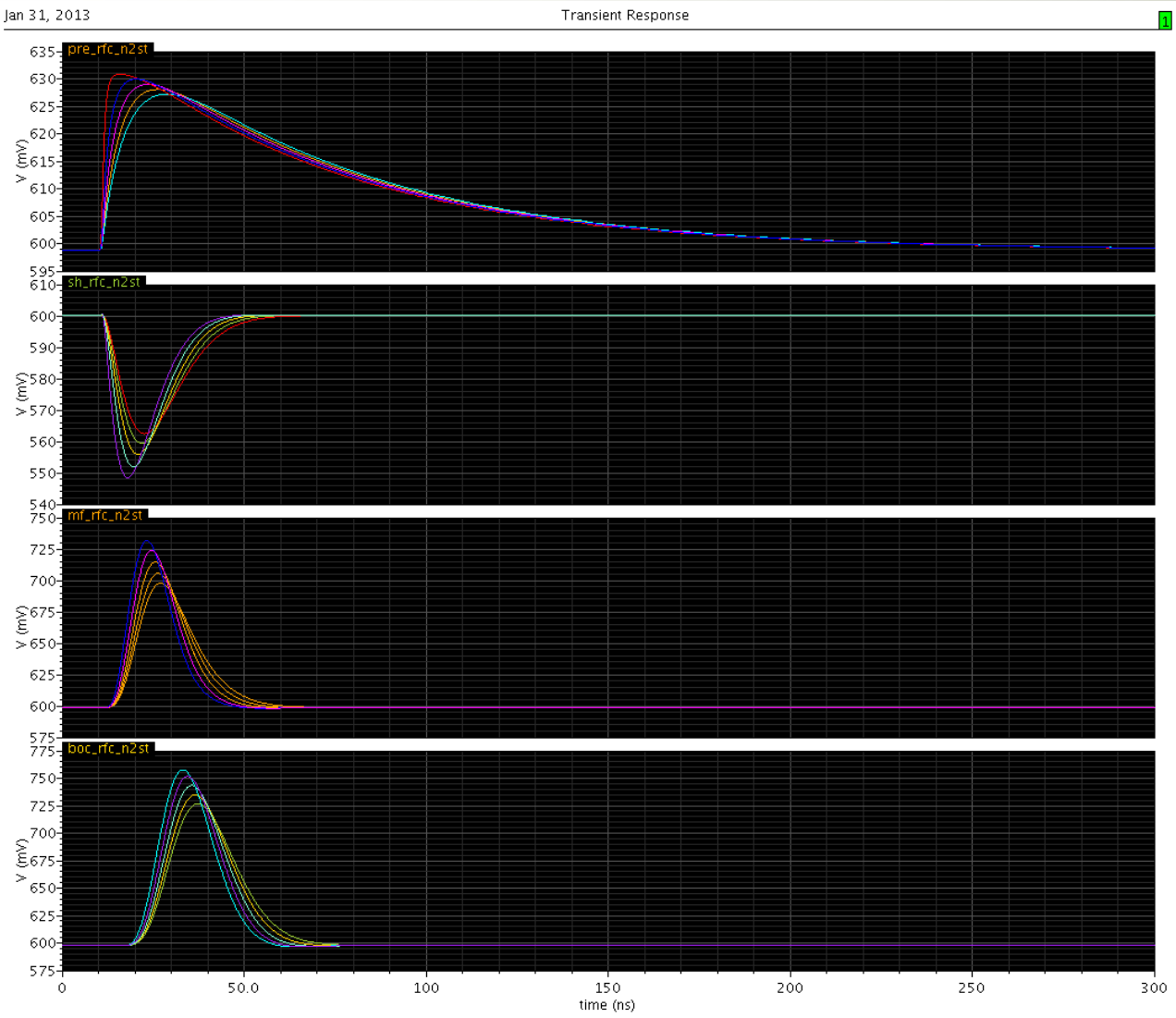
Preamplifier is followed by 3 shaping stages. 3rd stage under optimization, not shown here

Front-end architecture
Single-to-Differential converter



Converter has gain of 2

Front-end simulations
Cdet 5pF – 45 pF



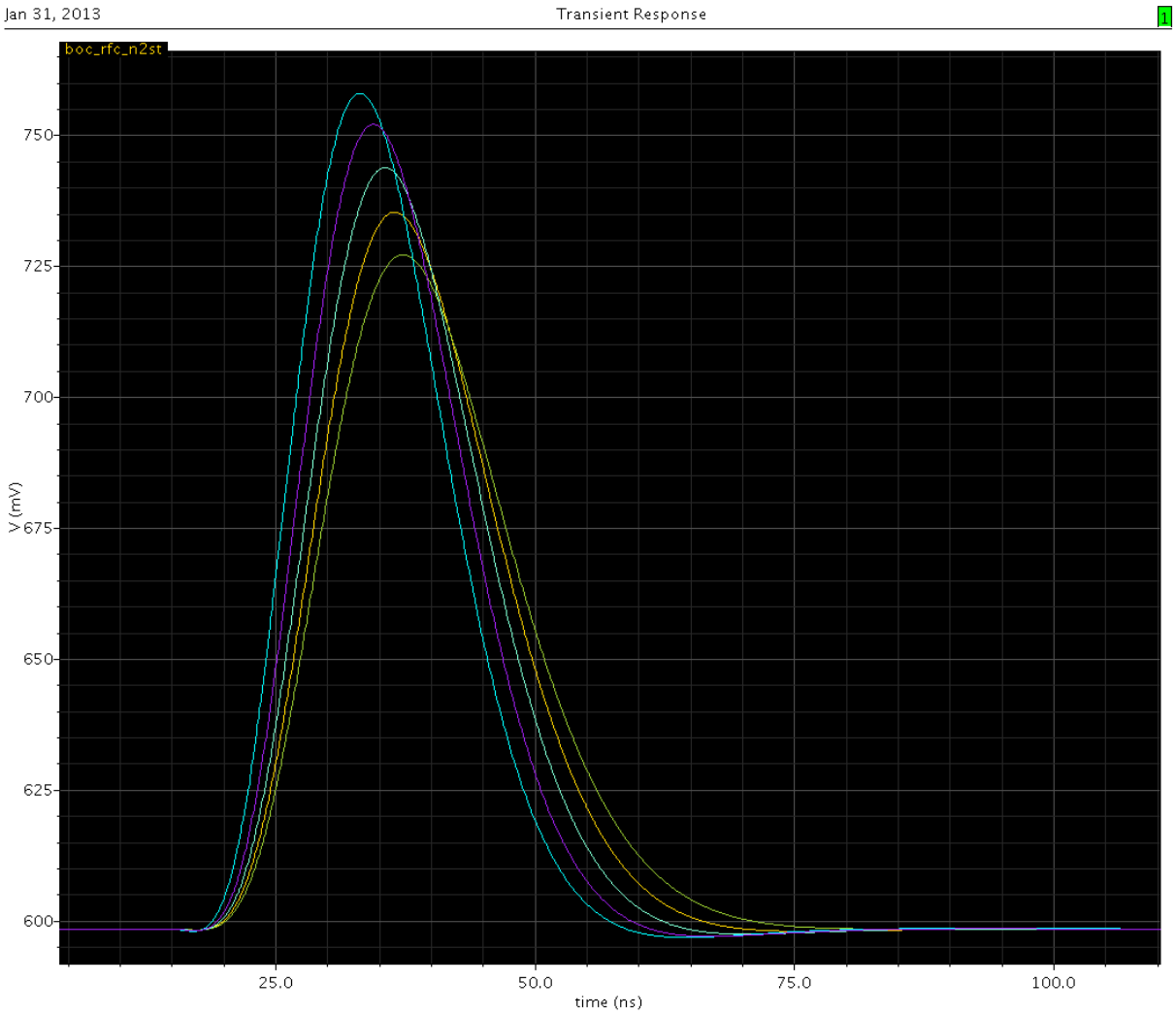
Preamplifier output

1st shaper stage output

2nd shaper stage output

3rd shaper stage output

Front-end simulations
Cdet 5pF – 45 pF



3rd shaper stage output

Front-end simulations
Power consumption

- Preamplifier
  - 1mA * 1.2V = 1.2mW
  - May be scaled down to ~400uW (worse charge sensitivity and noise)
- Shaper
  - 180uA * 1.2V * 3(stages) =~ 0.66mW
  - May be scaled down by about 50%
- Single to differential converter
  - 100-250uA * 1.2V, ~250uW
- Total power ~2mW, may be scaled down to less than 1mW

Summary

- First measurements of 10-bit SAR ADC showed that the blocks (ADC in particular) are functional
- Quantitative measurements in progress...
- Front-end design in critical stage – simulations not yet completed, layout in progress. Should be submitted by 19 of February
- Due to critical situation with man power, PCB for 6-bit ADC not sent to production yet (still 1-2 weeks...)