DECTRIS®

detecting the future

Development Process of CMOS Readout ASICs for Single-Photon Counting X-Ray Detectors

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Outline

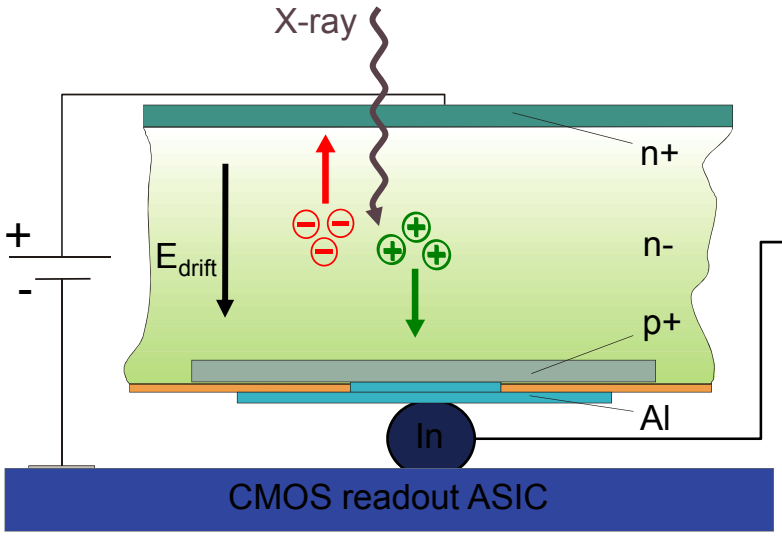
1. Introduction
2. Single-Photon Counting (SPC) Hybrid-Pixel X-Ray Detectors
3. DECTRIS Product Portfolio
4. DECTRIS Product Development Process
5. CMOS Readout ASIC Design
6. System Integration
7. Conclusions

Introduction: Educational Objectives

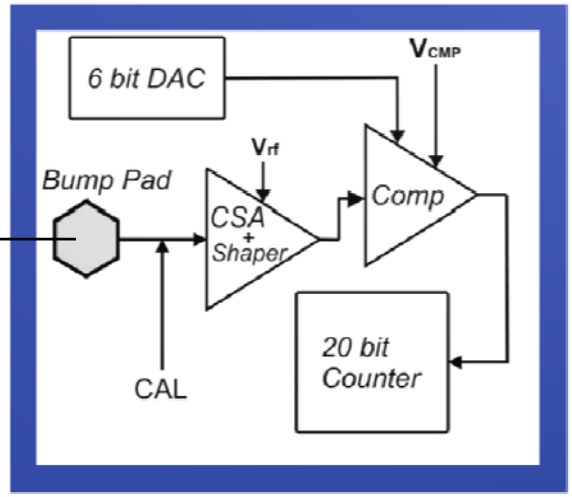
- *to understand the basic technology of single-photon counting hybrid-pixel x-ray detectors*
- *to know the basic steps of the DECTRIS product development process*
- *to identify the disciplines involved in the detector development*
- *to have a feeling for leading-edge detector technology*

SPC Hybrid-Pixel X-Ray Detectors: Hybrid-Pixel Technology

Solid-State Sensor Pixel



CMOS Readout ASIC Pixel



direct detection of x-rays in pixelated solid-state sensor:

→ *optimized sensor material and geometry*

→ *point spread function of 1 pixel*

single-photon counting in CMOS technology:

→ *zero dark signal, zero readout noise*

→ *very high dynamic range (20 bit)*

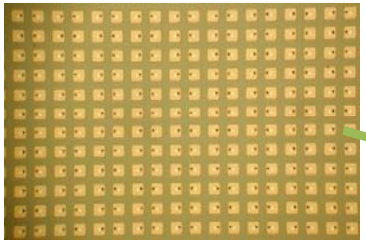
→ *fast readout*

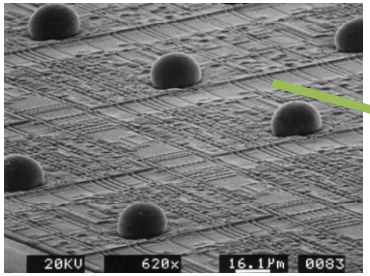
SPC Hybrid-Pixel X-Ray Detectors: Hybrid-Pixel Technology

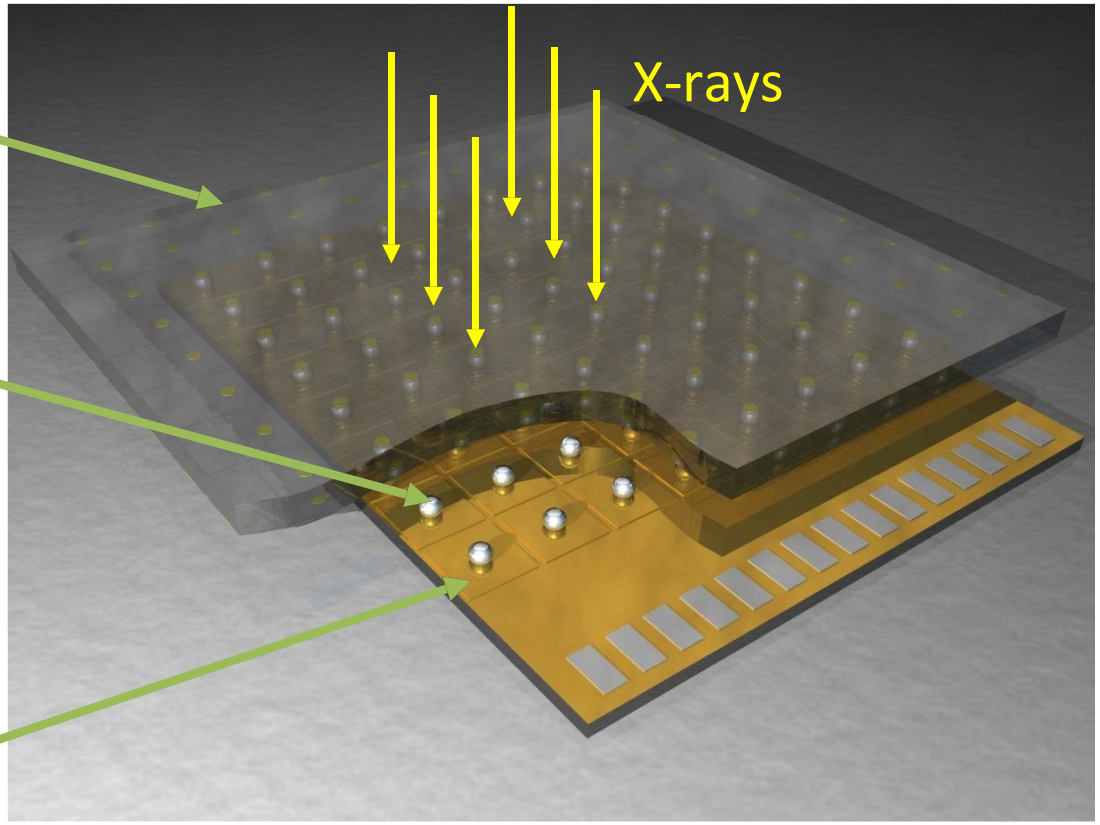
monolithic sensor with pixelated pn-diode structure

micro bump bonds (18 µm indium balls)

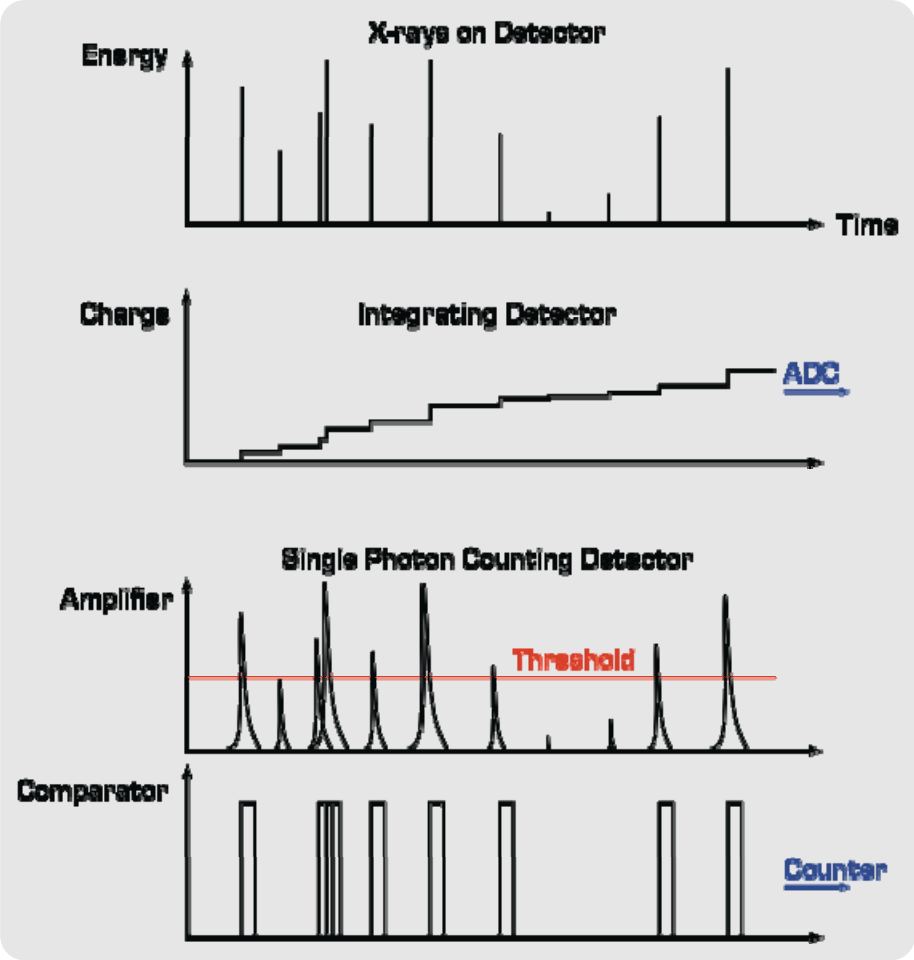
CMOS readout ASIC







SPC Hybrid-Pixel X-Ray Detectors: Single-Photon Counting Technology



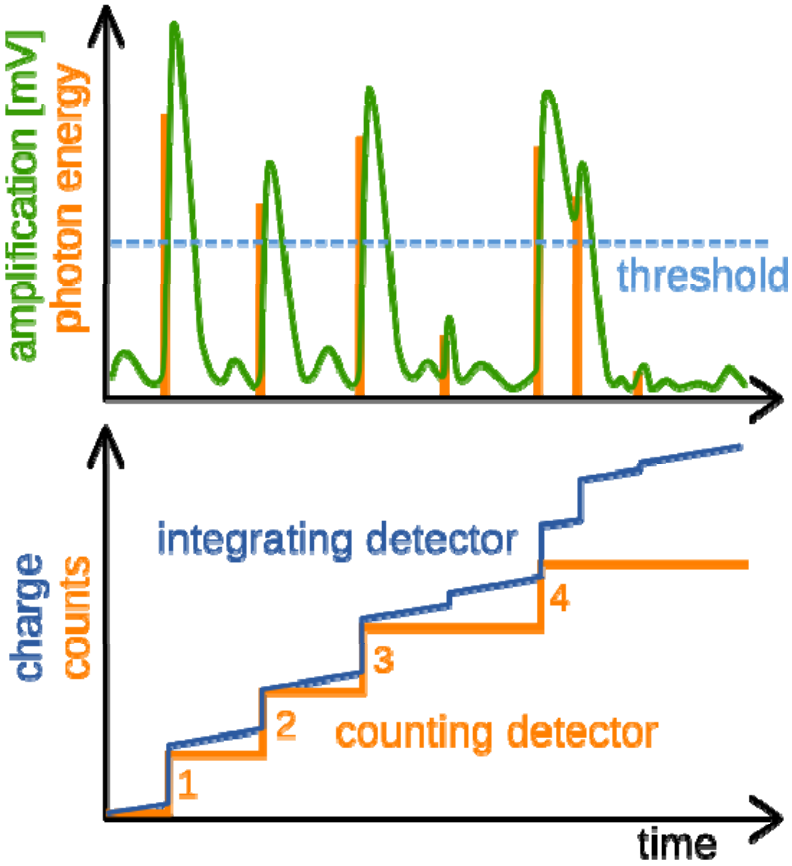
integrating detector (e.g. CCD):

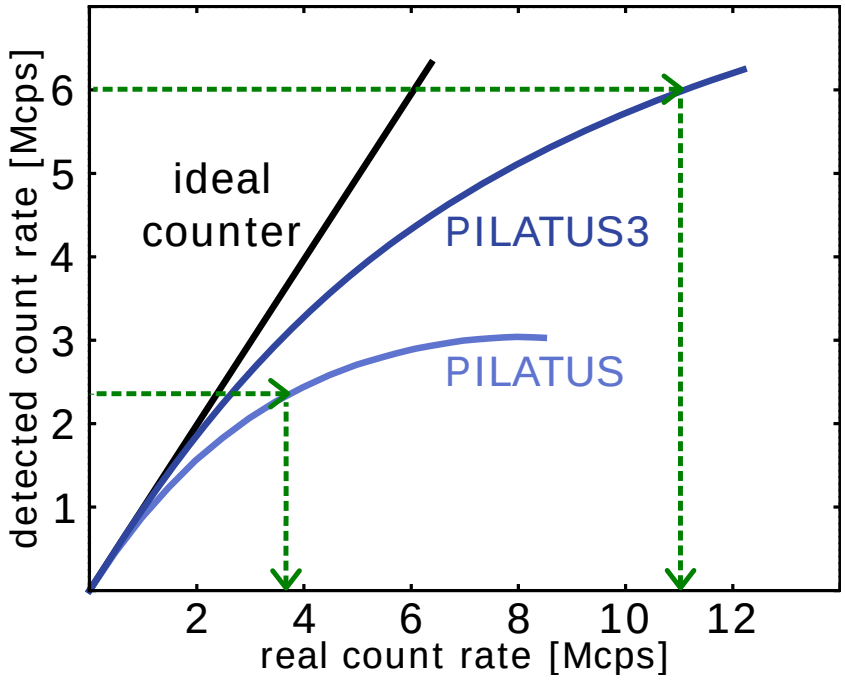
- *indirect detection*
- *dark current*
- *readout noise*

single-photon counting detector:

- *direct detection*
- *zero readout noise*
- *highest dynamic range*

SPC Hybrid-Pixel X-Ray Detectors: Single-Photon Counting Technology



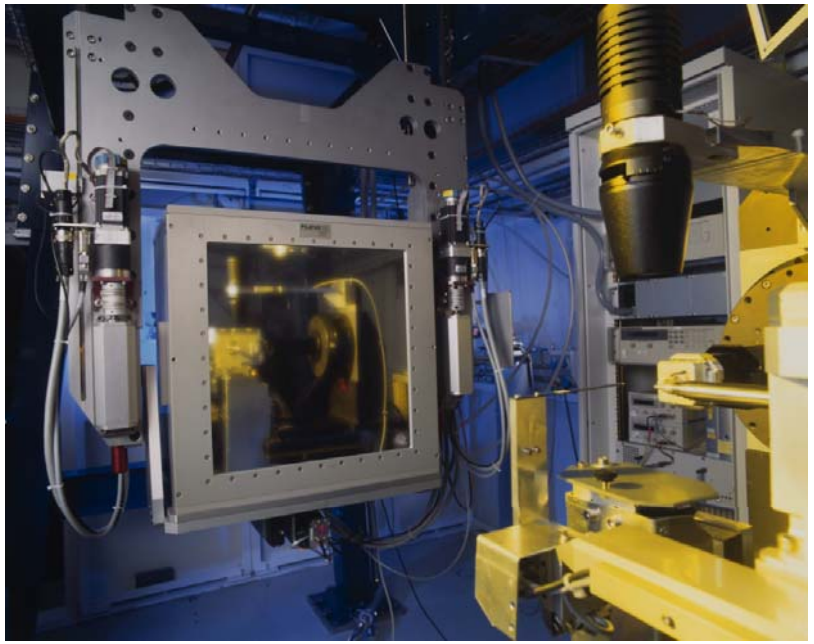


DECTRIS Product Portfolio: History

Research Project at Paul Scherrer Institute PSI (1997-2006):

PILATUS 6M – World's Largest and Fastest X-ray Camera

PILATUS 6M detector prototype



PILATUS 6M at SLS beamline X06SA

DECTRIS Product Portfolio: Evolution

2006: foundation of DECTRIS

2007: 6 employees
9 systems delivered

2008: 12 employees
relocation to Baden
20 systems delivered

2009: 20 employees
70 systems delivered

2010: 34 employees
127 systems delivered

2011: 40 employees
110 systems delivered

2012: 46 employees
(28 physicists and engineers,
2 trainees)
140 systems delivered

DECTRIS team 2012

DECTRIS Product Portfolio: Business Model

synchrotron	laboratory & industry	specific solutions
– highest performance detectors – solutions for beamline integration – worldwide service and support	– high Performance detectors – application development with OEM Partners – integration solutions	– special detector configurations based on customer requirements – product development

PILATUS3

Key Advantages

– *count rates up to 10 Mcts/sec/pixel*
– *frame rates up to 500 Hz*
– *readout time of 0.95 ms*
– *overflow-free 20 bit counter*
– *320, 450 and 1000 µm thick sensors*

Applications

– *macromolecular crystallography*
– *small-molecule crystallography*
– *surface diffraction and reflectometry*
– *scanning beam imaging (sSAXS, ptychography)*
– *time-resolved experiments*
– *SAXS, WAXS and GISAXS*

MYTHEN

Key advantages

– *direct detection of X-rays*
  => excellent line-spread function
– *single-photon counting mode*
  => zero dark signal, zero readout noise
– *fluorescence suppression*
– *24 bit counter depth and 1 Mcts/sec/strip*
– *short readout time and high frame rate*
– *maintenance-free*

Applications

– *powder diffraction*
– *phase analysis*
– *stress analysis*
– *texture and thin-film analysis*
– *pair distribution function analysis*
– *SAXS, WAXS, GISAXS*
– *time-resolved experiments*
– *dispersive fluorescence spectroscopy*

DECTRIS Product Portfolio: Specific Solutions

customer specific request

e.g.:

– *PILATUS 12M in high-vacuum*

– *specific geometry*

– *very low energy*

customer specific solution

e.g.:

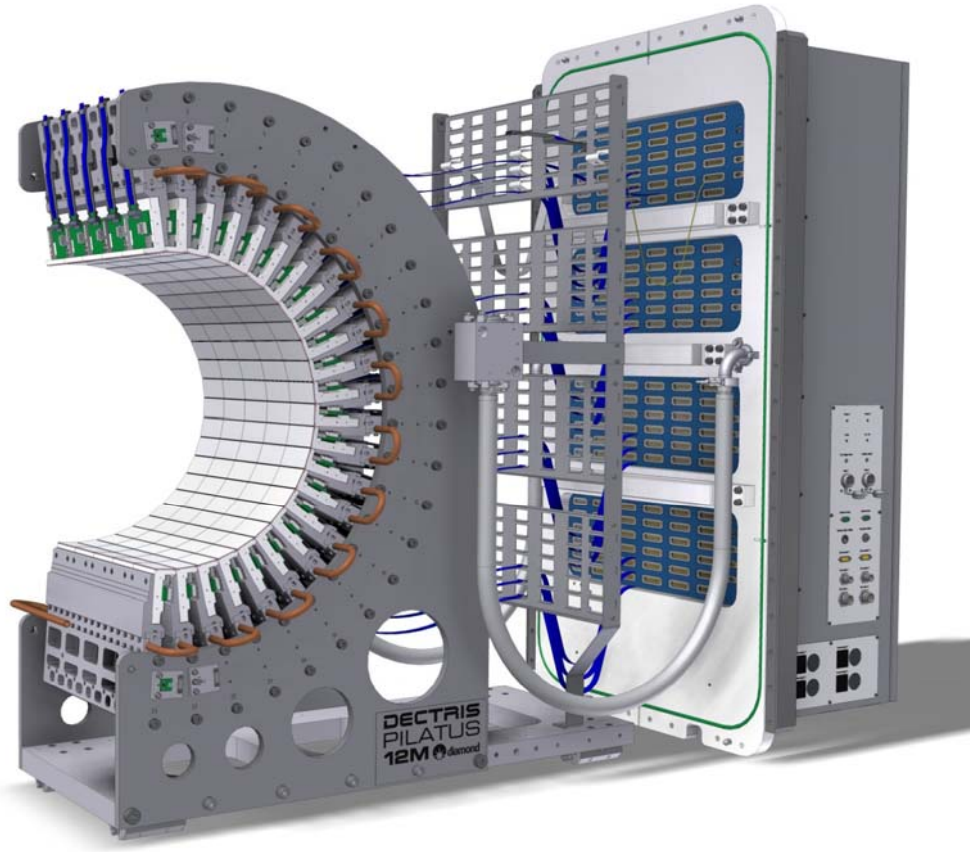
– *120 modules (0.34 m^2 active area)*

– *cylindrical arrangement (24 banks)*

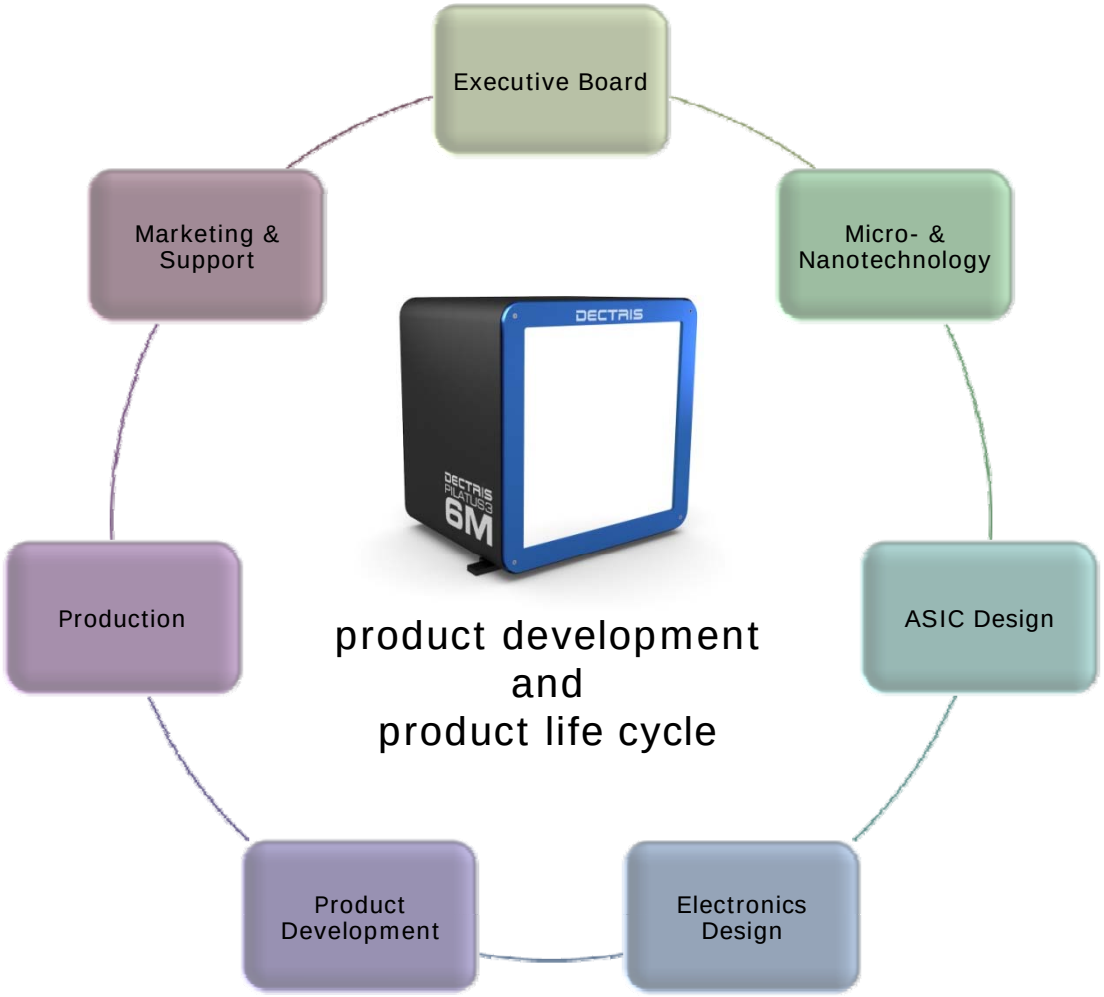
– *water-cooling*

– *in vacuum (calibration in vacuum)*

➔ ***PILATUS 12M-DLS***



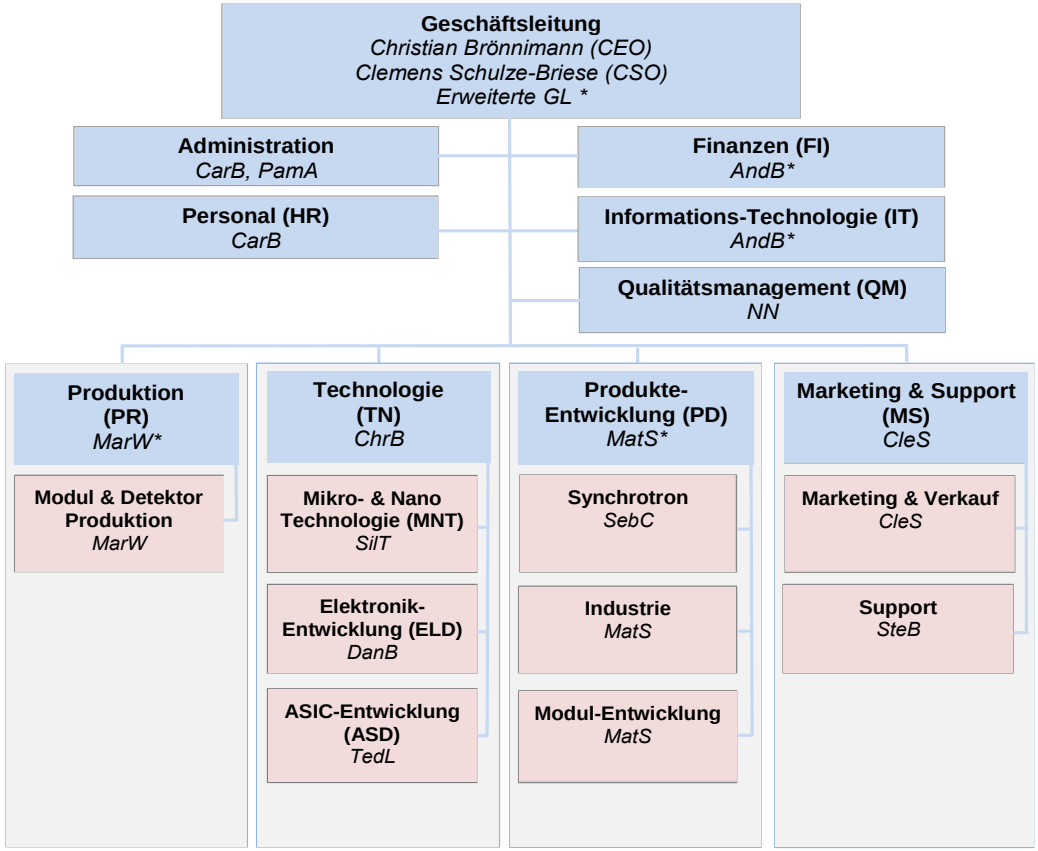
DECTRIS Product Develop. Process: Departments



DECTRIS Product Develop. Process: Organizational Diagram

DECTRIS®

Prov. Organigramm
gültig ab 1.1.2013



Erstellt:	Geprüft:	Freigegeben:	Geändert :
CarB 28.01.2011	ChrB 28.02.2011	ChrB 28.02.2011	CarB 22.11.2012

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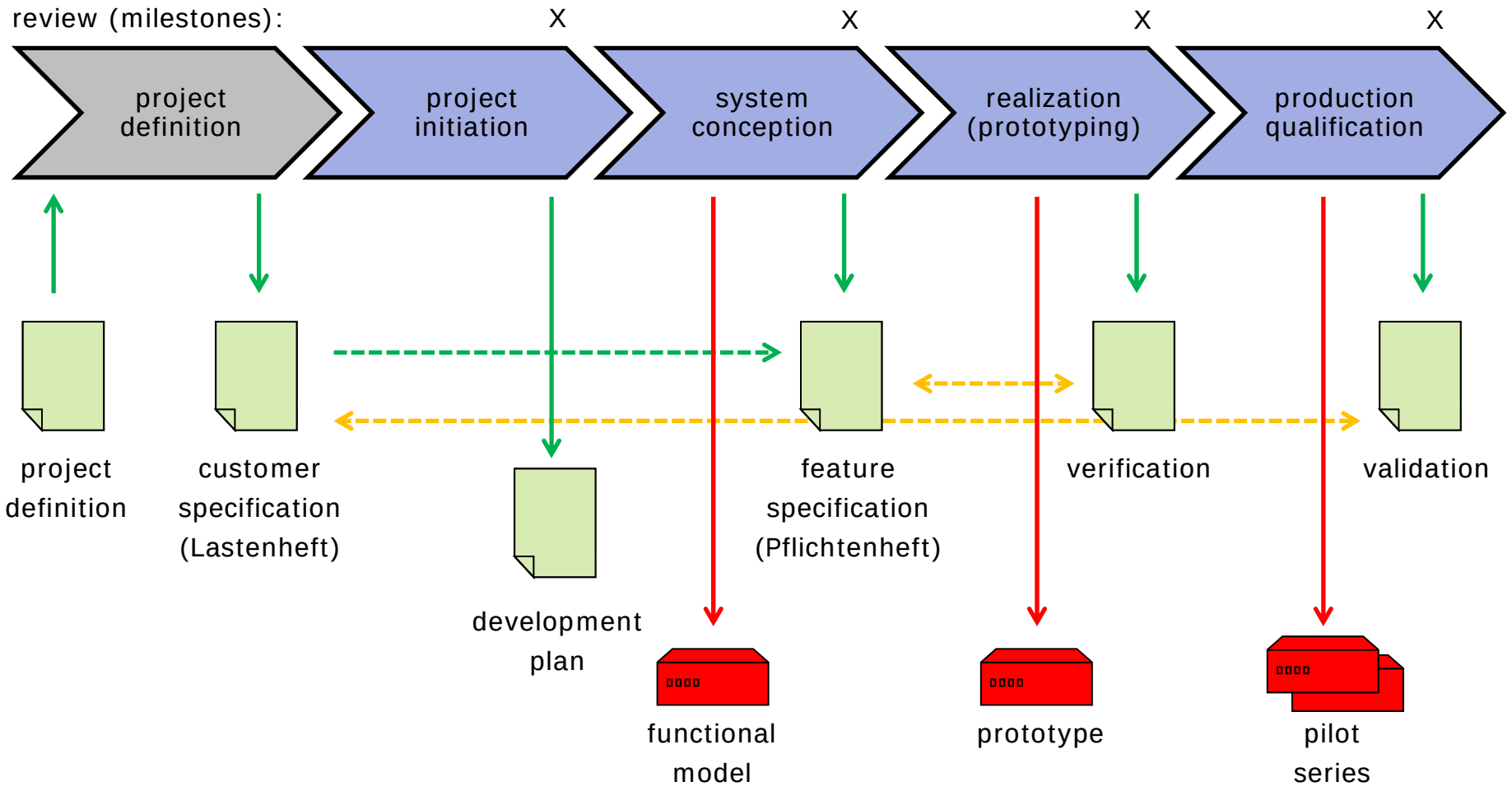
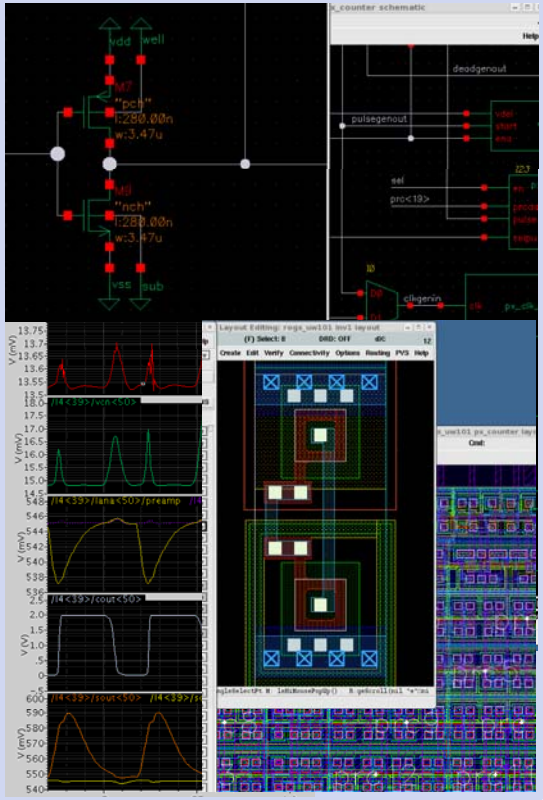
DECTRIS Product Develop. Process: Product Development Process



CMOS Readout ASIC Design: ASIC Design Group Responsibilities

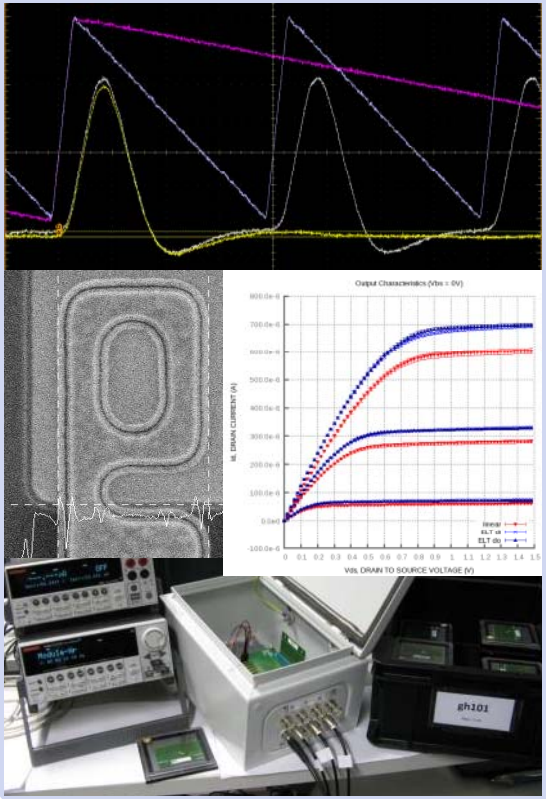
Mixed-Signal ASIC Design

Simulation, Layout



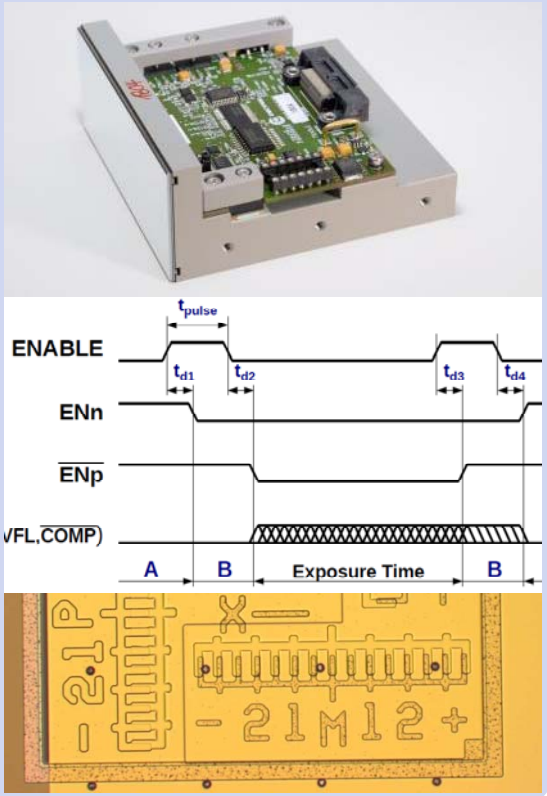
Characterization

Technology, Circuitry



Production Transfer & Support

Application, Reliability



CMOS Readout ASIC Design: Instant Retrigger Technology

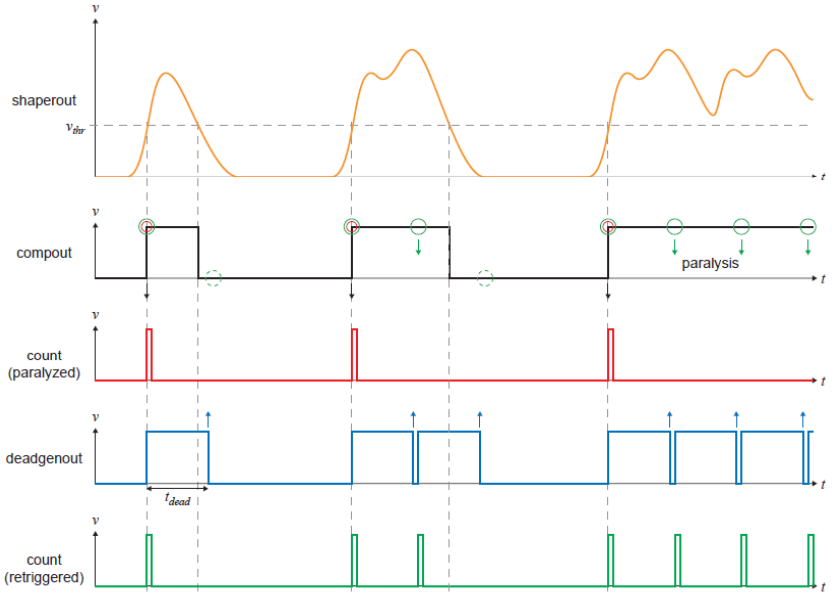


Fig.: Signal waveforms illustrating instant retrigger technology.

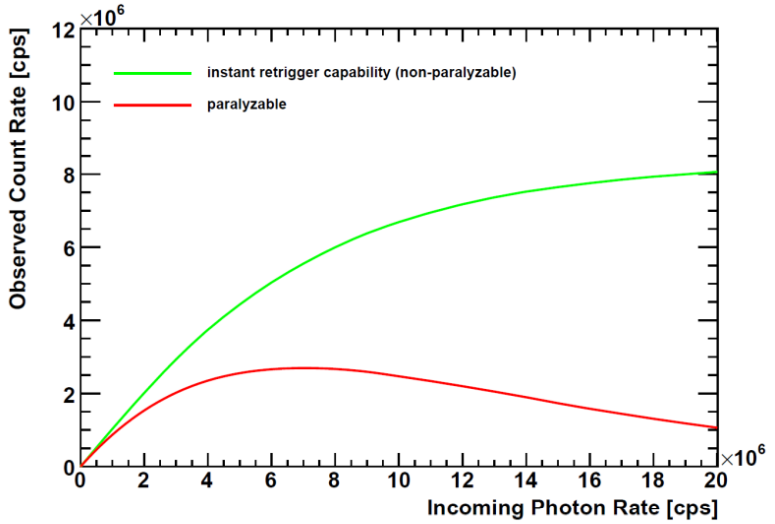


Fig.: Typical count rate characteristics for paralyzed (red) and retriggered (green) counting mode.

- *pulse signal re-evaluation after a predetermined dead time interval after each count and potential retriggering of the counting circuit in case of pulse pile-up*
- *adjustable dead time accounts for the width of a single photon pulse*

➢ *non-paralyzable counting*

➢ *improved **high-rate counting performance***

➢ *enhanced count rate correction*

CMOS Readout ASIC Design: PILATUS3 ASIC Features

- *compatibility with PILATUS2 ASIC*
- *instant retrigger technology with adjustable dead time*
- *improved high-rate counting performance:*
  - *non-paralyzable counting*
  - *counter overflow handling*
  - *improved pixel uniformity*
  - *reduced crosstalk*
  - ➢ *higher local and global **count rates***
  - ➢ *enhanced count rate correction for improved data quality at high count rates*
- *reduced readout time:*
  - ➢ *increased **frame rates***
- *ASIC version with CdTe sensor compatibility:*
  - ➢ ***energy range** extension for high energy applications*

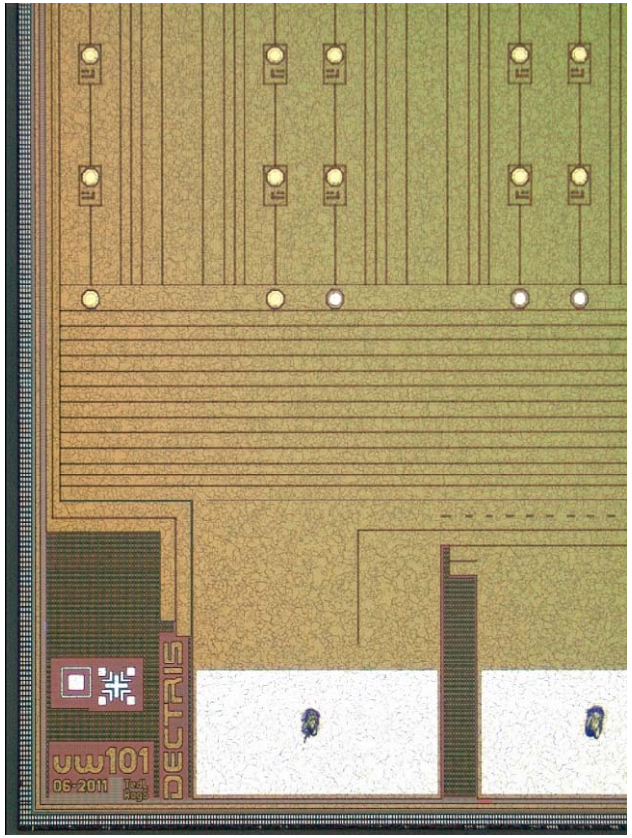


Fig.: Photograph of a detail of the PILATUS3 readout ASIC.

CMOS Readout ASIC Design: PILATUS3 Pixel Circuitry

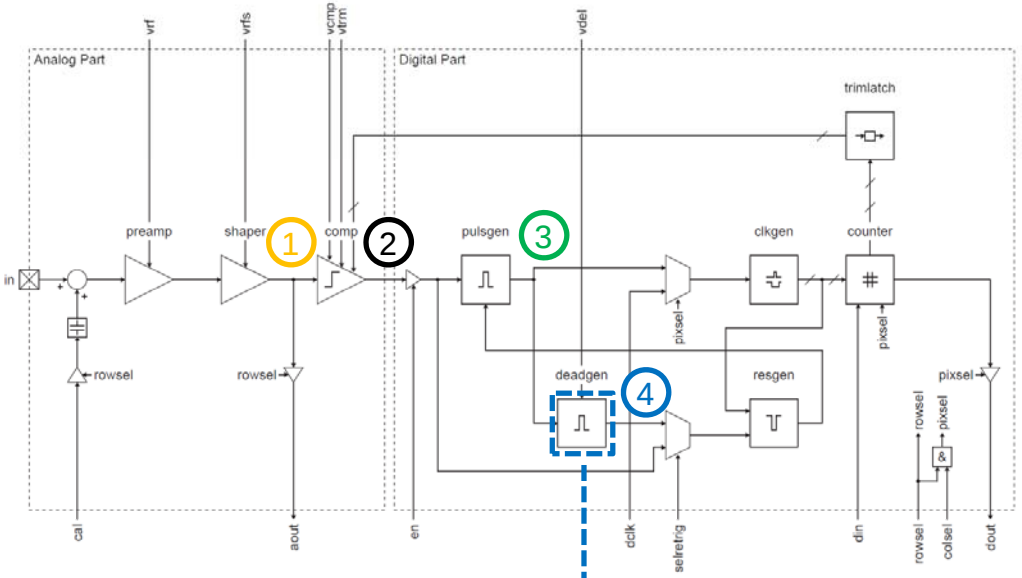


Fig.: Block diagram of the pixel.

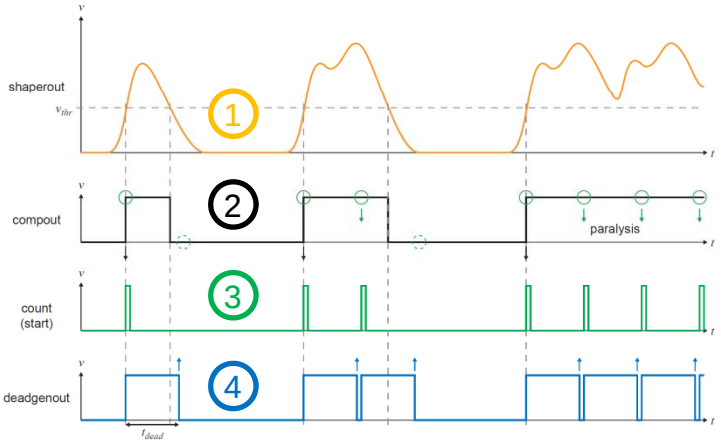


Fig.: Signal waveforms illustrating instant retrigger technology.

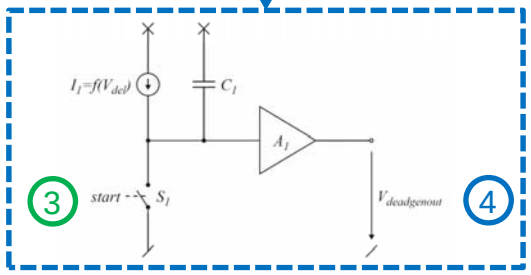


Fig.: Simplified schematic of the dead time generator.

- *selectable counting mode (paralyzed, retriggered)*

CMOS Readout ASIC Design: PILATUS3 Layout

- *UMC 0.25 µm CMOS technology:*
  - *5 metal layers*
  - *thick top metal option (2 µm thick)*
- ***radiation-tolerant layout** (hardness by design):*
  - *enclosed layout transistors (ELT)*
  - *guard rings*
- *pixel size 172 µm x 172 µm*
- *chip size 10.5 mm x 17.5 mm*
- *pin compatibility with PILATUS2 ASIC*
- *improvements compared to PILATUS2:*
  - *power supply routing (resistance, symmetry, isolation, decoupling, grid)*
  - *trimming circuitry (dummies, orientation, centroid)*
  - *readout path (timing, symmetry, coupling)*

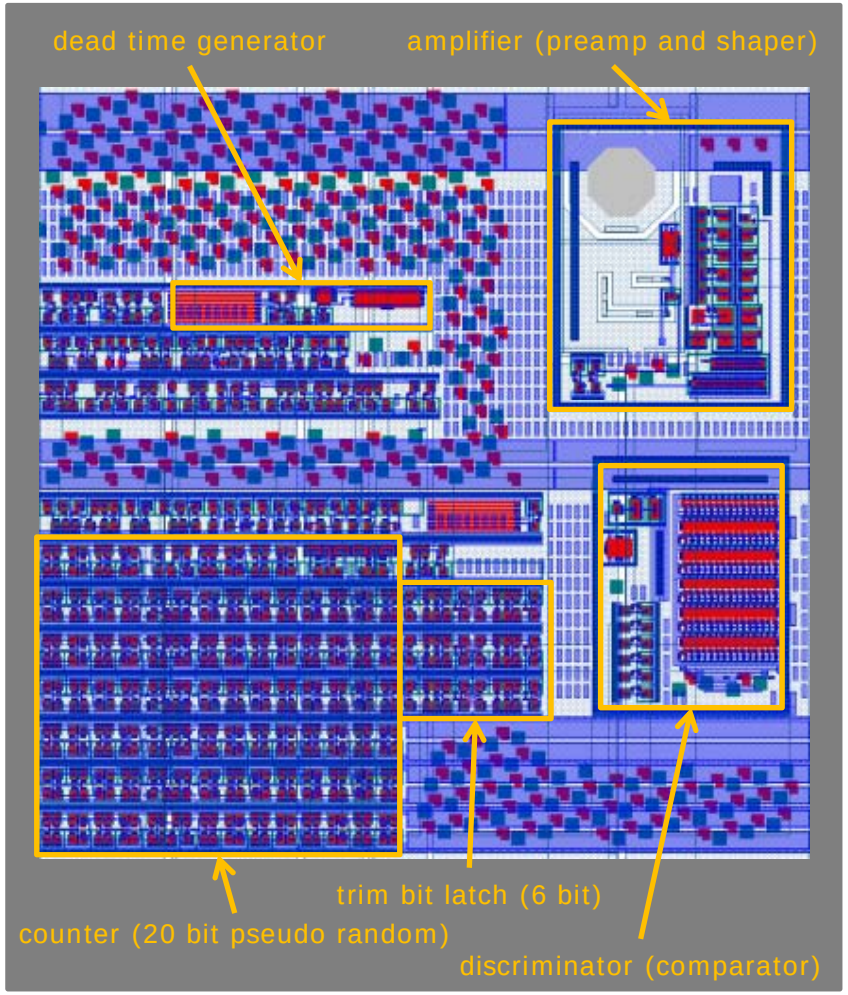


Fig.: Layout of a pixel of the PILATUS3 ASIC.

System Integration: Platforms

- ***ASIC technology*** *platform (130 nm CMOS technology with radiation-hard transistors, radiation-hard libraries)*
- *FPGA-based* ***firmware*** *platform (Xilinx Virtex-5 and Virtex-6; PILATUS2, PILATUS3 and EIGER; VHDL code framework)*
- *new* ***embedded system*** *platform (for different laboratory detector products)*
- ***electronics*** *platform (detector and bank control boards)*
- ***software*** *platform (universal readout system, scalable architecture, unified calibration algorithms; Python, C++, http-based user interface)*

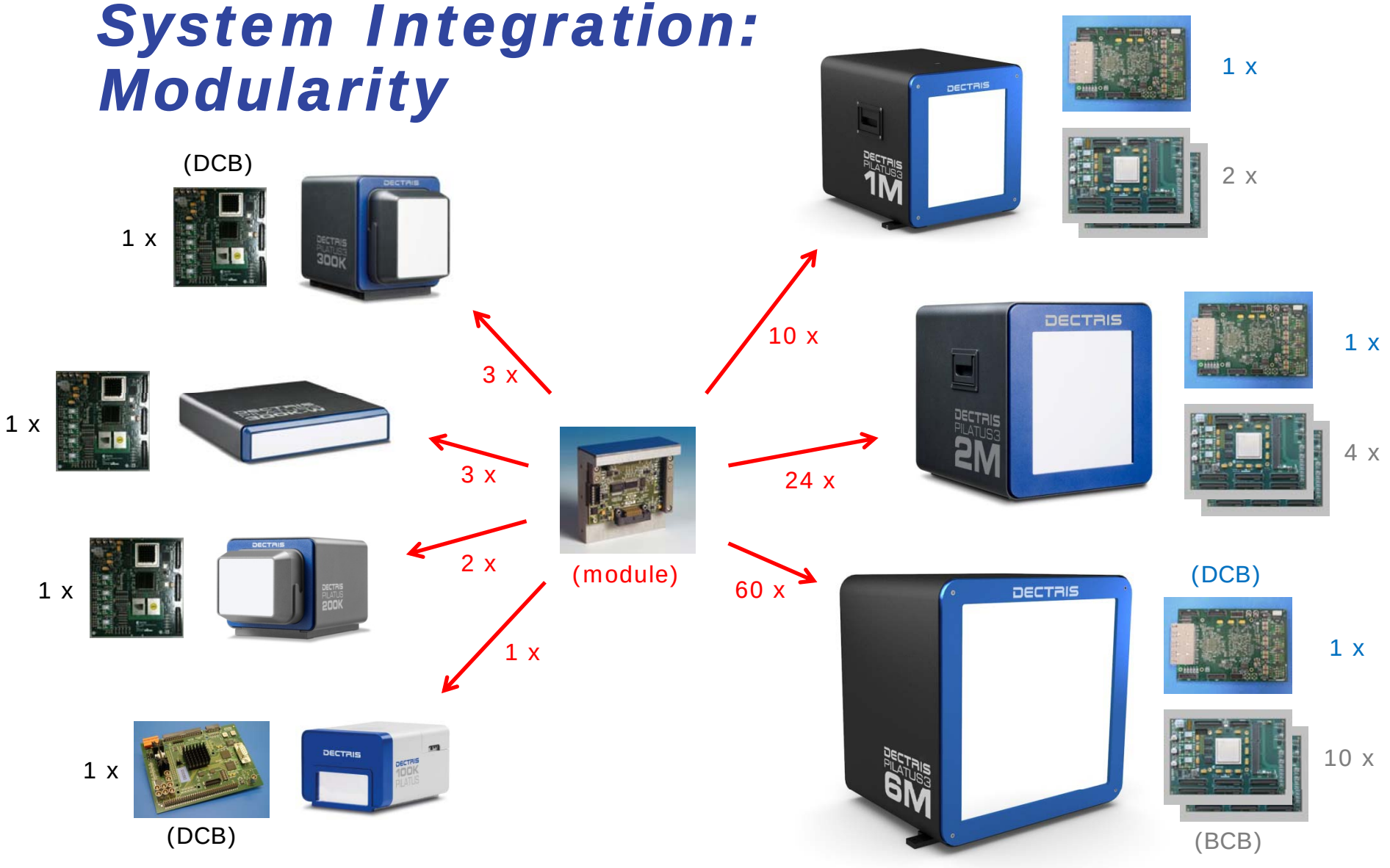
➢ *efficient development efforts through re-use*

➢ *short development cycles*

➢ *synergy effects among products*

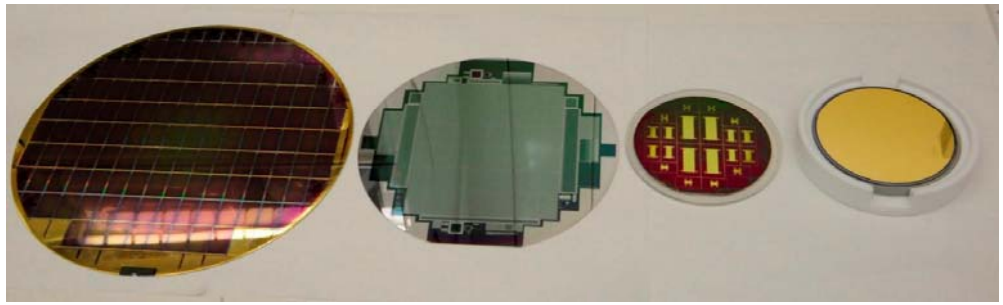
➢ ***platforms are essential for efficient product development***

System Integration: Modularity



System Integration: Micro- and Nano-Technology

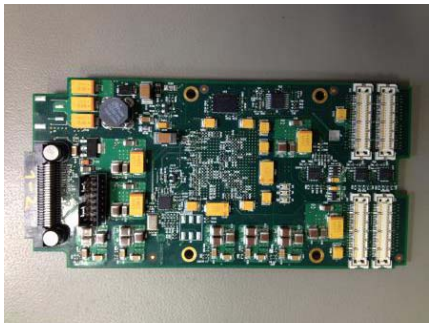
- ***interconnect technology*** *for hybrid-pixel detectors*
- *development of new fabrication processes in micro- and nano-technology*
- *wafer processing of sensors and CMOS readout ASICs in wafer production*
- *quality control in detector production*
- *research and development projects in collaboration with universities and industry*



- *external clean room at Paul Scherrer Institute (PSI) for 200 mm and 150 mm wafer processing*
- ***in-house clean room*** *facilities for assembly*

System Integration: Electronics Design

- *high-speed printed circuit board (PCB) design (up to 16 layers)*
- *complex **high-performance FPGA** programming*
- *challenges:*
  - *high-speed interfaces (multiple 10Gb/s-Ethernet links per board)*
  - *real-time data processing at very high sustained data throughput*
  - *integration of external intellectual property (IP) blocks*
  - *integration of DDR3 memories*



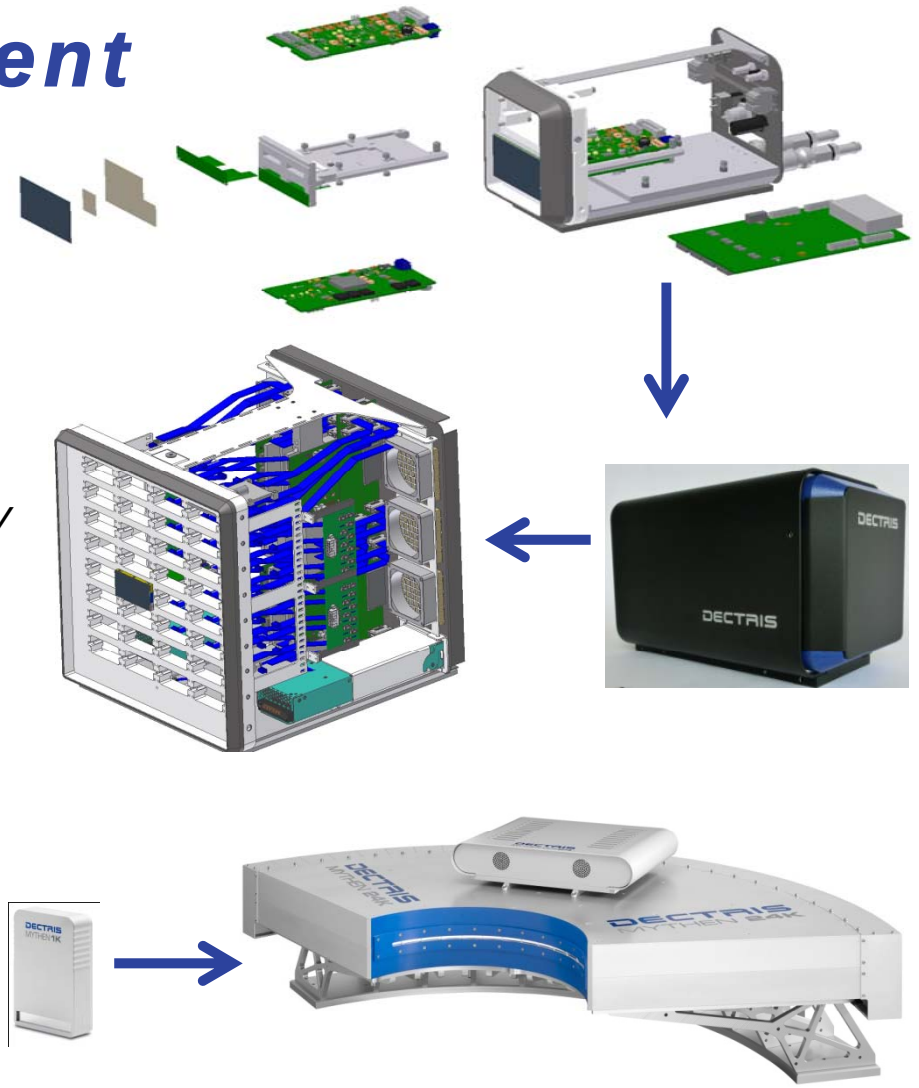
module control board (EIGER)

bank control board (PILATUS)

detector control board (EIGER)

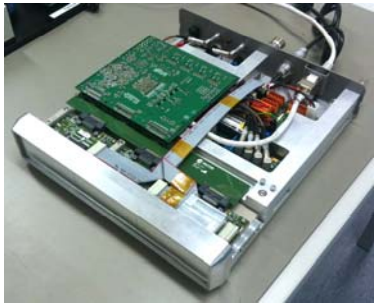
System Integration: Product Development

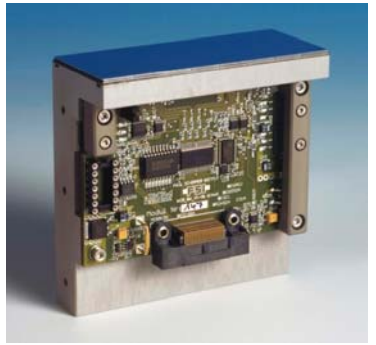
- *development of **fully integrated solutions***
- *system integration challenges:*
  - *ultra-high bandwidth data transfer (40 Gb/s detector readout and data transfer to storage)*
  - *mechanical engineering for extremely compact designs*
  - *advanced algorithms for detector calibration*
  - *diverse product variations (sensor material, sensor thickness, frame rate, detector size)*
- *specific solutions (vacuum compatibility, specific detector geometry, ...)*
- ***qualification** of new products based on pilot series production*

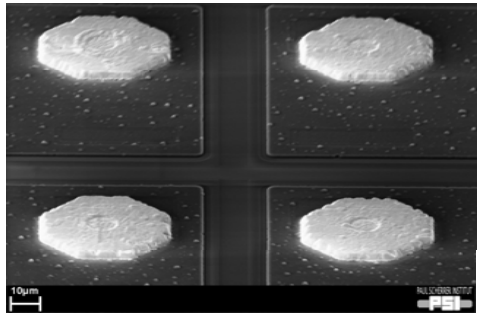


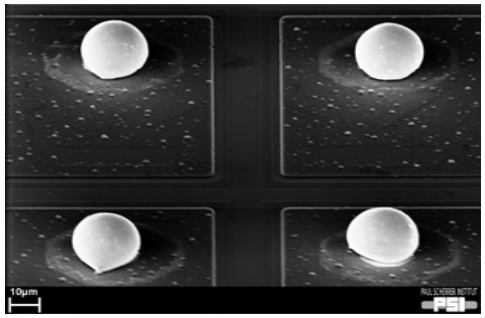
System Integration: Production

- ***pilot series production*** *for* ***series production*** *take-over*
- *robust* ***testing*** *(wafer test, optical chip inspection, chip test, bare-module test, module tests) as an essential part of the manufacturing process to achieve high yield*
- ***high in-house production depth*** *(from wafer processing to final detector calibration)*
- *core technologies using in-house clean room facilities (bump bonding, wire bonding, module assembly)*
- *Swiss quality provided by mostly Swiss suppliers*
- *quality assurance (e.g. factory acceptance tests)*









Conclusions

- *single-photon counting detectors achieve excellent signal-to-noise ratio, very high dynamic range, and high frame rates*
- *hybrid-pixel detectors use separately optimized solid-state sensors and CMOS readout ASICs to guarantee highest quality*
- *successful detector development is based on a well-structured process with many disciplines involved and clearly defined decision points*
- *advanced CMOS technologies offer high performance and wide functionality for continuous improvements in detector performance*
- *a small company is able to sustainably supply leading-edge detector technology*

DECTRIS®

detecting the future

DECTRIS Ltd.
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