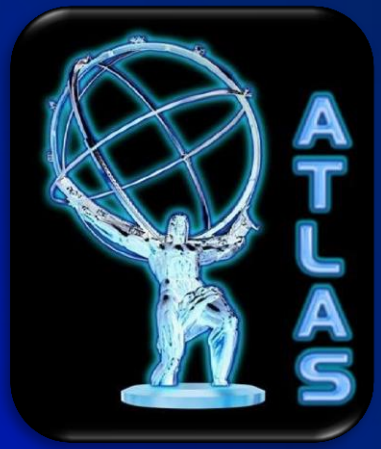

VMM ASIC

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Status Report - April 2013

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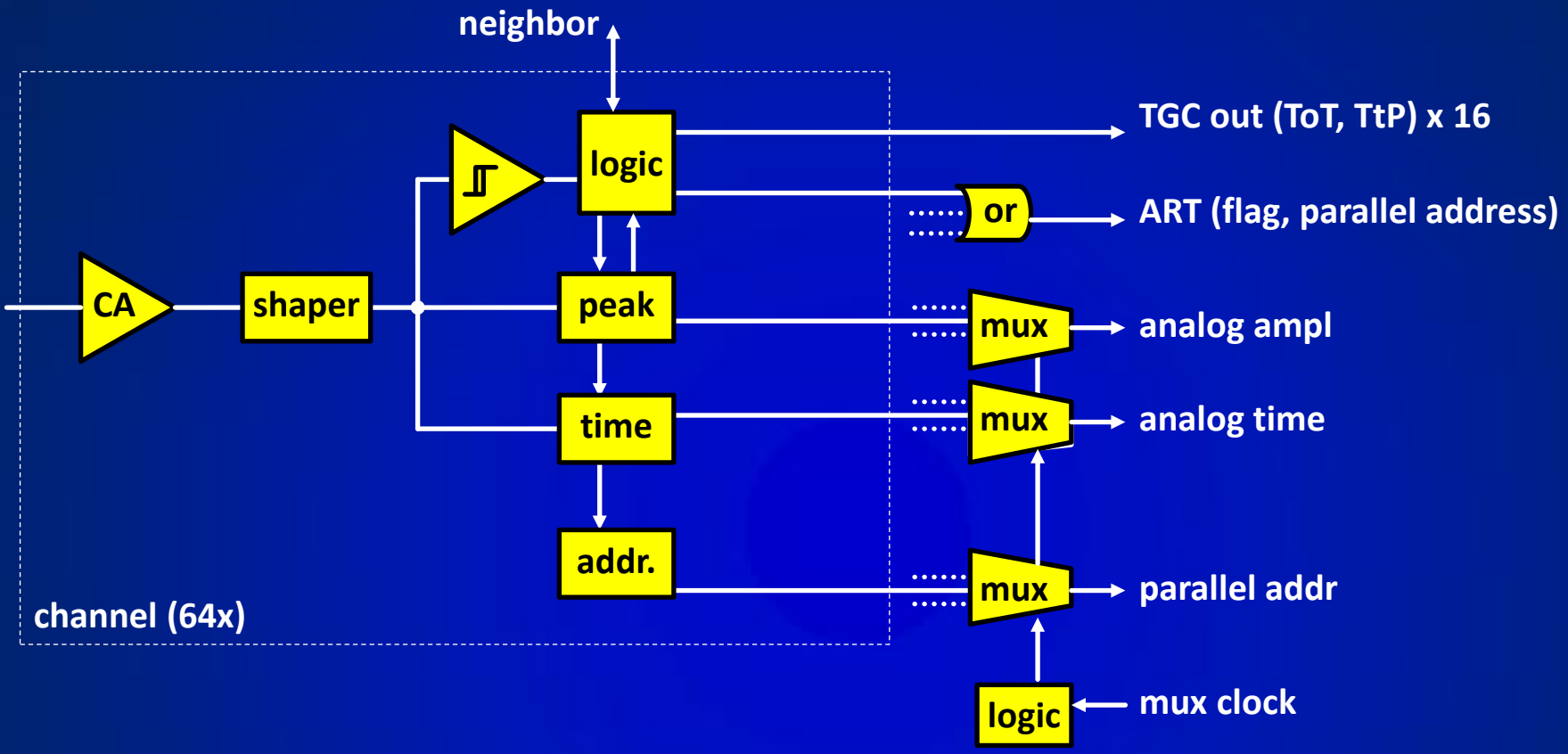
Outline

- VMM1 - tested
  - architecture and results (brief)
  - issues
- VMM2 - in design
  - architecture
  - fixes (issues from VMM1)
  - new features
  - pinout and packaging (tentative)
  - schedule (tentative)

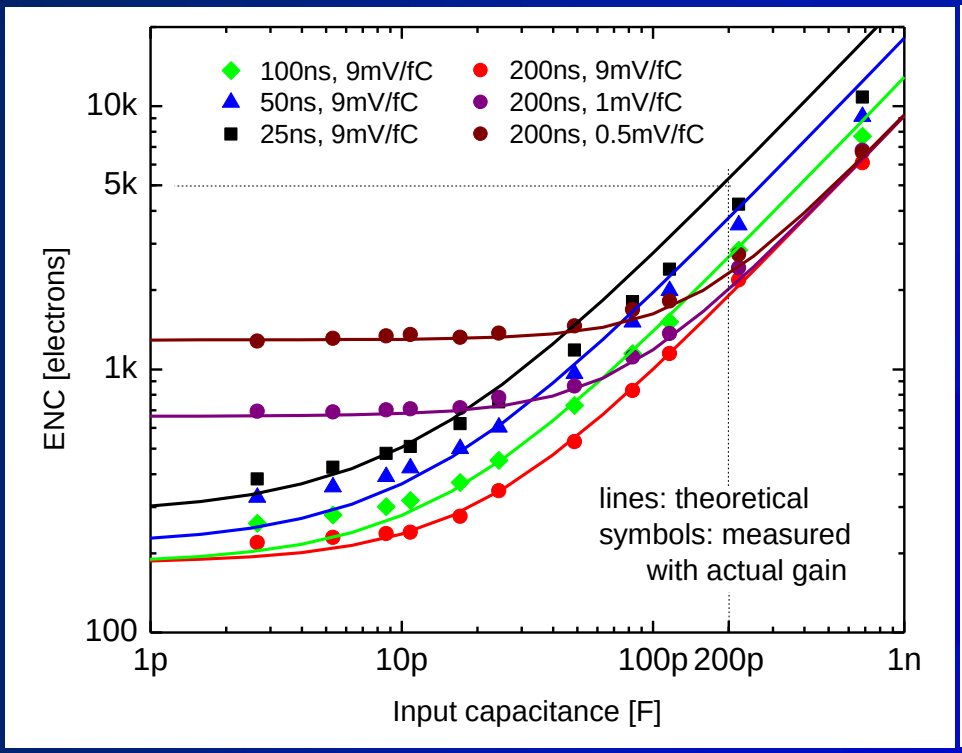
Architecture of VMM1



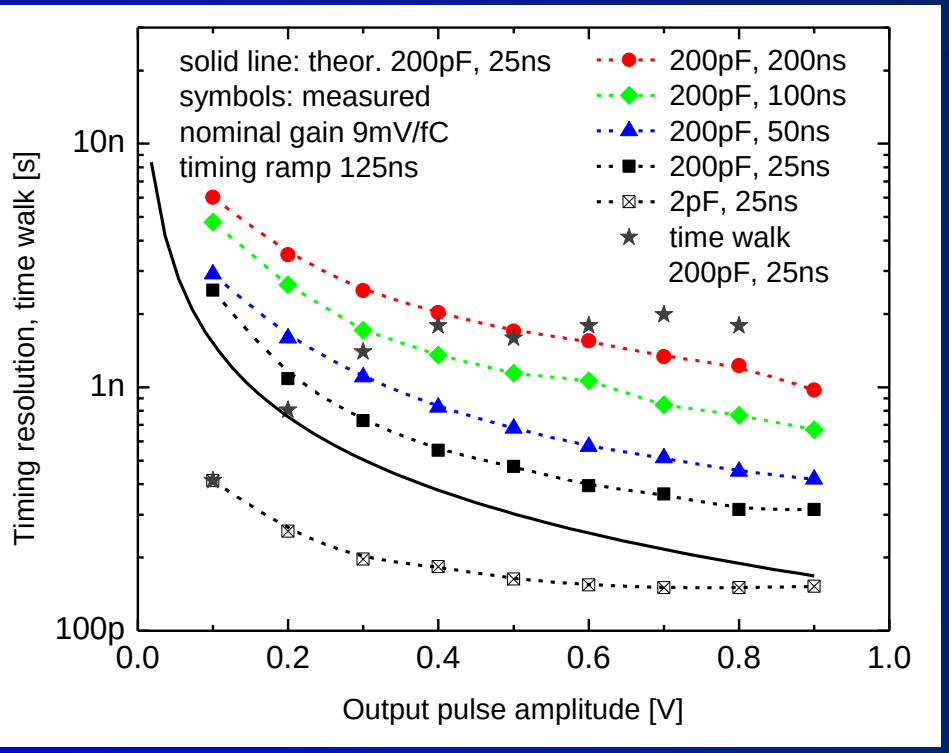
- dual polarity, adj. gain (0.5-9 mV/fC), adj. peaktime (25-200 ns), DDF shaper
- discriminator with sub-hysteresis and neighboring (channel and chip)
- address of first event in real time at dedicated output (ART)
- 16 direct timing outputs: time-over-threshold or time-to-peak
- peak detector, time detector <1 ns
- multiplexing with sparse readout and smart token passing (channel and chip)
- threshold & pulse generator, analog monitor, mask, temperature sensor, 600mV BGR, 600mV LVDS
- power 4.5 mW/ch, size 6 x 8.4 mm^2, process IBM CMOS 130nm 1.2V, test structures

Resolution Measurements

Charge



Timing

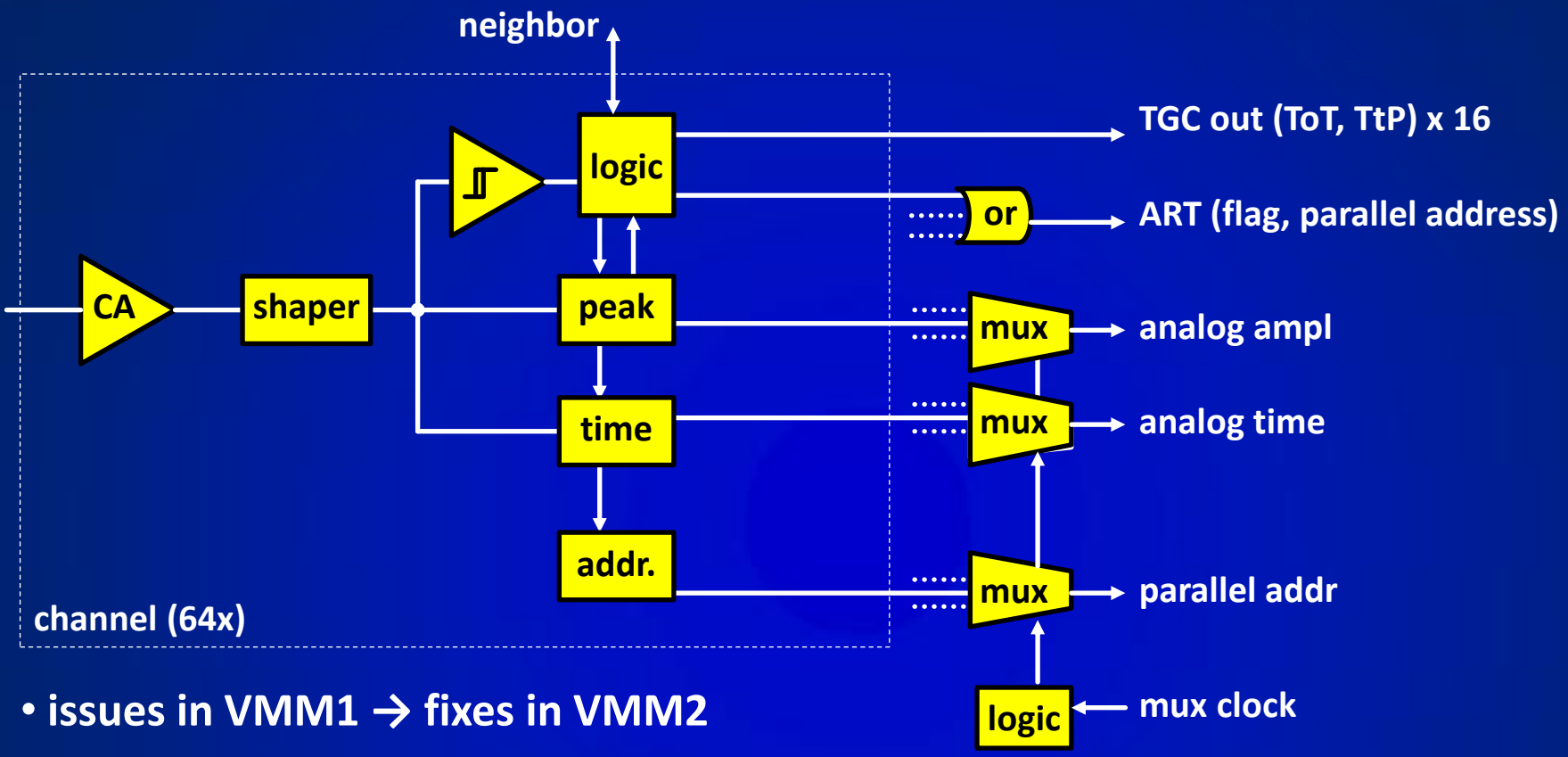


- **charge resolution** ENC < 5,000 e^- at 25 ns, 200 pF
- **analog dynamic range** Q_{max} / ENC > 12,000 → DDF
- **timing resolution** < 1 ns (at peak-detect)

$$\sigma_t \approx \frac{ENC\ \tau_P}{Q}\frac{\lambda_P}{\rho_P}$$

≈ 0.3-0.8

Architecture of VMM2



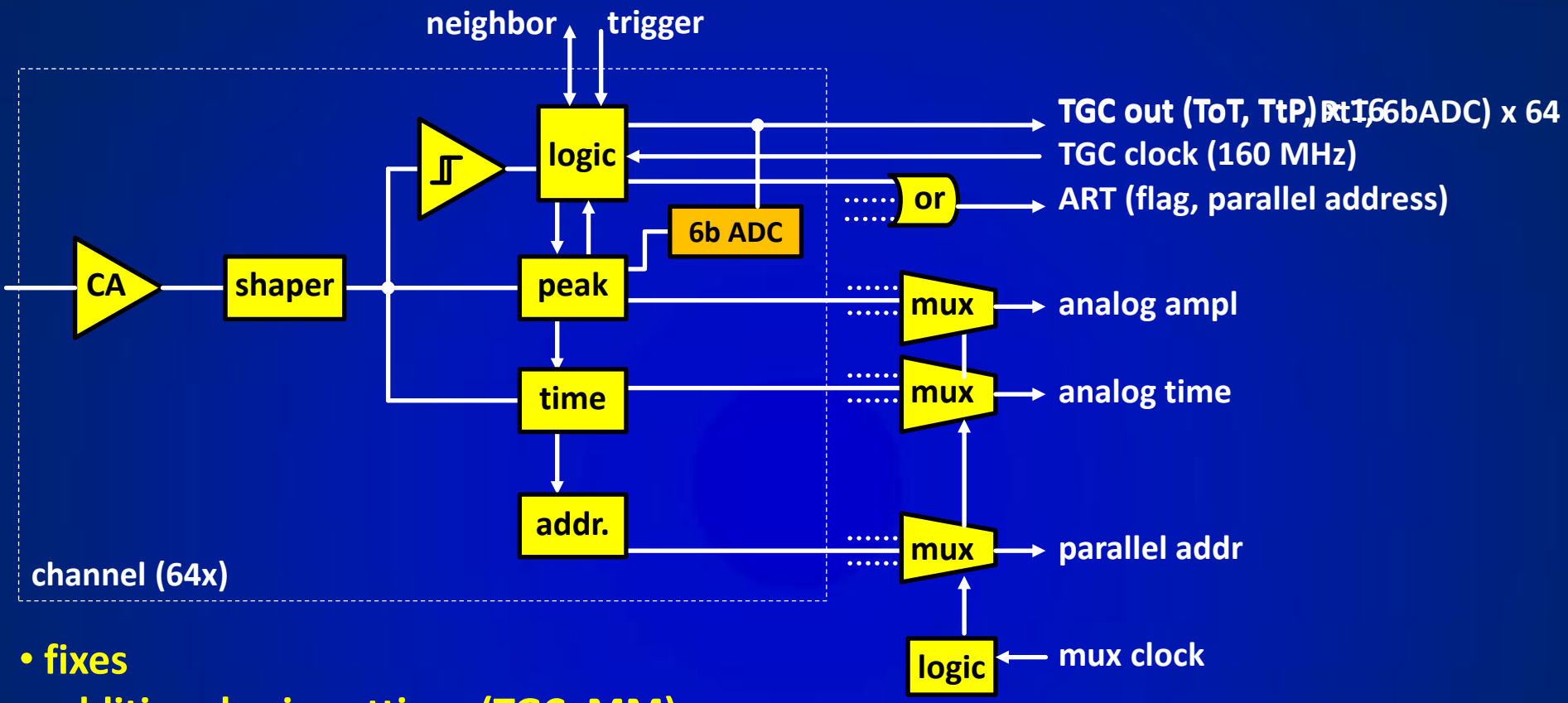
- issues in VMM1 → fixes in VMM2

Note: VMM2 will maintain all the functionalities of VMM1

Issues in VMM1 → Fixes in VMM2

- **power distribution**
  - voltage drop across power and ground wire-bonds
- **front-end**
  - stability at large capacitance (affects peaking time and gain)
  - saturation at high rate
  - leakage from ESD protection (disables positive charge operation)
  - test pulse linearity, settling time, range (needs optimization)
  - ESD protection (may need optimization)
- **discrimination**
  - digital pick-up in sub-hysteresis (affects low amplitudes)
  - threshold dispersion and trimming (needs optimization)
- **signal processing**
  - peak detector stability (affects low amplitudes)
- **direct timing (TGC)**
  - digital pick-up on pulse tail
  - delay and time walk (needs optimization)
  - possible locking in TtP mode
- **test and readout**
  - internal reset optimization
  - dedicated input for test-pulse strobe

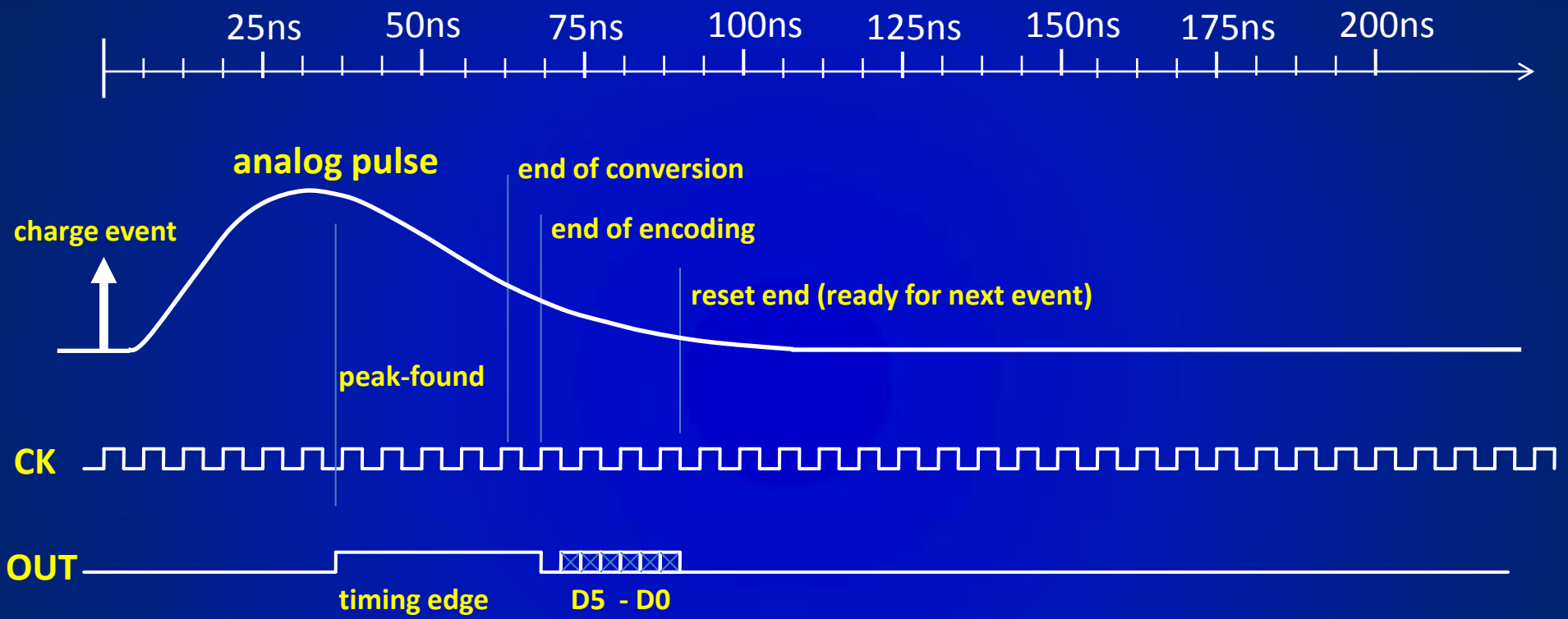
Architecture of VMM2



- fixes
- additional gain settings (TGC, MM)
- external trigger
- TGC: 64 outputs, 6-bit ADC 25ns serialized with dedicated clock

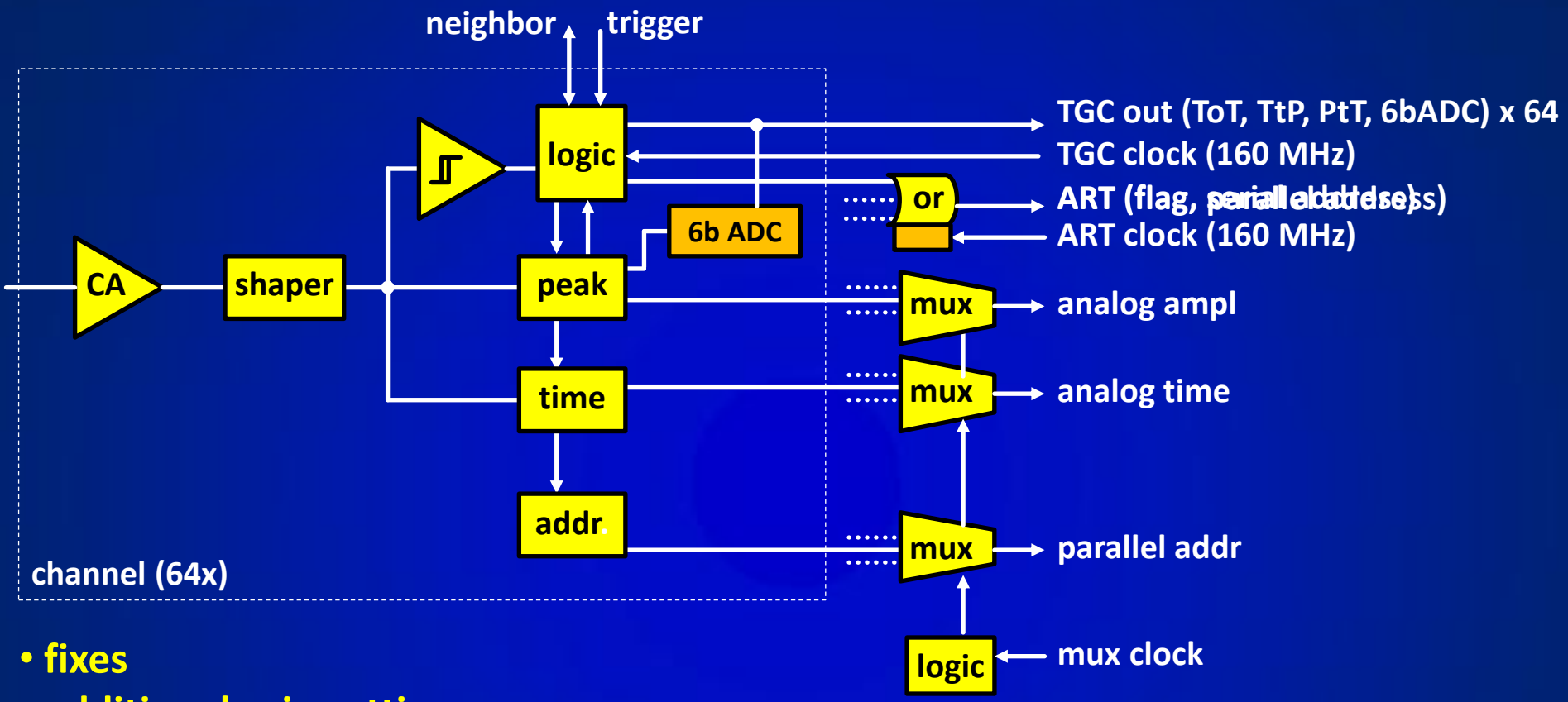
Note: VMM2 will maintain all the functionalities of VMM1

TGC ADC and Serializer



- 160 MHz external clock
- Conversion ends ~25ns after peak-found, programmable
- Dead time from charge event <100ns
- Amplitude data D5-D0 shifted at each clock edge

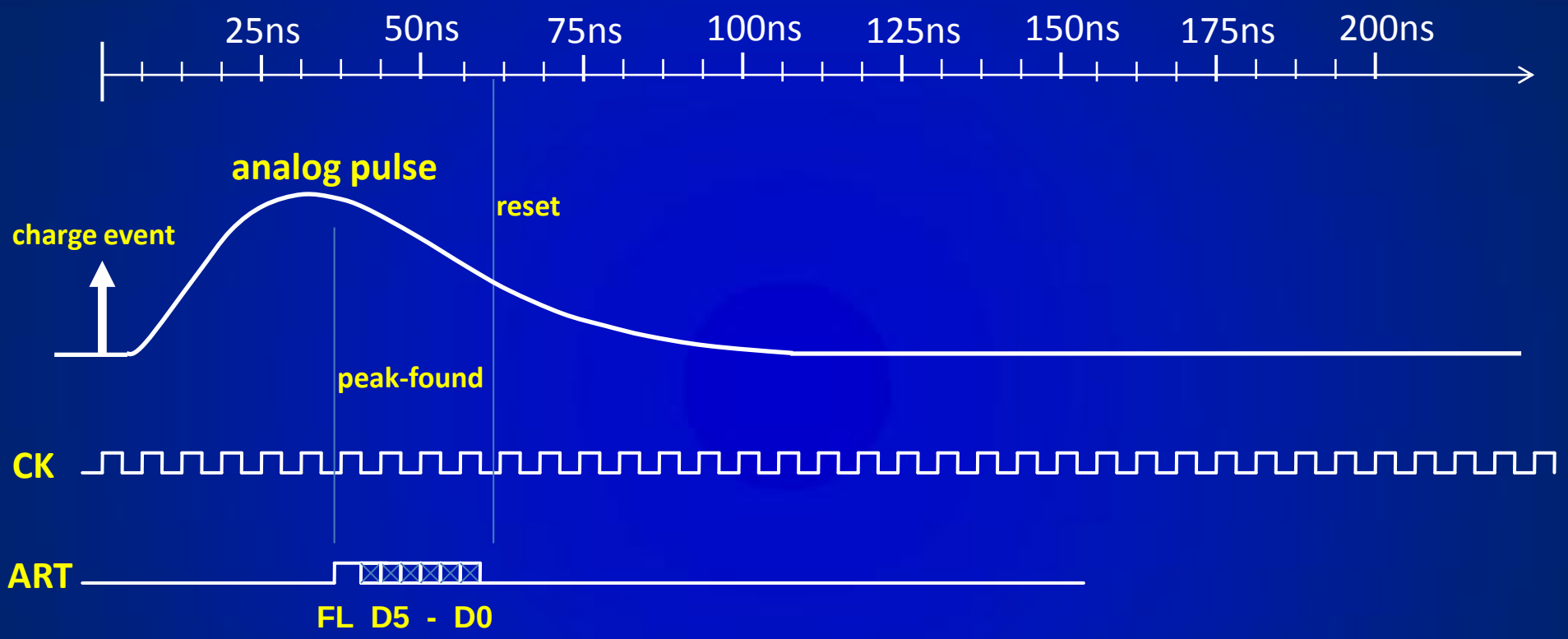
Architecture of VMM2



- fixes
- additional gain settings
- external trigger
- TGC: 64 outputs, PtT, 6-bit ADC 25ns serial with dedicated clock
- ART: flag and address serialized with dedicated clock

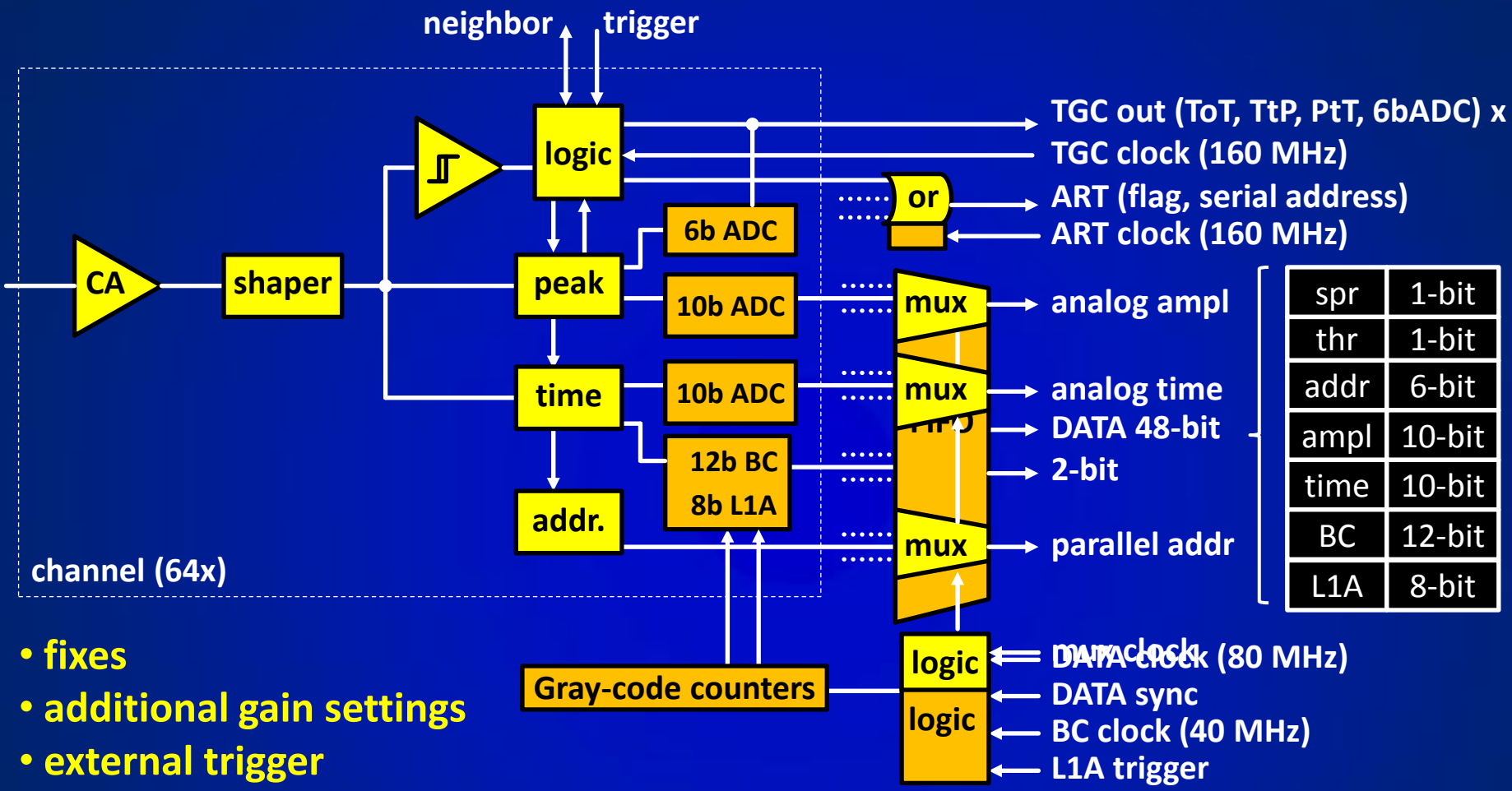
Note: VMM2 will maintain all the functionalities of VMM1

ART Serializer



- 160 MHz external clock
- Flag and address serialized
- Address data D5-D0 shifted at each clock edge

Architecture of VMM2



- fixes
- additional gain settings
- external trigger
- TGC: 64 outputs, PtT, 6-bit ADC 25ns serial with dedicated clock
- ART: flag and address serialized with dedicated clock
- 10-bit ADCs 200ns for amplitude and timing, digital memories
- Gray-code counters for BC-ID (12-bit) and L1A-ID (8-bit)
- 2-bit DATA output with dedicated sync and 80 MHz clock

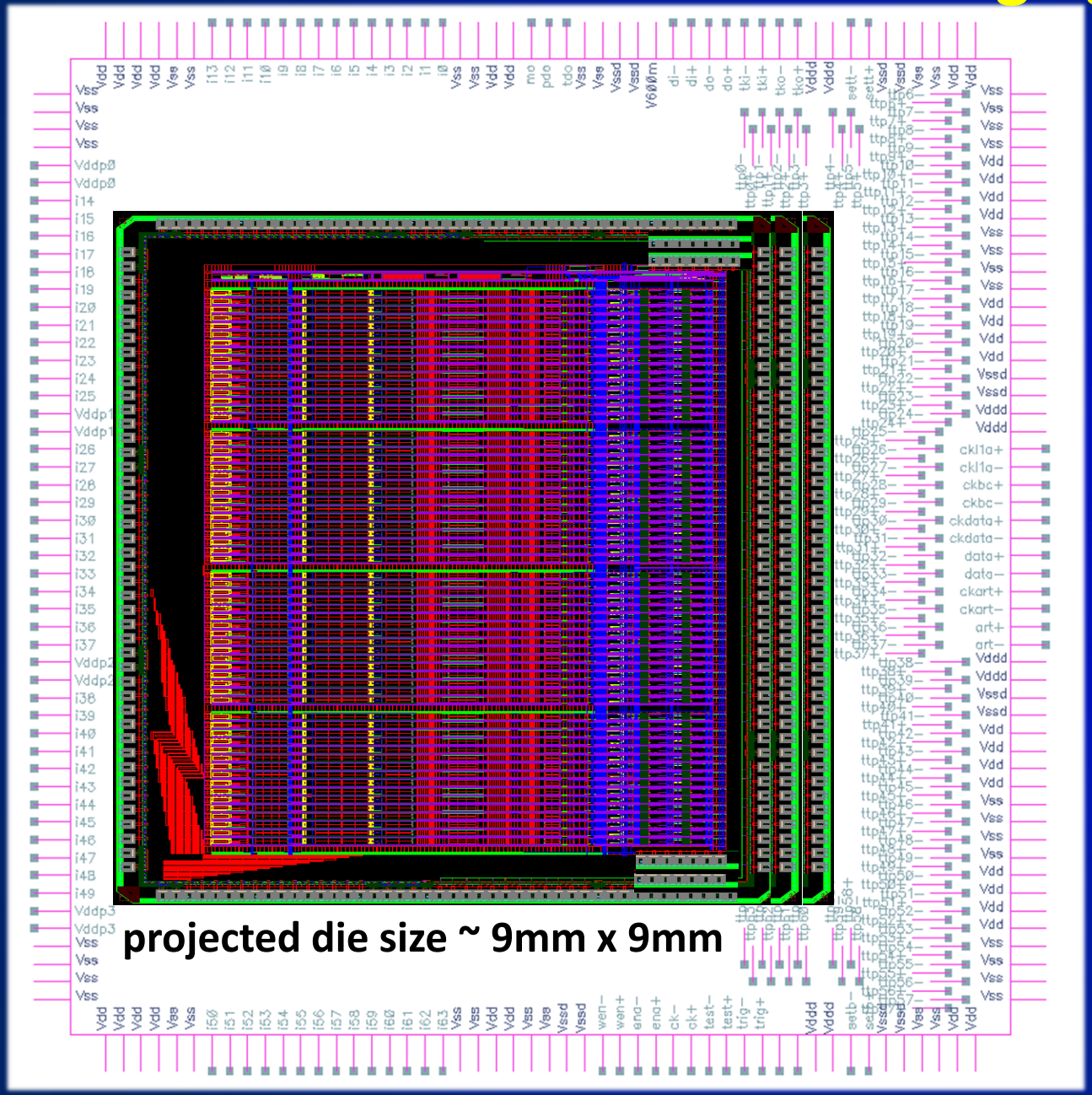
Note: VMM2 will maintain all the functionalities of VMM1

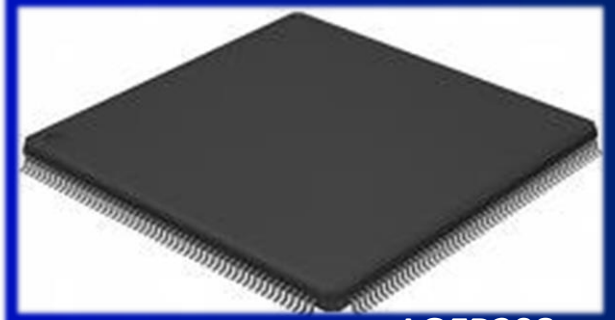
New Features

- **front-end**
  - additional gain settings to match signal sfrom TGC and MicroMegas
  - option to route monitors to PDO, TDO outputs for baseline acquisition
- **signal processing**
  - multi-phase current-output peak detector [1]
  - ADC 10-bit 200ns on PDO and TDO [1]
  - digital buffer, multiplexing, and logic for continuous acquisition [1]
  - counters and latches for BC-ID (12-bit) and L1A-ID (8-bit) [1]
- **ART (address in real time)**
  - serialized flag and address
- **trigger**
  - external trigger for non-data-driven operation
- **direct timing (TGC)**
  - from 16 to 64 channels (initially packaging-limited to 32)
  - pulse at peak (like ART)
  - ADC 10-bit 25ns with serial output after flag [1]
  - *fixed ramp discharge (PtT)* [2]
- **layout and packaging**
  - pads count from 176 to 208
  - dual-mode wire-bond (MM, TGC)
- **radiation tolerance**
  - off-ITAR switch circuit (CERN), *optimization* [2]

[1] Major developments
[2] *If time allows*

Pinout and Packaging





LQFP208

Schedule and Status

task	status
fixes	in progress ~50%
external trigger	complete
ART serializer	in progress ~30%
current-output PD	complete
6-bit ADC and serializer	complete
10-bit ADC and digital buffer	in progress 70%
counters and latches	queued
analog gain	queued
physical layout	June-July 2013
fabrication	**August 2013 (tentative)**

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