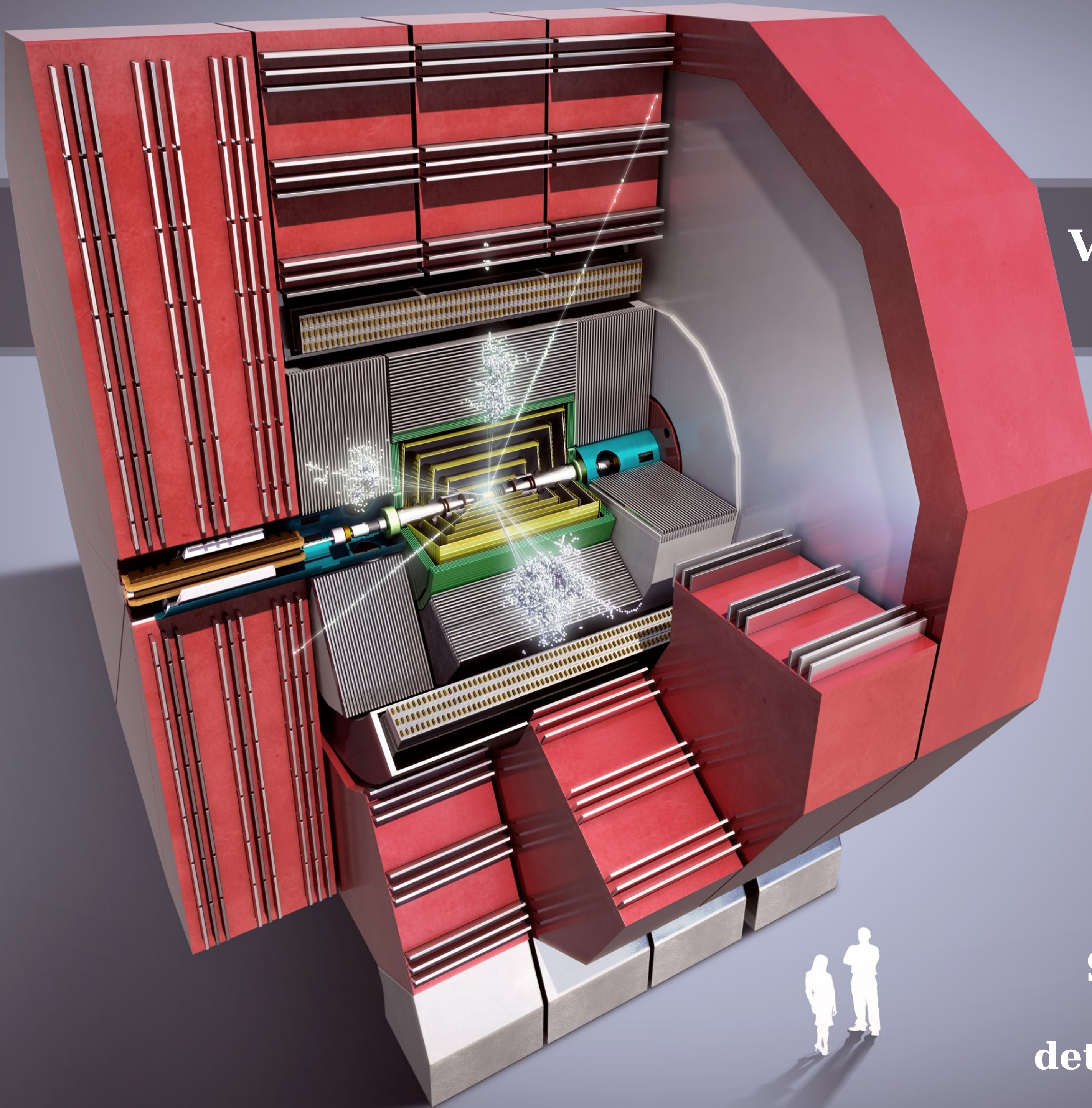

Vertex Detector R&D for CLIC

Szymon Kulis (CERN)
on behalf of the CLIC detector and physics study

Vertex 2013 Lake Starnberg, Germany, 16-20 September 2013

Agenda

- Compact Linear Collider (CLIC)
- Vertex detector at CLIC
- R&D programs
  - Thin sensor assemblies
  - Readout chip (CLICpix)
  - Power delivery and power pulsing
  - Cooling concept
  - Mechanical integration
- Summary

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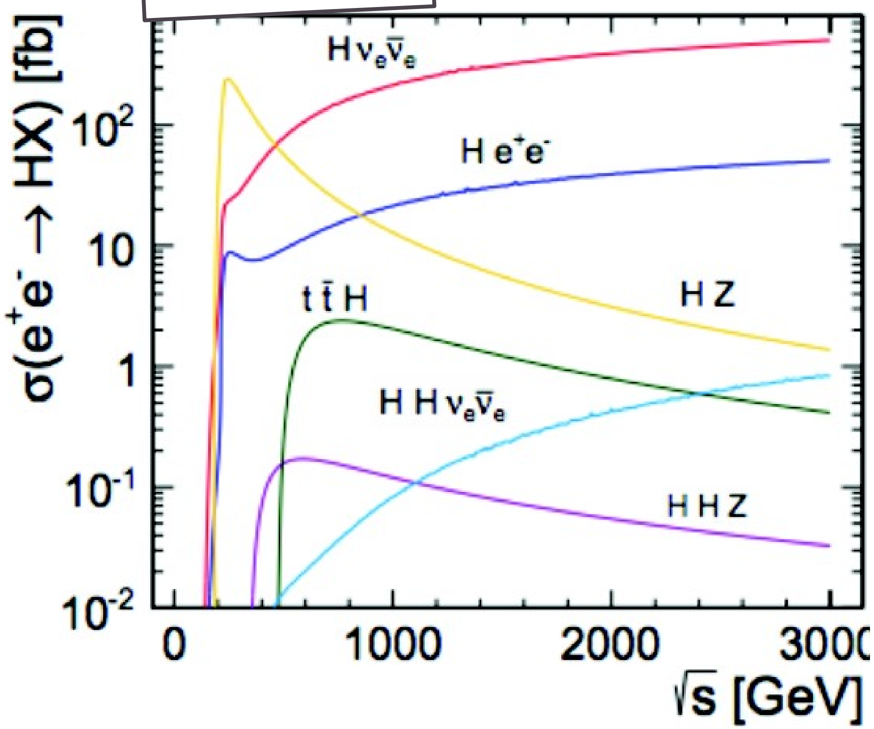
- Pre-collaboration structure based on **"Memorandum of Cooperation"** (MoC): http://lcd.web.cern.ch/lcd/Home/MoC.html
- CERN acts as host laboratory
- At the moment 18 institutes from 15 countries, **more contributors most welcome!**

  [The accelerator R&D is being conducted in collaboration with ~48 institutes]

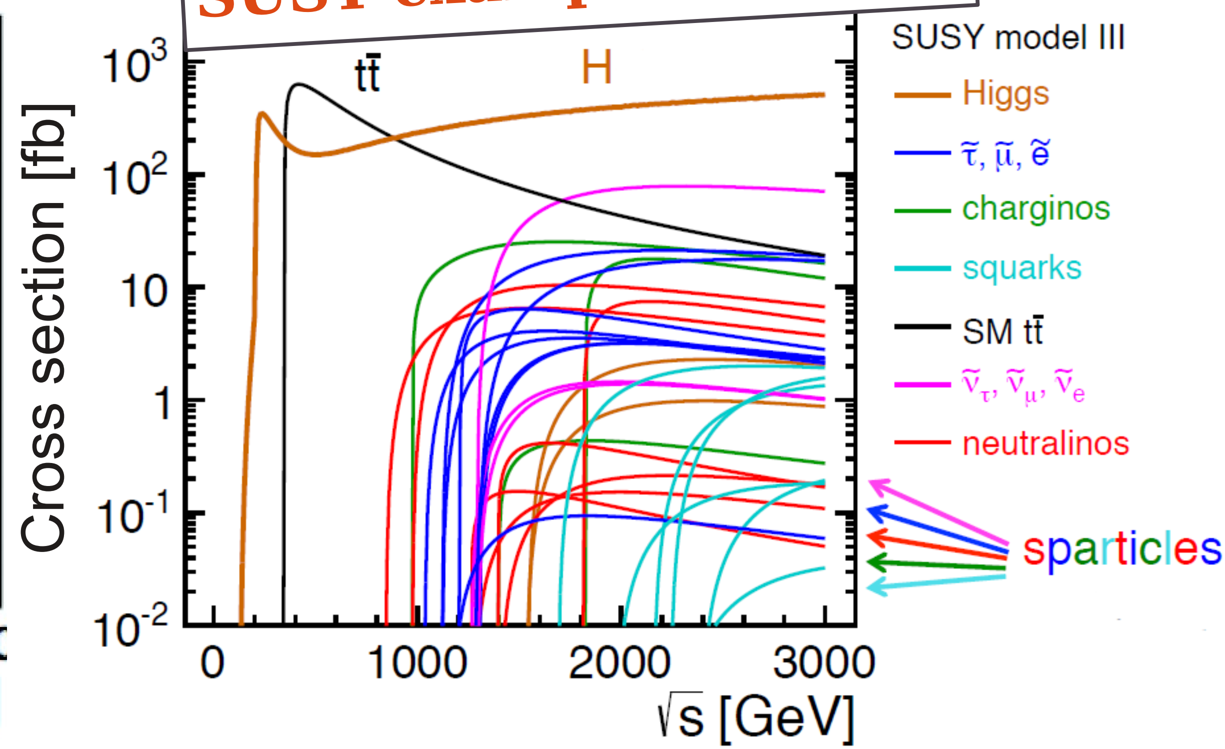
CLIC: concept for e^+e^- linear collider with √s up to 3 TeV, aiming at performing precision measurements of Standard Model (Higgs, top) and seeking new physics beyond Standard Model

… its program is complementary to LHC

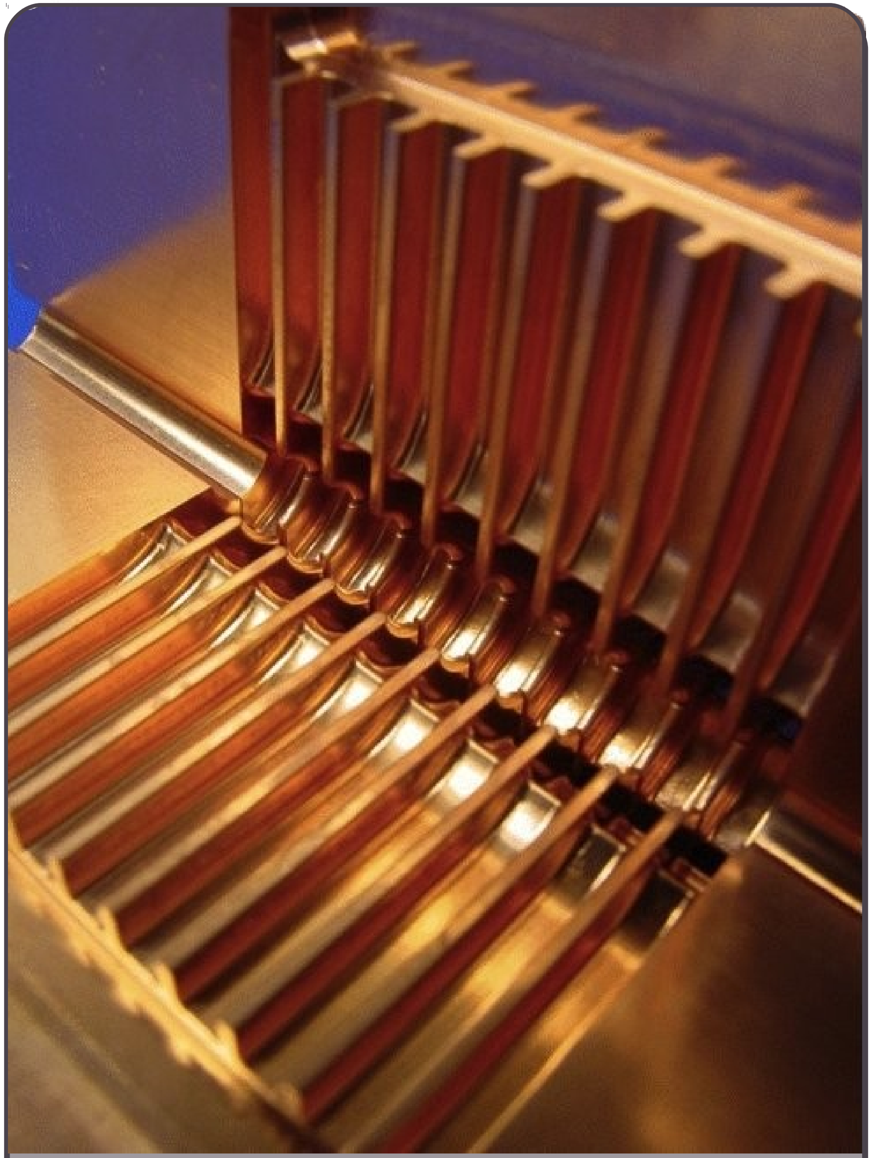
HIGGS



SUSY example scenario



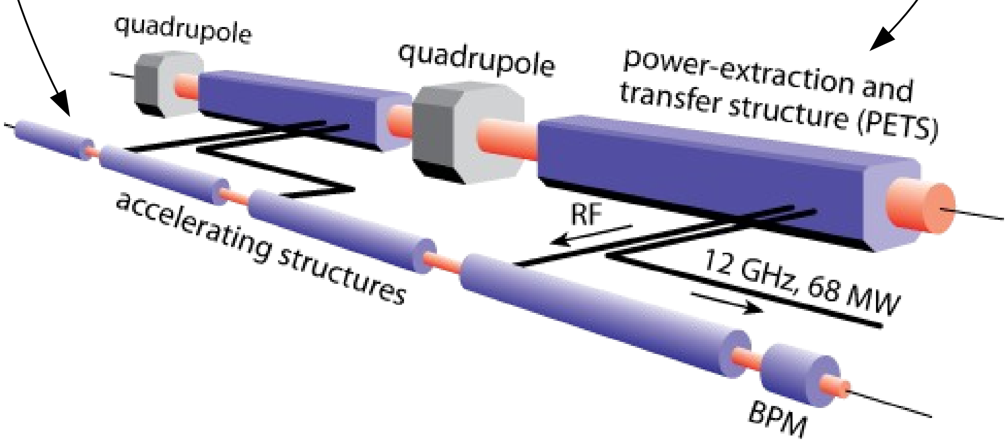
CLIC Accelerator



Acceleration Structure

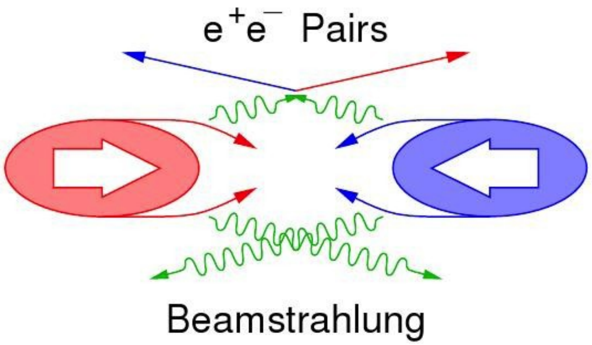
Two Beam Acceleration Scheme

- Drive Beam supplies RF power
  - 12 GHz bunch structure
  - Low energy: 2.4 GeV - 240 MeV
  - High current: 100A
- Main beam for physics
  - High energy: 9 GeV – 1.5 TeV
  - Current: 1.2 A
  - Gradient: 100 MV/m

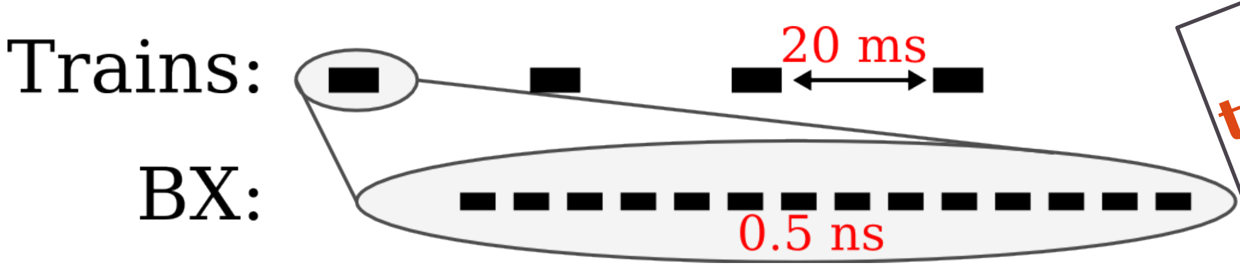


CLIC Machine environment

- Beam profile: **45 nm / 1 nm / 44 μm** (σx / σy / σz)
  → high E-fields → **beam related background**
  - incoherent e+e- pairs:
    ($9 \cdot 10^7$ particles per bunch train, at small angles)
  - $\gamma\gamma$ → hadrons:
    (10^3 events per bunch train expected)



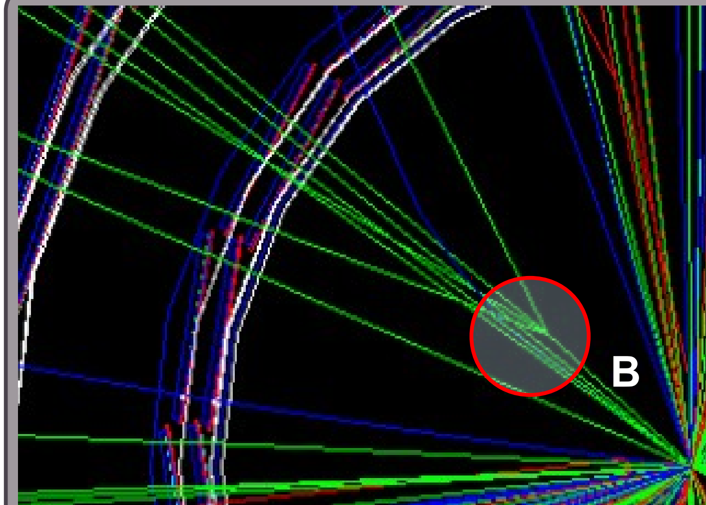
- Time beam structure:
  - Bunch crossing separation : **0.5 ns**
  - Bunches per train : 312 **(156 ns)**
  - Repetition rate : 50 Hz



Drives **timing requirements** for CLIC detectors

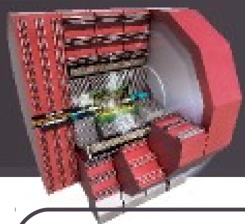
Vertex Detector Requirements

- Efficient tagging of heavy quarks
  (through precise determination of displaced vertices)
  - good single point resolution: **σ_{SP}~3 μm**
    → small pixels <**~25x25 μm²** (analog readout)
  - low material budget: **X ≲ 0.2% X_0 / layer**
    (corresponds to ~200 μm Si, including supports, cables, cooling)
    → very thin sensors and ASIC (**~50 + 50 μm**)
    → gas-flow cooling
    → low-power ASICs (**~50 mW/cm²**)



Displaced Vertex Event (MC)

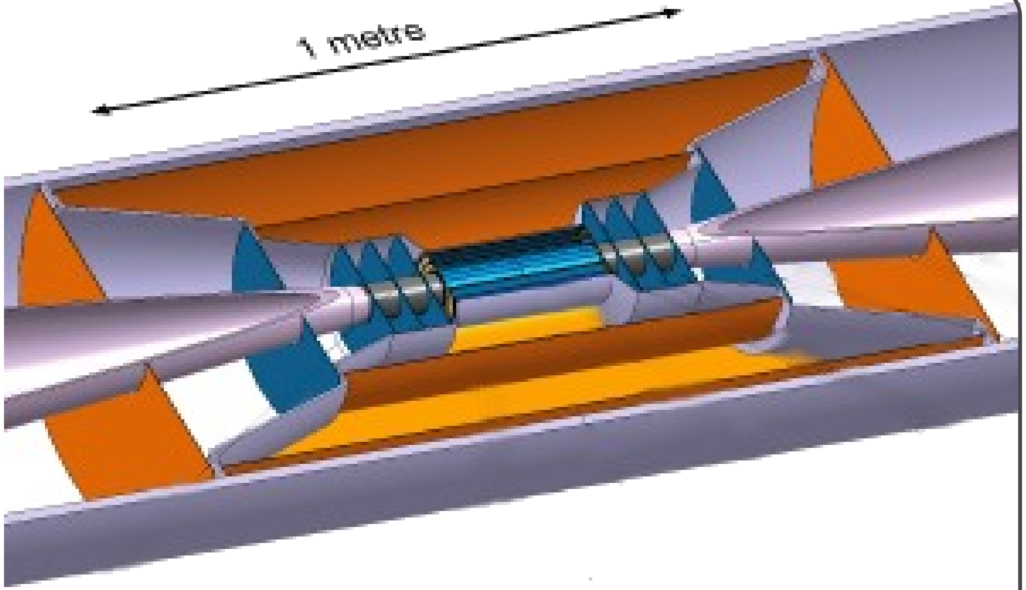
- 156 ns bunch trains → **trigger-less readout**
- 20 ms gaps between trains → **power pulsing**
- High magnetic field (4-5 T) → Lorentz angle becomes important
- Maximum **occupancy of few %** (from beam-induced backgrounds)
  → **time stamping ~10 ns** (high-resistivity sensors, fast readout)
- Moderate radiation exposure (NIEL < 10^{11} n_{eq}/cm²/y, TID < 200 Gy / year)



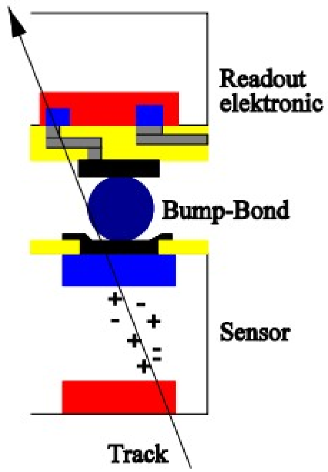
Vertex Detector Concepts

Geometry

- Barrel + endcap
- 5-7 detection layers arranged in singlets or doublets
- Inner radius ~ 30 mm (very close to beam)



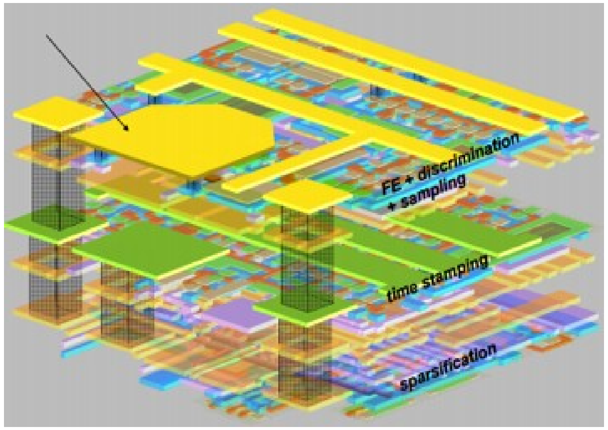
CLIC_ILD inner tracking layout



Hybrid

Technology options:

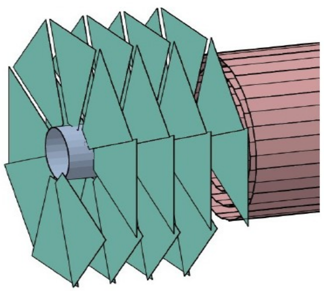
- Hybrid with ultra-thin sensors and ASICs (VDSM), TSV
- Emerging technologies: 3D-integrated, SOI…



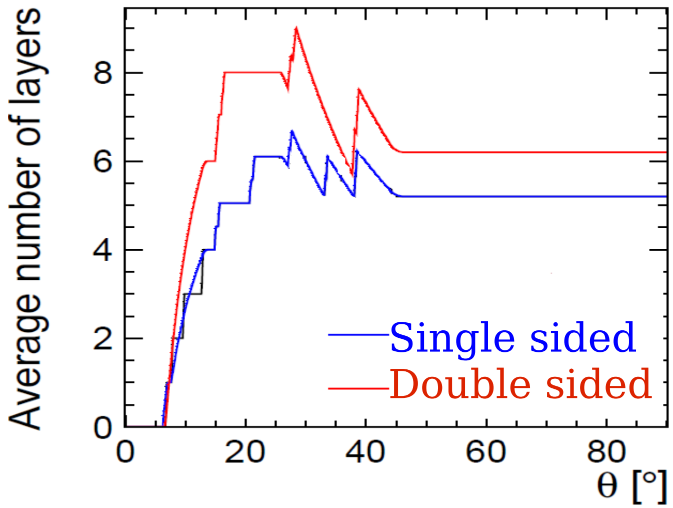
3D-integrated

Use flavor-tagging performance as benchmark for detector layout optimization

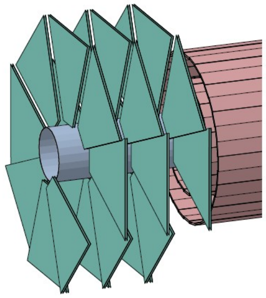
Single sided



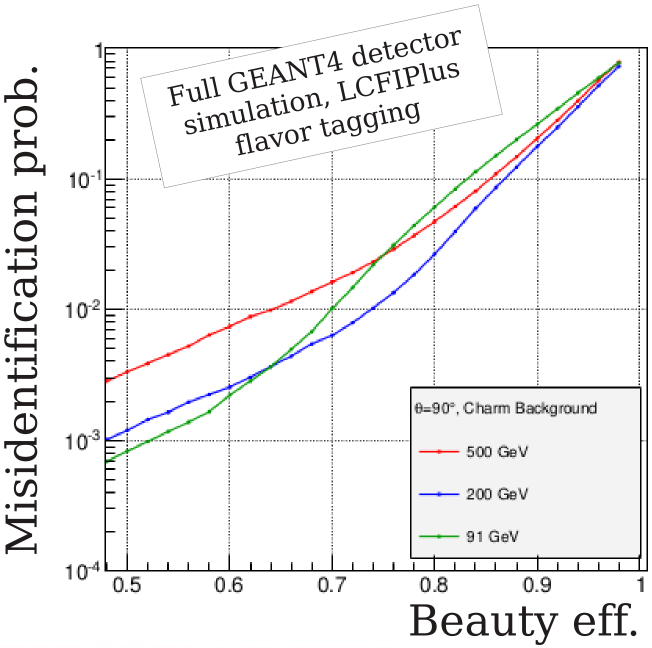
(5 barrel + 4 endcap)

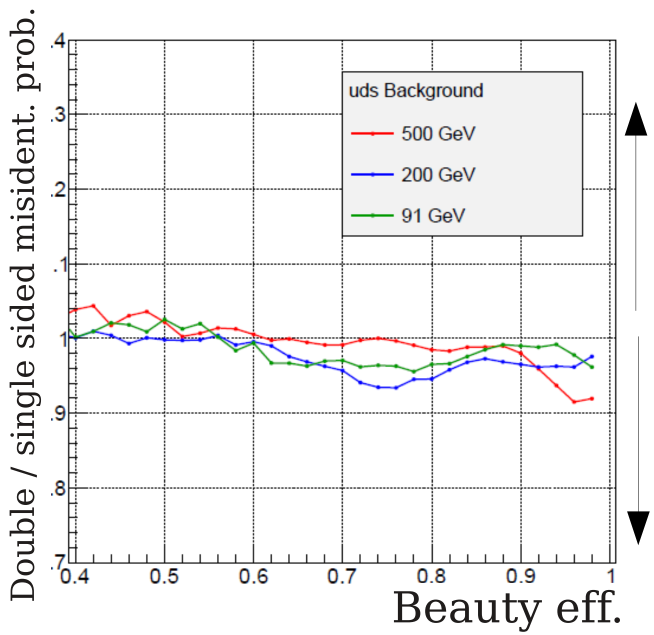


Double sided



(3x2 barrel + 3x2 endcap)





> 1
Double sided better than Single sided

< 1
Single sided better than Double sided

Very similar performance for both geometries

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Thin assemblies - road map

Motivation: **Evaluate performances and yield of thin pixel sensor and demonstrate the feasibility of a good tracking efficiency with thin assemblies**

Ultimate goal: **50 µm thick sensors + 50 µm thick ASICs, 25µm pixel pitch**

- Thin sensors simulations
  see *"12:30 TCAD Simulation of Silicon Radiation Detectors using commercial simulation products"* by Mathieu Benoit, today 12:30
- Thin sensor +"normal" Timepix assemblies
  - **Feasibility tests** of ultra-thin sensors
  - Assemblies with **50, 100, 200 µm** sensor thickness (delivered 08/2013)
- Assemblies with **thinned Timepix (100 µm)** and **thin sensors (100 µm)** - **in the pipeline**
- Sensors with **25x25 µm²** pixels - **end 2013?**

50 µm dummy wafer

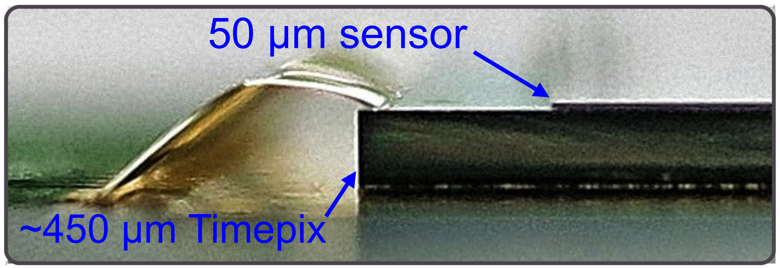
Advacam

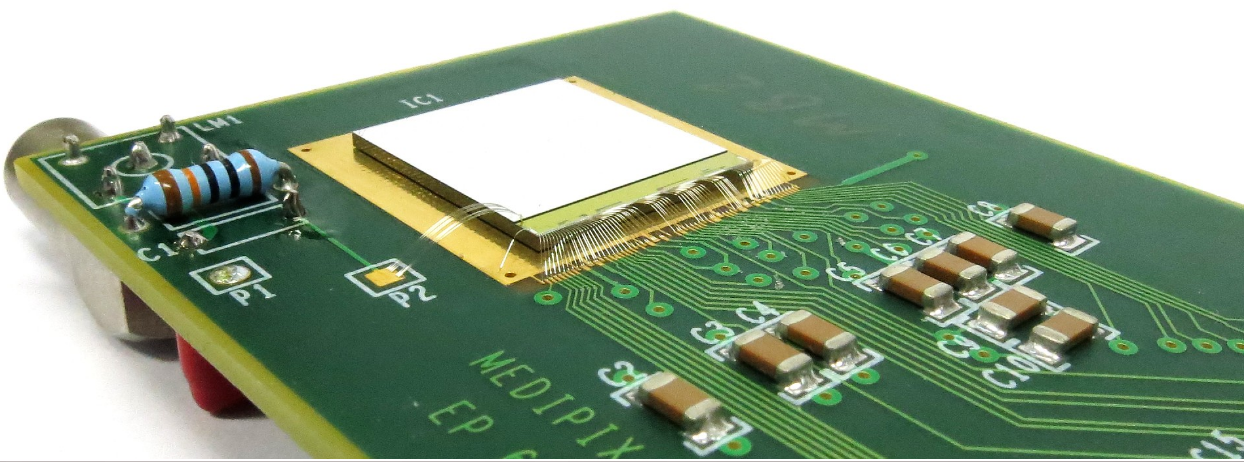
- **50 µm thin** with **20 µm and 50 µm active-edge** assemblies on standard thickness Timepix ASIC *(delivered July 2013)*
- **Excellent sensor quality**, few (<8) unconnected bumps
- Depletion at **15V**
- *5 x assemblies tested at DESY*

Test beam @DESY 08/2013 > billion tracks

Micron Semiconductor + IZM

- **100, 150, 200 µm** pixel sensor (Timepix compatible)
- *3 x 100 um assemblies tested at DESY*

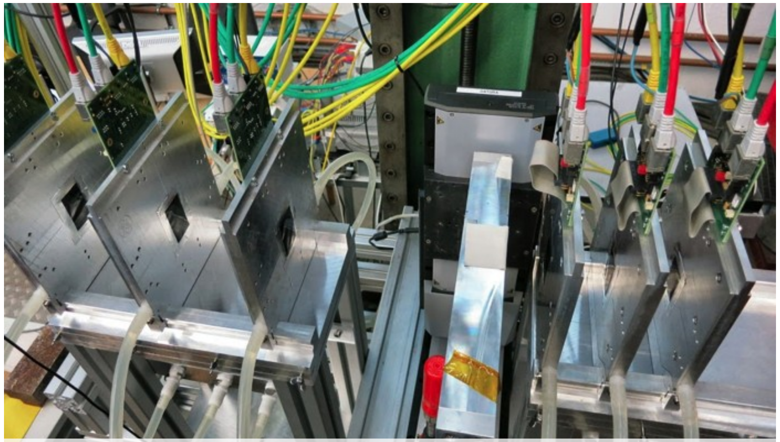




Testbeam Setup and Infrastructure

Test beam infrastructure @ DESY:

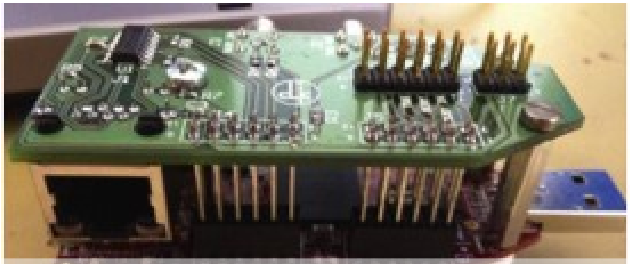
- **Electron** beam (energies **up to 6 GeV**)
- **Telescope** based on MIMOSA detectors
- **DAQ** framework provided:
  - EUDAQ (software)
  - Trigger Logic Unit (hardware)
- **Reconstruction** and analysis **software**
- Very good **user support**



EUTelescope at DESY

Test beam setup for thin sensor assemblies studies:

- **Optimization** of telescope **geometry** (distances between planes)
- Assemblies (DUT) mounted on translational and rotational stages
- FITpix readout for Timepix
- **Man in the middle TLU** device (MIM TLU)
  - synchronization with the telescope
  - increase track rate
- Dedicated **data producer** (plug-in to EUDAQ framework)
- Extensions to the reconstruction and **analysis software**

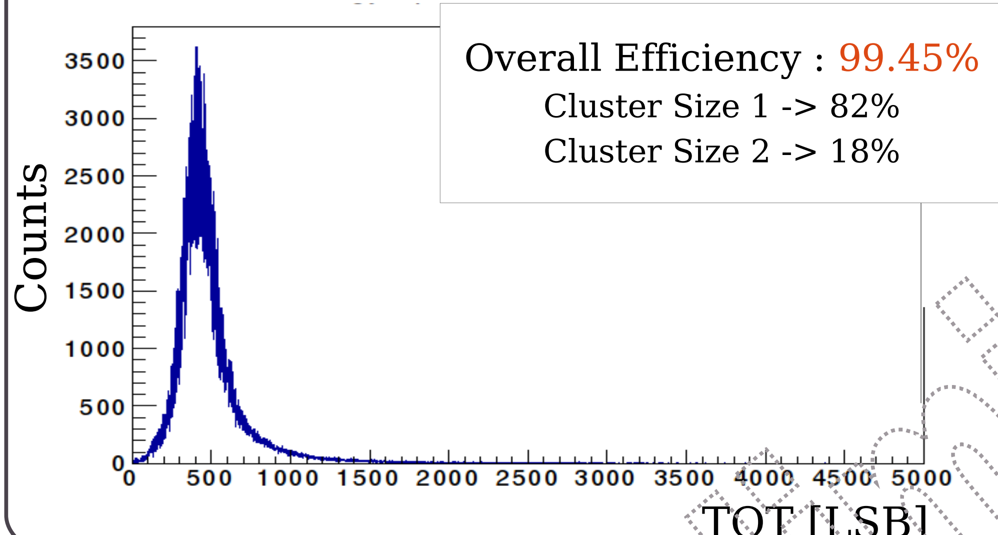


MIM TLU

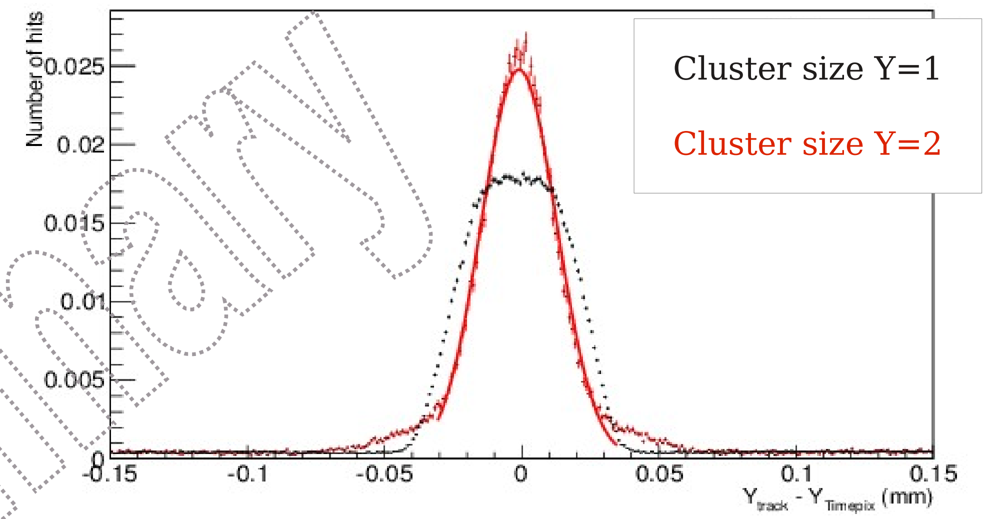
Testbeam results

50μm sensor thickness (15 V bias), 50 μm active edges (from Advacam)

Energy spectrum (all cluster sizes)

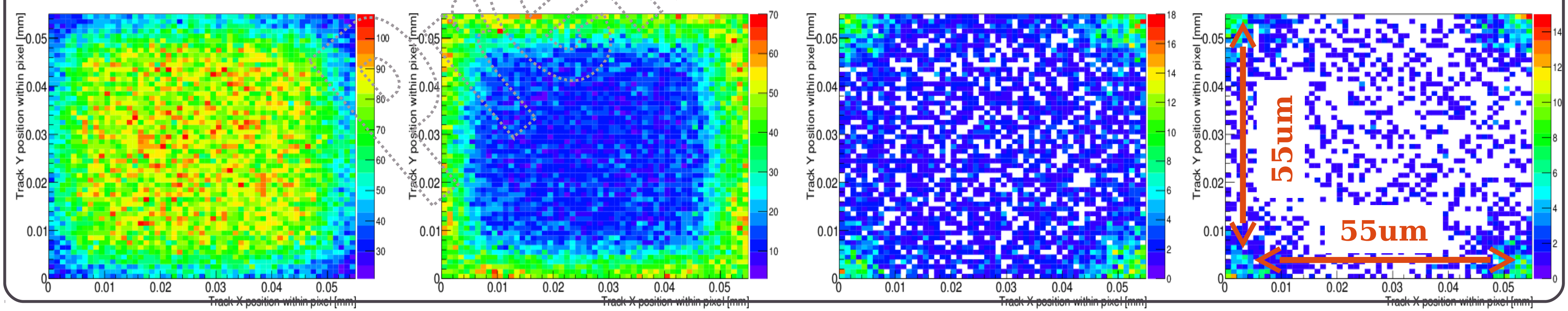


Residuals



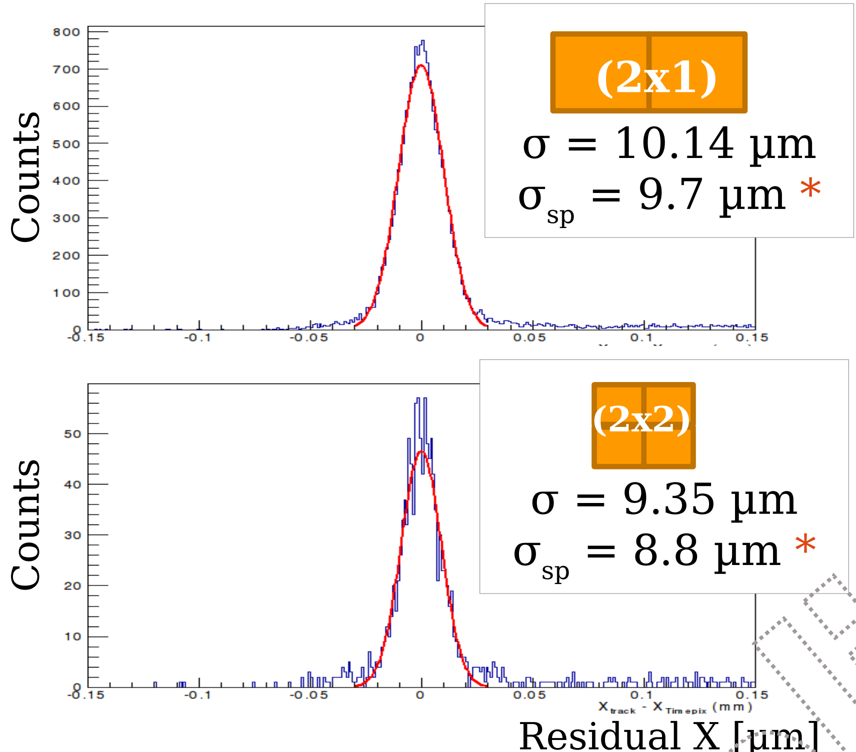
Hit position distribution within a pixel

Cluster Size 1 | Cluster Size 2 | Cluster Size 3 | Cluster Size 4



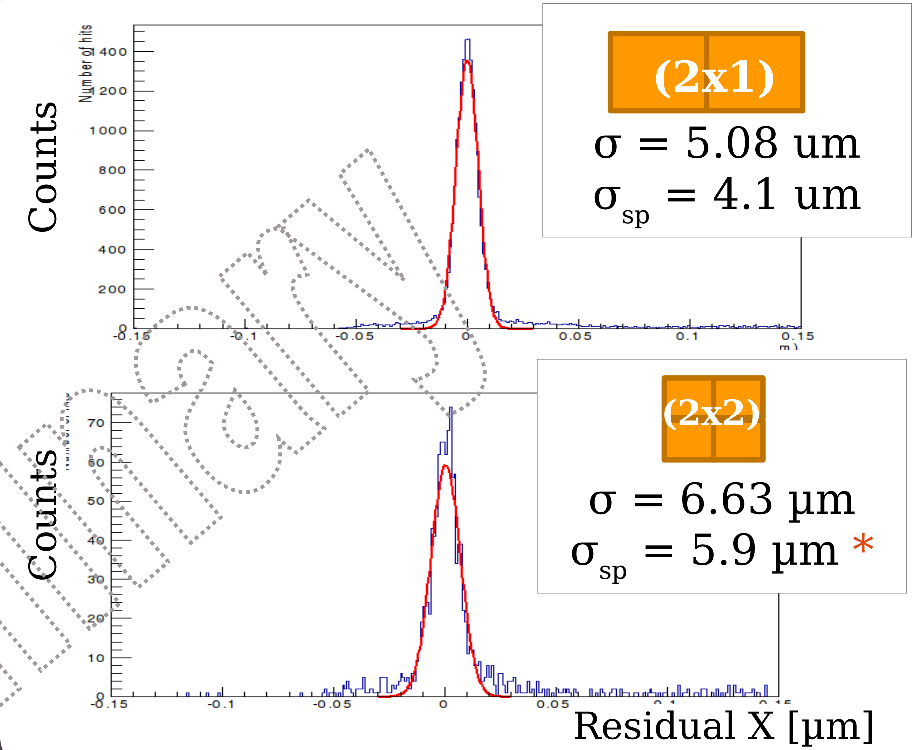
TB: Single point resolution

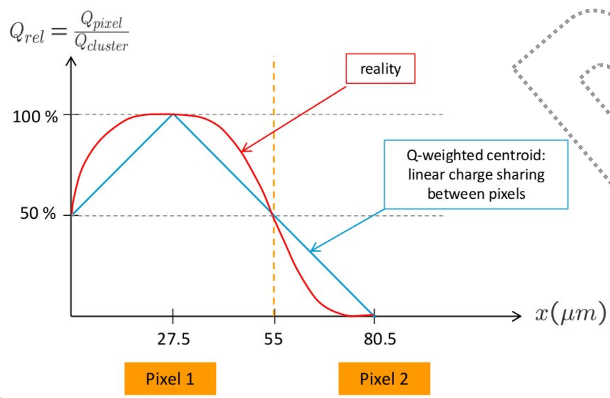
QWeighted



*) $\sigma_{tracking}$ = 2.9 um

EtaCorrection





Using **TOT Information**, it is possible to correct for non-linearities in charge sharing between pixel and **gain up to a factor 2 in single-point resolution** (for cluster size > 1).

For **50 μm** thick sensor, this represent only 20% of data, smaller pixel size is needed

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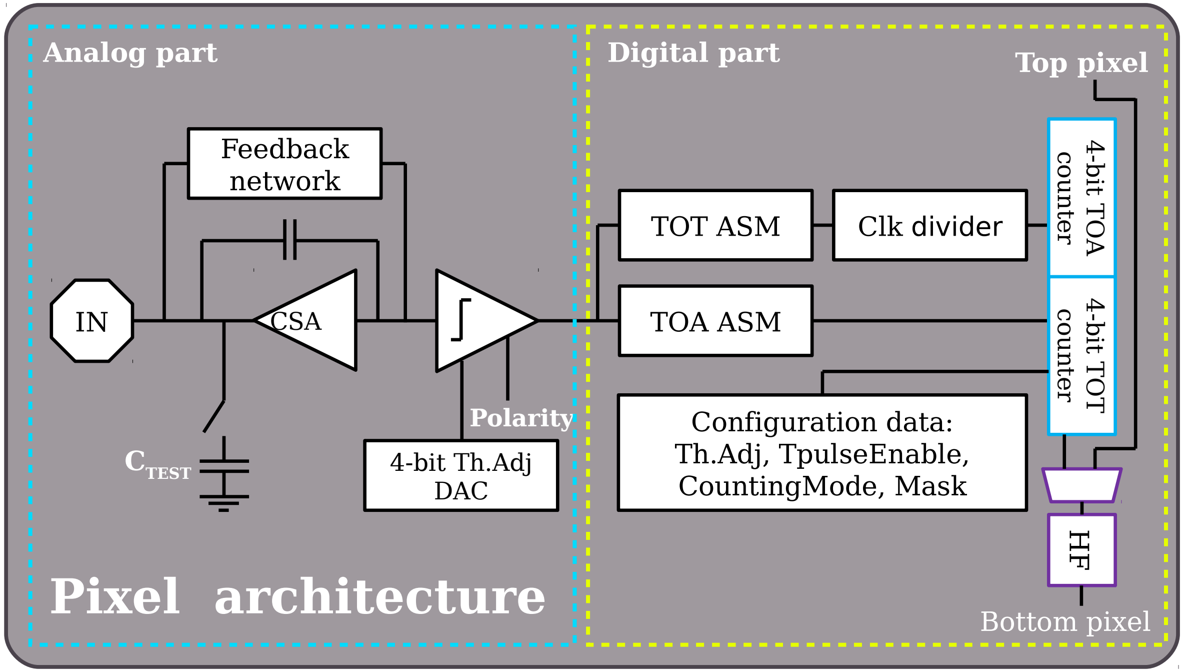
CLICpix Readout Chip

CLICpix is a hybrid pixel readout chip to be used in vertex detector

Main features:

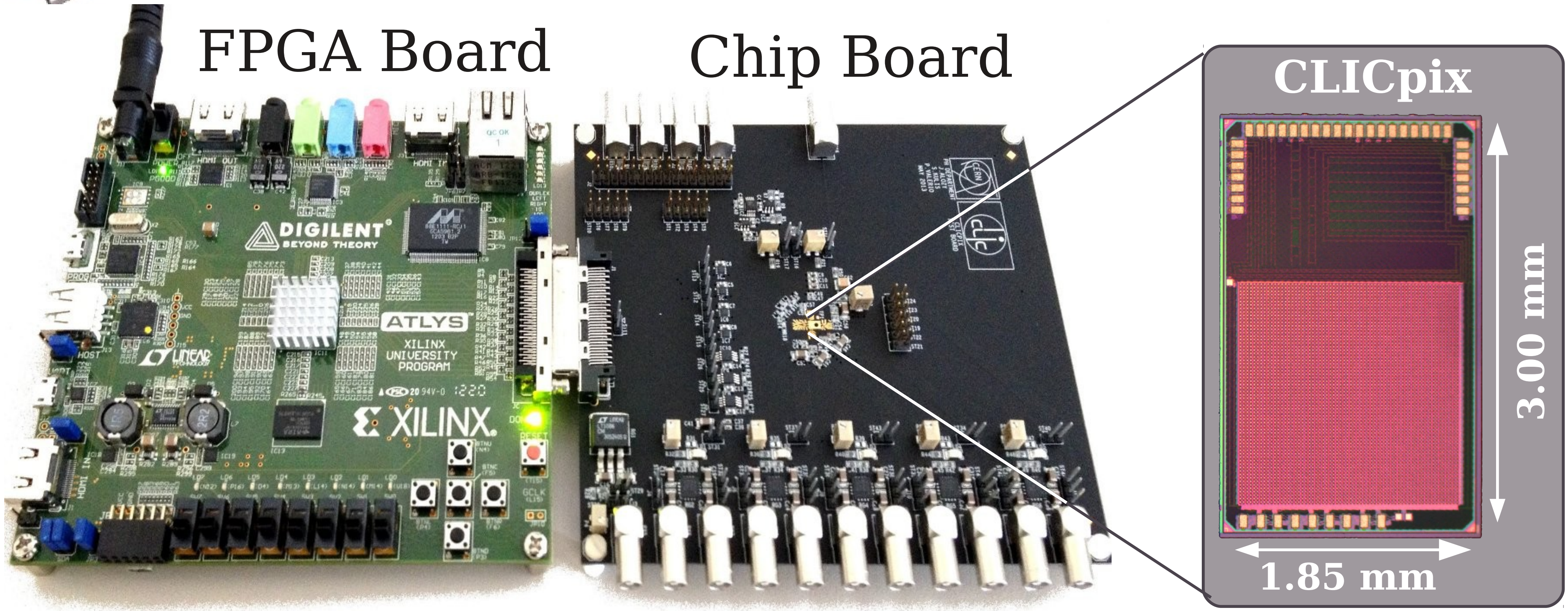
- Small pixel pitch (**25 µm**),
- **Simultaneous TOA** (4 bits) & **TOT** (4 bits) measurements
- **Power pulsing**
- **Data compression**
- Both pulse polarities can be handled



Demonstrator CHIP:

- commercial **65 nm CMOS technology** (proven to be radiation resistant)
- **array of 64x64** pixels
- The **Krummenacher architecture**, with a single ended preamp, a two stage discriminator and a 4-bit DAC

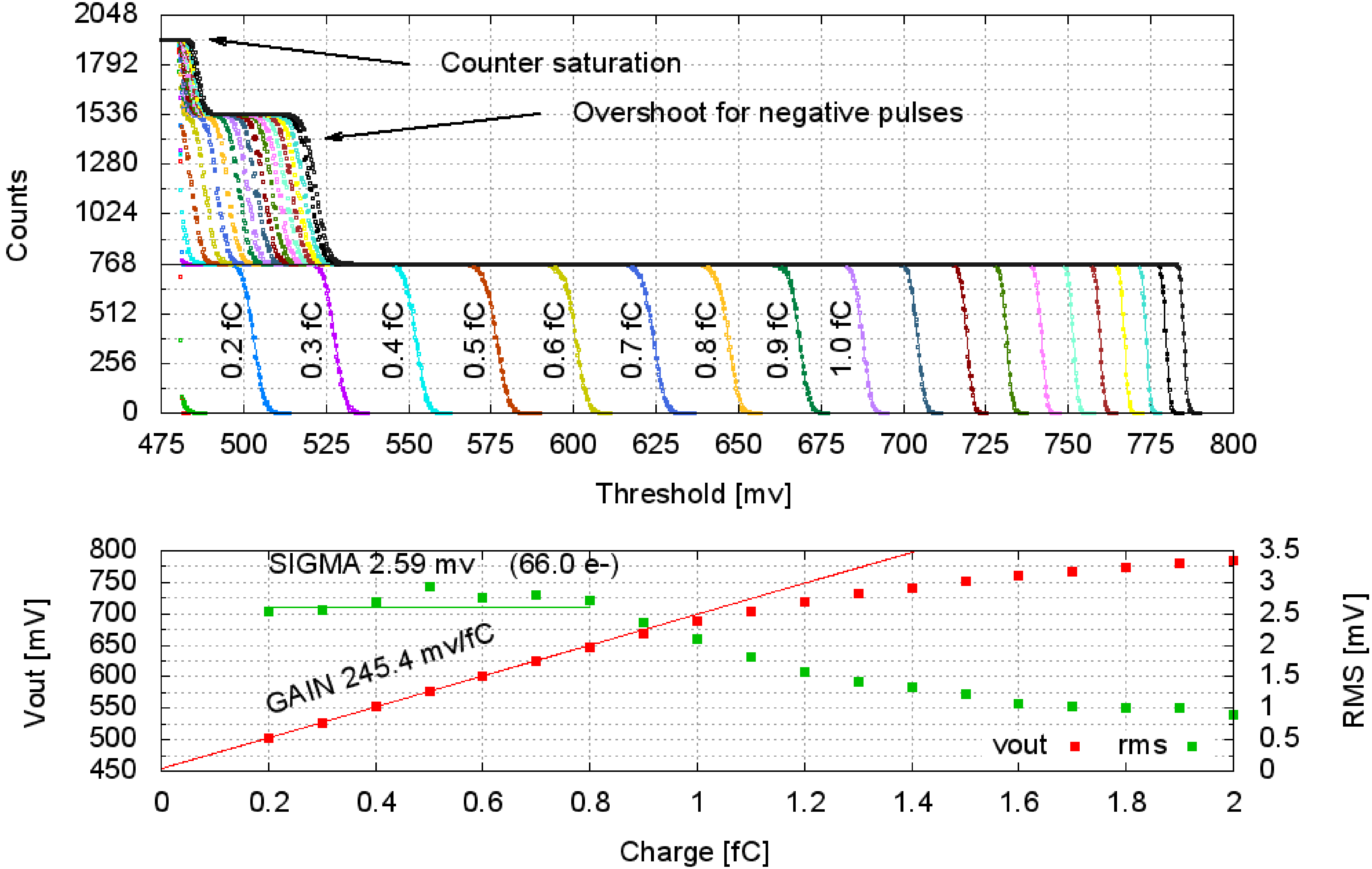
CLICpix Test Setup



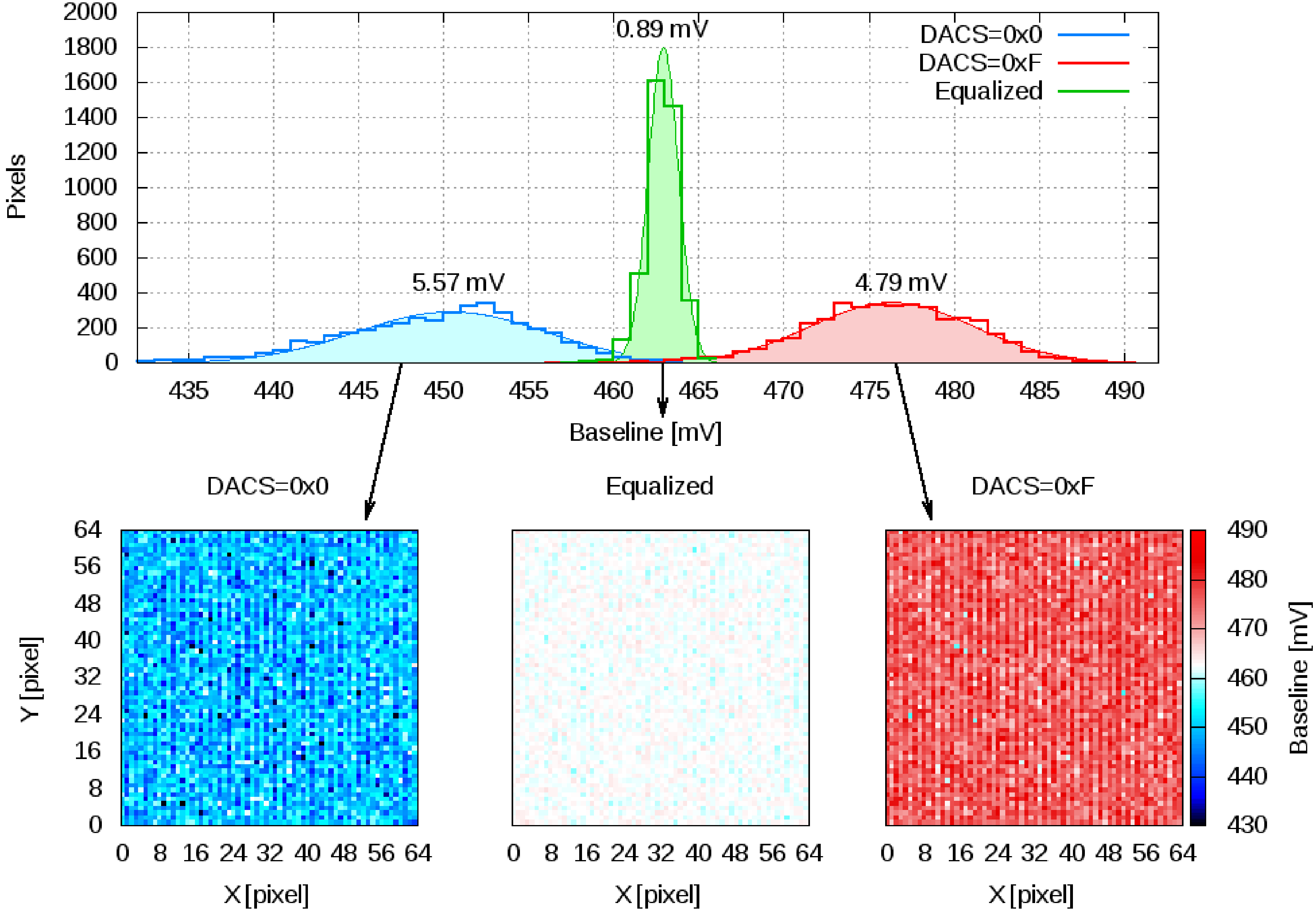
FPGA based readout system:

- Spartan 6 XILINX FPGA (on Atlys evaluation board)
- 1 Gbit Ethernet interface (TCP/IP & UDP/IP)
- CHIP ↔ FPGA Serial link up to 400 Mbps (not fully tested yet)
- Very-high-density cable interconnect (VHDCI)

CLICpix S-curves



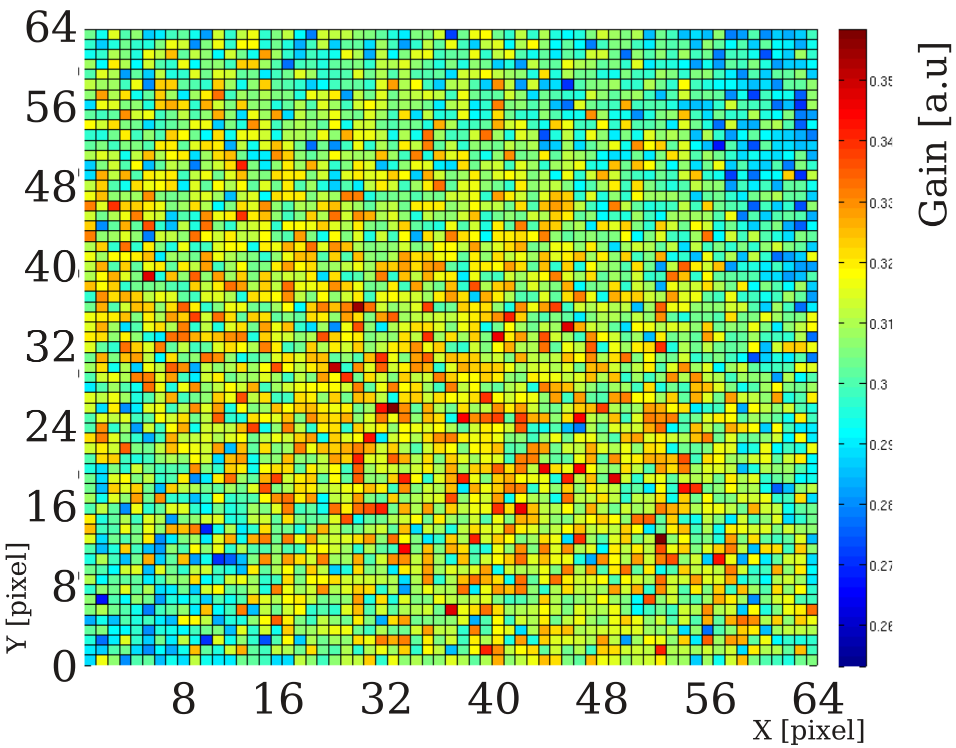
CLICpix Matrix Equalization



Calibrated spread is 0.89 mV (about 22 e-) across the whole matrix

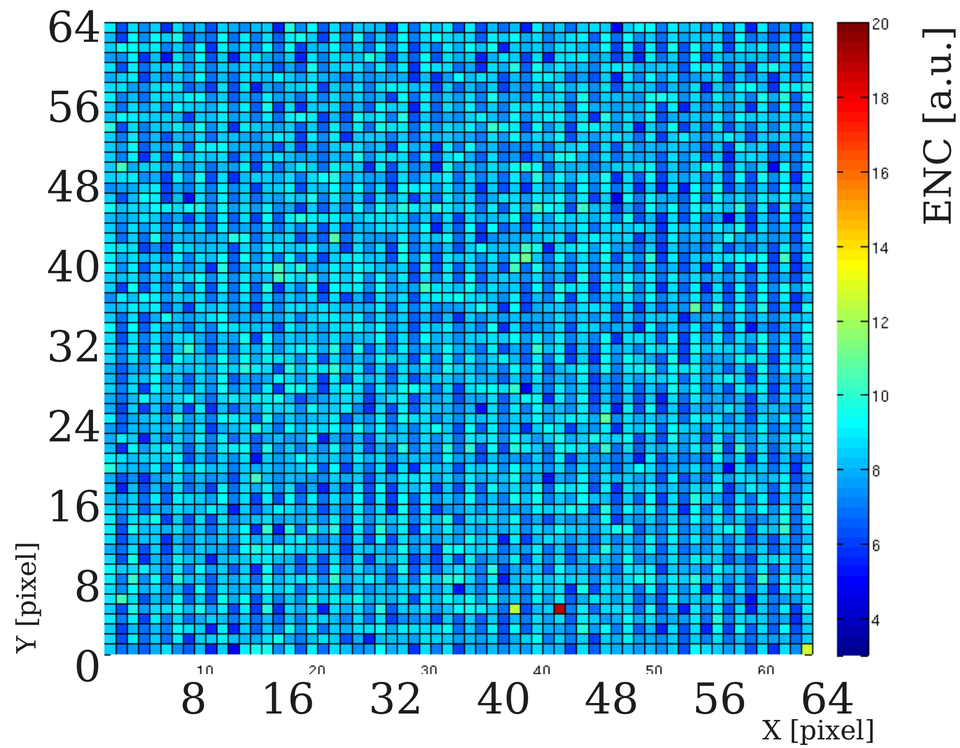
CLICpix Matrix Uniformity

Time Over Threshold gain distribution



- Uniform gain across the whole matrix
- Gain variation is **4.2% r.m.s.** (for nominal feedback current)

Equivalent Noise Charge distribution



- Uniform ENC across the whole matrix
- Mean ENC is **55 e^-** (without sensor)

CLICpix Summary

Parameter	Unit	Simulations	Measurement
Rise time	[ns]	50	-
TOA accuracy	[ns]	<10	<10
Gain	[mV/e^-]	44	40 *
Dynamic range	[e^-]	44 k (configurable)	40k * (configurable)
INL (TOT)	[LSB]	< 0.5	< 0.5
ENC (without senor)	[e^-]	~60	~55 *
DC spread σ (uncalibrated)	[e^-]	160	128 *
DC spread σ (calibrated)	[e^-]	24	22 *
Power consumption	[µw/pixel]	6.5	7

- The power pulsing works according to specifications
  (reducing the power consumption by more than one order of magnitude in power off state)
- The power-on and power-off times can be programmed
  (the front-end wake-up time is less than 15 µs)

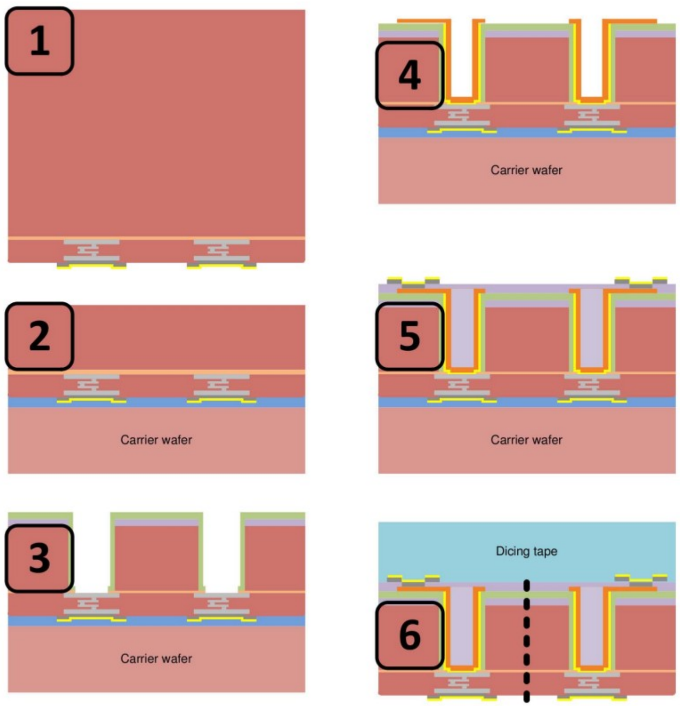
***) no calibration with sensor available yet (results obtained with electrical test pulses)**

Through-Silicon Vias (TSV)

Through Silicon Via: vertical electrical connection passing through Si wafer

- eliminates need for wirebonds
- 4-side buttable chips
- increased reliability, reduced material budget

CEA-Leti via-last process flow



(1) UBM deposition

(2) Temporary bonding, thinning to 120 µm

(3) Via etching + isolation

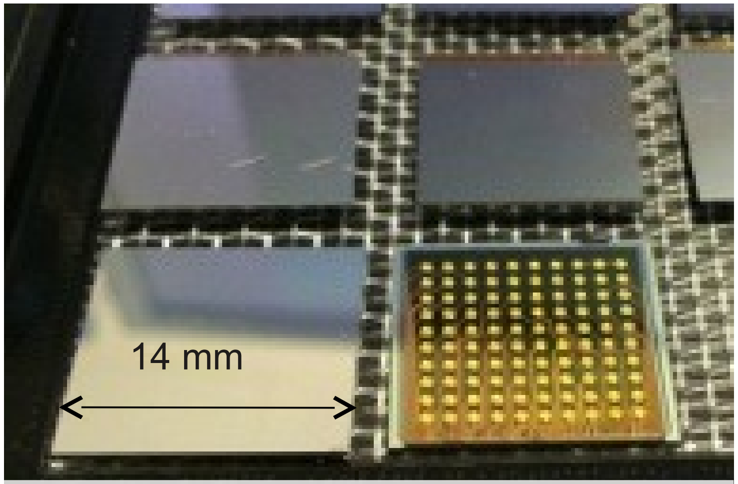
(4) Cu deposition + Patterning

(5) Backside passiv. + UBM deposition

(6) Debonding + attachment to dicing tape

Medipix TSV project with CEA-Leti

(ALICE, CLIC, ACEOLE and AIDA)



130 nm Medipix wafers

Status:

- successful completion of first phase: demonstrate feasibility
- on-going second phase: demonstrate good yield

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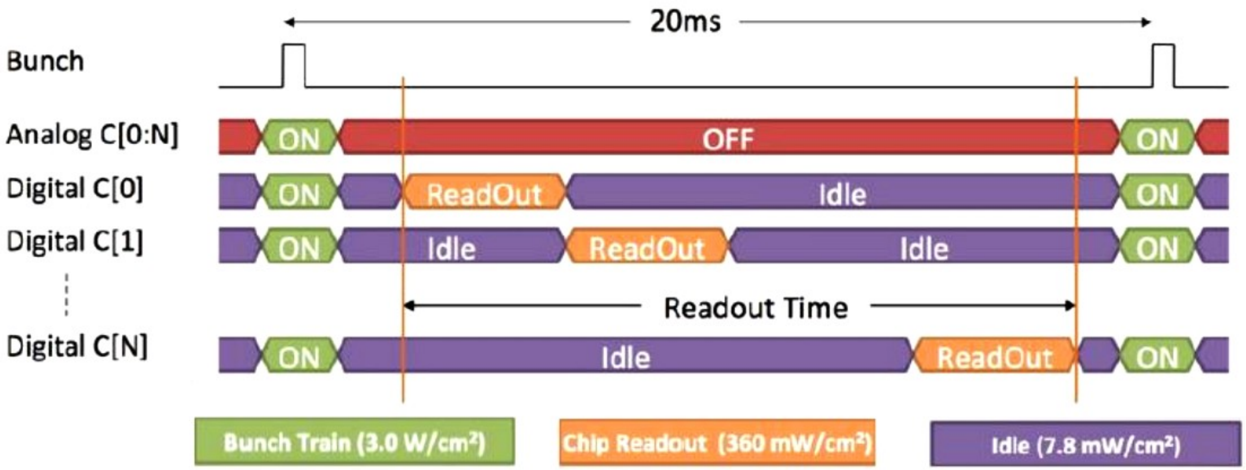
Powering Scheme

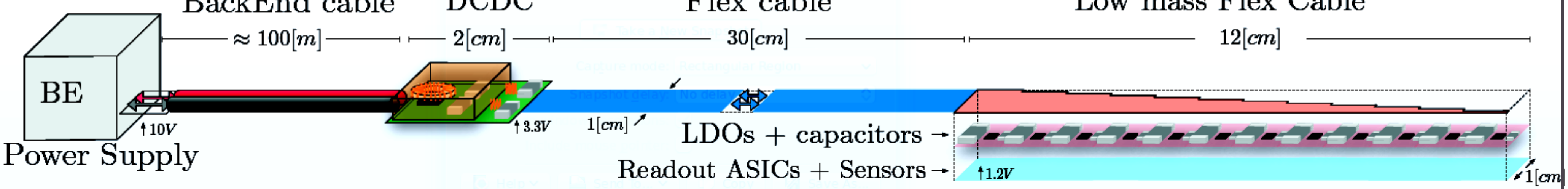
Power delivery scheme



Power pulsing (of unused blocks) to reduce average power consumption!

Challenges:

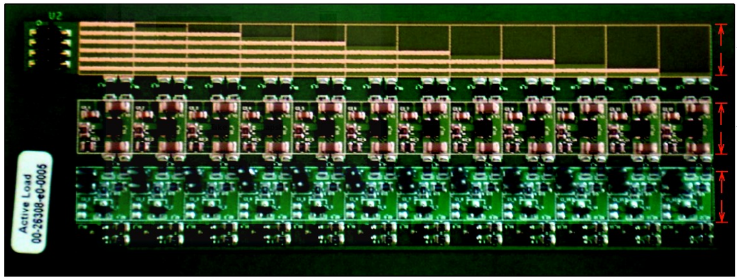
- High peak cur. **>40A/ladder**
- High magnetic field **4-5T**
- Material budget **< 0.1% X_0**
- Regulation **< 5% (60 mV)**



Implementation:

- **aluminum cables** on kapton tape
- **silicon capacitors** (80 µm thick, low mass)
- **LDO voltage regulators** (good regulation)

Achieved material budget : 0.1 %X_0



Cooling Concept

Requirements:

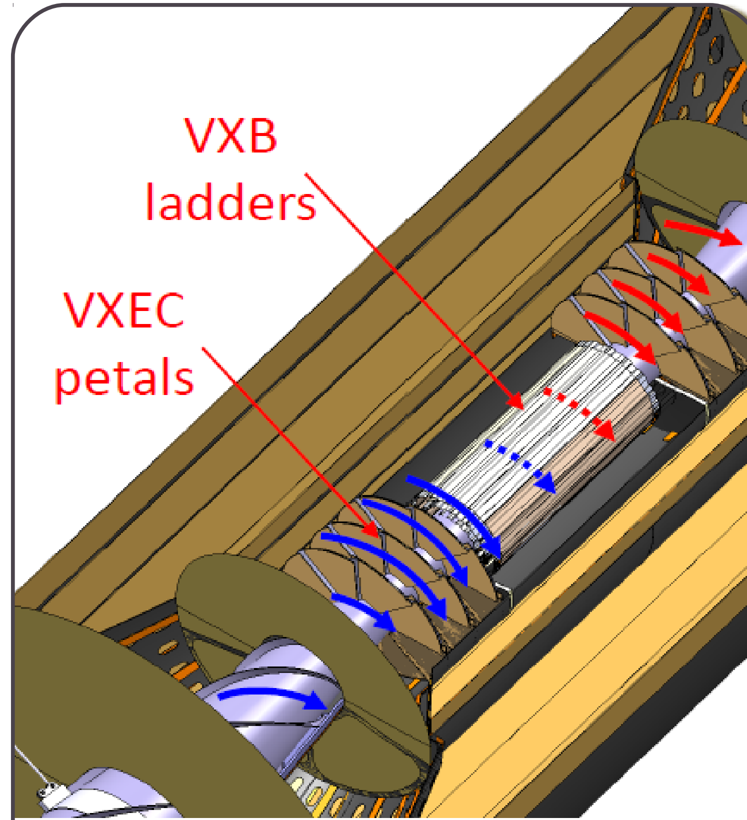
- Proper sensor and ASICs cooling

Challenges:

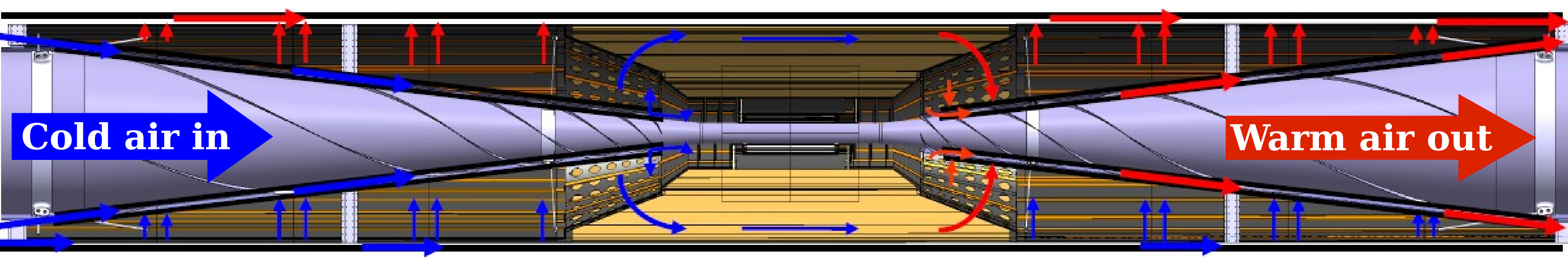
- Low material budget
- ~470 W heat load to extract
- High dimensional stability
- Assembly and cabling integration

Solution:

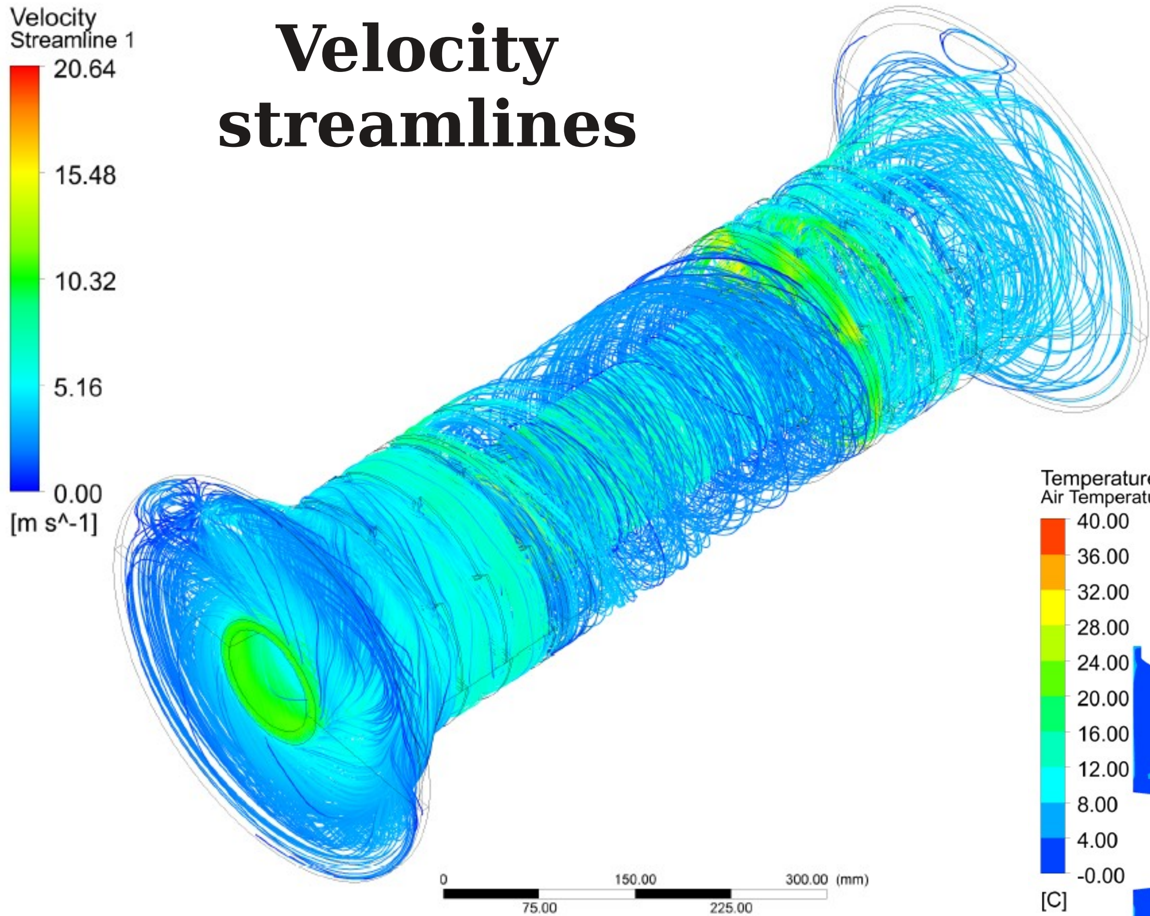
- Forced air-flow cooling, spiral end-cap geometry



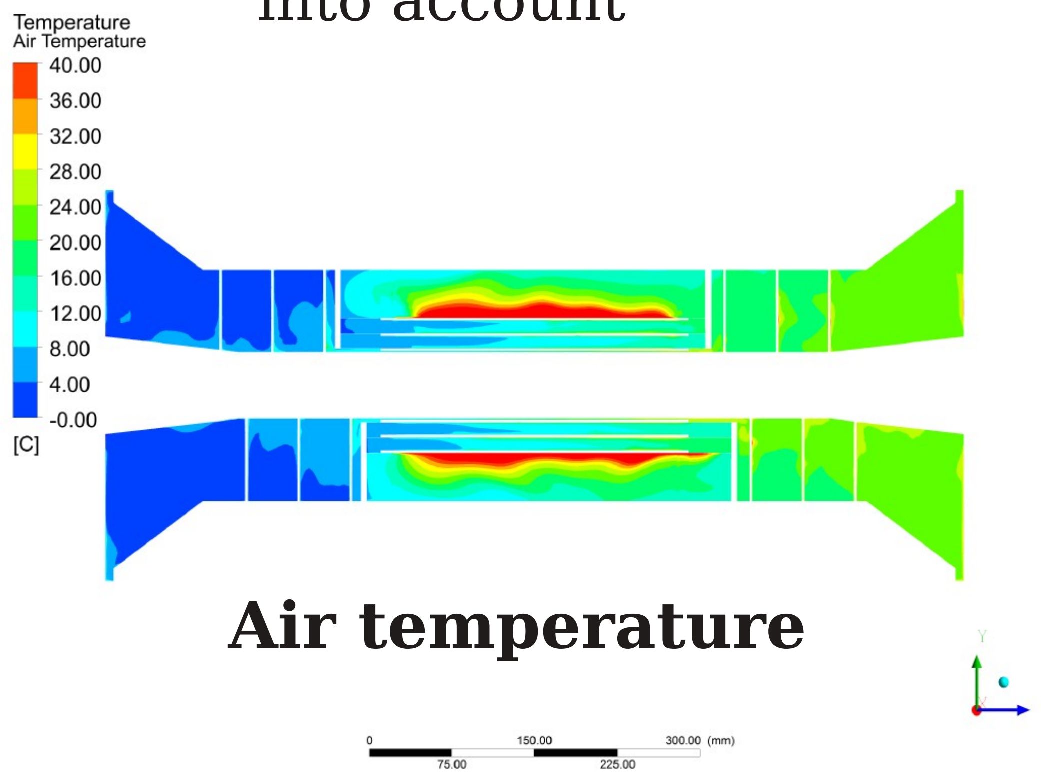
Zoom on vertex region



Velocity streamlines



- Silicon temperature below **30°C** *(except for outer most barrel layer)*
- Conduction not taken into account



Air temperature

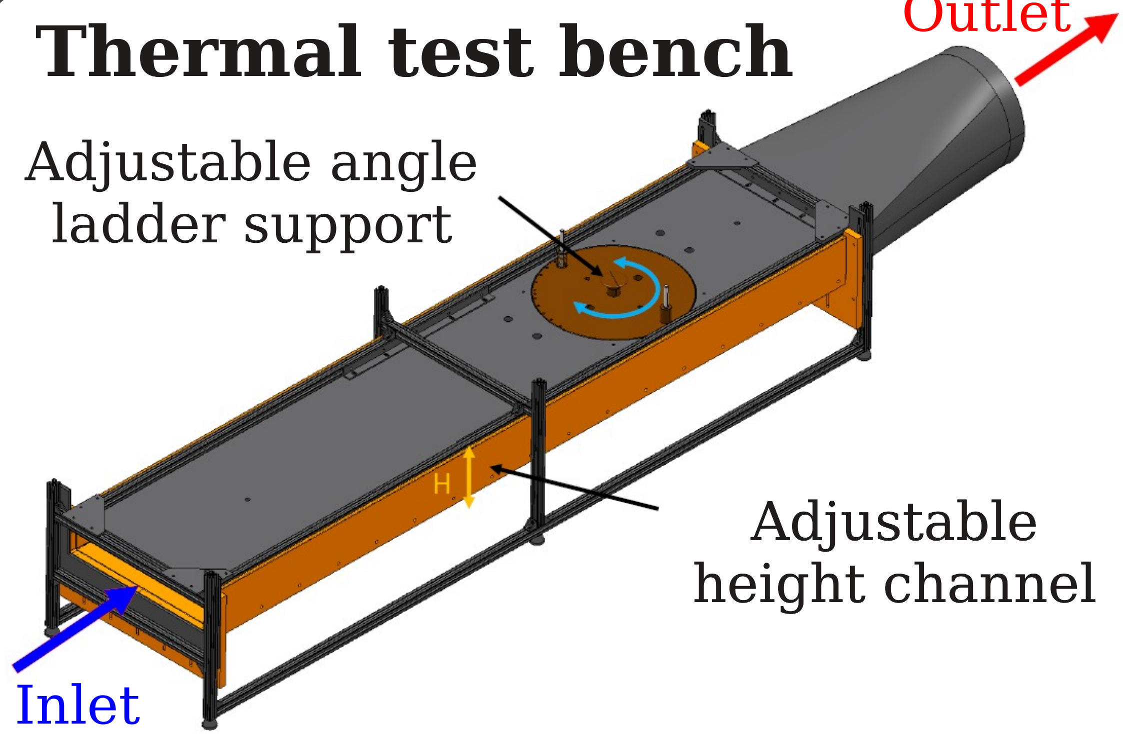
- Mass flow: **19.9 g/s**
- Avg. velocity in barrel: **6.3 m/s**

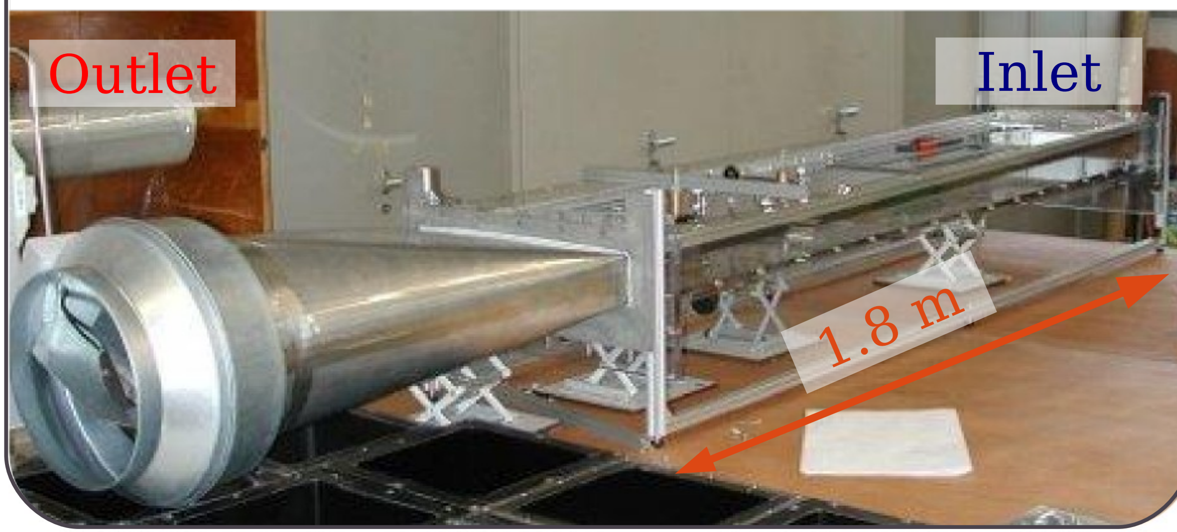
Cooling Mockup Setup

Test program:

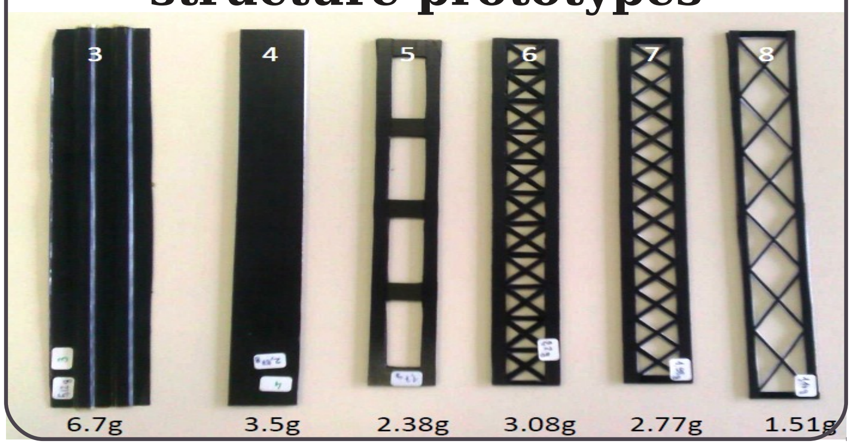
- Evaluate forced convection air cooling
- Measure & characterize air-flow induced vibrations
- Validate the dedicated finite element simulations
- Develop and characterize low-mass ladder support *(~0.05% X_0)*

Thermal test bench

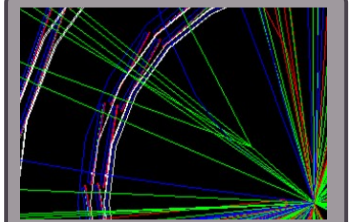




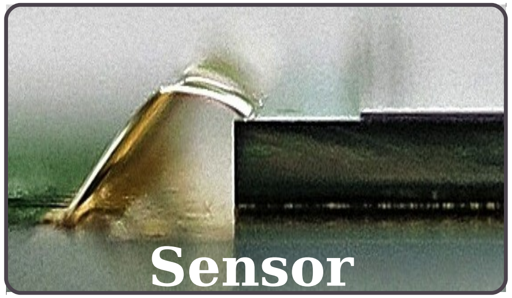
Ladder support structure prototypes



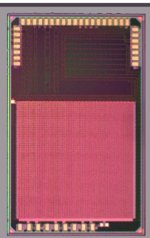
Integrated approach



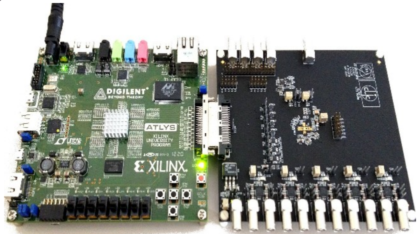
Simulations



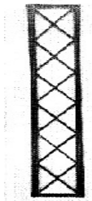
Sensor



Readout

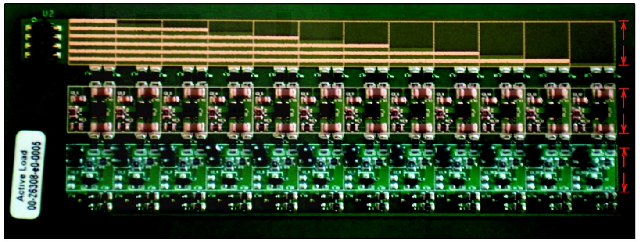


DAQ

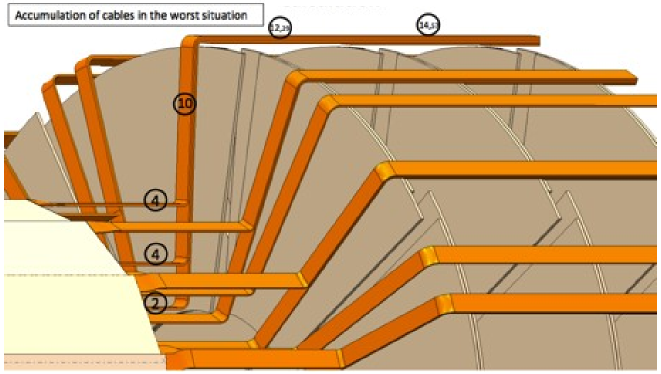


Sup.

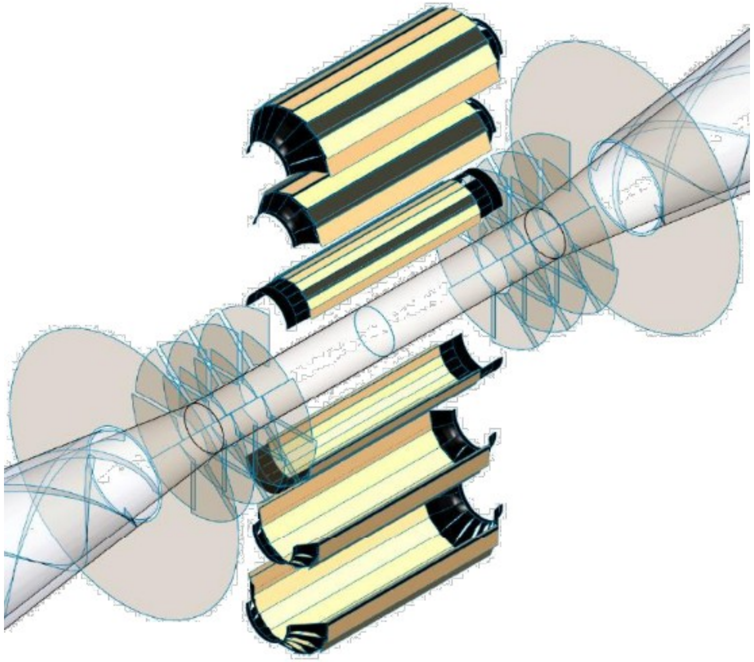
Powering



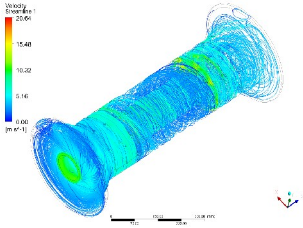
Cabling



Assembly scenarios



Cooling



Summary

- CLIC environment + physics requirements pose challenging demands on vertex-detector system (a new kind of challenges compared to LHC)
  - Less radiation damage but ...
  - Higher spatial resolution precision (~3 µm)
  - Finer time stamping (~10 ns)
  - Lower power (0.3 µW/channel, 50 mW/cm^2)
  - Lower material budget (0.2 % X_0)
- Ongoing active R&D on:
  - Thin sensors
  - Readout technologies
  - Power-delivery and power pulsing
  - Mechanics, cooling