DEPFET active pixel detector

THE PIXEL DETECTOR FOR BELLE II AT SUPERKEKB

C. Lacasta IFIC-Valencia
On behalf of the DEPFET collaboration

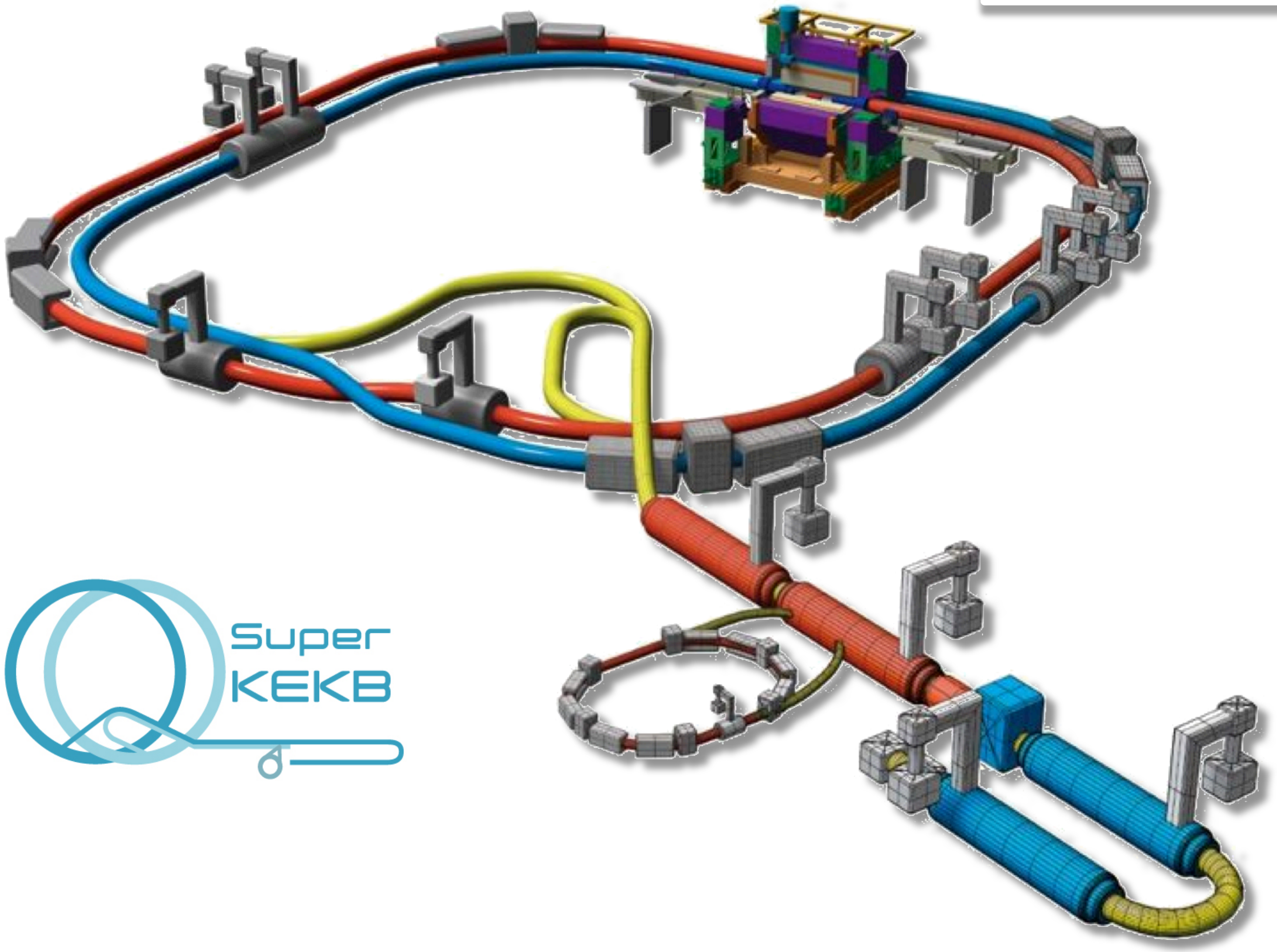
The KEKB upgrade

Asymmetric energy (4, 7 GeV) e^+e^- collider at the $E_{cm}=m(\Upsilon(4S))$

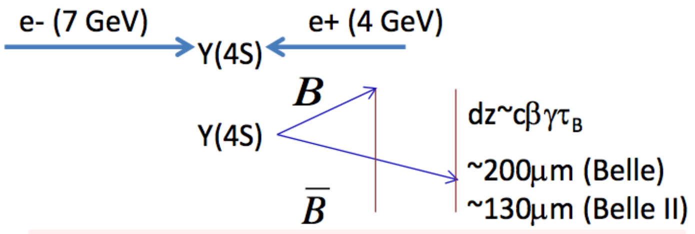
Very small spot-size beams (*nano beam*) and higher currents.

Final luminosity $8 \cdot 10^{35}$ cm^{-2} s^{-1}:

aim for 50 ab^{-1}

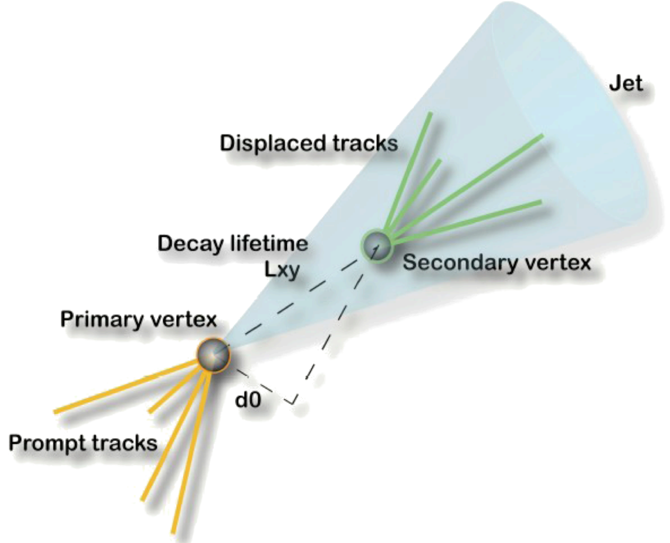


Super KEKB



SuperKEKB βγ=0.28 : e-(7GeV), e+ (4GeV)

KEKB βγ=0.42: e-(8GeV), e+ (3.5GeV)

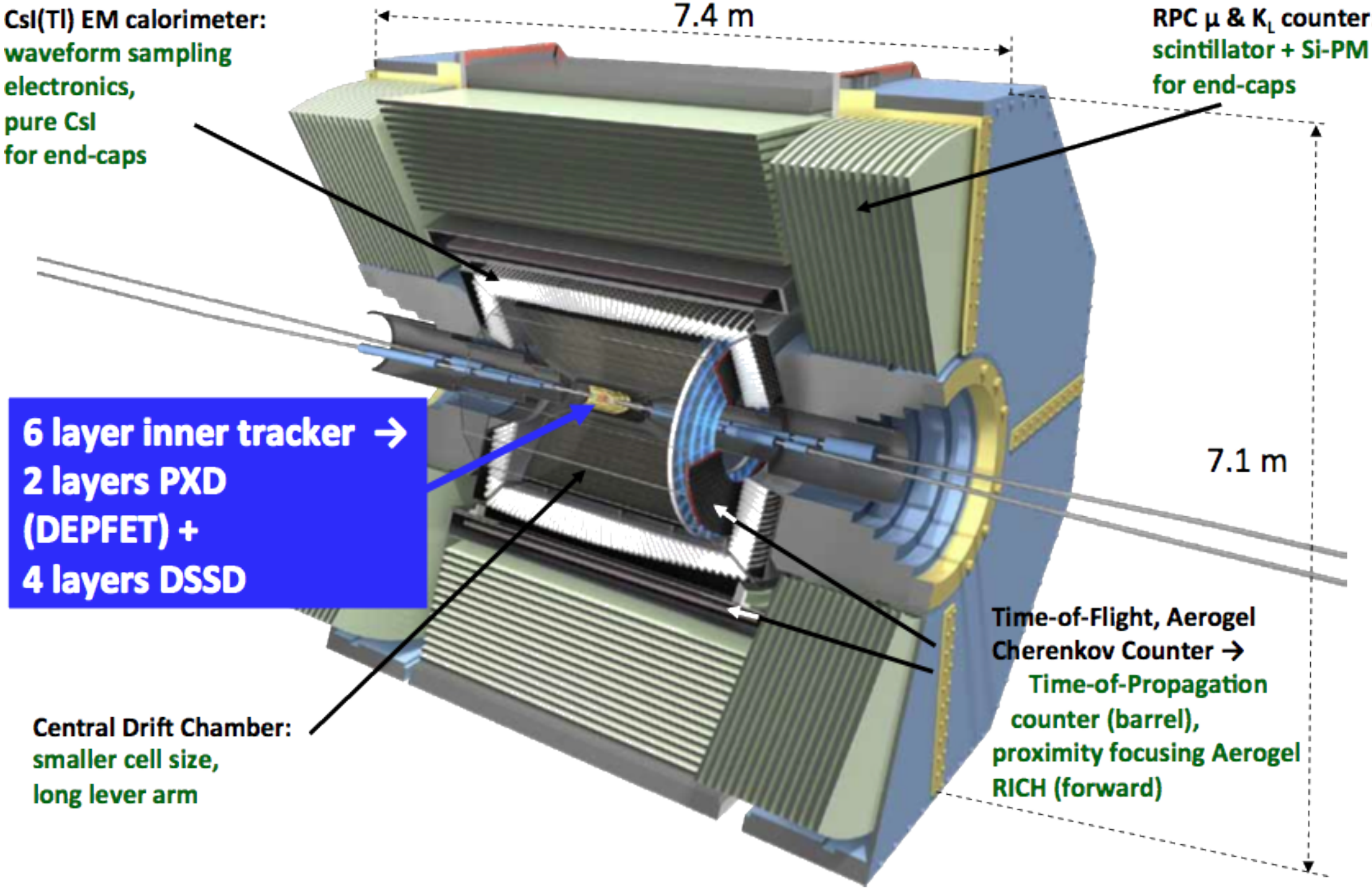


Decreased boost γβ

We need better vertexing

The Belle II detector

Higher backgrounds (x20): higher occupancy and radiation damage
Higher event rate: faster trigger, DAQ
Ready for 1st physics run in 2016



CsI(Tl) EM calorimeter:
waveform sampling
electronics,
pure CsI
for end-caps

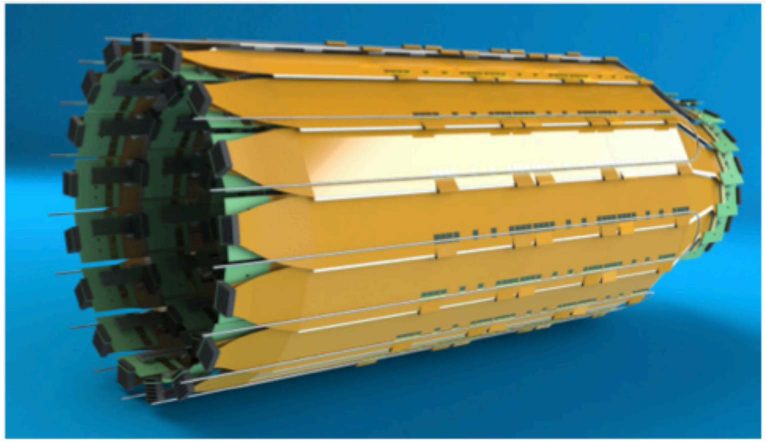
RPC μ & K_L counter:
scintillator + Si-PM
for end-caps

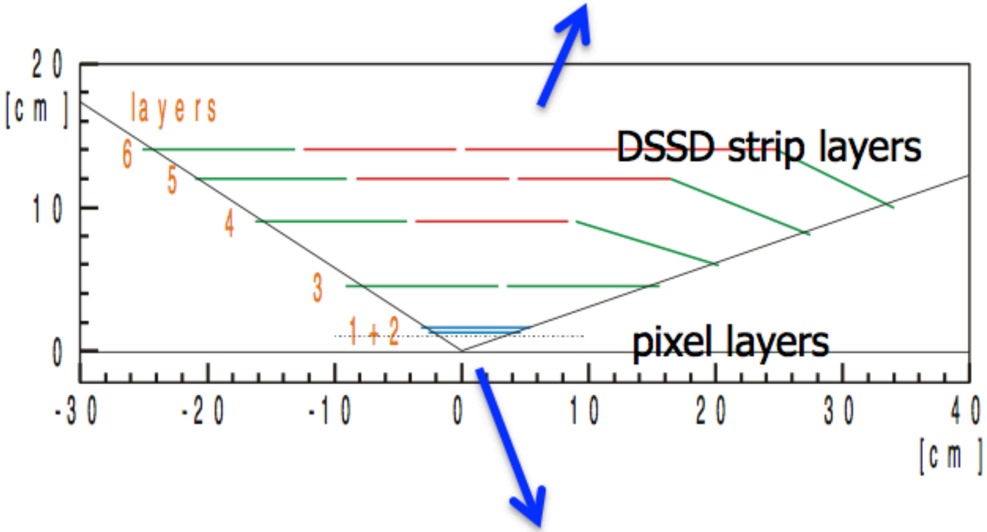
6 layer inner tracker →
2 layers PXD
(DEPFET) +
4 layers DSSD

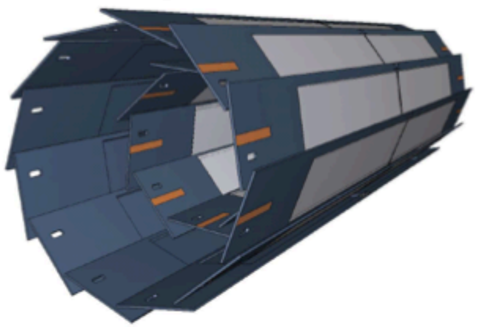
Time-of-Flight, Aerogel
Cherenkov Counter →
Time-of-Propagation
counter (barrel),
proximity focusing Aerogel
RICH (forward)

Central Drift Chamber:
smaller cell size,
long lever arm

Belle II Vertex Tracker







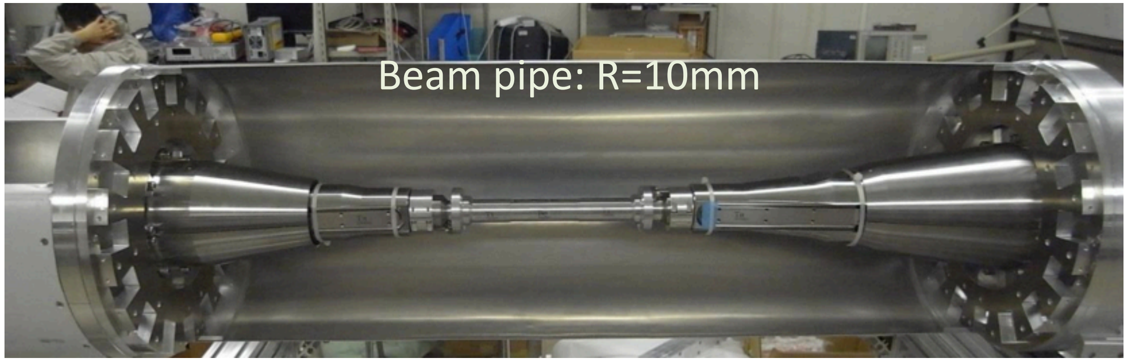
SVD

Silicon Vertex Detector

4 layer double sided Si strip detector

R=3.8, 8.0, 11.5 and 14 cm

(See next talk by T. Bergauer)



Beam pipe: R=10mm

PXD

Pixel Detector

2 layer Si Pixel at R=1.4 and 2.2 cm

DEPFET technology

Thickness: 75 µm

Requirements for the pixel detector

	Belle II
Occupancy	0.4 hits/µm^2/s
Radiation	>1Mrad/year
Frame time	20 µs (continuous r.o. mode)
Acceptance	17°-155°
Momentum range	Low momentum (< 1GeV)

Low momentum of the tracks implies

- Low material budget to avoid multiple scattering
- Multiple scattering sets the lower limit of the spatial resolution (10 µm)

Continuous r/o mode means that ASICs are “ON” all the time

- This and material budget limit the options for cooling

DEPFET: DEpleted P-channel FET

Amplifying transistors in a **fully depleted** bulk

Internal gate forms **potential minimum for e^-**

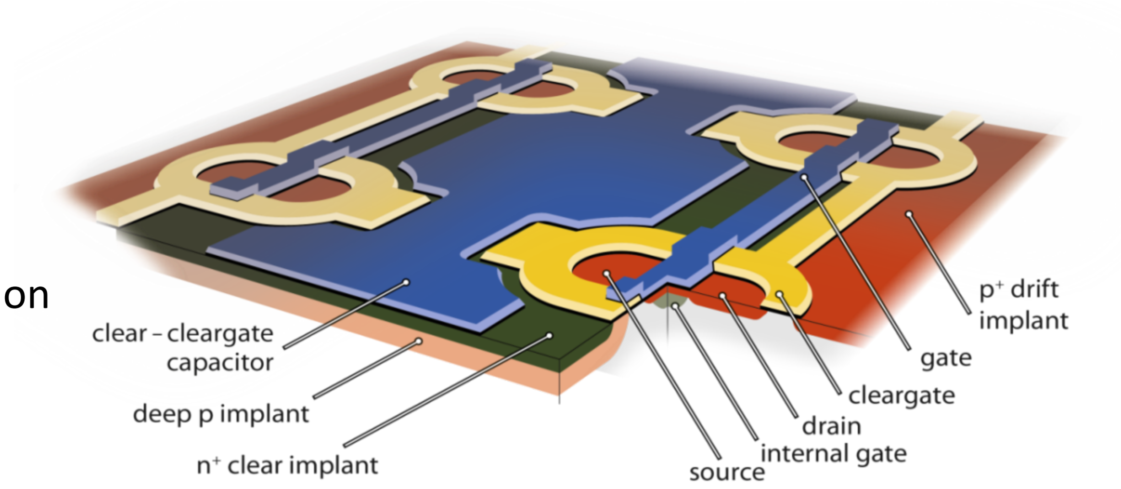
Stored charge **modulates the channel current**

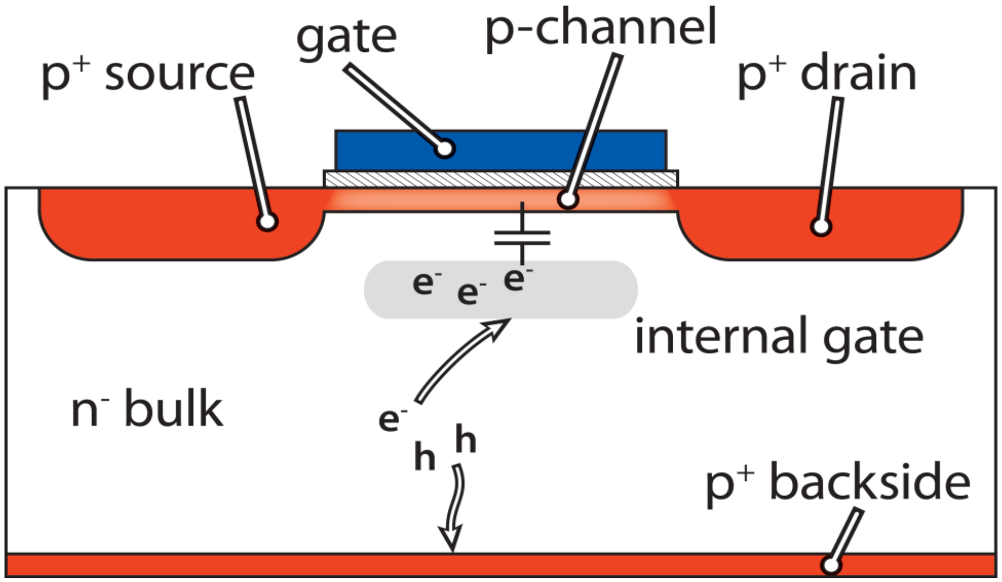
Small intrinsic noise: ~50 nA

Sensitive in the off-state: much reduced power consumption

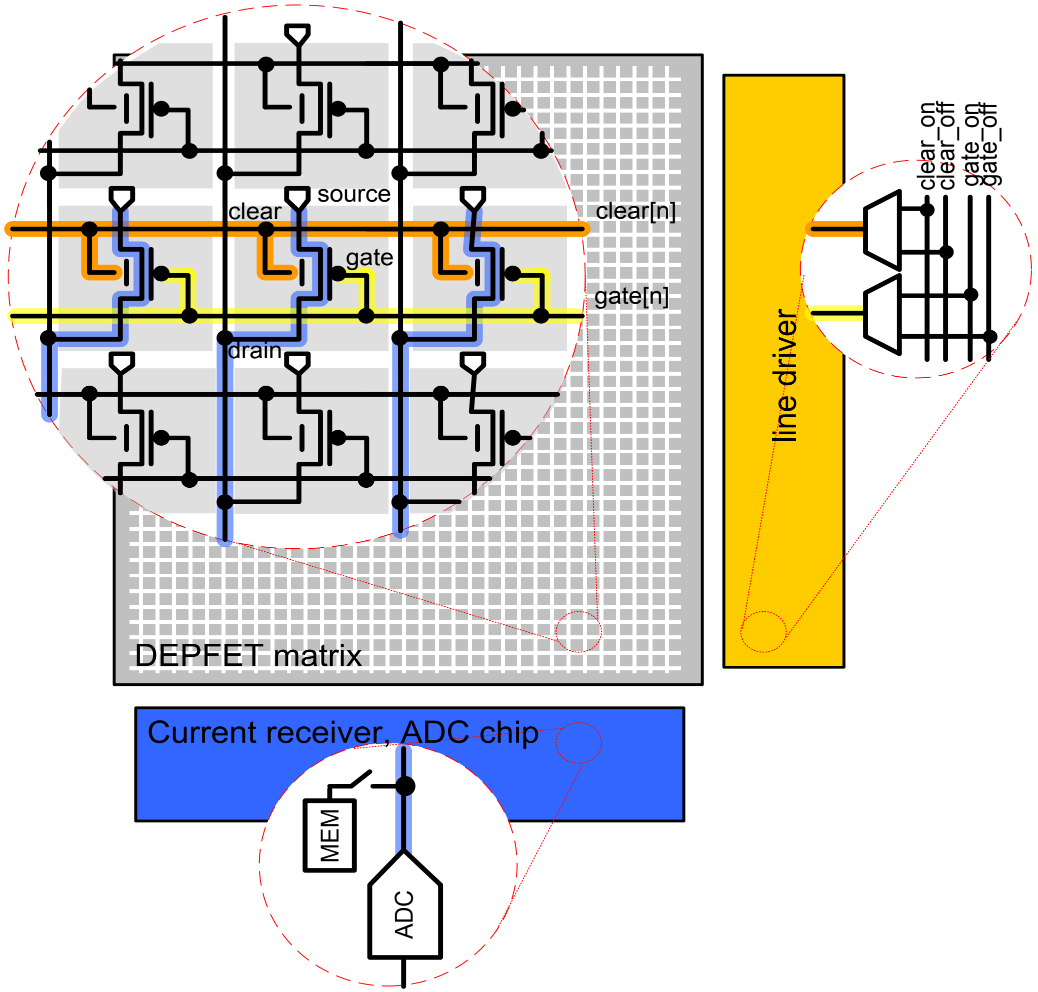
Internal amplification: $g_q \approx 0.5$ nA/e^-

Charge has to be removed “properly and fast” from the internal gate





DEPFET pixel array



- ✓ Pixels arranged in a matrix
- ✓ Gate, Clear lines need switcher steering chip
- ✓ Row-wise readout
  - ➔ For Belle II 4 rows are read at a time
- ✓ Long drain read out lines to keep most of the material out of the acceptance region
- ✓ Only "activated" rows consume power
  - ➔ The others are still sensitive to charge
  - ➔ Low power consumption

Thinning technology

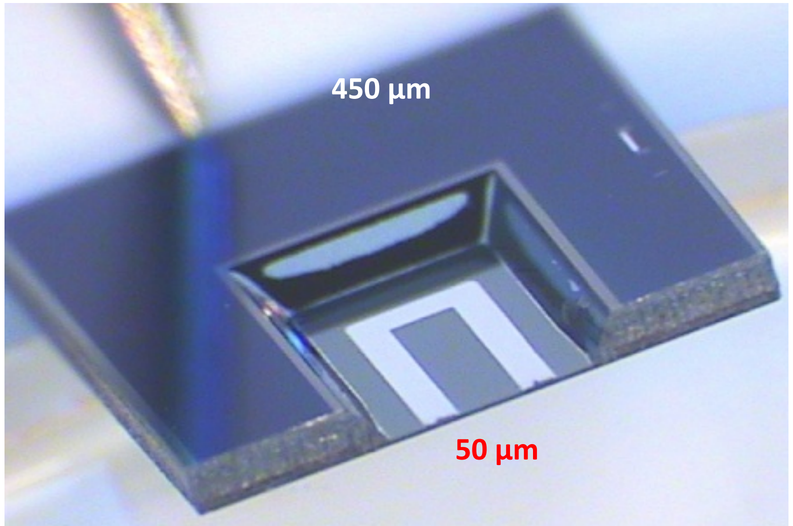
Process backplane

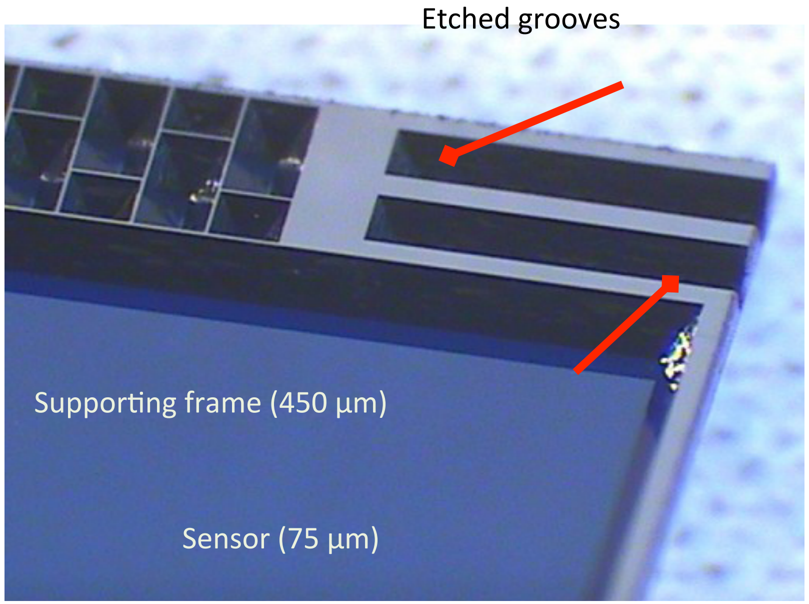
Wafer bonding SOI process

Thinning of top wafer

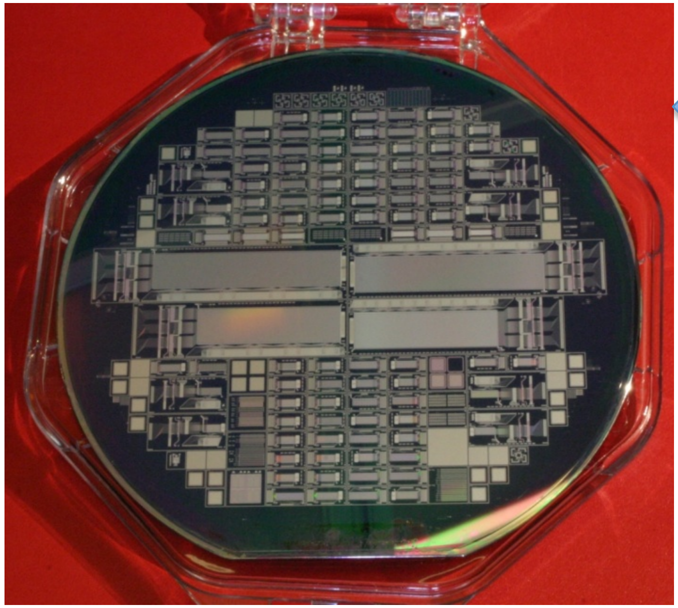
Process

Etching of handle wafer

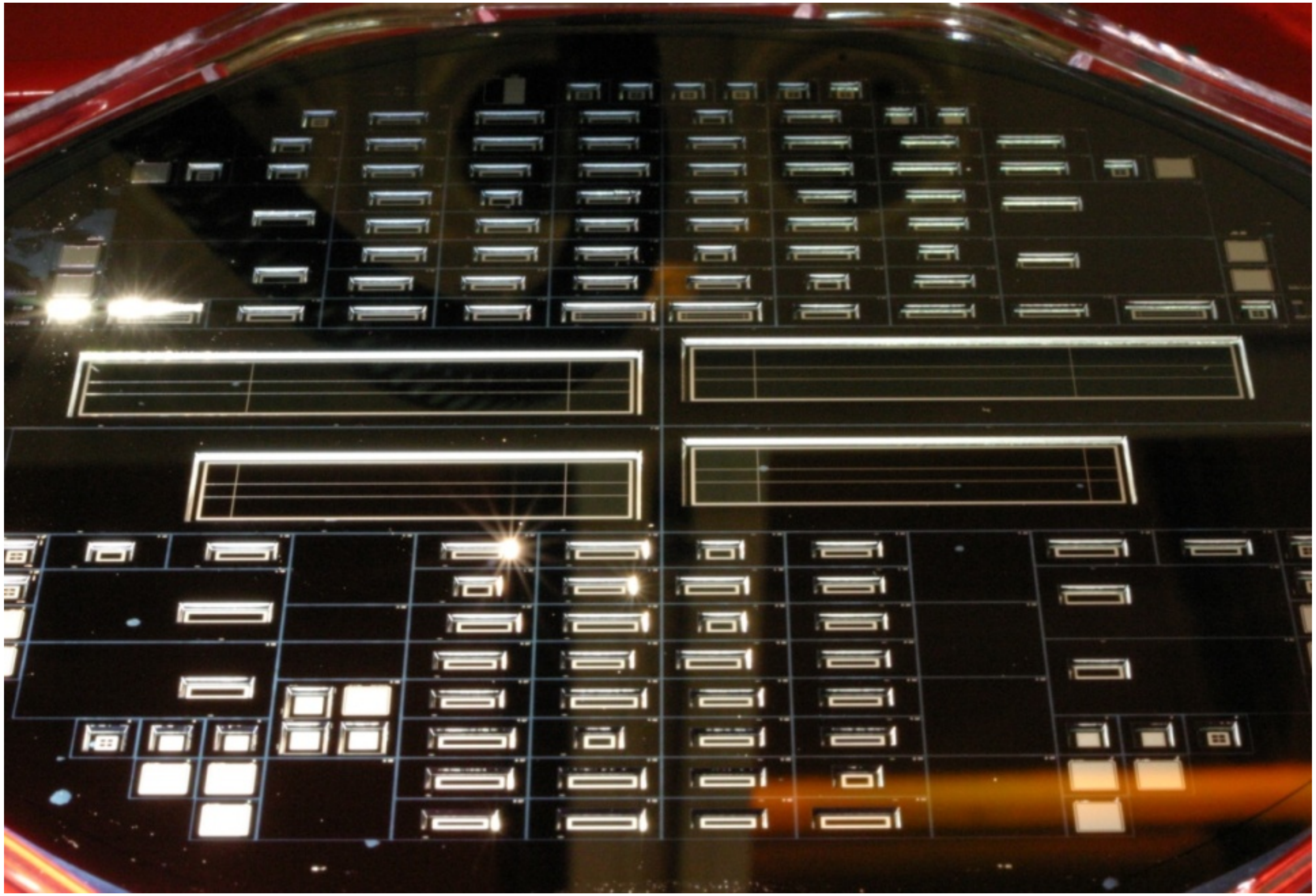




PXD6 thinned wafer



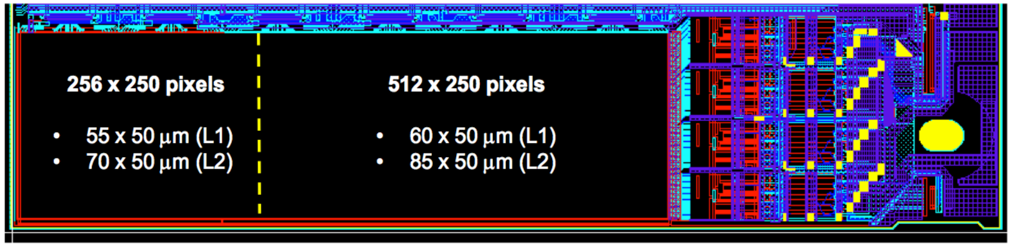
TOP side



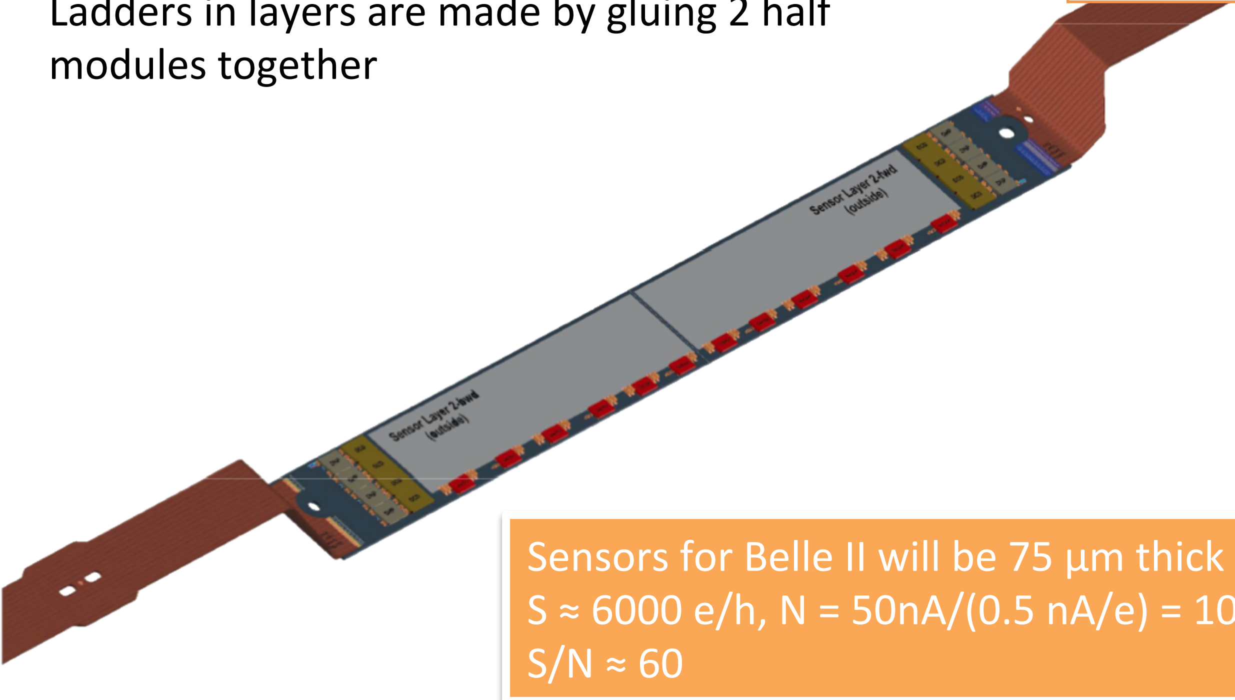
Back side

The DEPFET module

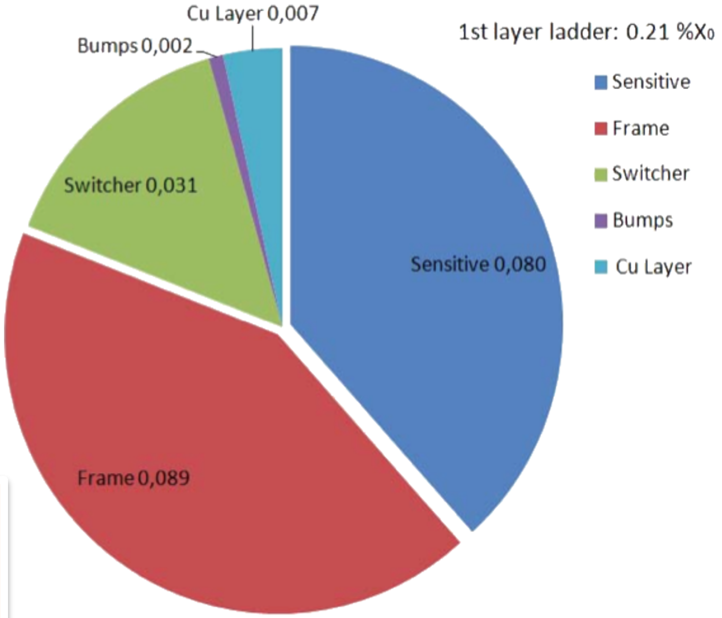
	Inner Layer (L1)	Outer Layer (L2)
# modules	8	12
Distance from IP (cm)	1.4	2.2
Thickness (µm)	75	75
#pixels/module	768x250	768x250
Total no. of pixels	3.072×10^6	4.608×10^6
Pixel size (μm^2)	55x50 60x50	70x50 85x50
Sensitive Area (mm^2)	44.8x12.5	61.44x12.5



Wafer size limits the largest possible module. Ladders in layers are made by gluing 2 half modules together



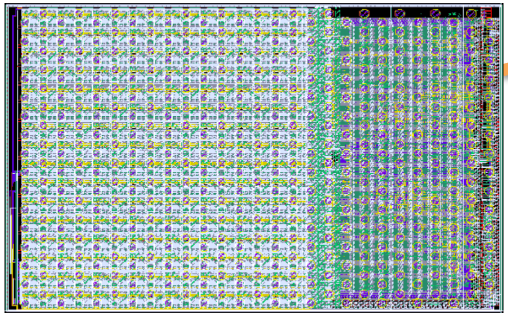
Sensors for Belle II will be 75 µm thick
S ≈ 6000 e/h, N = 50nA/(0.5 nA/e) = 100e ENC
S/N ≈ 60



Material 1st layer ≈ $0.2\%X_0$

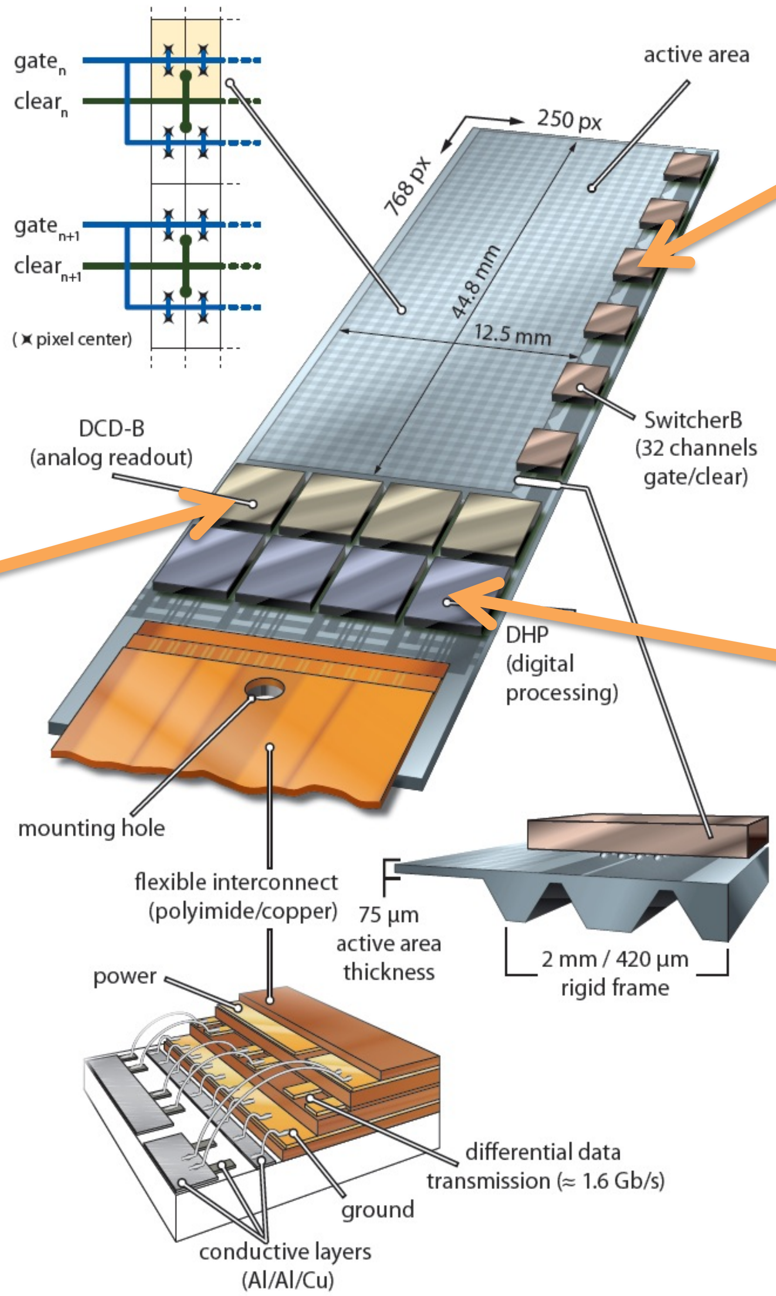
The DEPFET half/module

DCDB (Drain Current Digitizer)
Analog frontend

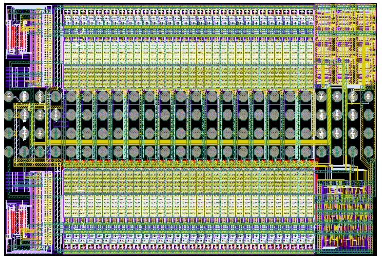


Amplification and digitization of DEPFET signals.

256 input channels
8-bit ADC per channel
92 ns sampling time
UMC 180 nm
Rad hard design

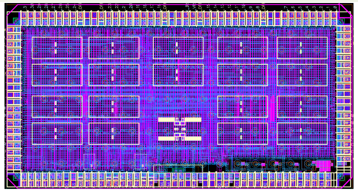


SwitcherB
Row Control



AMS/IBM HVCMOS 180 nm
Size 3.6 × 1.5 mm^2
Gate and Clear signal
32x2 channels
Fast HV ramp for Clear
Rad. Hard proved (36 Mrad)

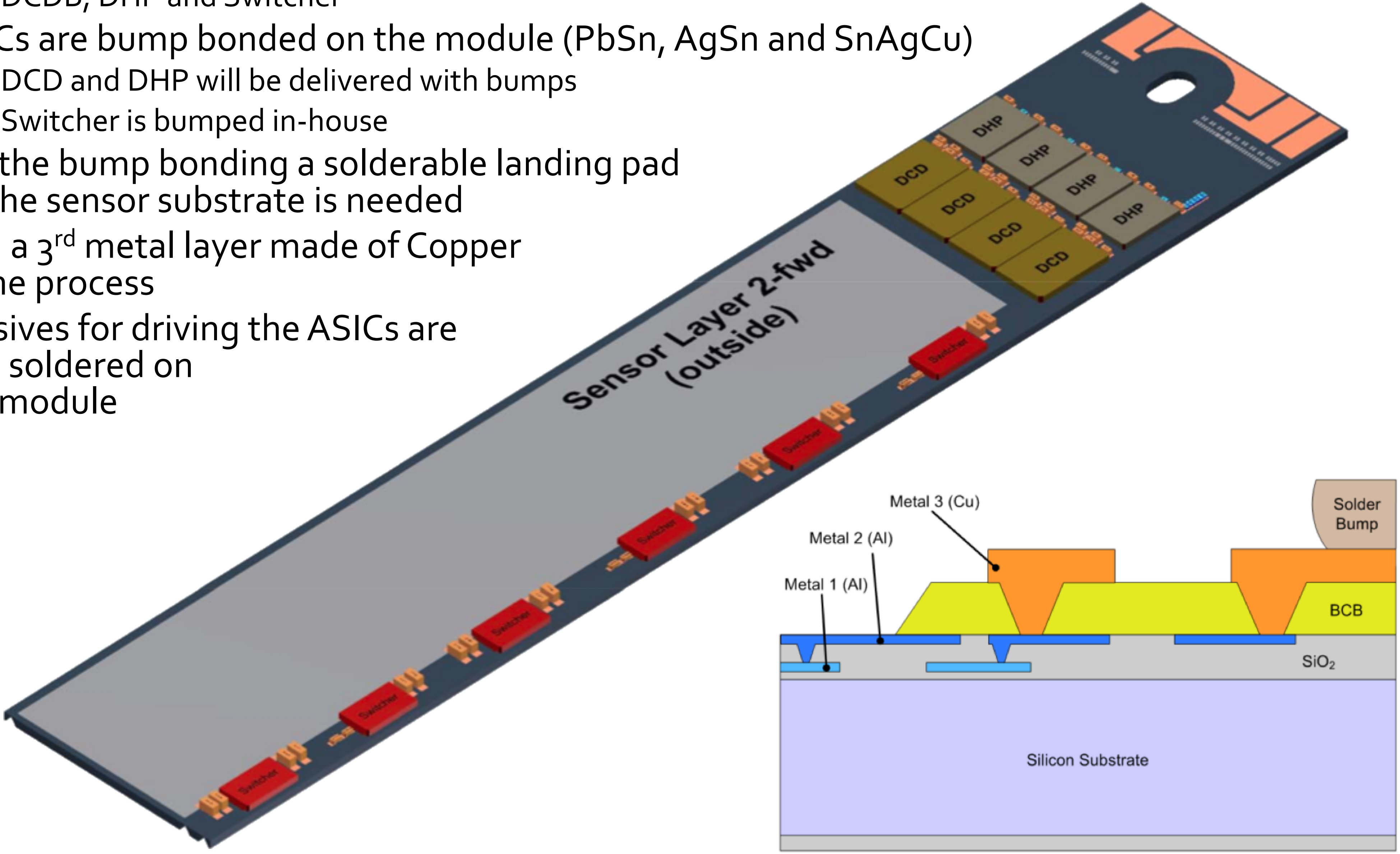
DHP (Data Handling Processor)
First data compression



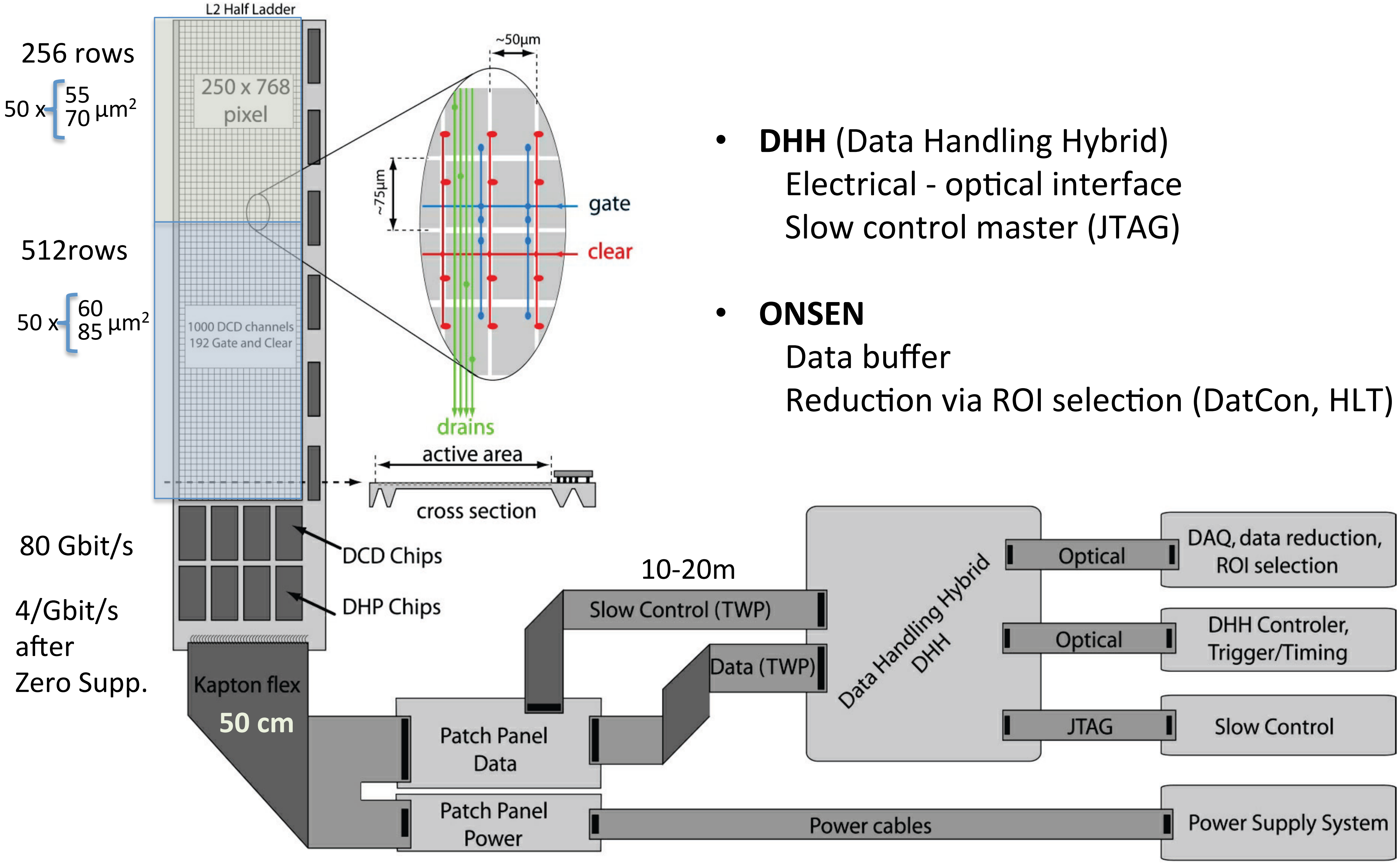
IBM CMOS 90 nm (TSMC 65 nm)
Size 4.0 × 3.2 mm^2
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing and trigger control
Rad. Hard proved (100 Mrad)

The DEPFET half module

- ✓ Three different types of ASICs on the module
  - ➔ DCDB, DHP and Switcher
- ✓ ASICs are bump bonded on the module (PbSn, AgSn and SnAgCu)
  - ➔ DCD and DHP will be delivered with bumps
  - ➔ Switcher is bumped in-house
- ✓ For the bump bonding a solderable landing pad on the sensor substrate is needed
- ✓ Add a 3rd metal layer made of Copper in the process
- ✓ Passives for driving the ASICs are also soldered on the module



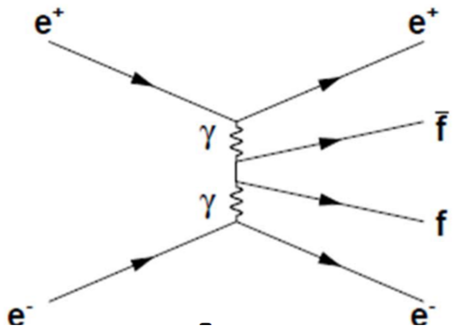
Off module signal flow



- **DHH** (Data Handling Hybrid)
  Electrical - optical interface
  Slow control master (JTAG)
- **ONSEN**
  Data buffer
  Reduction via ROI selection (DatCon, HLT)

Background sources

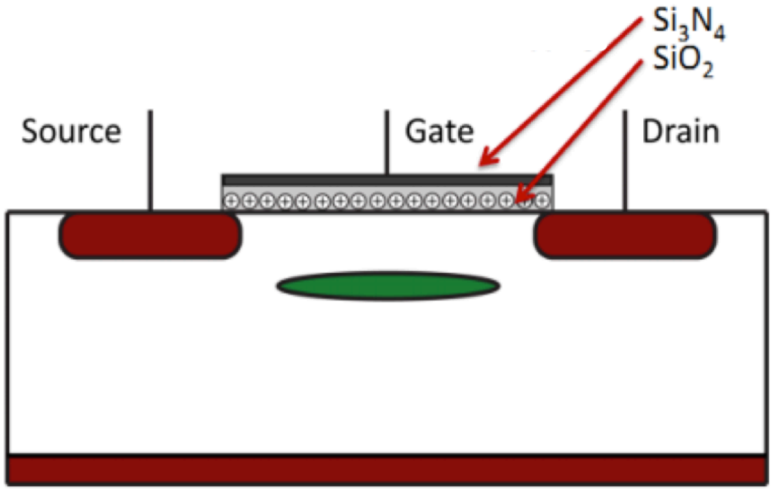
- ✓ PXD occupancy should be below 2%
- ✓ Radiation environment
  - ➔ 4-fermion final state QED processes
  - ➔ Touschek effect
  - ➔ Beam-gas interactions
  - ➔ Radiative Bhabha scattering
  - ➔ Synchrotron radiation (being studied)

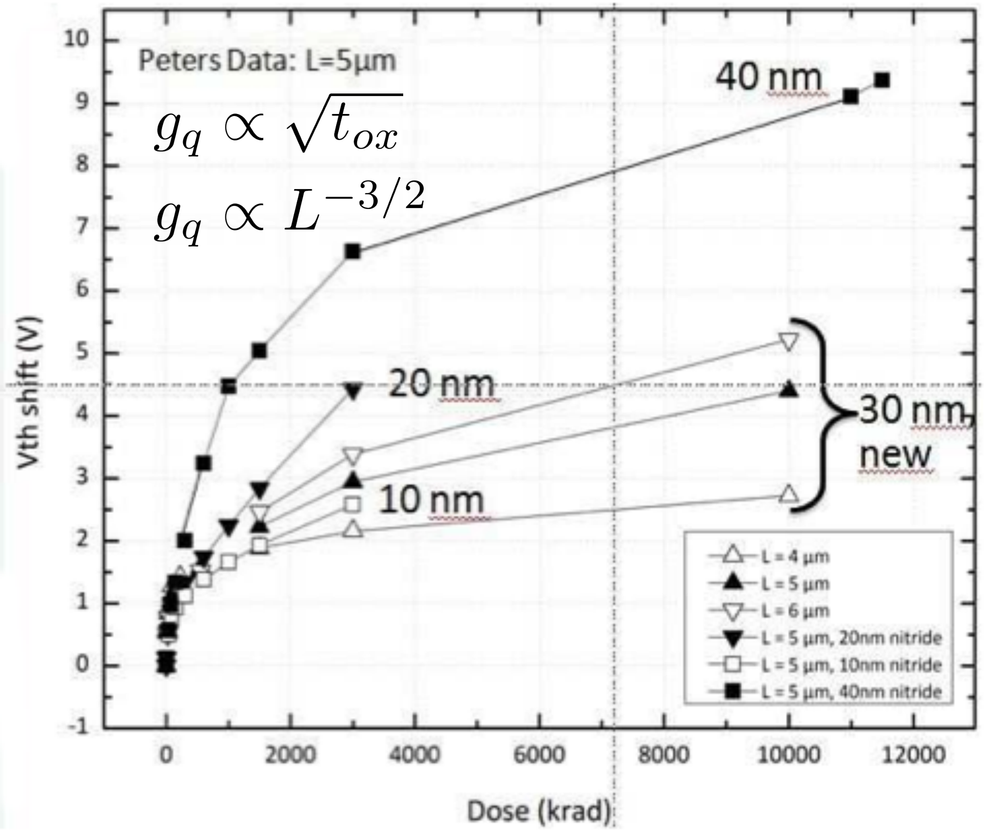


Background	Occupancy(%)	
	Layer 1	Layer 2
Two gamma	0.8	0.3
Touschek	<0.03	<0.03
Radiative Bhabha	<0.13	<0.13
Beam-gas Coulomb	<0.01	<0.01
Total	**<1**	**<0.5**

Radiation Tolerance

- ✓ PXD damage
  - ➔ Surface or oxide damage.
    Expected dose 1.9 Mrad/y
    - ↳Change in operating voltage
    - ↳SWB can cope with it.
  - ➔ Bulk damage
    Φ_{eq}=1.2x10^{13} cm^{-2} /y
    - ↳Increase in leakage current
    - ↳No type inversion expected until Φ_{eq}~ 2x10^{14} cm^{-2}~
- ✓ Can be operated for 10 year lifetime

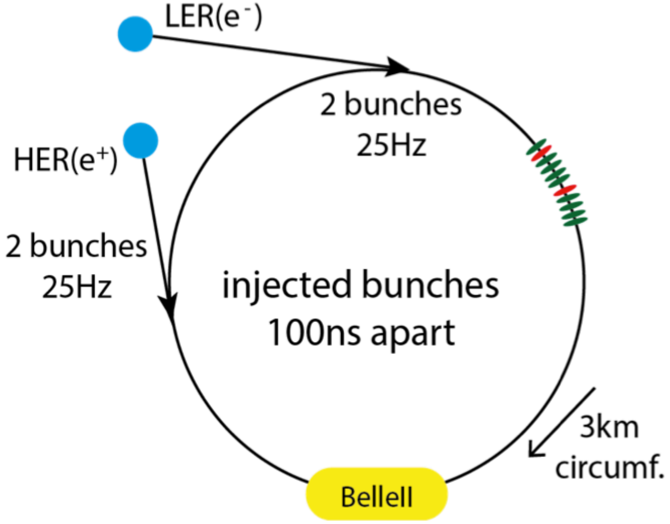




Thinner gate oxide (SiO_2)
SiO_2 layer covered by an extra Si_3N_4 layer
Optimal oxide thickness is a trade of between:

- Threshold voltage shift and
- Internal amplification (g_q)

Gated clear



LER(e^-)

HER(e^+)

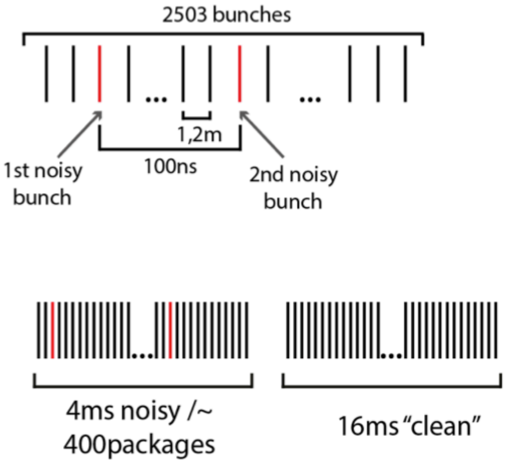
2 bunches
25Hz

2 bunches
25Hz

injected bunches
100ns apart

3km
circumf.

BelleII



2503 bunches

1st noisy
bunch

100ns

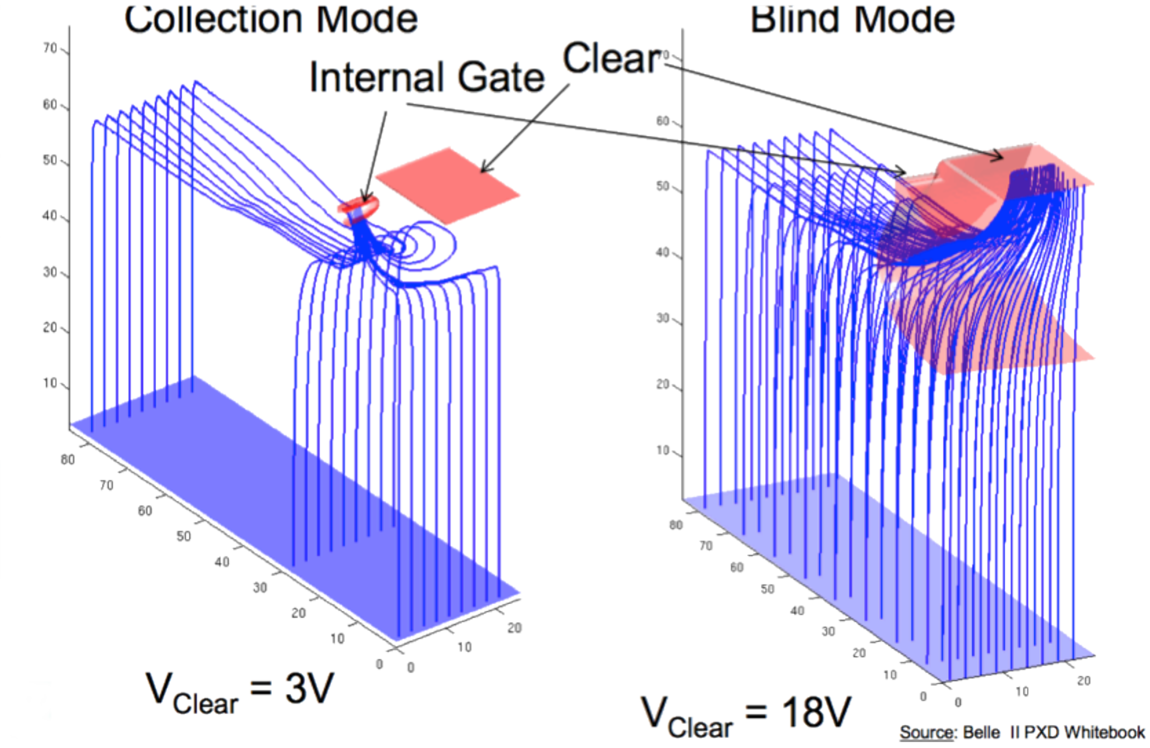
1,2m

2nd noisy
bunch

4ms noisy /~
400packages

16ms "clean"

SuperKEKB operates in **continuous injection**
Noisy bunches appear during the first 4ms
They appear in a very "specific" time window



$V_{Clear} = 3V$

$V_{Clear} = 18V$

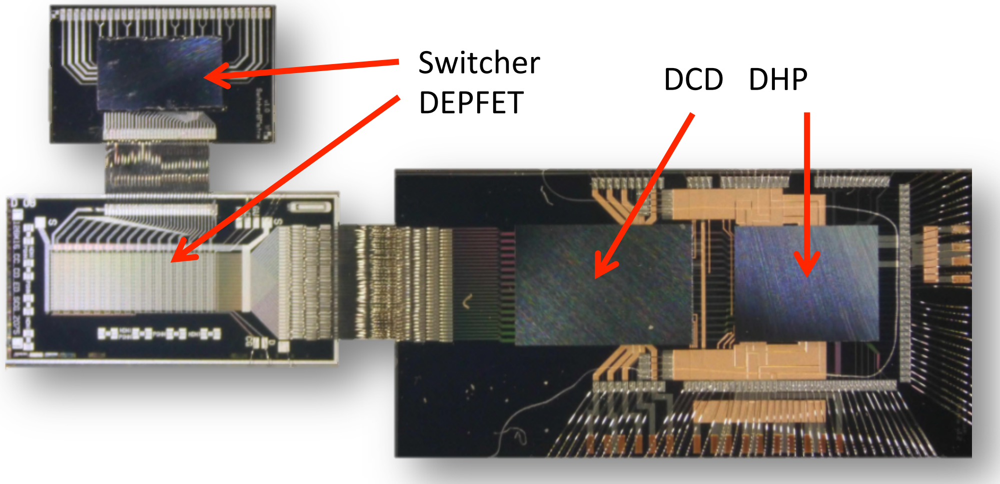
Source: Belle II PXD Whitebook

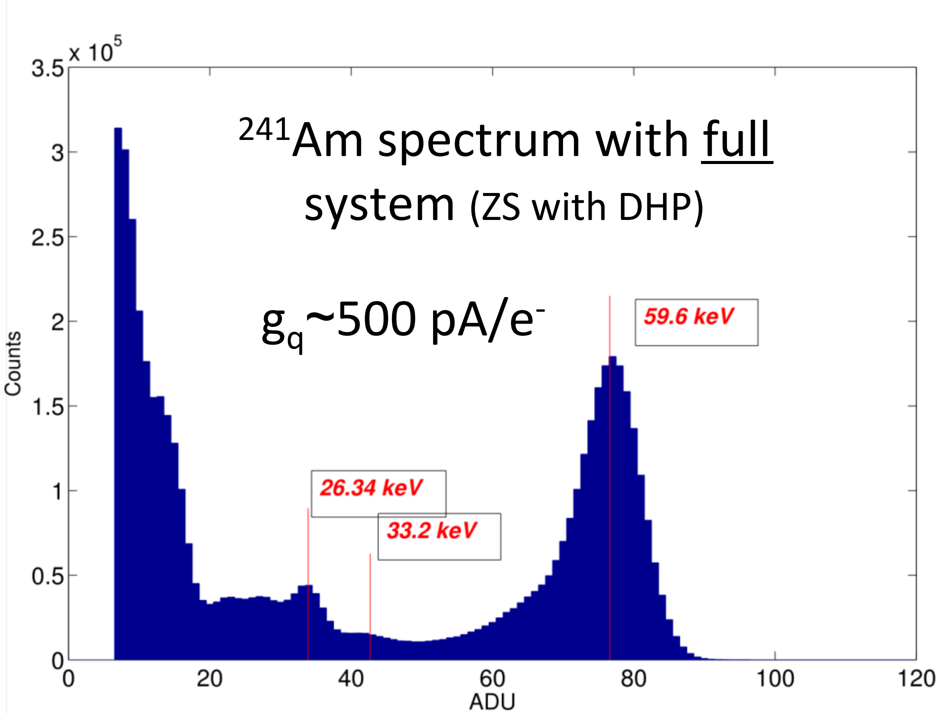
DEPFET operated in "blind mode" during "noise injection"

Signals detected in "clean" periods are preserved

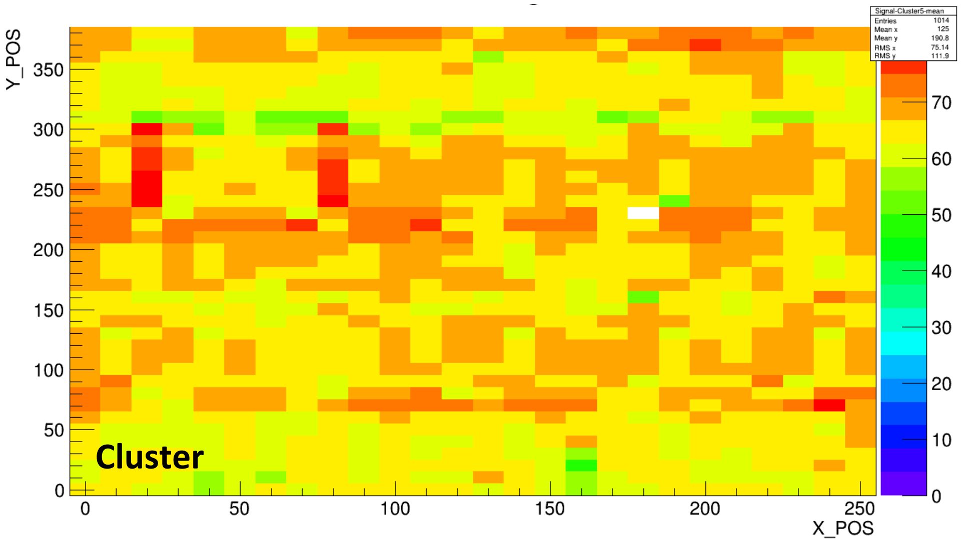
Laboratory tests: DEPFET sensor

- Biasing optimization (HV, ClearGate, Drift)
- Laser scan
  - Charge collection homogeneity
  - In pixel studies
- Radioactive source
  - System calibration




^{241}Am spectrum with full system (ZS with DHP)

g_q~500 pA/e$^-$



Homogeneous charge collection

Beam tests

PXD6 Belle II design

Thin (**50** µm) sensor 32x64 pixels

Pitch 50x75 μm^2

SwitcherB and DCDB at full speed

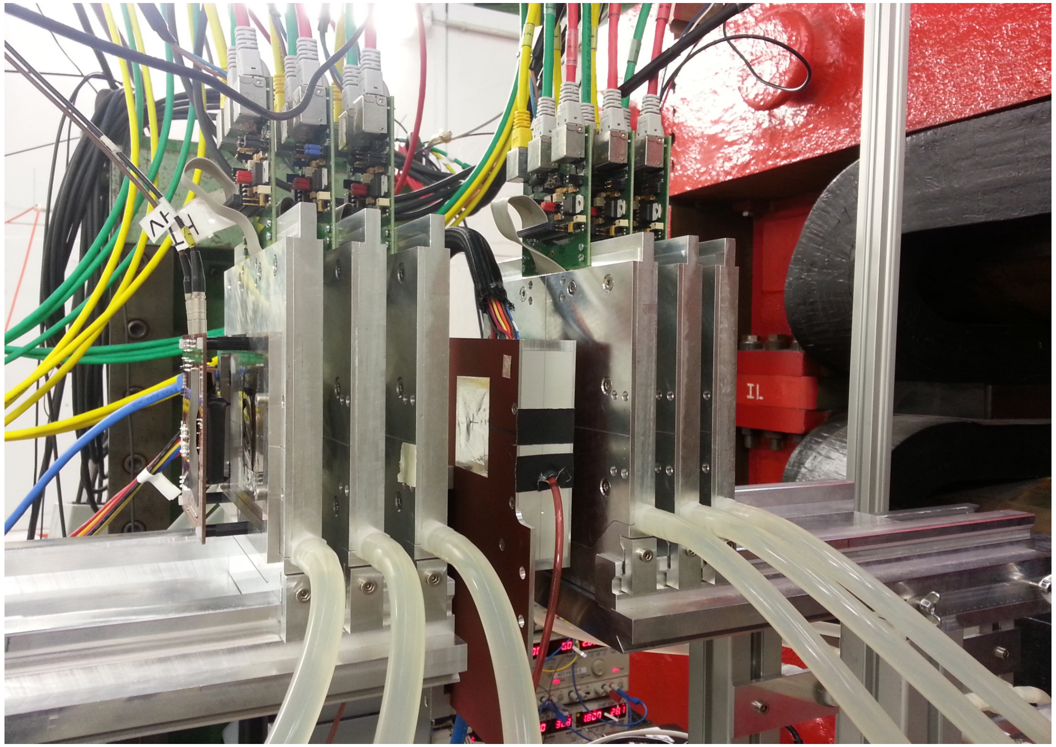
Belle II prototype power supply

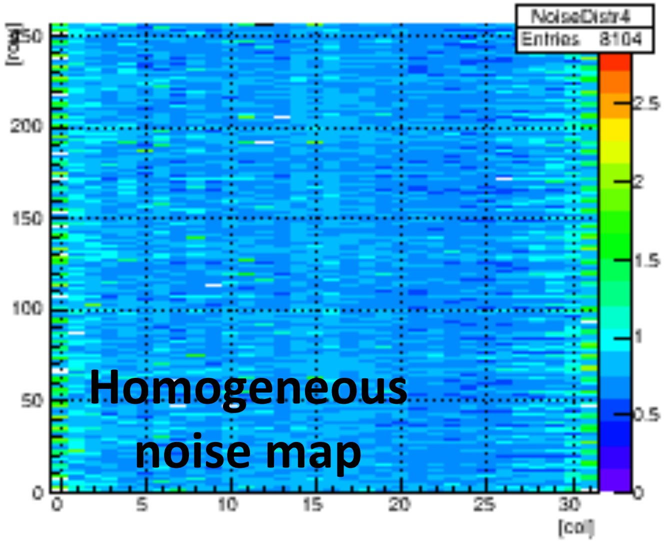
DCDB readout at 320 MHz

100 ns row time

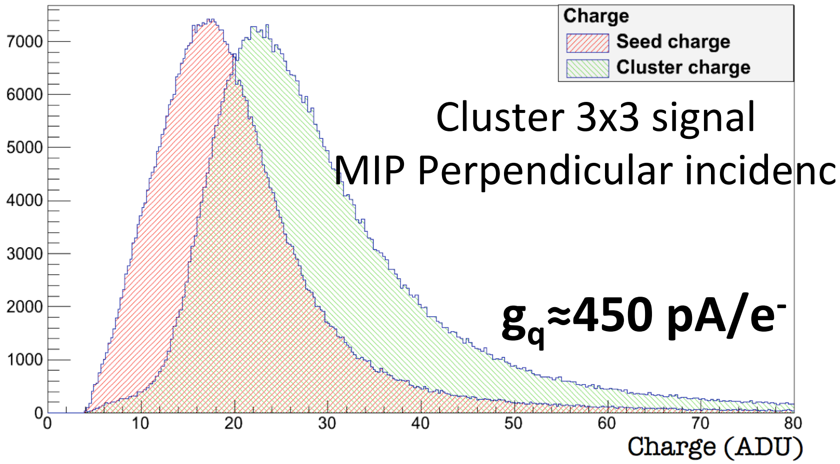
99% Efficiency

Signal-to-Noise ratio for MIPs: 20-40 depending on gate length





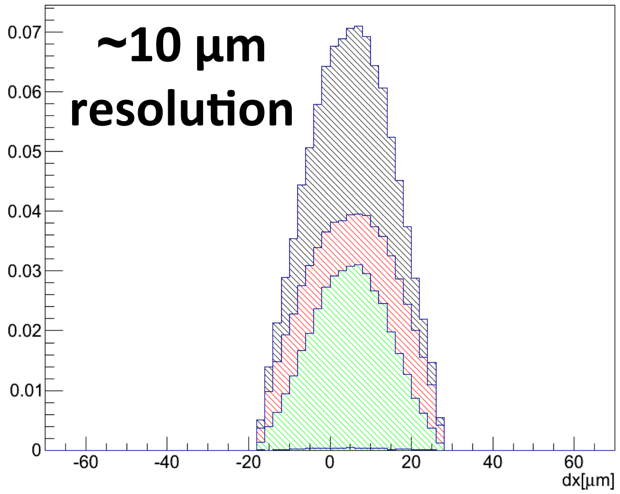
Homogeneous noise map



Cluster 3x3 signal

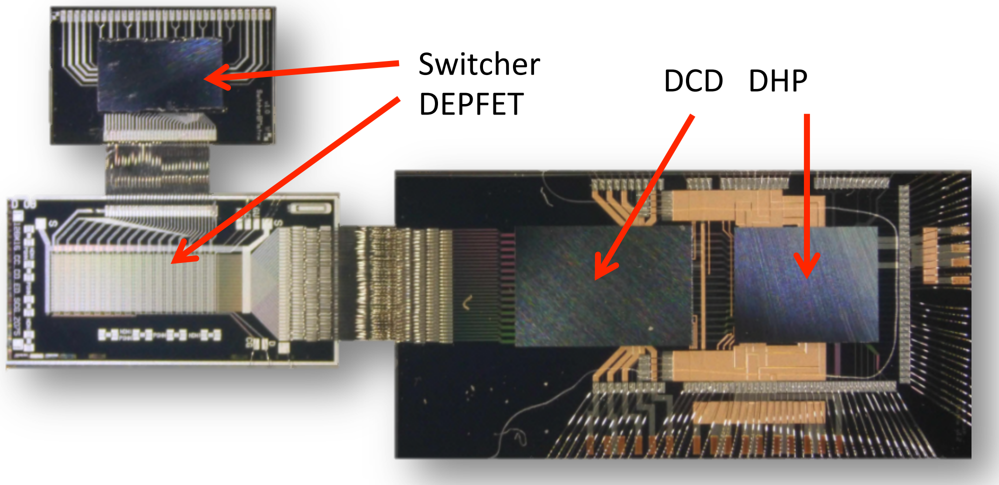
MIP Perpendicular incidenc

$g_q \approx 450$ pA/e$^-$



~10 µm resolution

Beam tests

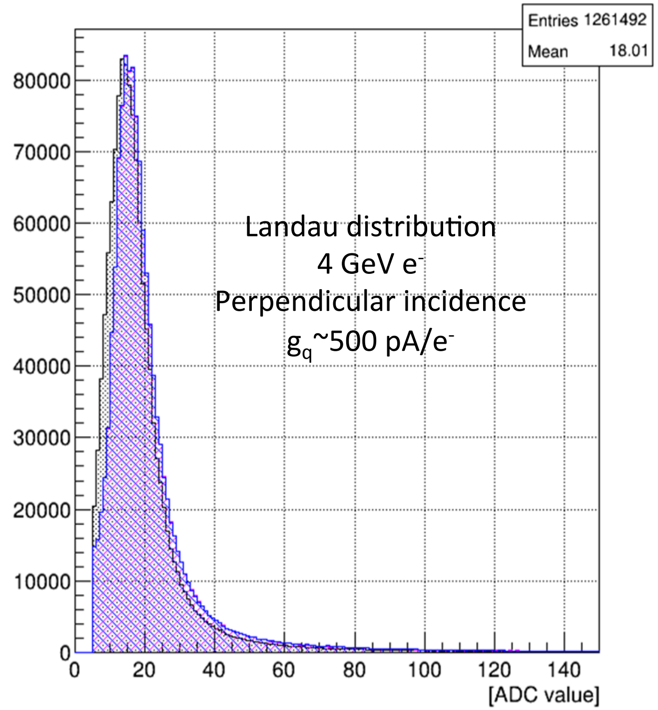


May 2013: Beam Test with hybrid 5.0
Test complete readout chain

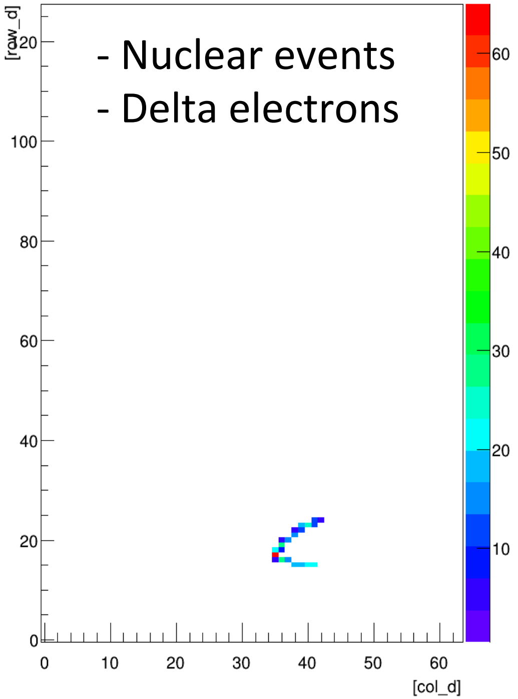
DEPFET => DCD => DHP => DHH => Onsen

Uses 'final' components:
Power Supplies
DAQ Software
Slow Control Software

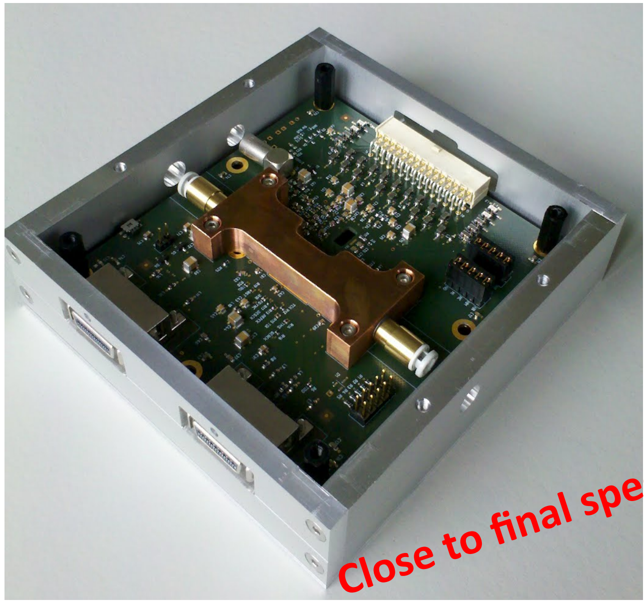
Analysis in progress



Landau distribution
4 GeV e^-
Perpendicular incidence
g_q~500 pA/e^-

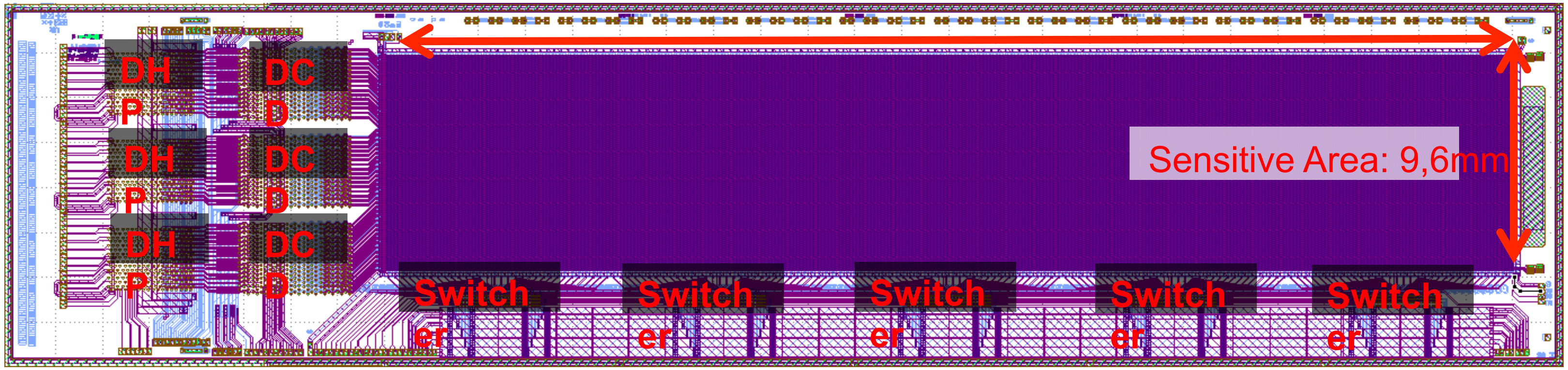


- Nuclear events
- Delta electrons

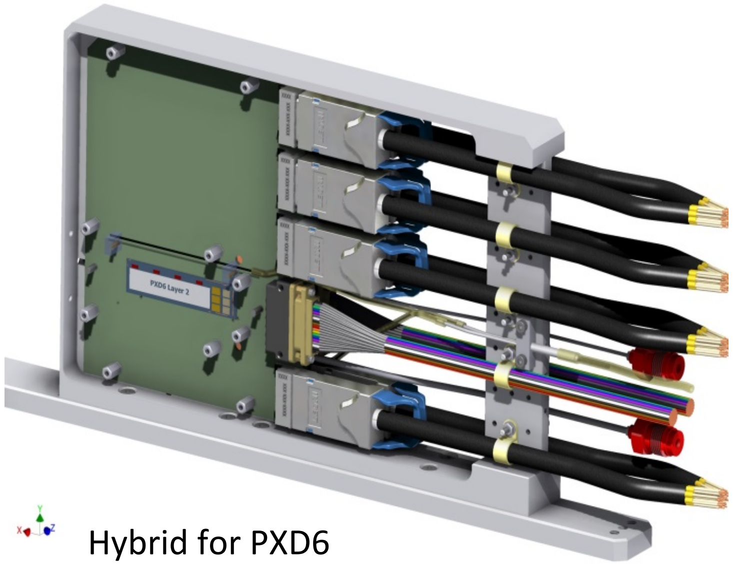


Close to final specs!

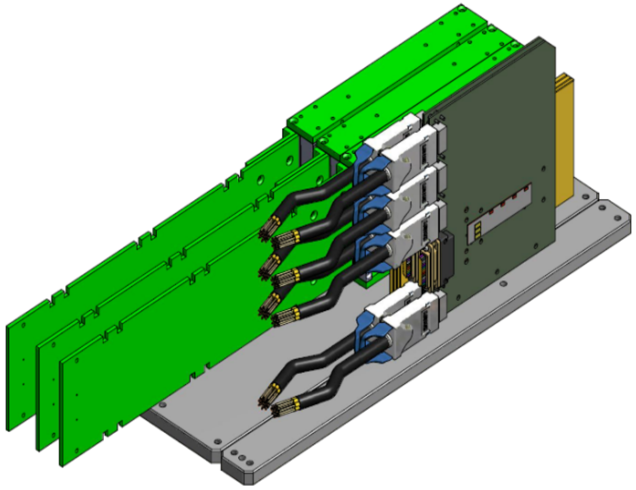
PXD/SVD Beam test at DESY 2014



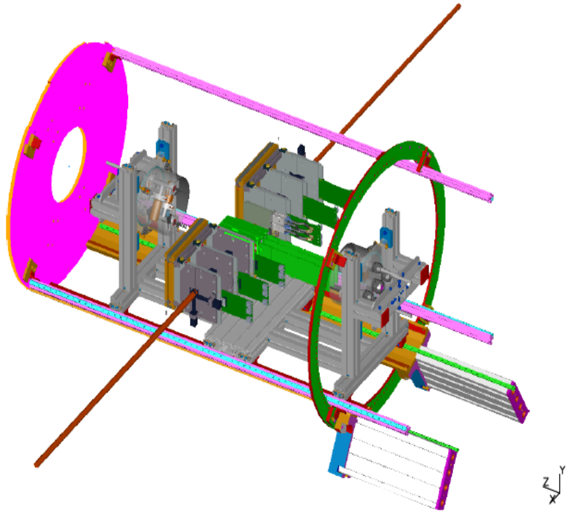
Modules from PXD6 prototype production (slightly different from final PXD9)



Hybrid for PXD6

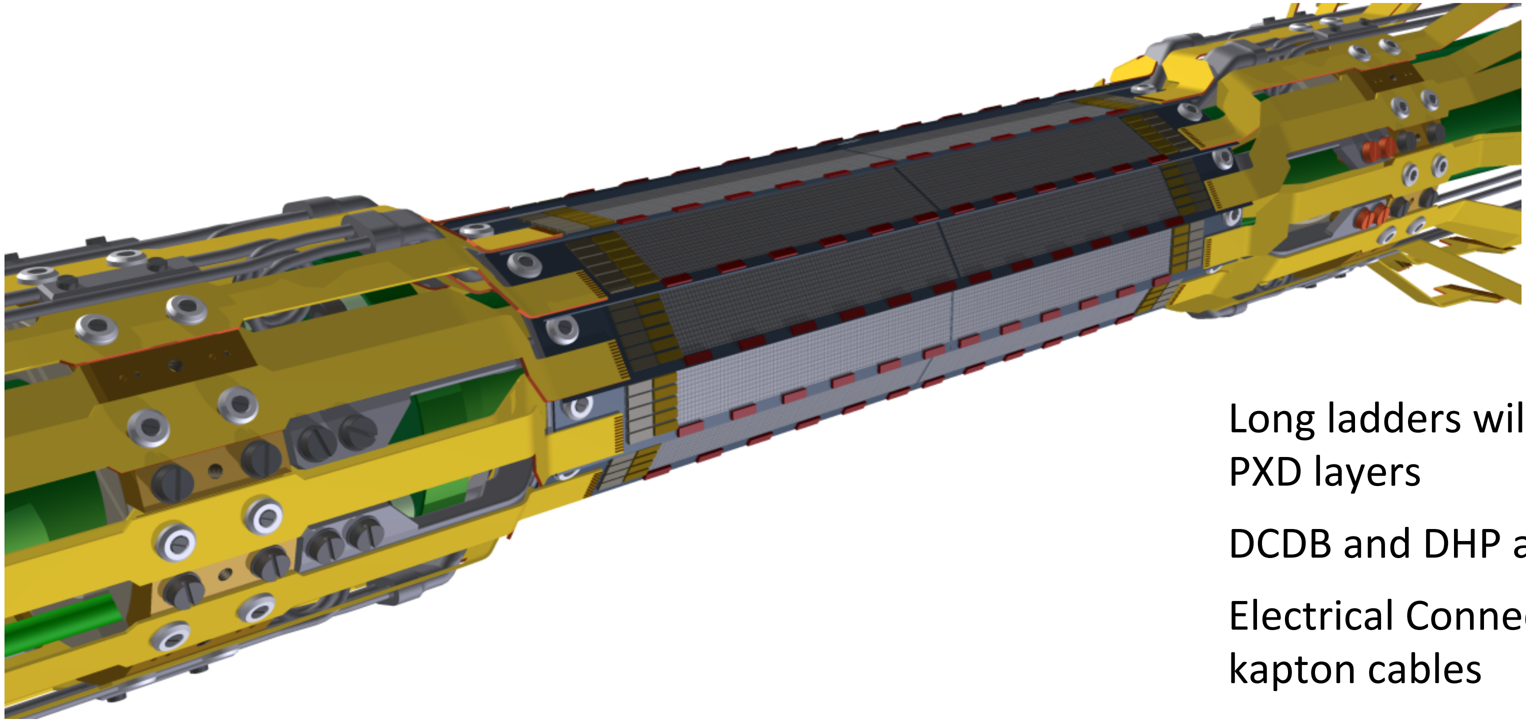


3 SVD and 2 PXD modules



Arrangement in magnet with EUDET telescope

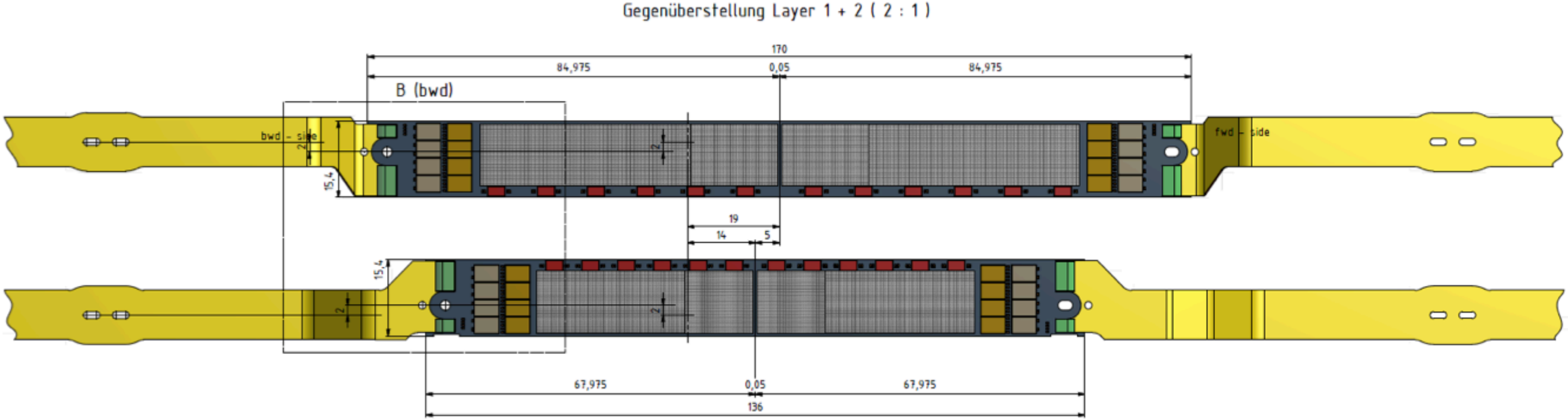
The DEPFET modules



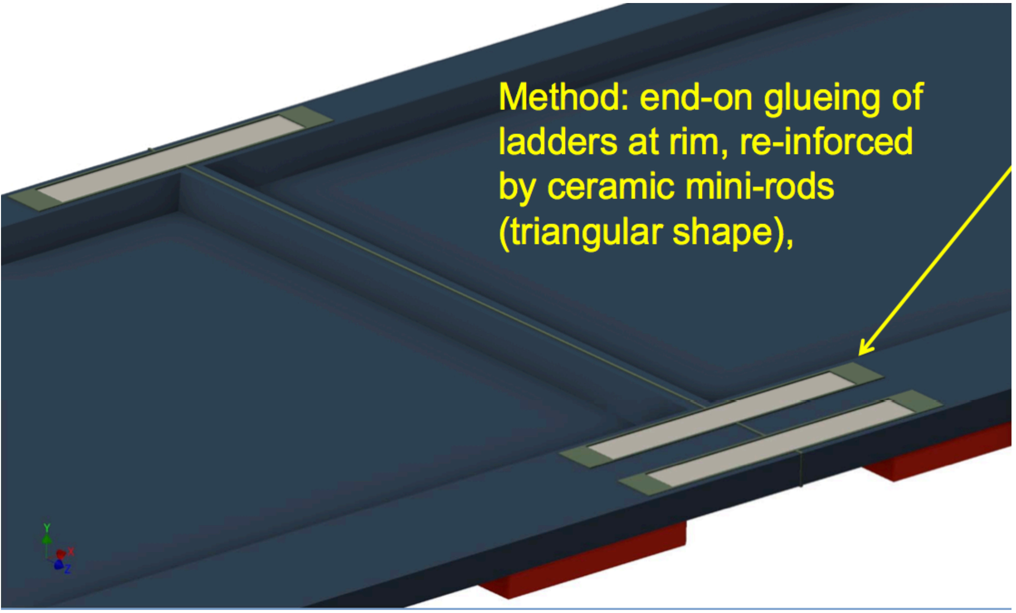
Long ladders will form the cylinders of the two PXD layers

DCDB and DHP are outside the acceptance

Electrical Connection to outside world is via kapton cables

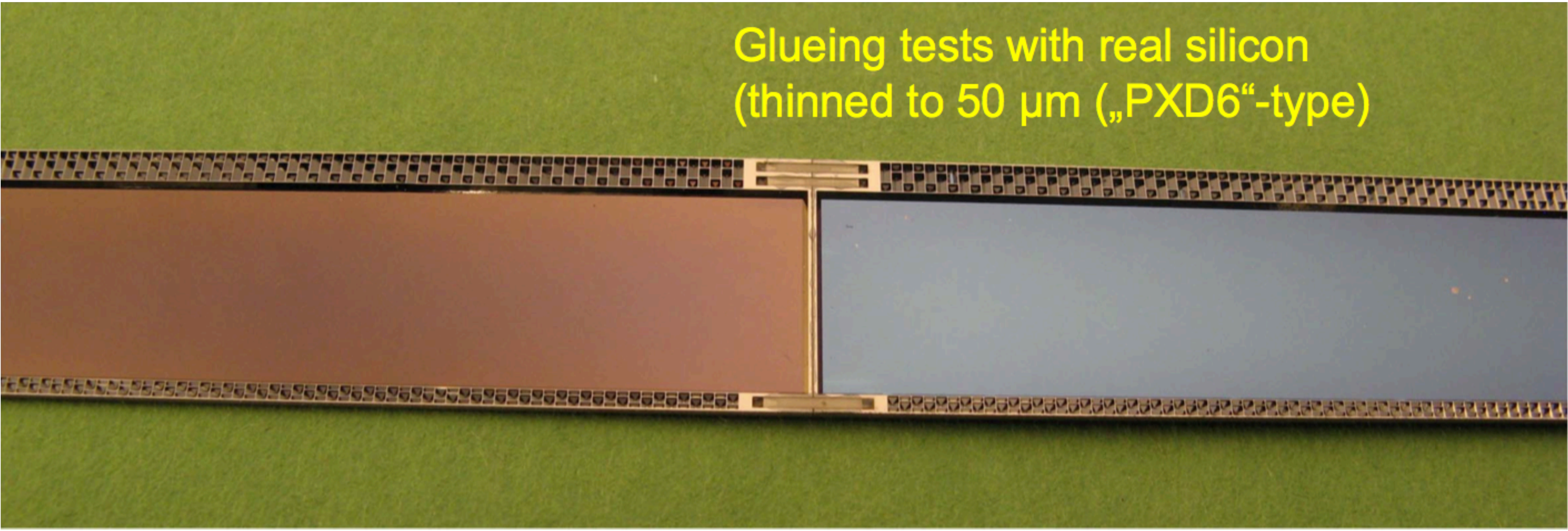


The long ladder



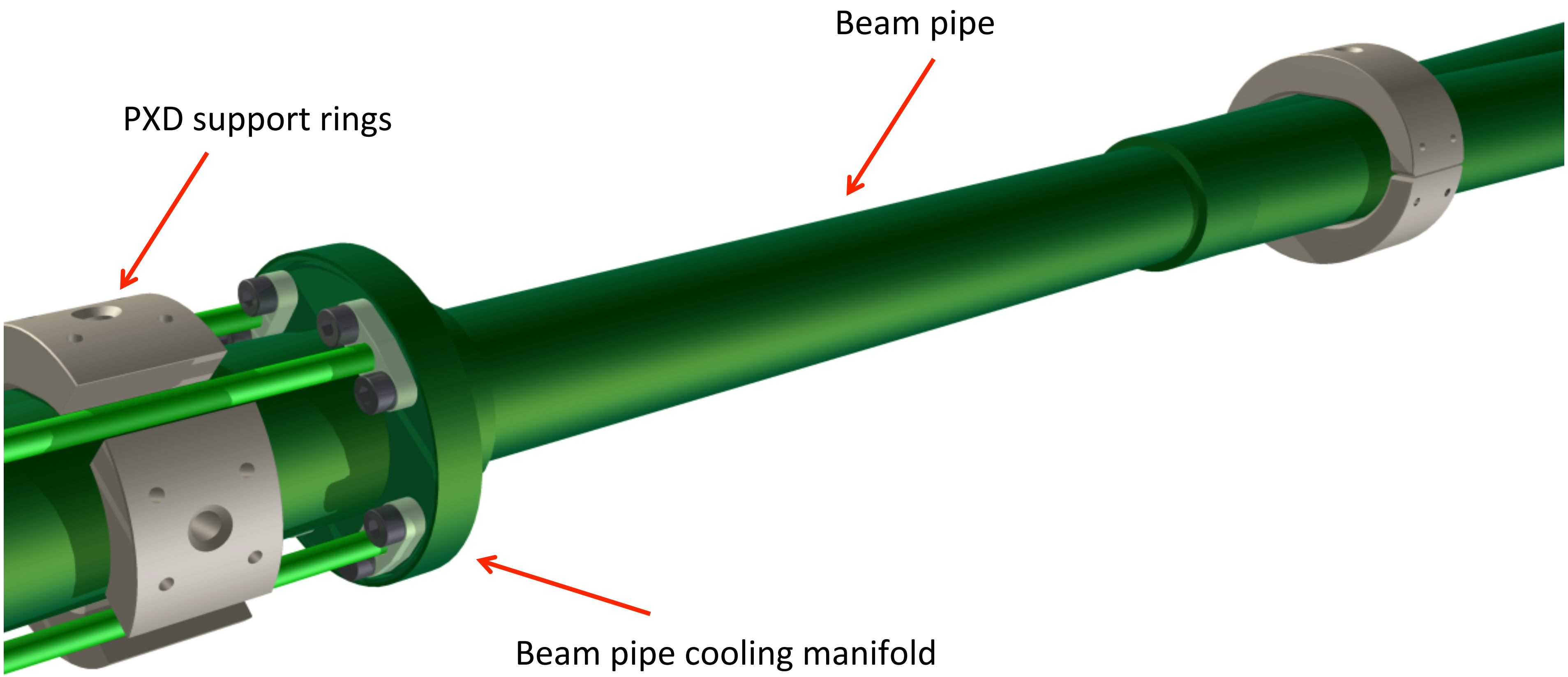
Method: end-on glueing of ladders at rim, re-inforced by ceramic mini-rods (triangular shape),

Two half modules are glued together to make the long ladder



Glueing tests with real silicon (thinned to 50 µm („PXD6“-type)

PXD mechanics

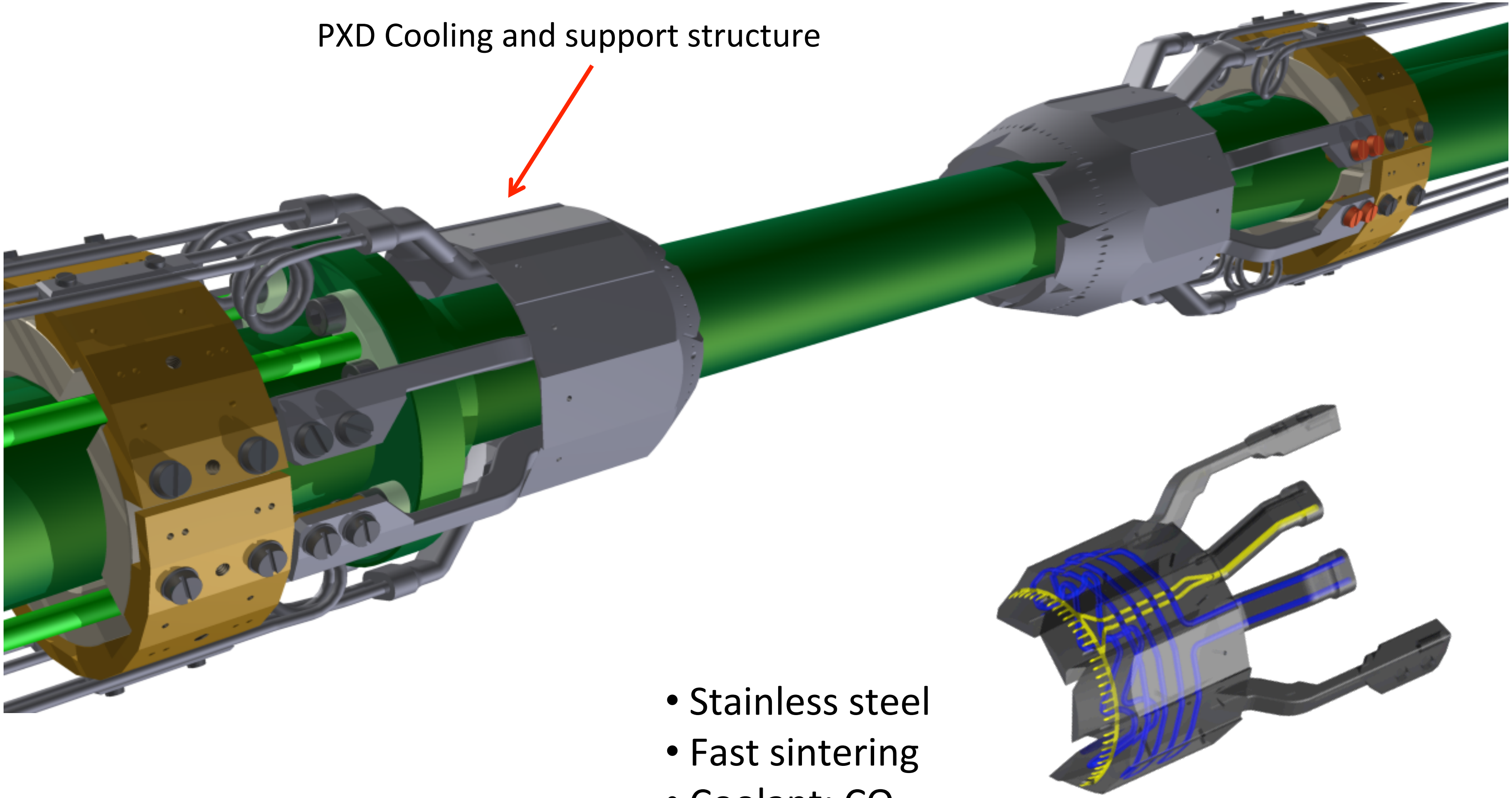

Beam pipe

PXD support rings

Beam pipe cooling manifold

- Thinner pipe
- Smaller radius
- Lighter materials

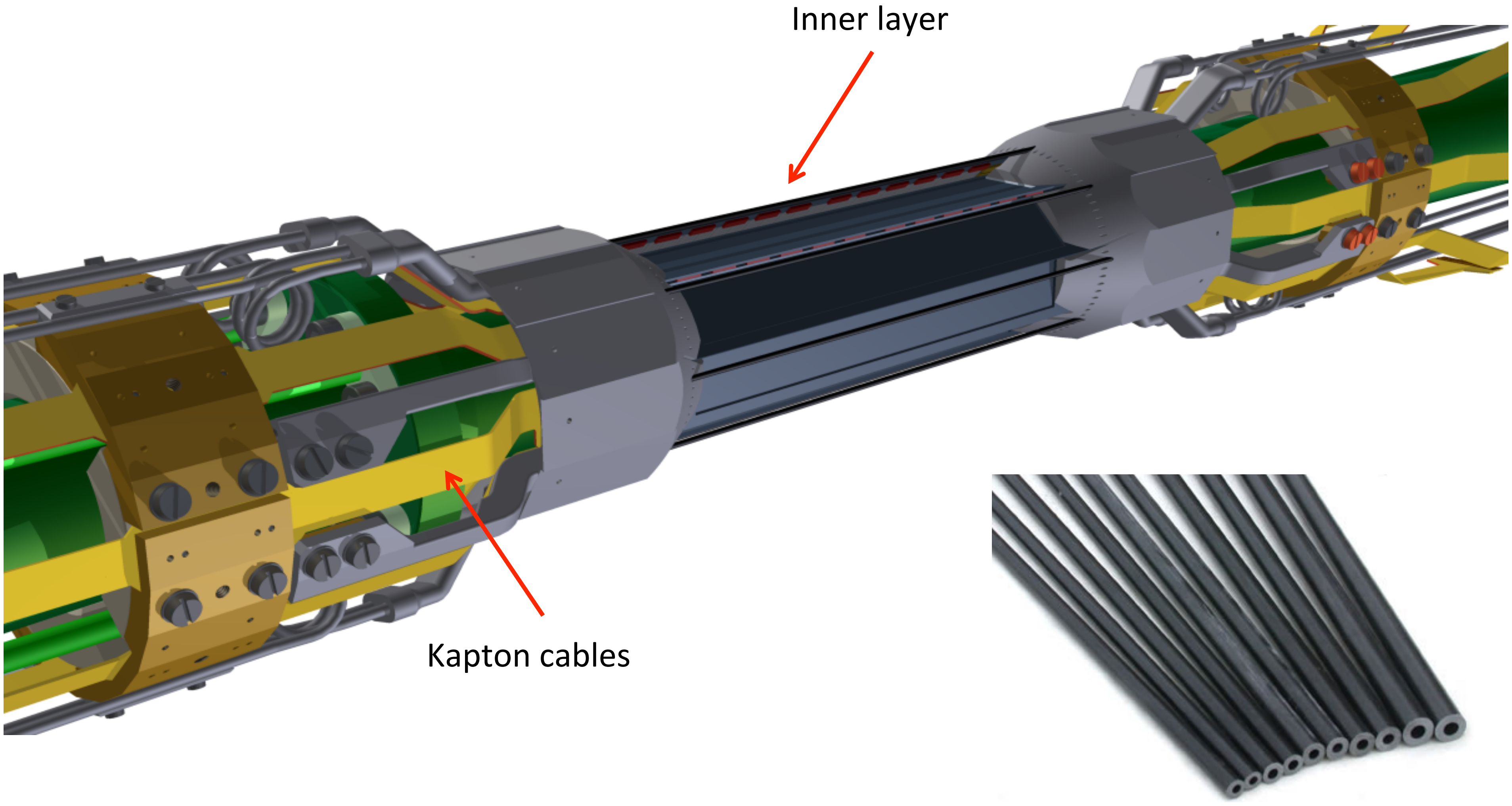
PXD mechanics


PXD Cooling and support structure

- Stainless steel
- Fast sintering
- Coolant: CO_2

Blue: CO_2 capillaries
Yellow: Air channels

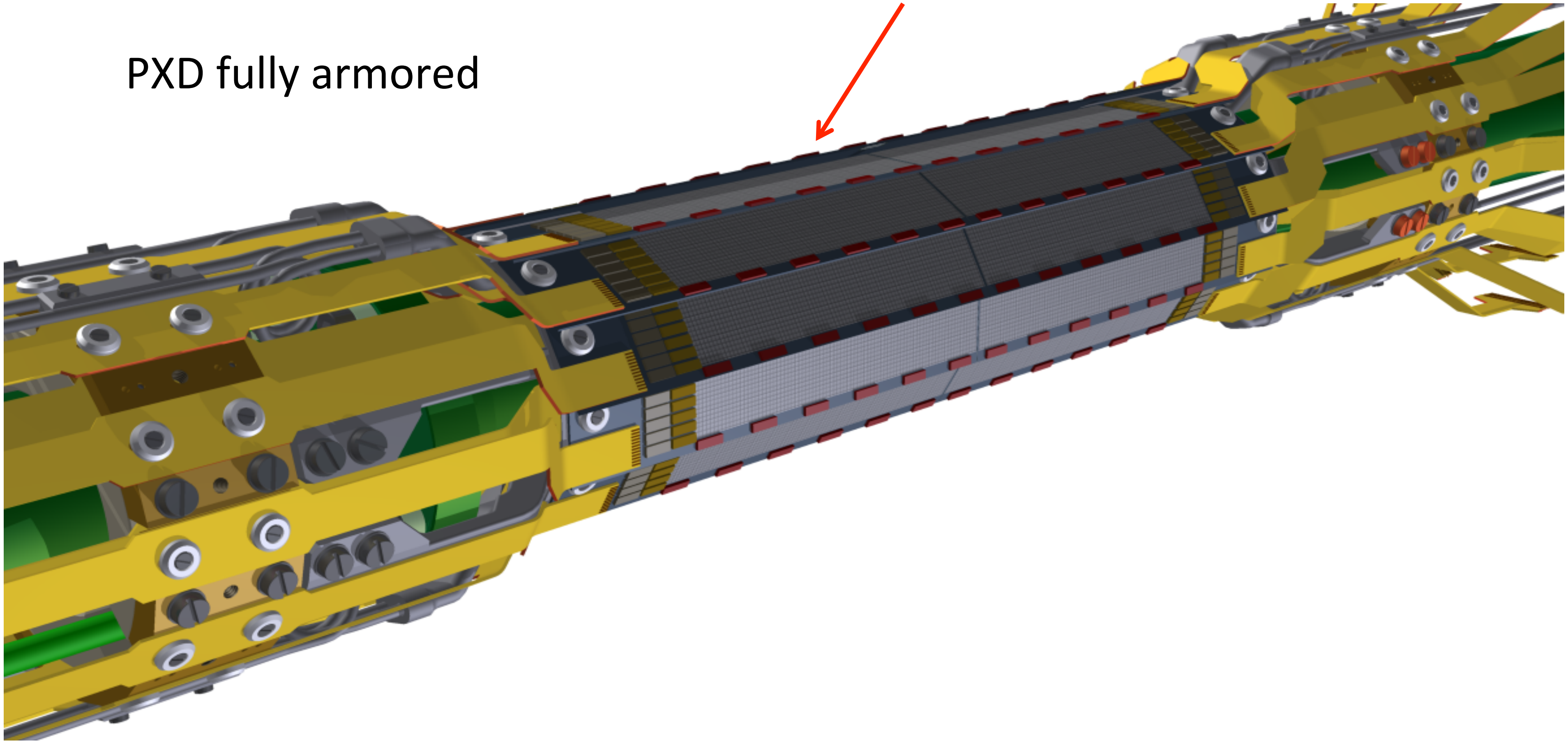
PXD mechanics



Inner layer close to the IP (14mm)

Additional carbon fibers capillaries to cool the Switchers, if needed (not tested yet)

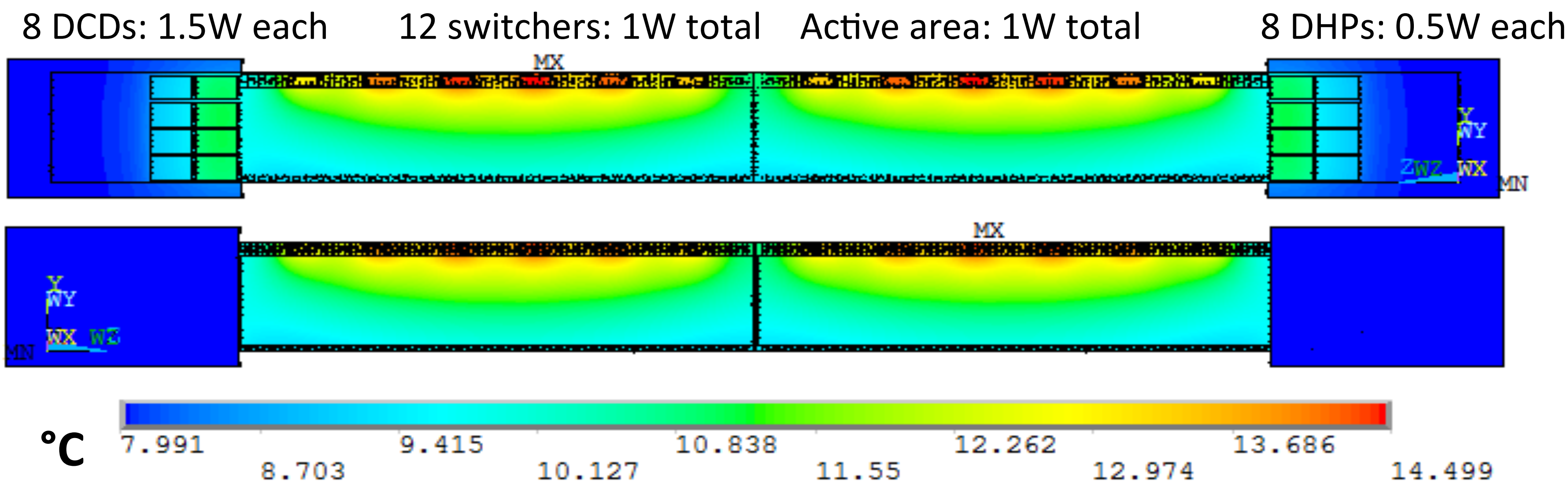
PXD mechanics

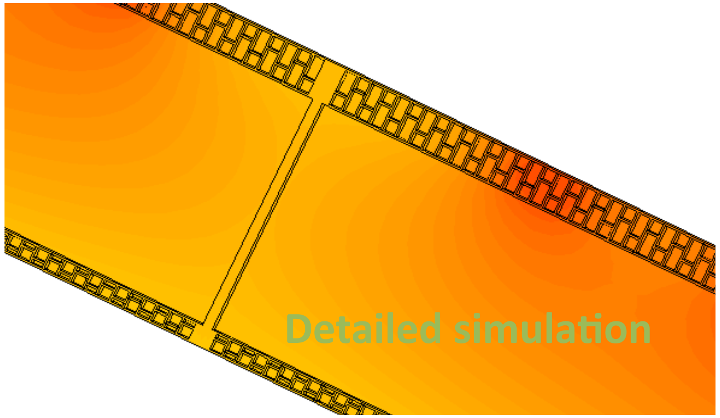

PXD fully armored

- Low material budget cooling
  - Massive structures outside the acceptance to cool down the readout chips
  - The center of the ladder rely on cold air

Temperature simulation

18W one ladder 360W full PXD





Set of reasonable environment conditions

T_{env}=-5°C
T_{cb}=8°C

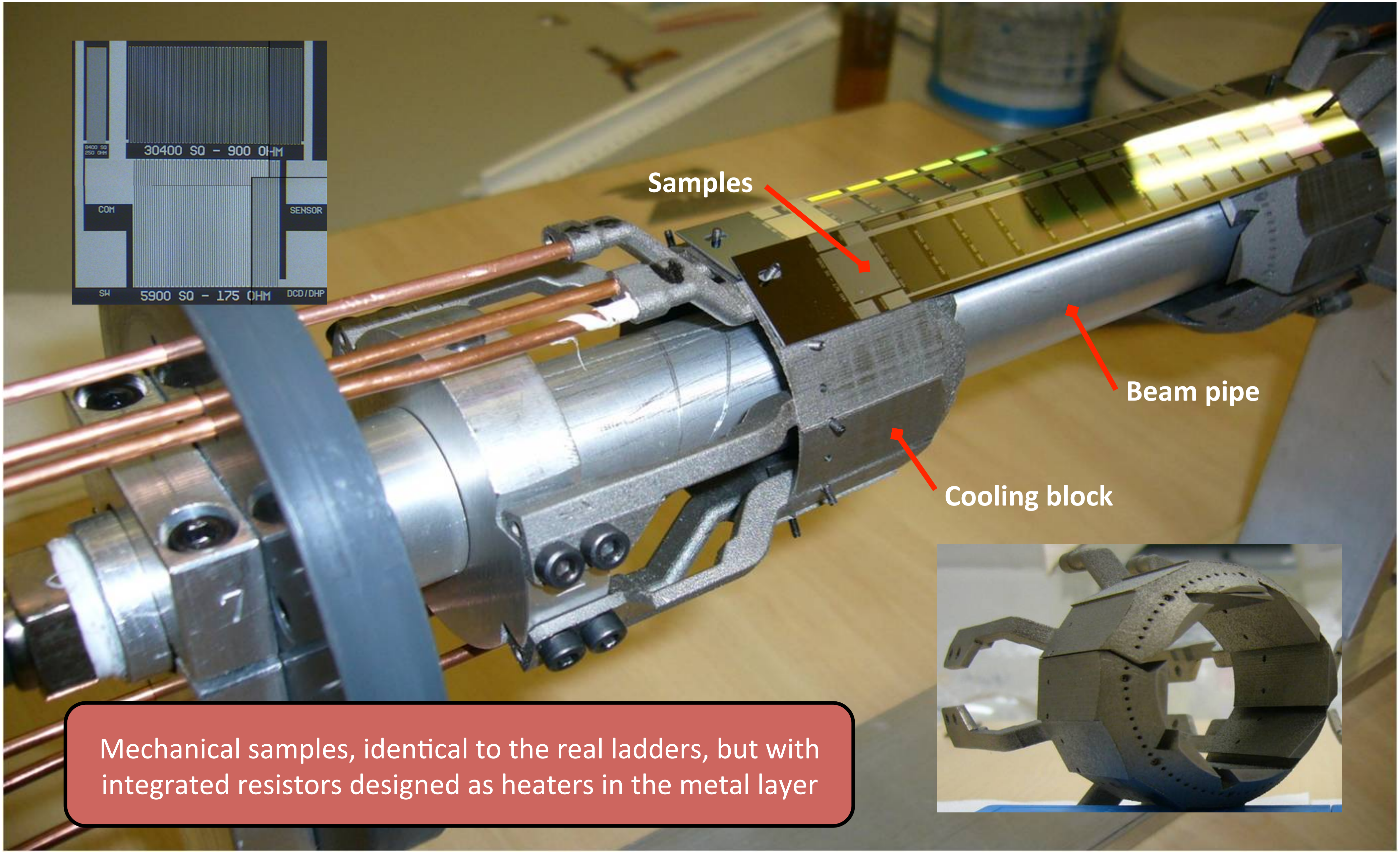
→

$T_{SENSORmax}$=14°C
DeltaT=4.7°C

$$\Delta L < 3\mu m$$

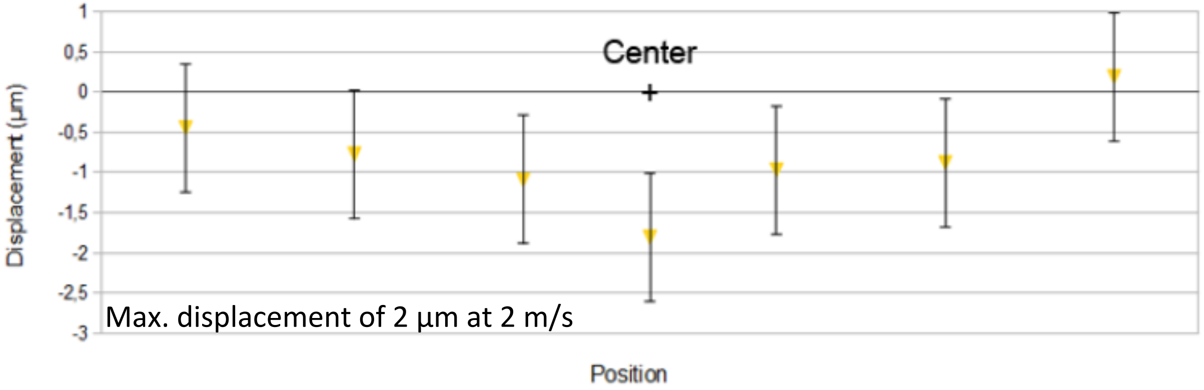
Just a **gentle air flow (2 m/s)** is enough to decrease and homogenize the temperature distribution

Thermo-mechanical measurements

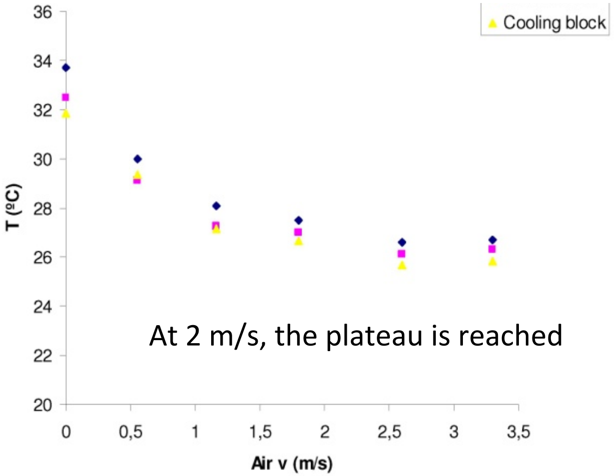


Mechanical samples, identical to the real ladders, but with integrated resistors designed as heaters in the metal layer

Thermo-mechanical measurements

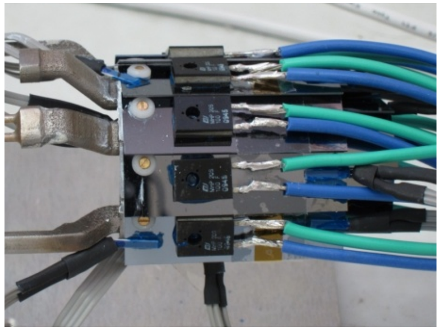


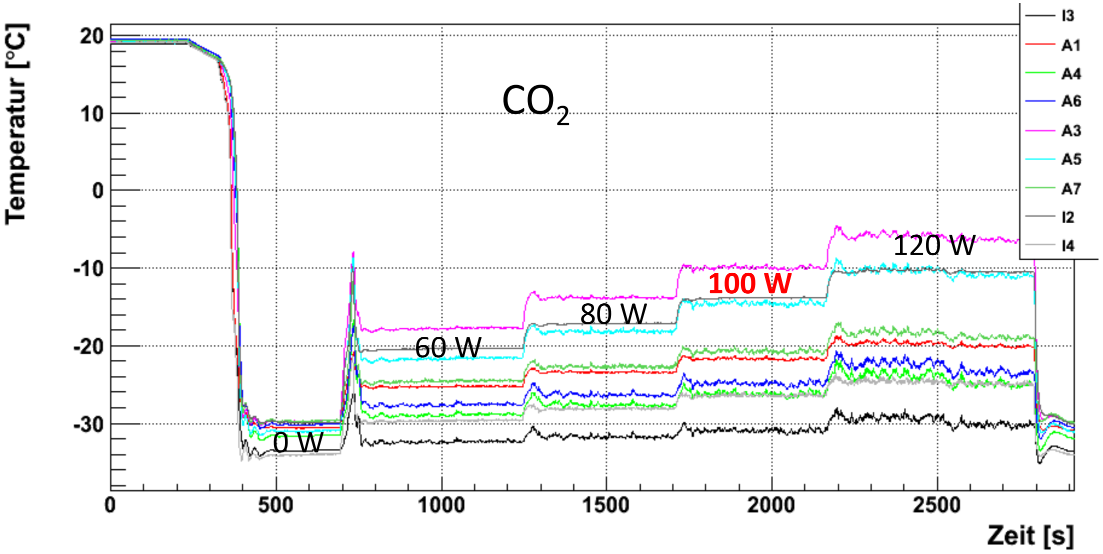
Max. displacement of 2 µm at 2 m/s

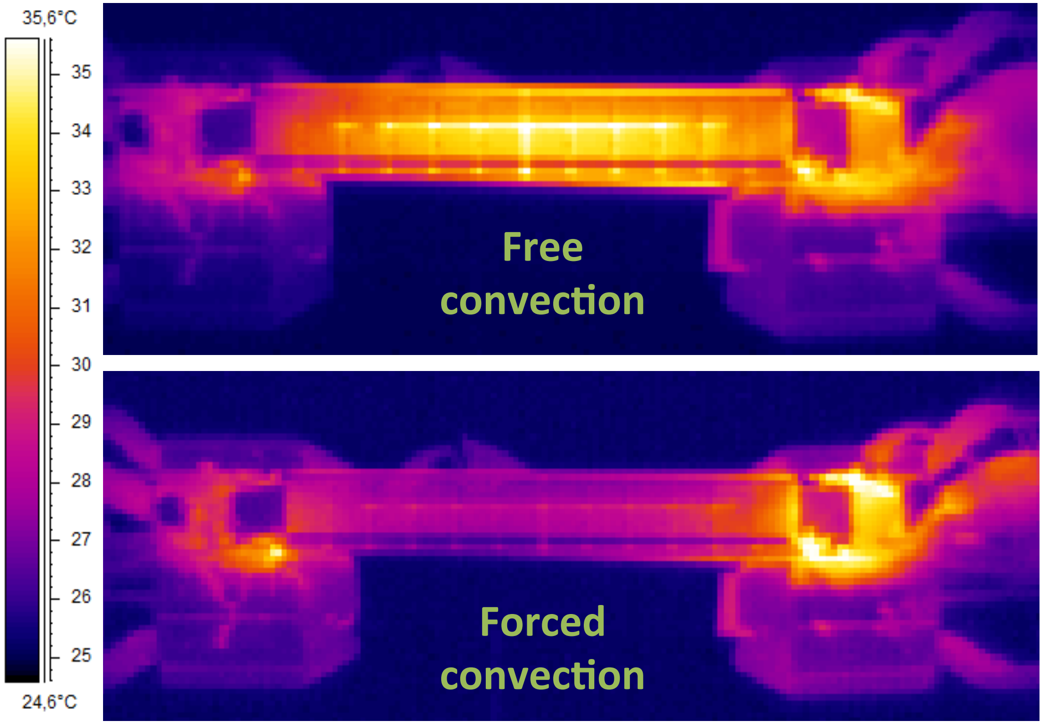


At 2 m/s, the plateau is reached

- Stainless steel
- Fast sintering
- Blue: CO_2 capillaries
- Yellow: Air channels







Cooling proof of principle

CO2 cooling: MARCO

Multi-Purpose Apparatus for Research in CO2

Collaboration between CERN, NIKHEF and MPI
Principles by CERN/NIKHEF, design and construction by MPI

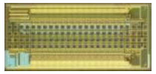
Common commissioning at CERN,in July delivered to DESY for the combined PXD/SVD test

Electric Multichip Module

E-MCM: Everything but the DEPFET

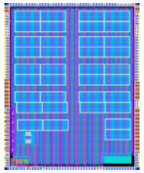
Electrically active prototype of a half ladder

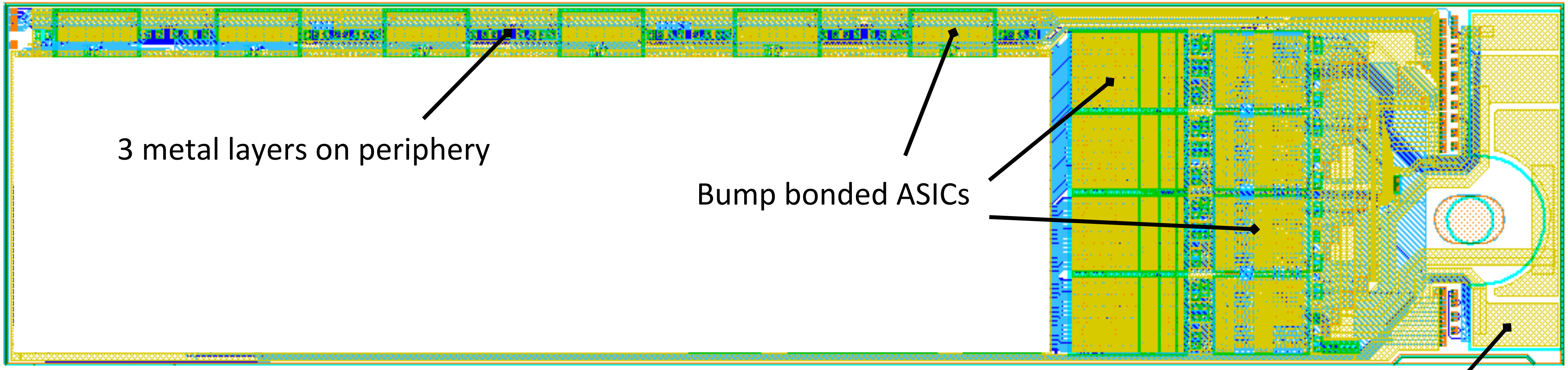
SW



DCD

DHP





3 metal layers on periphery

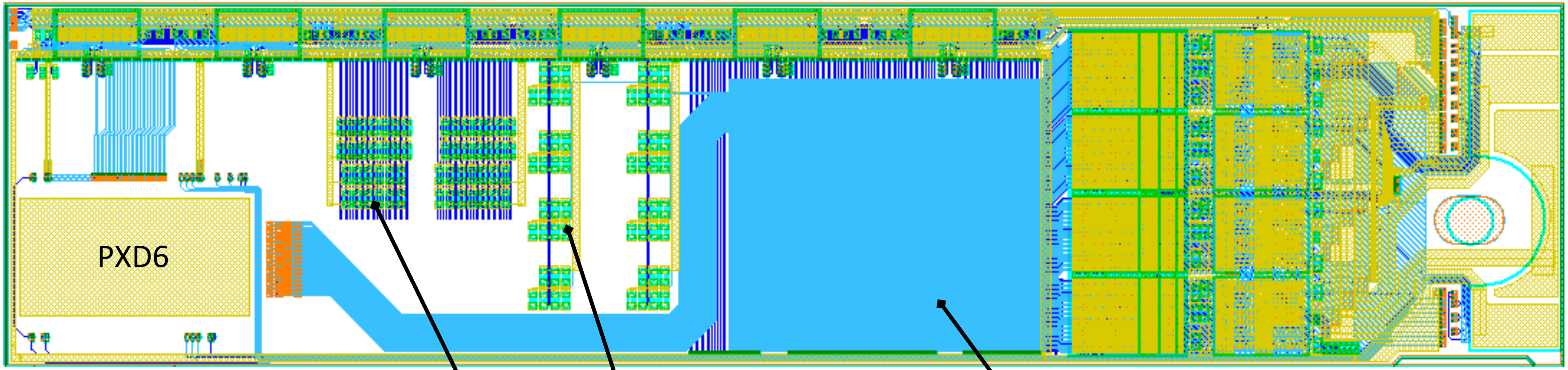
Bump bonded ASICs

4 layer kapton cable attached and wire bonded to Si-Module for I/O and power

Electric Multichip Module

E-MCM: Everything but the DEPFET

Electrically active prototype of a half ladder



Circuitry for DEPFET emulation

Long drain lines to DCD

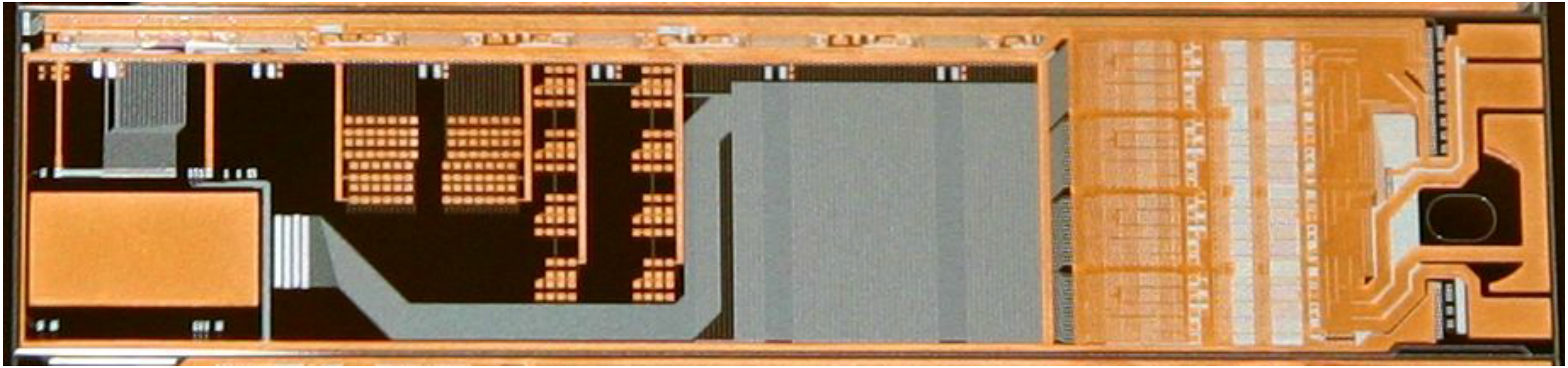
Capacitors for SW tests

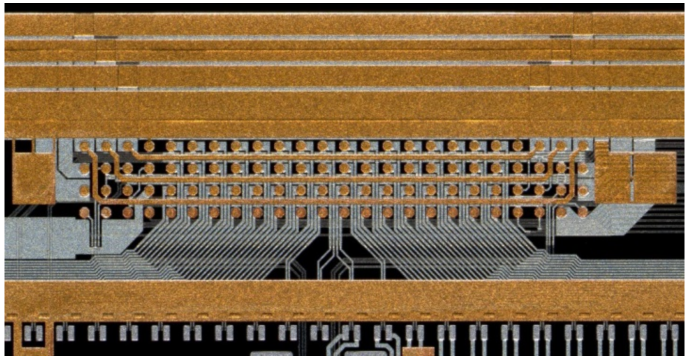
Metal process as close as possible to final: electrical information
Commissioning: Flipchip, passive and kapton attachment
Start preparing QA for production: needle probe card

Electric Multichip Module

E-MCM: Everything but the DEPFET

- Electrically active prototype of a half ladder





Detail of the Switcher landing area

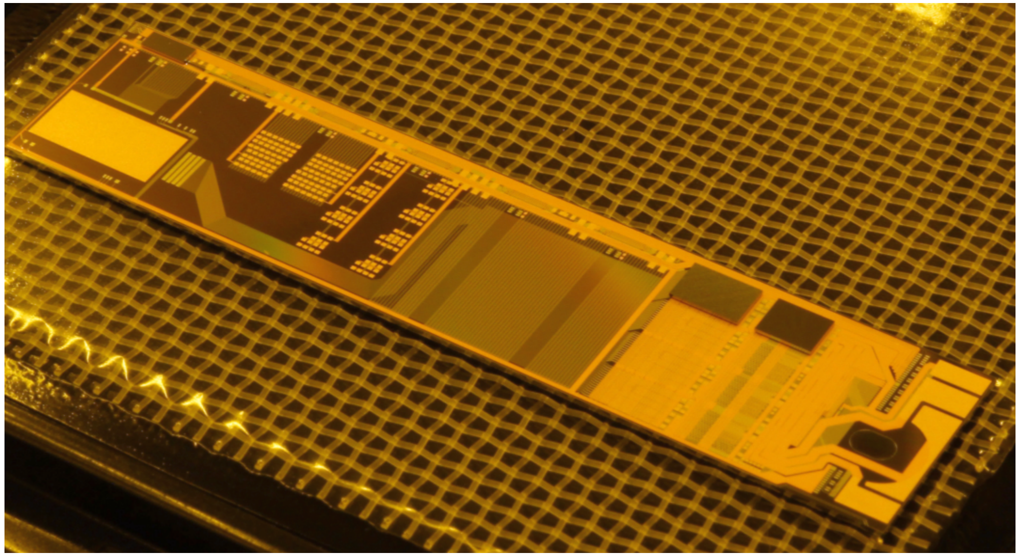
Electric multichip module

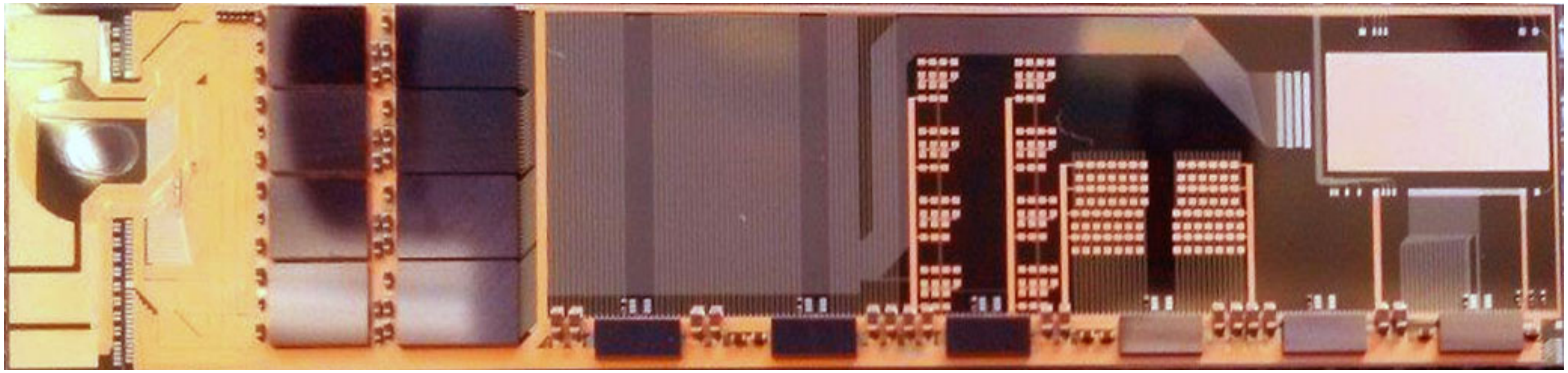
First module with real chips ready for first tests:

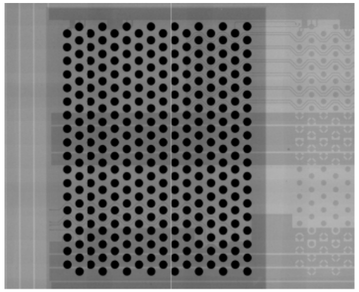
- 2 with one DCDB/DHP/SWB
- 1 fully populated device

FLipChip @ IZM Berlin

Passive placement @ Finetech/Berlin

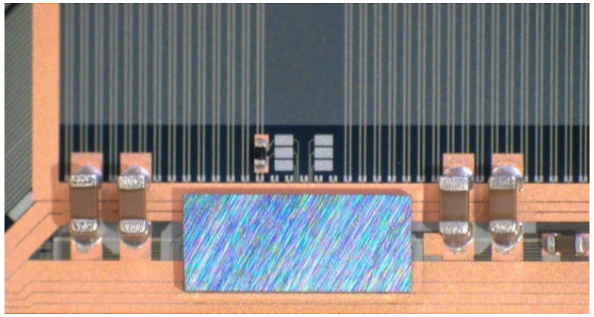






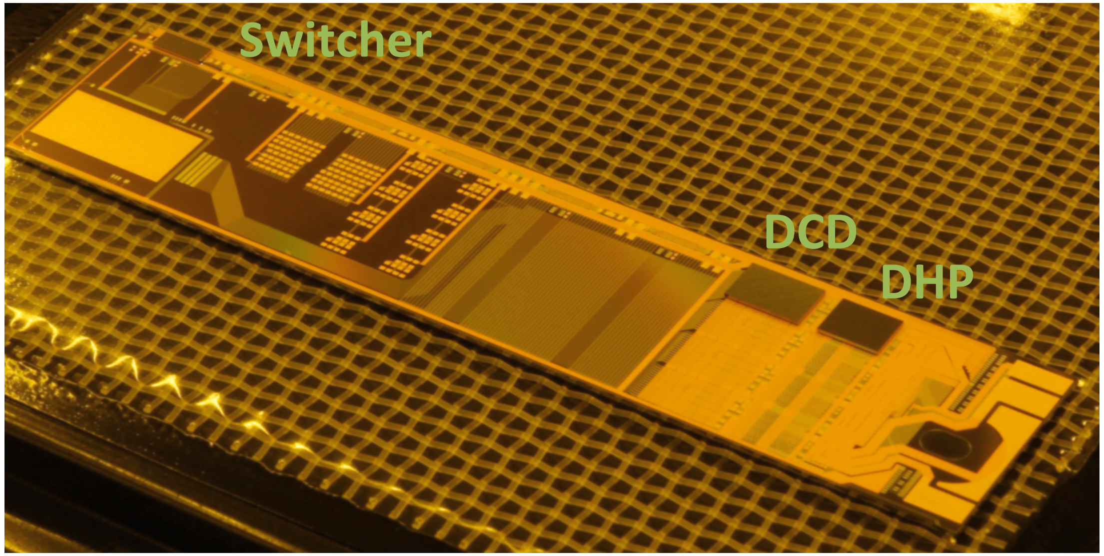
X-ray of bumps

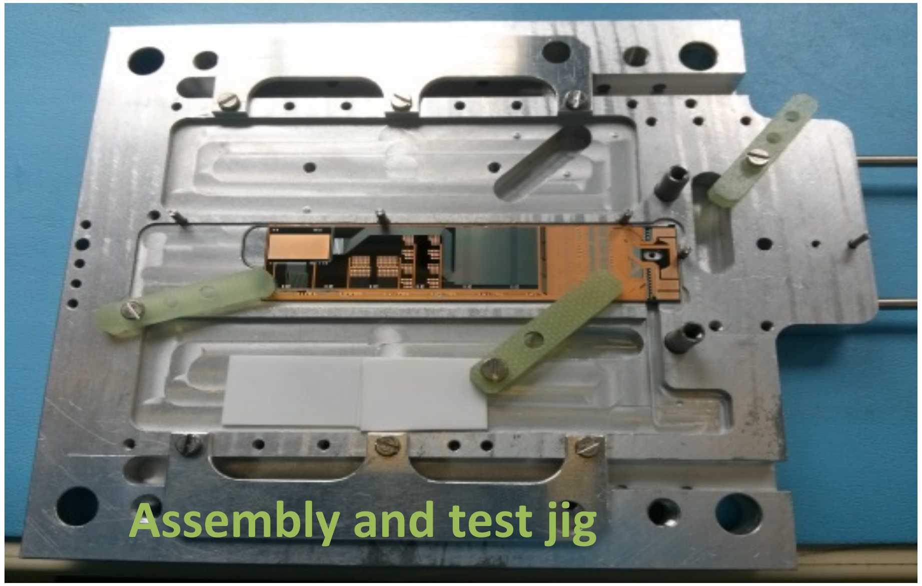
Assembly of passive components
(about 70 resistors and capacitors)



Electric multichip module

2 EMCM fully assembled and under test
Fully populated EMCM needs kapton to be attached





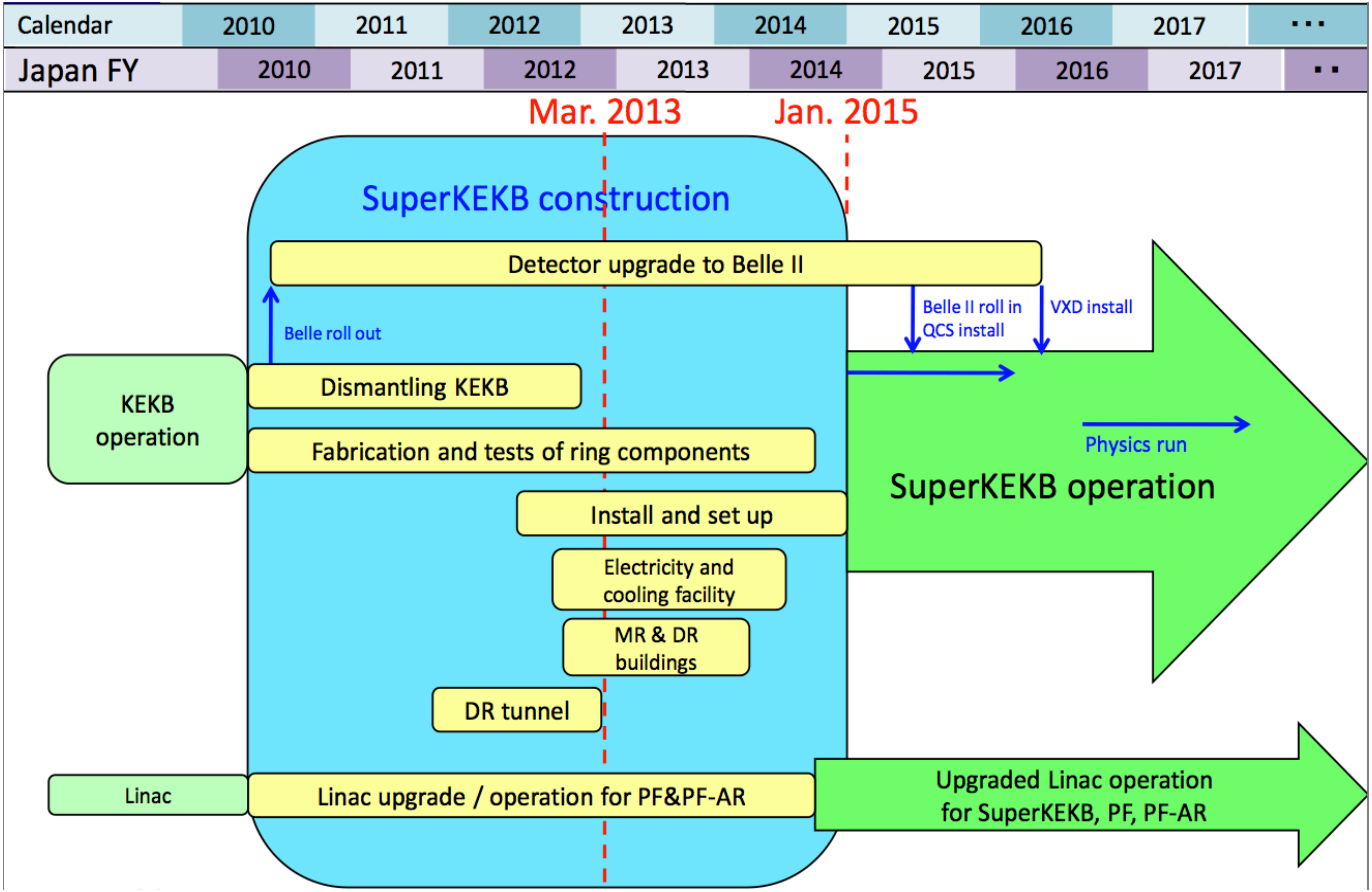
Conclusions

- ✓ SuperKEKB will provide a factor 40 higher luminosity than KEKB
- ✓ New, improved tracking+vertexing system needed
- ✓ Pixel detector will be based on the DEPFET technology and fits all the requirements
- ✓ Successful operation with small DEPFET matrices demonstrated in Lab. and beam tests.
- ✓ Engineering aspects (cooling, services) well under control
- ✓ EMCM will allow to test many aspects of the system in particular for production

DEPFET collaboration

- CNM/IFAE, Barcelona
- Charles University, Prague
- DESY Hamburg
- IFCA Santander
- IFIC Valencia
- IFJ PAN, Krakow
- IHEP, Beijing
- KEK-PF, Tsukuba
- LMU Munich
- TU Munich
- MPI Munich / HLL
- University of Barcelona
- University of Bonn
- University of Heidelberg
- University of Giessen
- University of Göttingen
- University of Karlsruhe

Belle II schedule



Calendar	2010	2011	2012	2013	2014	2015	2016	2017	···
Japan FY	2010	2011	2012	2013	2014	2015	2016	2017	··

Mar. 2013

Jan. 2015

SuperKEKB construction

Detector upgrade to Belle II

Belle roll out

Belle II roll in
QCS install

VXD install

KEKB
operation

Dismantling KEKB

Fabrication and tests of ring components

Install and set up

Electricity and
cooling facility

MR & DR
buildings

DR tunnel

Physics run

SuperKEKB operation

Linac

Linac upgrade / operation for PF&PF-AR

Upgraded Linac operation
for SuperKEKB, PF, PF-AR