Recent Results for 3D Pixel Integrated Circuits using Copper-Copper and Oxide-Oxide Bonding

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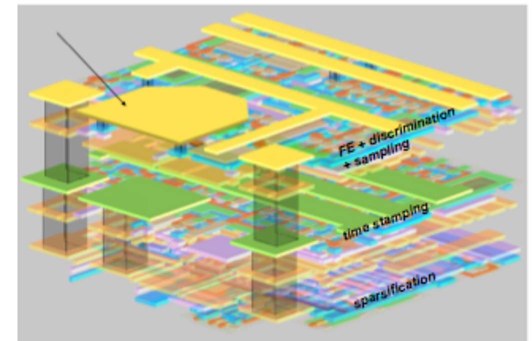
Introduction

- A 3D integrated circuit is comprised of 2 or more thinned IC layers that are bonded together and have numerous electrical connections between them by means of small vias or pads.
- The inspiration to develop 3D integrated circuits by Fermilab for HEP began a number of years ago. We thought that 3D could open the doors to new concepts and significant improvements for detector electronics.
  - Finer pitch pixels
  - Less mass
  - Higher localized "on detector" functionality
  - Bump bond alternative
  - Non dead space arrays

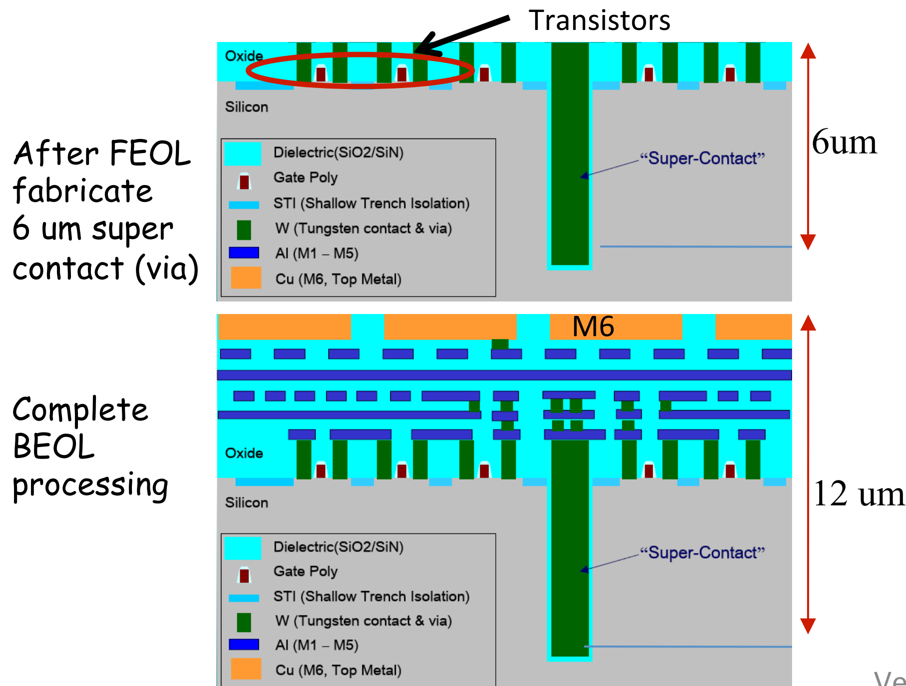


- Over the years we have explored 3D bonding of ICs with various vendors and technologies.
- The two technologies receiving the most attention have been copper-copper thermo-compression and oxide-oxide bonding with copper pads.
- This talk will start with a quick overview of the first attempts with copper-copper bonding for one circuit design, then move to describe the most recent results with copper-copper and oxide-oxide bonding for the same design.
  - In addition, will present results of chip to sensor chip bonding.

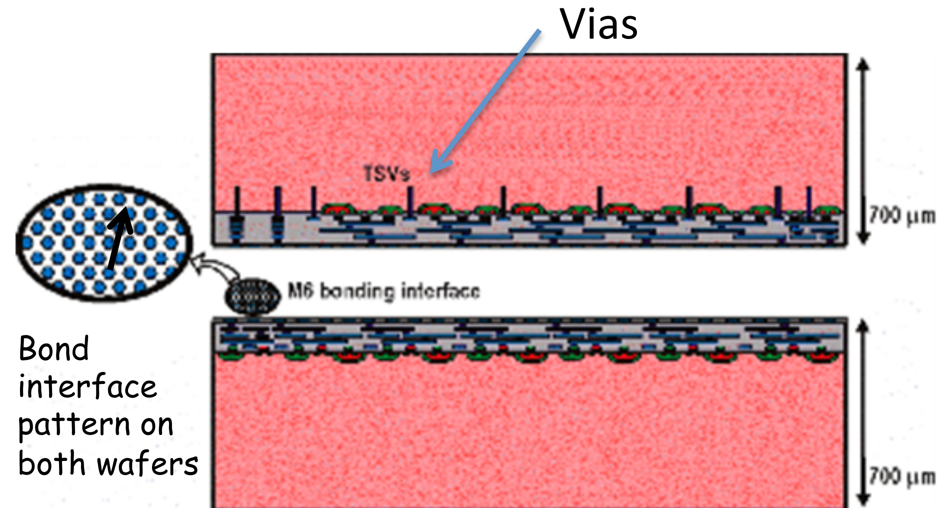
3D wafers Fabricated in 0.13 um CMOS Process at Global Foundries

- Access to Global foundry thru Tezzaron [1]
- After fabrication of transistors 1 um dia, 6 um deep, blind vias (super contact) inserted (via middle process).
- Super contact filled with tungsten at same time connections are made to transistors.
- BEOL, M1-M6 completed.
- M6 used to make pads for bonding.
- Very regular pattern of M6 copper bond pads is critical for good bonding.
- Copper bond pitch used is about 4 um
- In 2 tier assembly, the wafers are bonded face-to-face with vias pointing into the substrate as shown below.
- Vias may be present in both wafers

After FEOL fabricate 6 um super contact (via)



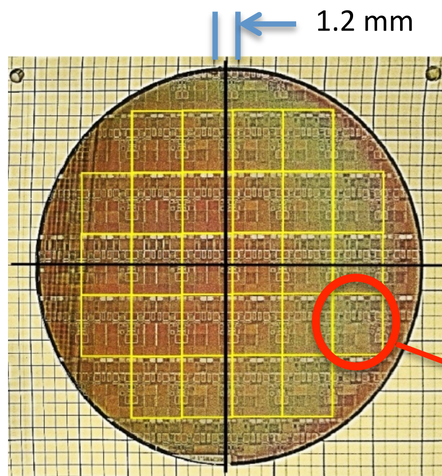
Complete BEOL processing



Bond interface pattern on both wafers

Numerous Problems Encountered

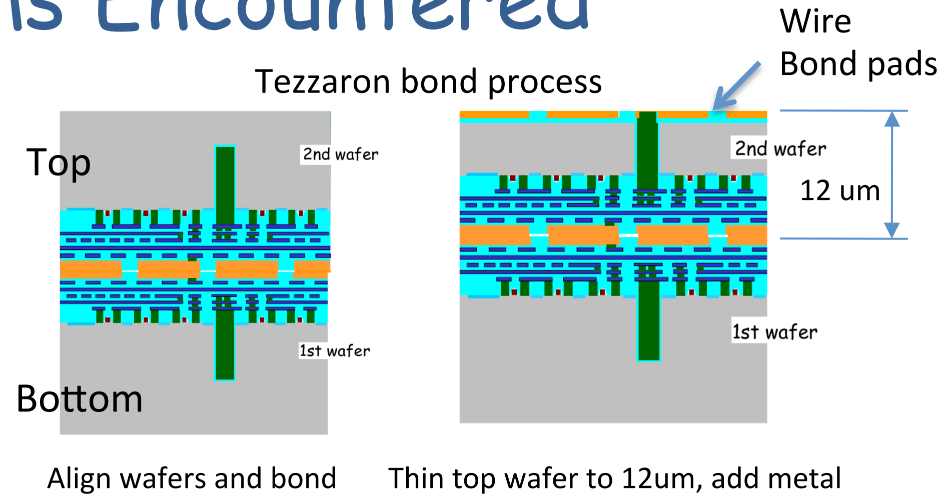
- 3D consortium submitted ten designs with 2 tiers for fabrication
- Design and submission problems [2]
- Fabrication problems
  – Full lot of wafers (30) lost due to improper frame placement (1.2 mm off center line)
- New lot re-fabricated



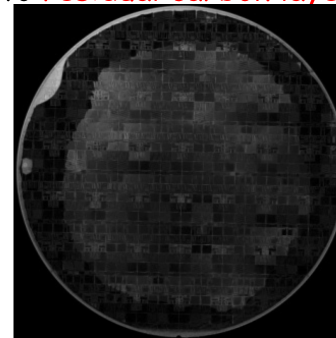
Frames not placed symmetrically about wafer center line – prohibits bonding due to bonder limitations.

TXL	TYL	TYR	TXR
AL	BL	BR	AR
CL	DL	DR	CR
EL	FL	FR	ER
GL	HL	HR	GR
IL	JL	JR	IR

- Bonding started on new lot using the Tezzaron Cu-Cu TC bond process
  – Prepare Cu bond pads for bonding
  – Align for face to face bonding
  – Cu-Cu thermo compression bond
  – Thin one side to expose vias
  – Add back metalization for wire bond pads

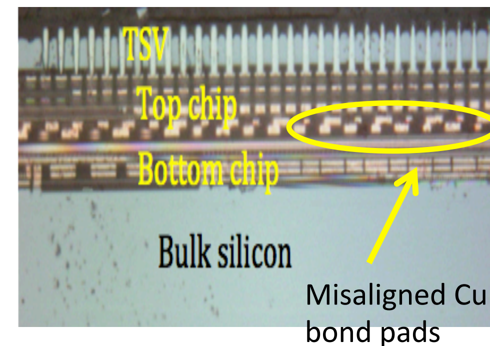


First 6 wafers bonded at EVG Tempe, due to poor bonding due to residual carbon layer



Acoustic image of wafer (light sections show poor bonds).Poor bonding may be due to lack of forming gas in Tempe bonder.

Second 6 wafers bonded at EVG Tempe lost due to misalignment

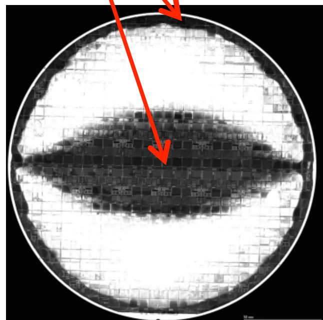


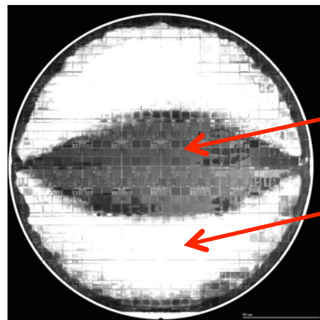
Decision made to bond remaining wafers at EVG Austria due to different wafer alignment process and use of forming gas.

Other Wafer Bonding Results

- Remaining 16 wafers sent to EVG Austria for Cu-Cu bonding.
  - First 8 wafers would not bond
    - Tried many bond pressures with forming gas.
    - Attributed to larger copper grain boundaries which have been found to develop over time. (Documented by Tezzaron). Wafers were "old".
  - Next 8 wafers sent to Ziptronix for bond pad processing and then sent back to Austria
    - 1 wafer pair broke in the EVG bonder at high pressure
    - 3 remaining wafer pairs exhibited poor bonding due to trapped gas.
      - Cu bond pads insufficiently exposed during etch process.
      - Oxide bond occurred around rim of wafer trapping gas.

Relatively good bonding





Poor

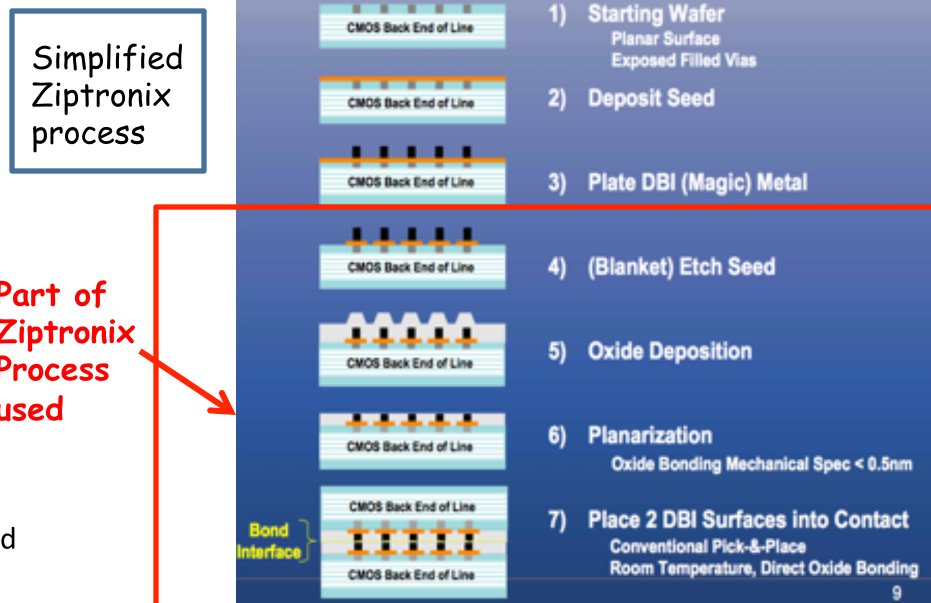
Bad

Bonded wafer acoustic images, white areas are bad bonding

- Decided to try oxide bonding wafers using Ziptronix DBI (Direct Bond Interface) process. [3]
  - However, no unused wafers left.
  - Ziptonix separated one pair of poorly bonded Tezzaron wafers from EVG in Tempe
  - Wafers were reprocessed for oxide bonding and partially bonded at Ziptronix.

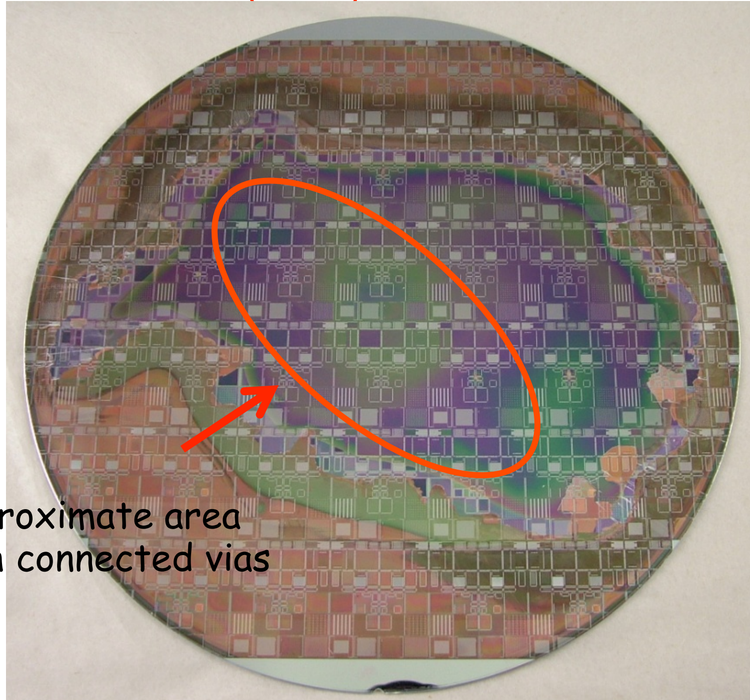
Simplified Ziptronix process

Part of Ziptronix Process used



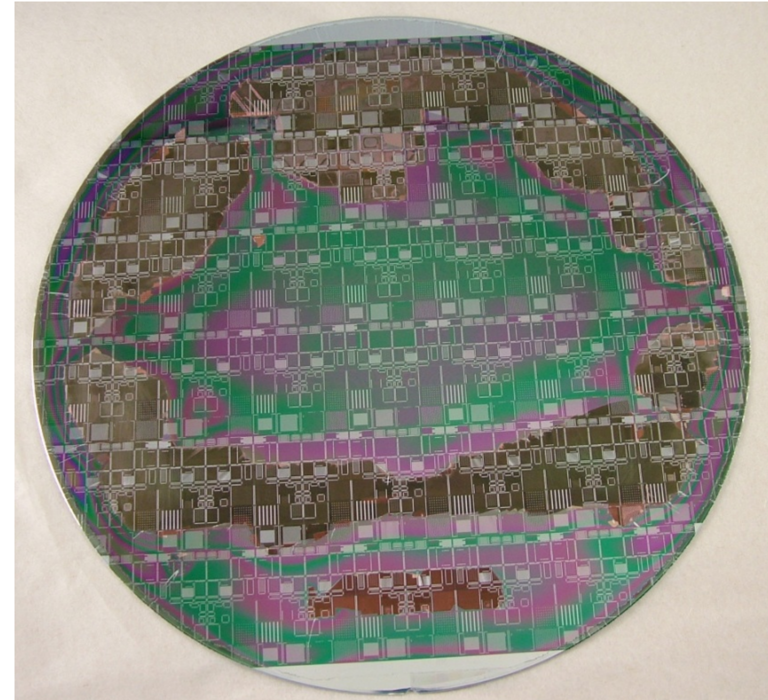
Only 2 Wafers from Initial Lot of 30 Wafers Good Enough to be Diced for Test Parts

- One Ziptronix bonded wafer
  - Used refurbished Tezzaron bonded wafers as a test for DBI process
  - Limited number of useable parts for testing
  - Parts distributed to 3D consortium
  - 3 Fermilab parts
    - VIP2b (not tested yet)
    - VICTR (partially tested)
    - VIPIC (tested)



Ziptronix bonded wafer – non-uniformity of Si CMP caused by non-uniform bonded area resulted in right side TSVs being buried and not connected.

- One Tezzaron bonded wafer
  - Eye pattern of useable parts (in center)
  - Limited number of useable parts for testing
  - Parts distributed to 3D consortium
  - 3 Fermilab parts
    - VIP2b (not tested yet)
    - VICTR (partially tested)
    - VIPIC (tested)

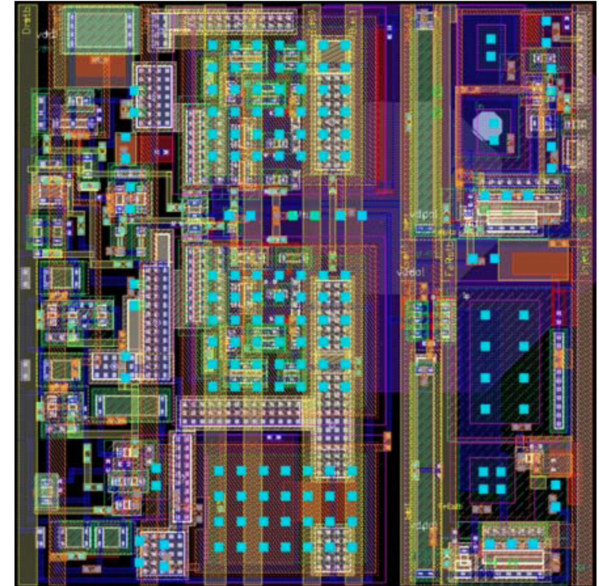


Tezzaron bonded wafer – TSVs appear to connected across the entire bonded area (eye pattern in center).

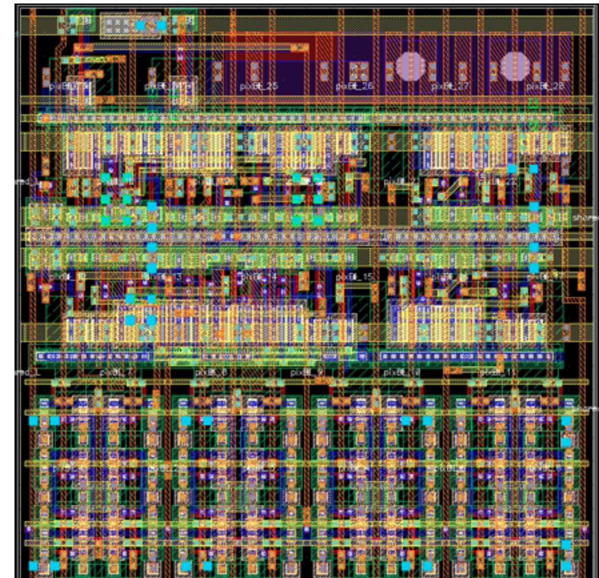
VIP2b (Vertically Integrated Pixel)

- VIP2b-Third version of full function 3D chip designed for ILC pixel detector
- 3D technologies used to reduce mass and increase functionality in each pixel
- Main Features
  - Readout between ILC bunches
  - High speed data sparsification
  - Dead timeless read out
  - Test input for every pixel
  - 192 x 192 array with 24 um pixels
  - Separate analog and digital tiers
  - 8 bit time stamping for 3.9 us time resolution
  - Analog output for digitization
- Chip waiting 2 years for testing

Analog tier

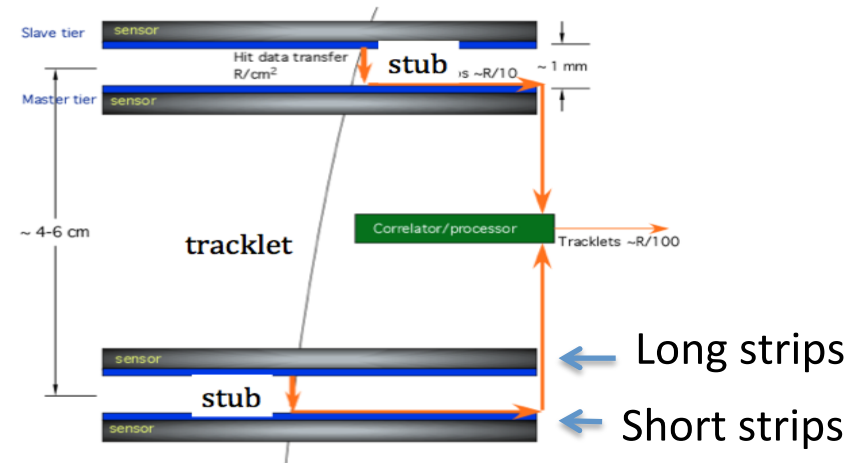


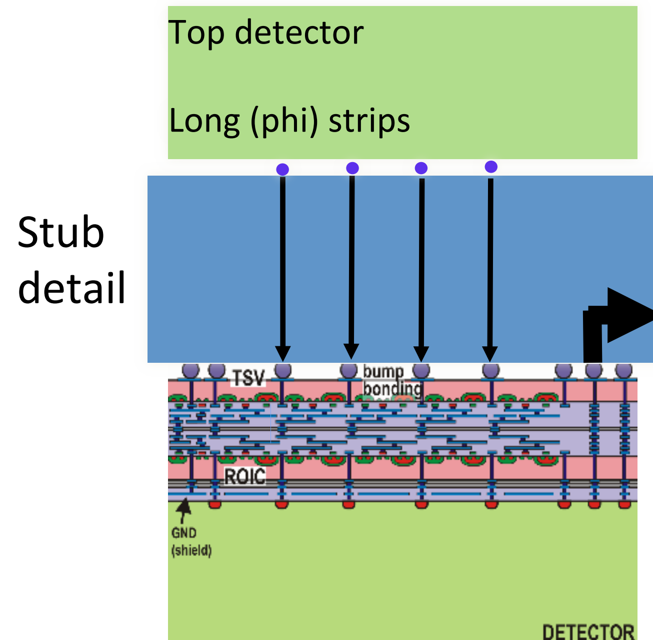
Digital tier



VICTR (Vertically Integrated CMS Tracker)

- CMS upgrade requires a L1 trigger based on fully reconstructed tracks at Level 1 (6us) for HL-LHC in the mid-2020's
- Approach taken based on assemblies of sensors and 3D readout chips that form track stubs and tracklets looking for track curvature
- Stubs found locally from sensor pairs
  - A top detector comprised of long strips for phi
  - A 1 mm interposer
  - The VICTR ASIC (2 tiers)
  - A bottom detector comprised of short strips for z
- Some test results available [4]



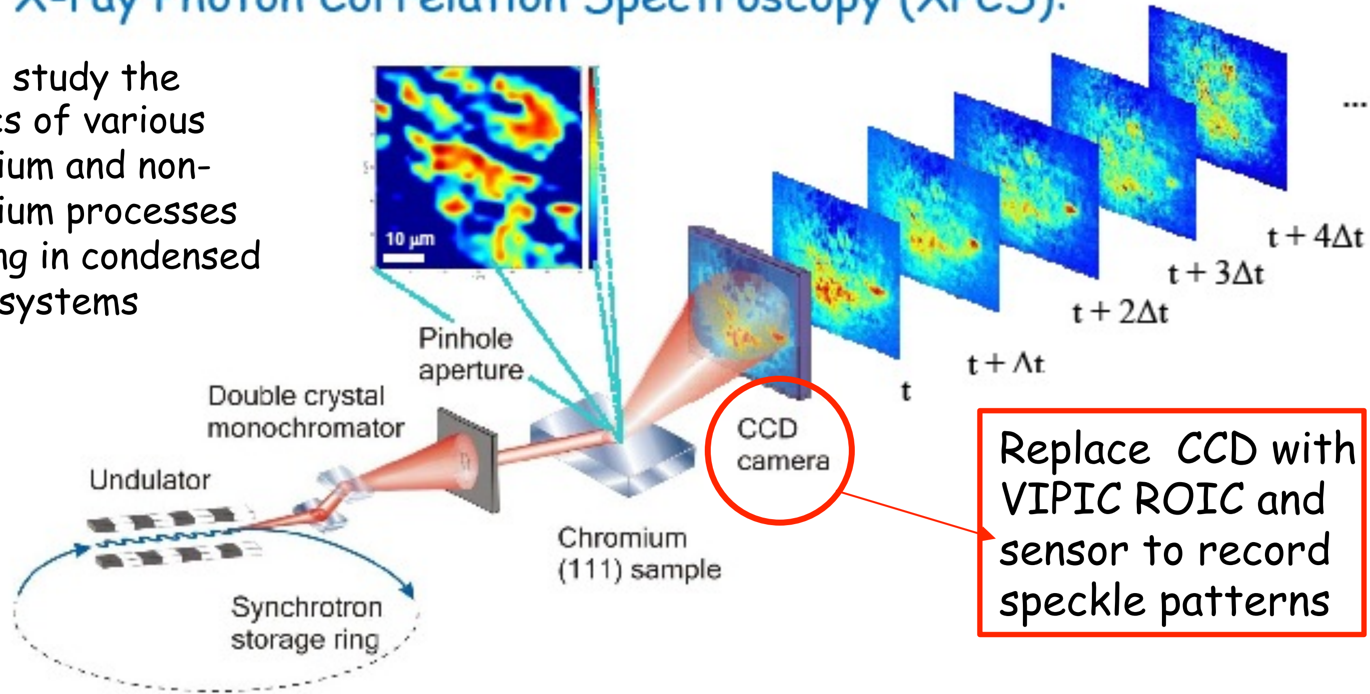


VIPIC

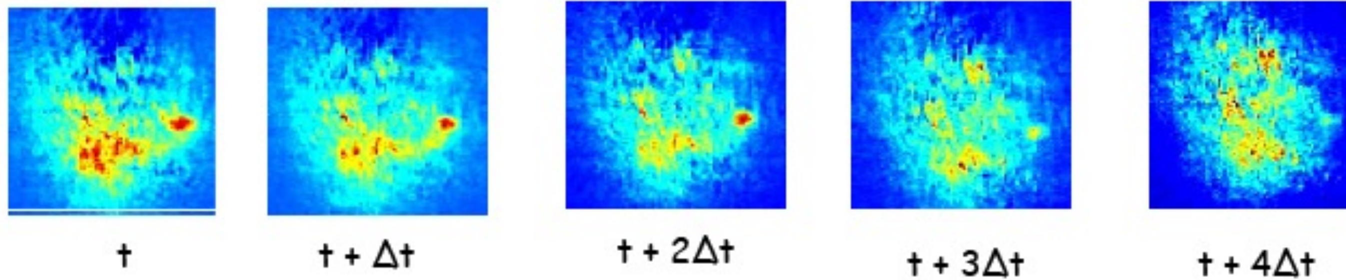
- Vertically Integrated Photon Imaging Chip
- Goal is to provide a small-pixel detector for XPCS (X-ray Photon Correlation Spectroscopy) which will reduce the range of correlation times downward by a factor of 1000 to the microsecond scale, and reduce data traffic to a manageable level
- The first prototype designed for 10us time slices, the ultimate goal is ~100ns.
- VIPIC collaboration members
  - Grzegorz Deptuch, Marcel Trimpl, Ron Lipton, Raymond Yarema
    - *Fermilab*
  - Paweł Gryboś, Piotr Kmon, Piotr Maj, Robert Szczygieł
    - *AGH University of Science and Technology, Krakow, Poland*
  - P. Siddons, Abdul Rumaiz
    - *BNL*
  - Zhi Yong (Arthur) Li
    - *NJIT, resident at BNL.*
  - Gabriella Carini,
    - *SLAC (ex-BNL)*

X-ray Photon Correlation Spectroscopy (XPCS):

Used to study the dynamics of various equilibrium and non-equilibrium processes occurring in condensed matter systems



Replace CCD with VIPIC ROIC and sensor to record speckle patterns



Speckle pattern changes with time

O. G. Shpyrko et al., *Nature* **447**, 68 (2007)

Idea is to output time stamped information with Δt=10 us for long exposure times and low occupancy <10 ph/mm^2/10us

VIPIC (Vertically Integrated Photon Imaging Chip)

- The VIPIC is designed to quickly count the number of hits in every pixel and read out the # of hits, and addresses in a dead timeless manner.
- To achieve the desired speed requires a sparsified digital readout, where only the pixels which have registered a hit are read out.
- To implement the sparsified readout requires a digital design which would not fit in the desired pixel size of 80 x 80 um along with the analog circuitry.
- Thus design was split into analog and digital design layers of equal area to meet the pixel size requirement.
- This required a large number (25) of signals to be passed between the analog and digital section of every pixel (over 100,000/chip)
- Chip operates in 2 modes
  - Timed Readout of # of hits and addresses at low occupancy (~ 10 photons/cm^2/10 usec)
  - Imaging – alternating 5 bit counters read out # of hits in each time slot without addresses (less data output without addresses)

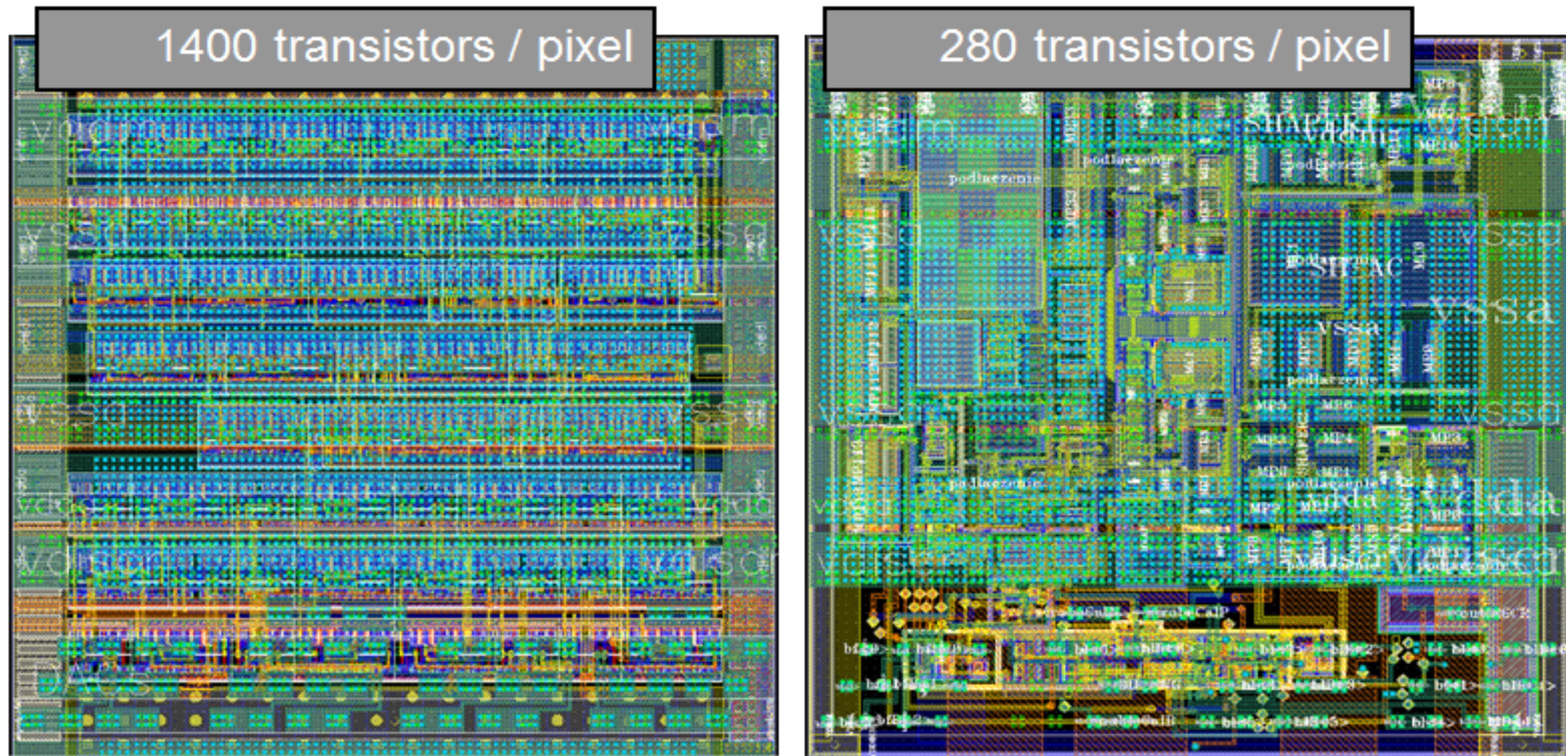
Specification Summary

detector

- 64×64 pixels, pixel area: 80×80 μm
- Separate analog (280 transistors) and digital tiers (1400 transistors)
- Active area: 5120×5120 μm, chip: 6.3×5.5 mm
- Power consumption 25 uW/analog pixel
- CSA: noise ENC < 150 e^-, t_p < 250 ns,
- Gain 115 mV/ 8 keV, C_{feed}=8fF
- Single threshold for discriminator
- Trim DAC/pixel for offset corrections.
- 7 bits discriminator threshold trim, 3 bits CSA feedback adjust
- Permanent *pixel set* and permanent *pixel reset* bit per pixel
- Test charge injection circuitry, C_{inj}=1.7 fF
- Single ended or differential configuration of the front-end

- a) sparsified binary data, time slicing mode,
- b) imaging binary readout mode (5 bit signal depth)
- Dead-timeless and trigger-less operation in both readout modes
- Sparsification using priority encoder based on fast sparsification circuitry
- 16 parallel serial LVDS output lines (16 groups of 4×64 pixels)
- Two 5 bit counters per pixel for recording multiple hits per time frame (useable in the imaging mode)
- Frame readout at 100 MHz serial readout clock
  - 160 ns / hit pixel in sparsified time slicing mode
  - 50×10^3 frame/s in imaging mode (5 bit counting)

3D-IC: Fermilab designs – VIPIC [5]



Digital part of pixel | **Pixel 80x80 μm^2** | **Analog part of pixel**

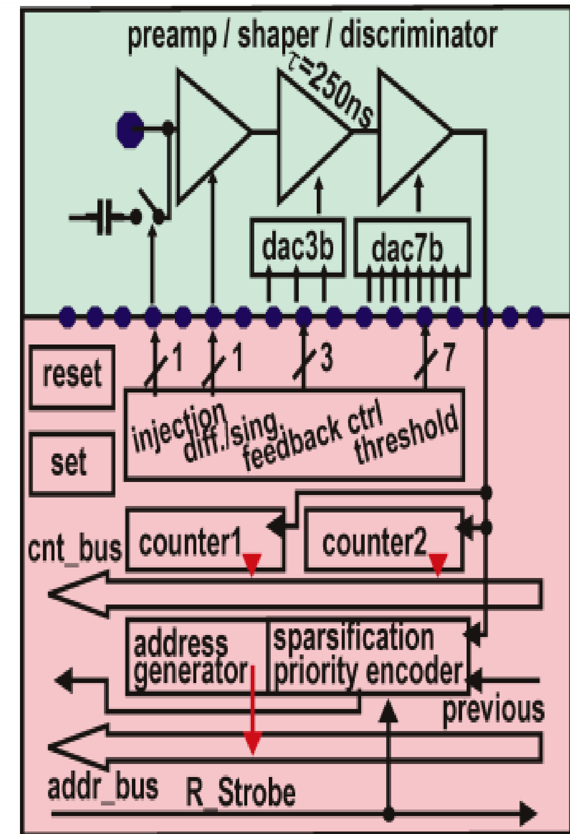
- 64 × 64 array of 80 mm^2; shaping time τ_p=250 ns, power ~25 μW / analog pixel, noise <150 e^- ENC
- Two dead-time-less modes of operation (64 × 64 matrix / in 16 sub-matrices of 4 × 64 pixels):
  1) timed readout of hits acquired at low occupancy (address and hit count) σ_t=10μs
  2) imaging – counting of events
- Sparsified readout with priority encoder circuit (hit pixel address readout only)

17 DOE Detector R&D review July 24-26, 2012

VIPIC Block Diagram (4096 Pixels)

16 Serial Output Lines (LVDS)

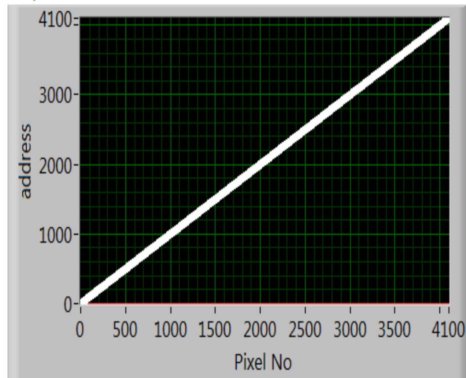
256 pixels/output



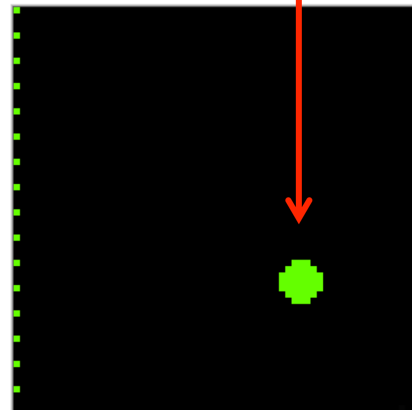
Single pixel

Test Results (Without Sensor) [6]

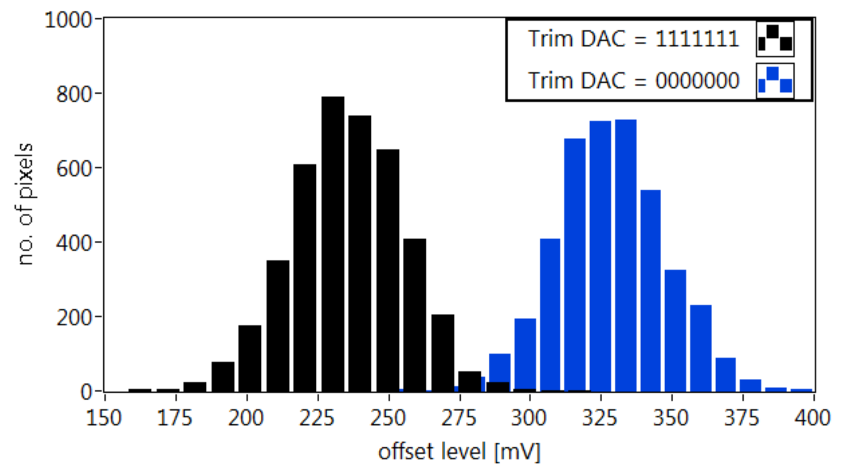
- Bonded 5 chips after visual inspection
  - 1 Tezzaron bonded chip is working
  - 2 Ziptronix bonded chips are working
- Testing confirms operation in both modes
  - Configuration shift registers (up to 49152 bits long) are working.
  - Shifted hit 1's to all cells with cal strobe and read out every address in normal readout mode in sequential order.
  - Found address encoder generating proper addresses
  - Thinned analog tier operation closely matches simulated performance. (Power and noise)
  - Reset (kill) all pixels and set pixels in region of interest, found appropriate sparsified addresses
  - Reduced threshold to get noise hits and found pixel counters reading out non-zero values. Chip fully working from input to output
  - Outputs fully functional
    - 16 serializers
    - 16level converters
    - 16 LVDS buffers
  - Changed 7 bit threshold DAC to 2 end values and found appropriate shift in threshold distributions (DAC range wide enough to correct for offsets)
- All 25 signal connections between top and bottom tiers appear to be active



Proper sequential address read out when 1's shifted into all cells (using normal read out mode)



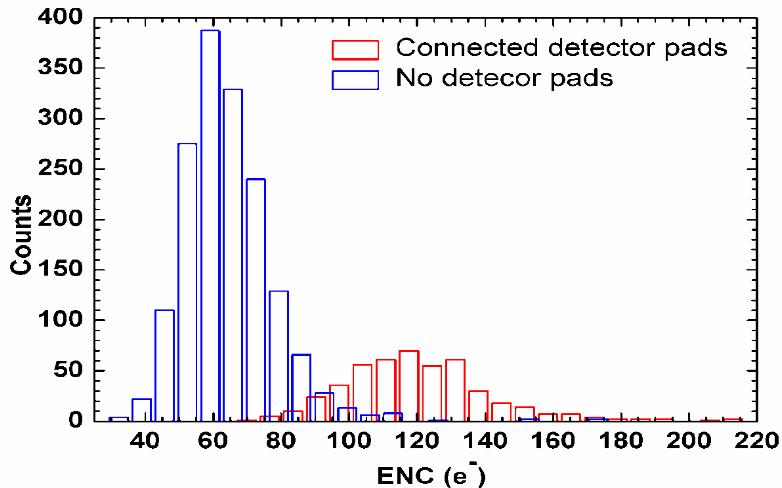
Normal array read out with all pixels killed except small area in green (sparsification works)

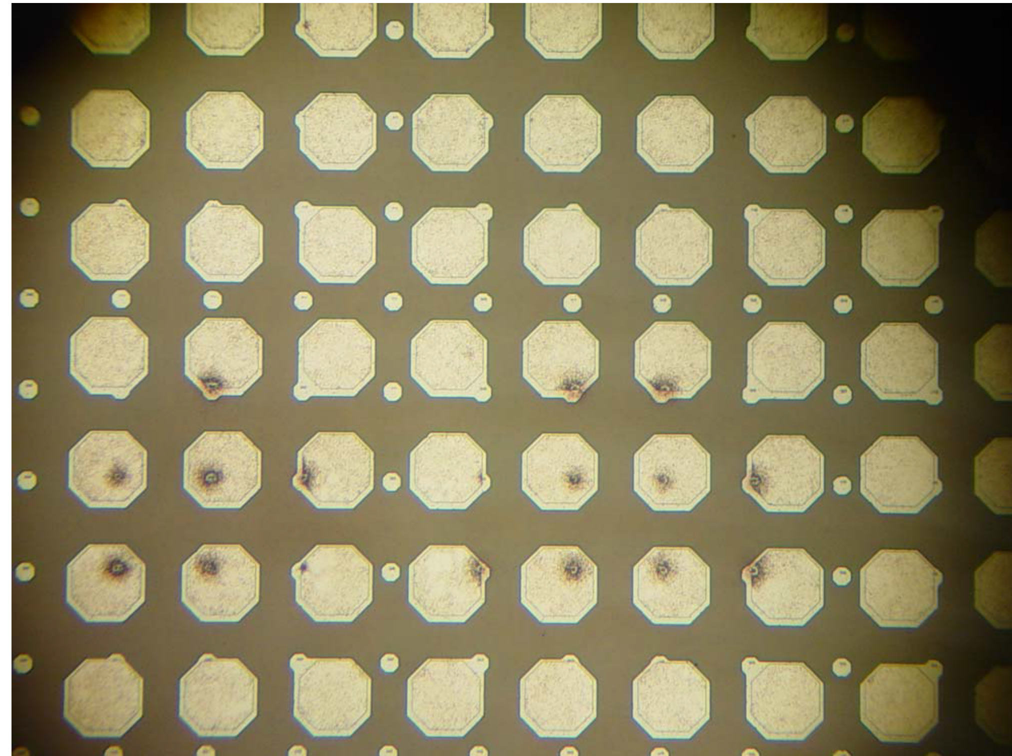


Noise hits for all pixels at extreme end of DAC settings

Measured VIPIC Noise Performance

- Specification was for an ENC of 150 electrons, so that a minimum number of false hits would be generated with thresholds set for 8keV photons.

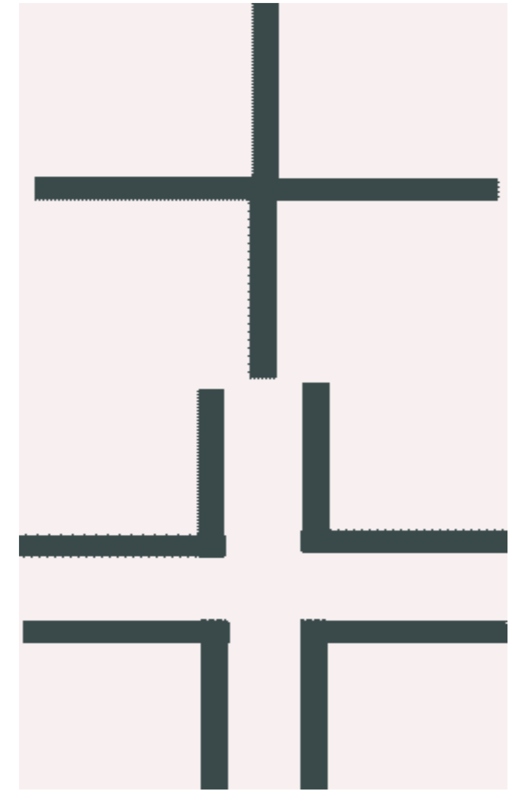


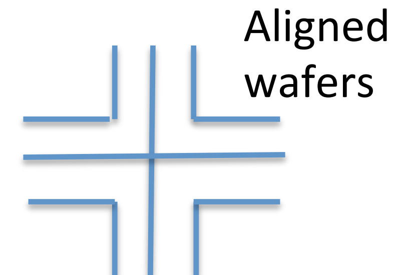


Al pads on VIPIC for connection to 100um pitch pixel sensor. Note every 5th input is skipped

Fabrication history of useable wafers

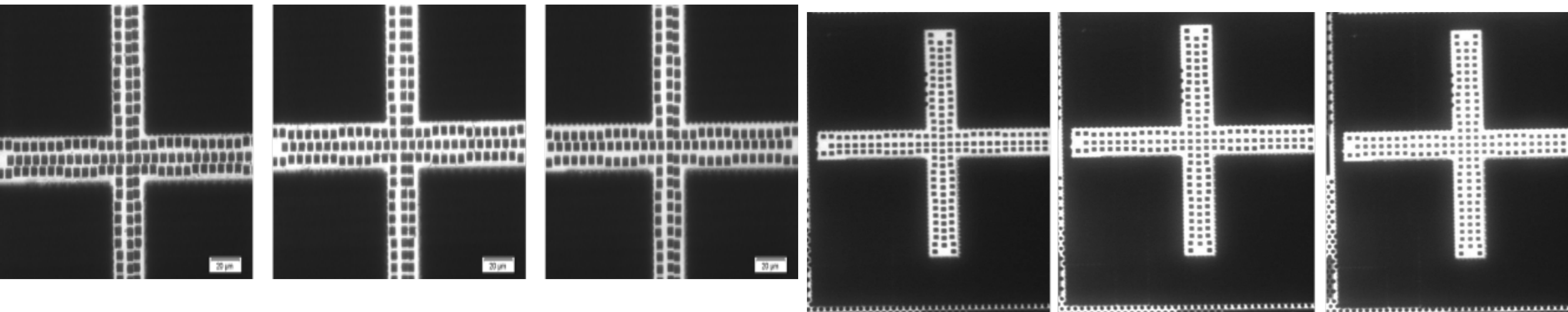
- Numerous diagnostic tools such as acoustic imaging, focused ion beam cross sectioning, as well as simple visual inspection have been used to investigate the 3D bonding problems that have been encountered.
- The tool which we now find the most useful is examination of the wafer alignment keys with infrared after bonding.
- The alignment keys on our wafers are comprised of 3.8 um squares with a 6um pitch that are arranged in two distinct cross patterns as shown on the right.
- One cross is on the top wafer and the other is on the bottom wafer.
- These alignment keys are located in several positions on each wafer (e.g. left, middle, right).
- It is important to note that our copper bond interface is comprised of 2.7 um dots arranged in a hex pattern on a 4 um pitch which means that alignment between wafers should be better than 1 um across the wafer to avoid bonding problems





Two Diced Wafers from Original Wafer Lot of 30

- The two wafers shown in slide 6 were the best bonded and aligned wafers from the original lot of 30 wafers. All other wafers showed misalignment >> 1um and/or other problems.
- These wafers received 6/12 and dice used for previous results
- The alignment keys for these two wafers are shown below.
- In general the DBI/Cu bonded wafers were better aligned and provided more stable behavior over time.
- These are the wafers that yielded the the first useable devices



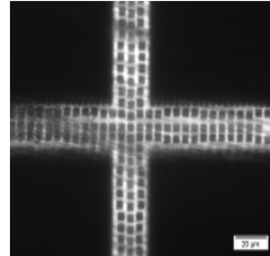
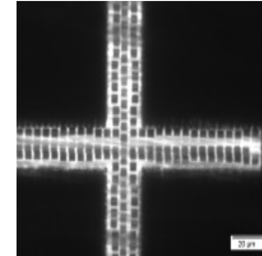
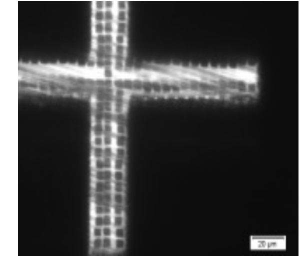
Cu-Cu TC : left, middle, and right keys DBI /Cu: left, middle, and right keys

Results from New 18 Wafer Recovery Lot

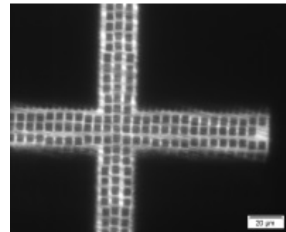
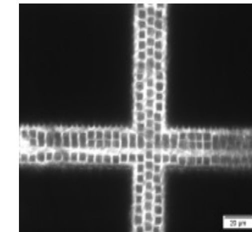
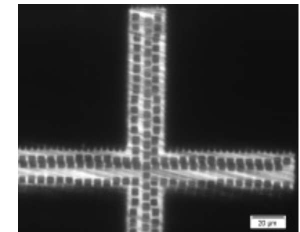
- A lot of 18 new wafers was fabricated to replace failed assemblies in earlier production
- 2 Cu-Cu TC bonded pairs received 3/13
- 2 more Cu-Cu TC bonded pairs received 6/13
- All wafers appeared visually good
- Initial tests on Fermilab diced chips from one wafer found opens and shorts
- Some wafers exhibit some misalignment greater than allowed in some areas, however, alignment is acceptable in most areas.
- Two Cu-Cu wafers appear good enough wafer bonding to sensors and one for harvesting diced chips.

Alignment Keys for Cu-Cu Bonded Wafers

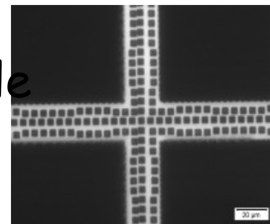
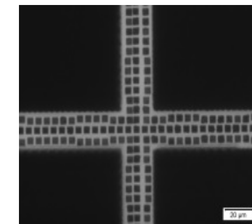
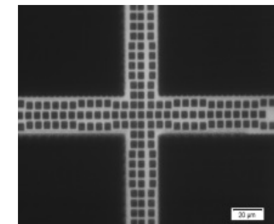
Wafer 1 – worst alignment

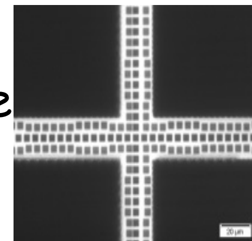
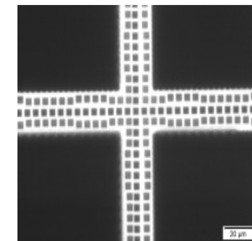
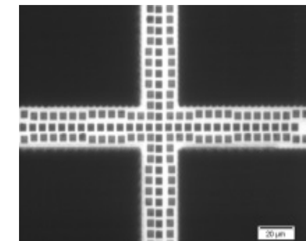
Wafer 2 – Poor alignment

Wafer 3 – should be acceptable
Misalignment is , ~1 um

Wafer 4 – good, should provide acceptable die

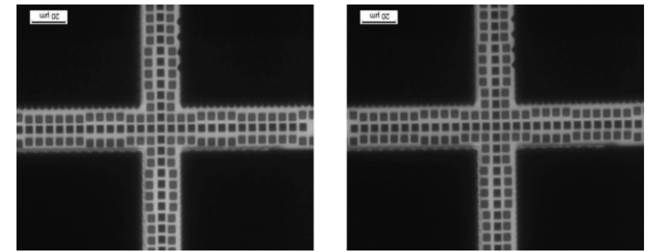




Left Middle Right

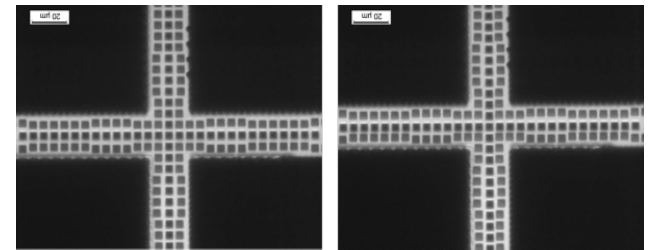
Alignment Keys for DBI/Cu bonded Wafers

- Bonded wafers 5,6,7,8 received June/July 2013
- Wafer 6 diced, ready for delivery to consortium
  - Several VIPIC tested
  - High yield
- Wafers 5,7,8 to be bonded to sensors from BNL
- No more wafers in the queue.

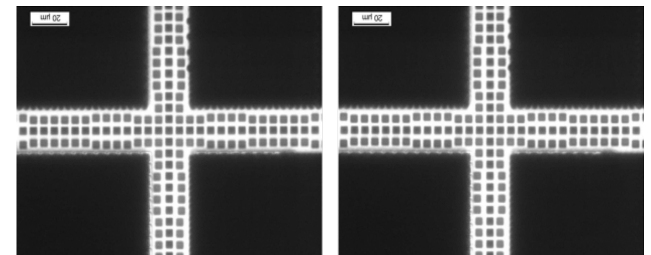
Wafer 5



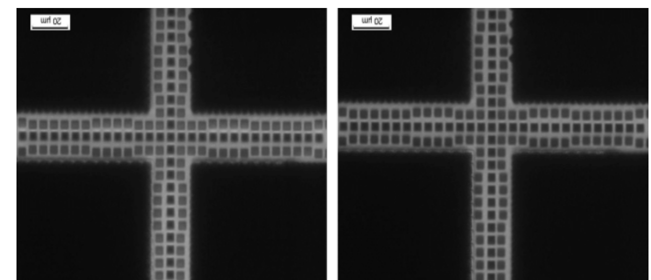
Wafer 6



Wafer 7



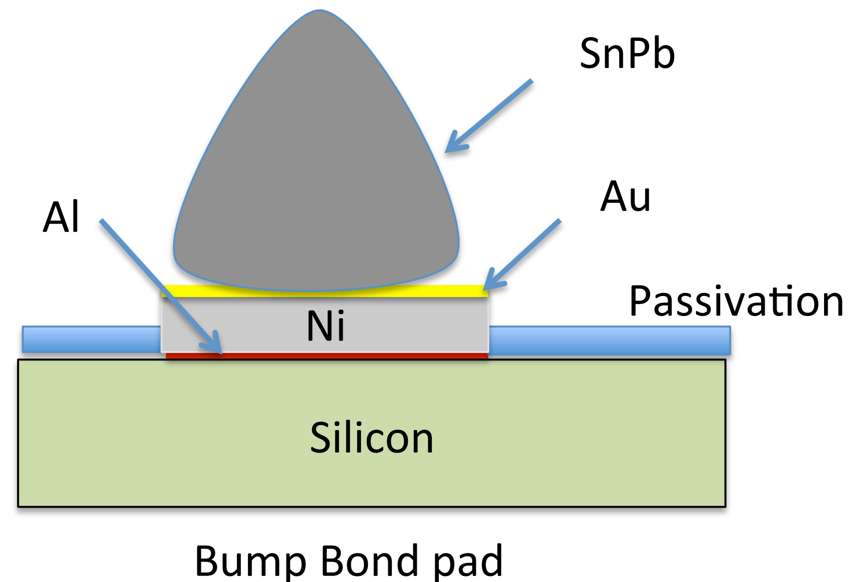
Wafer 8



Left Right

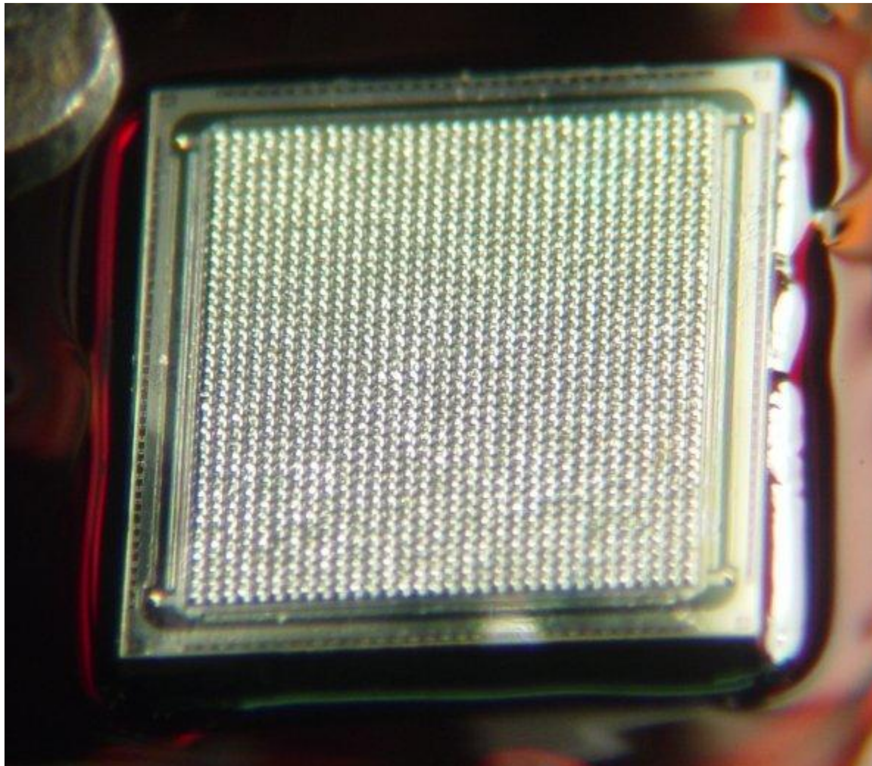
Bonding sensor to VIPIC

- Initially, die to die bump bonding used to connect wafer 6 die to sensor. [7]
- Sensor die preparation by CVInc
  - Add solderable UBM comprised of Ni and Au to AL pads
  - Adequate AL on pad is essential
  - Add 75 um high eutectic SnPb bumps (100% yield)
  - Pads on VIPIC are 60 um dia octagonal
  - Pads on sensor are 60 um dia round
- After attaching sensor to VIPIC
  - Bumps are 45-50 um high
  - Underfill added between sensor and VIPIC for mechanical strength

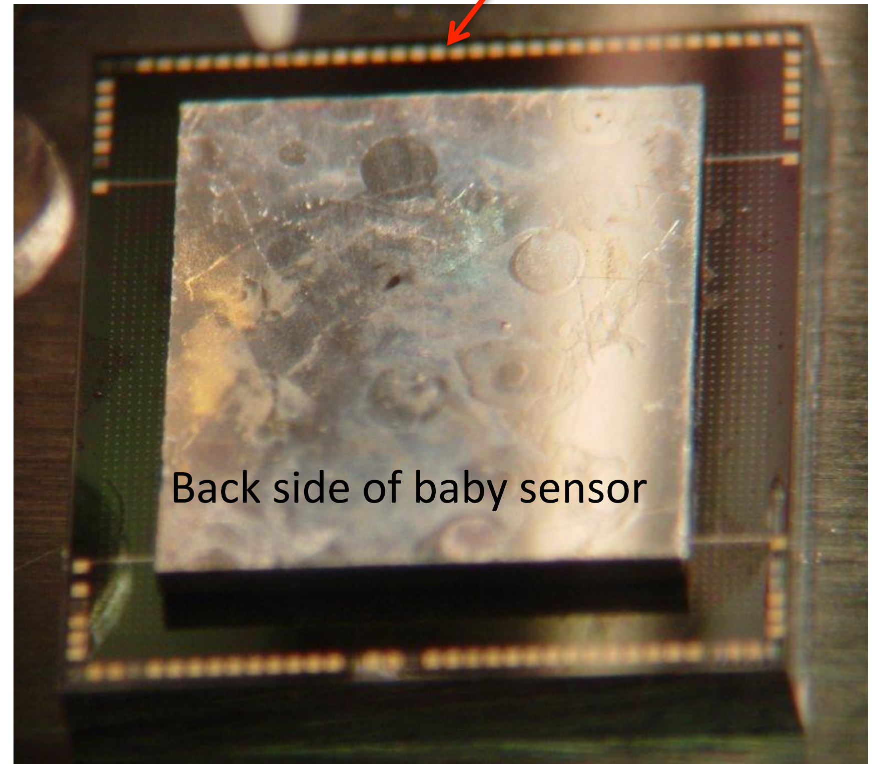


Bump bonding

500 um thick sensor



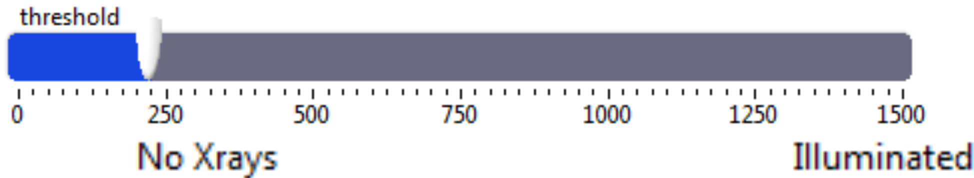
VIPIC wire bond pads



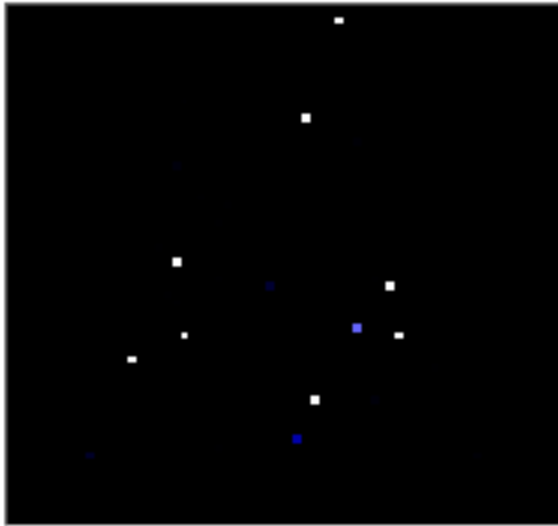
- 100 um pitch Hamamatsu pixel baby-sensor with Sn-Pb bumps deposited using a deposition technique on a single die with ENIG UBM on Al substrate pads by CVInc.

- VIPIC1 with a flip-chip bonded sensor; underfill used to strengthen the structure.

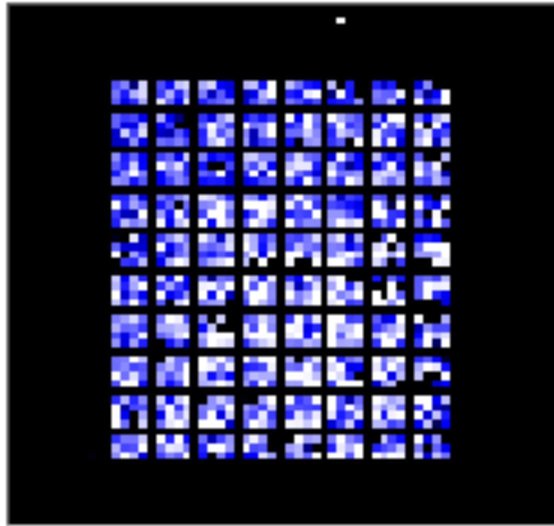
X-rays seen with the 3D VIPIC chip bonded to a 32x38 pixel sensor



No Xrays



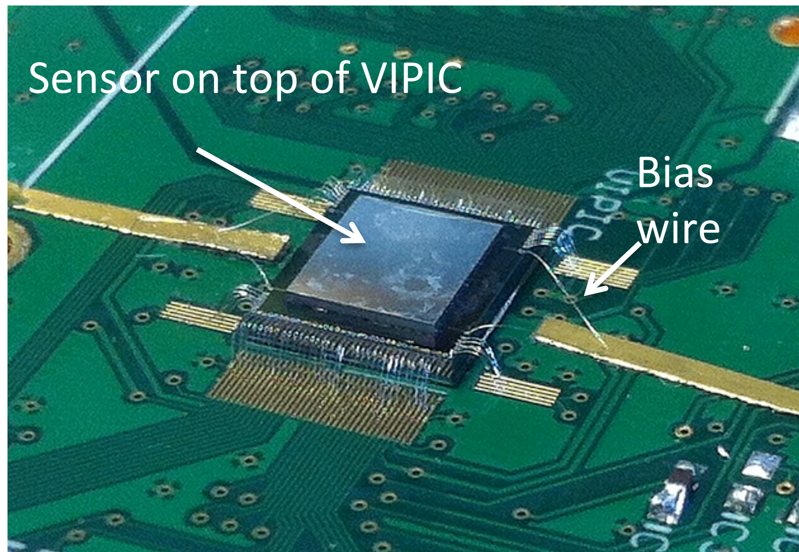
Illuminated



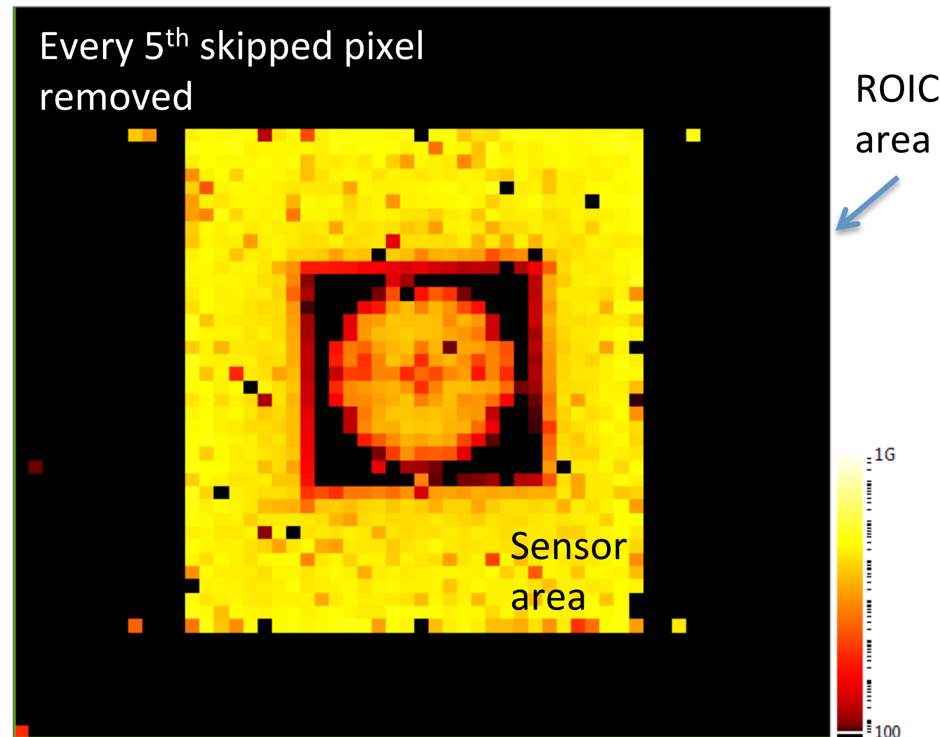
Threshold ~40 mv (200 ADC counts) causes noise hits to disappear (left plot). With source, X-rays are visible in right plot. If threshold raised to ~240 mV (1200 counts) no more hits visible; gain estimation ~40uV/e- (22keV -> 6100e/h)

- VIPIC1 – bonded to 32x38 pixel baby sensor
- VIPIC1-80um pitch Sensor-100um pitch
- Every 5th channel skipped because of pixel pitch mismatch
- ^{109}Cd 22keV source
- Sensor not biased

3D VIPIC - Results with biased Sensor



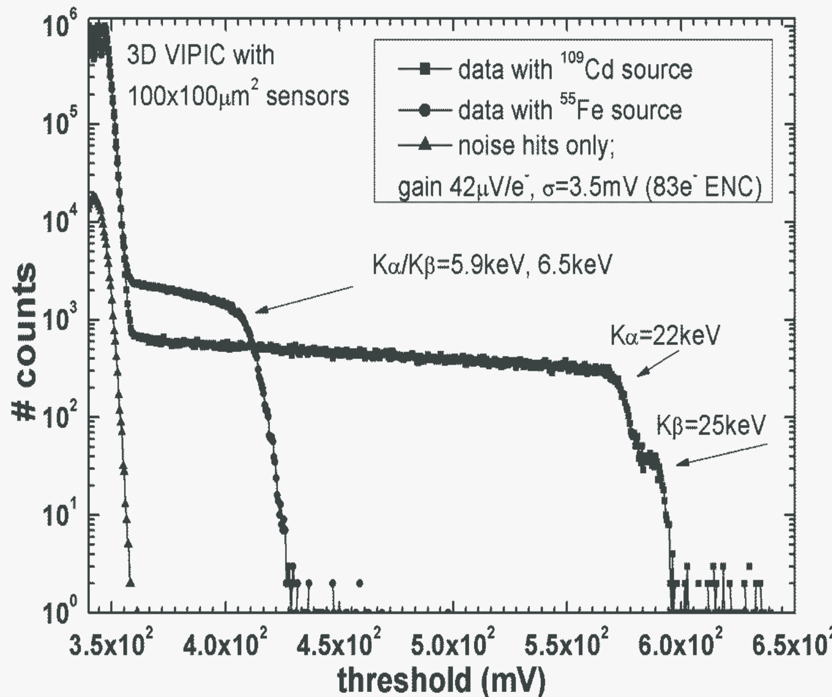
- Detector biased at 120V
- Detector tested using 2 sources ^{109}Cd 22keV and ^{55}Fe 5.9keV (mask not shown in above photo)



Transmission radiogram of a small W mask (2.5x2.5 mm^2) put on top of the sensor; back-side illumination of the fully depleted sensor using ^{55}Fe source, all signals integrated above noise,(mask has features smaller than the sensor pitch)

Full sparsified readout from all 16 groups of 4x64 pixels used in the acquisition and readout

Estimation of gain and noise



Threshold scans performed with fine 0.5 mV step resolution on fully depleted sensor

.

Full sparsified readout using 50MHz clock with data serialization from every group

- Selected results from a single pixel from a run in which a flat field illumination was used with:
  - ^{109}Cd 22keV (1mCi)
  - ^{55}Fe 5.9keV (10mCi)
  - Reference data without source

Fe photon -> 1600 e/ph

Gain = (420-350)mv/ph*1ph/1600 e = 43 uv/e

Noise = 3.5mv rms *1e/43uV = 83 e rms

VIPIC designed for 8KeV photons

Response is approximately linear up to 18 KeV

Readout speed performance

- The sparsified read out speed performance of VIPIC cannot be directly tested with a laboratory source. A higher intensity X-ray source is necessary.
- The spec is to read out 10ph/mm^2/10us frame.
- For the current sensor (3.2 x 3.8 mm) => 12.1 mm^2 that amounts to 121ph/mm^2/10 us.
- With the current ^{55}Fe source, about 1 ph/mm^2/10us is recorded. A 100X brighter source is needed.
- Bench tests can be done that indicates the speed performance will be met.
  - The VIPIC is 5.1 x 5.1 mm => 25 mm^2. For spec of 10 ph/mm^2/10 us one would need to read out 250 pixels/10 us
  - In the imaging mode, the entire chip (4096 pixels) was read out with each of the 16 outputs handling 256 pixels in 80 us using a 50 MHz clock.
  - At 100 MHz, all 4096 pixels should be read out in 40 us.
    - 250 pixels sould be read out in 2.4 us
- Thus it appears that the current VIPIC chip is capable of providing time slices that easily meets the specification.

Near future plans

- Die to wafer bonding of sensors to full 3D wafer is in progress at Ziptronix using the DBI oxide-oxide bond process with nickel bond pads.
  - 80 um pitch sensors
  - All VIPIC readout channels connected (no skipped channels)
  - No bump bonds in the final assembly
- Planned X-ray beam test in the near future.

Acknowledgements

- These results would not have been possible without the extra special efforts by Piotr Maj from AGH-UST who came to Fermilab to perform tests and to Terence Collier at CVInc who spent considerable time working closely with Fermilab on perfecting the solder bumping on our chips. Thank you.

Conclusions/Insights

- We have made numerous attempts with Cu-Cu bonding and DBI/Cu oxide bonding to fabricate 3D circuits.
- It is only recently that we have made significant progress along with acceptable yields.
- At the present time, the DBI process with copper pads has given us the best results.
- The results of the VIPIC 3D chip mated with a sensor and illuminated with X-rays have been presented in this talk.
- Further work including sensor to wafer bonding using the DBI process and beam tests is planned
- In hindsight, if we had used larger size copper bond pads for the bond interface or taken a different bonding approach we might have saved ~ 2 years and avoided a lot of grief .
- That's why this is called research!!

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