The path towards the application of new microelectronic technologies in the AIDA community

Valerio Re

INFN

Sezione di Pavia

Università di Bergamo

Dipartimento di Ingegneria

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AIDA

- Advanced European Infrastructures for Detectors at Accelerators (AIDA)

WP1: Project management and communication
Scientific coordinator Laurent Serin, LAL-CNRS, Deputies : T. Benhe (DESY) & P. Soler (STFC)
Svet Stavrev, CERN administrative coordinator

Networking	Transnational access	Joint research
WP2: Common software tools (Frank Gaede, DESY, Pere Mato, CERN)	**WP5: Transnational access DESY** (Ingrid Gregor, DESY)	**WP8: Improvement and equipment of irradiation and test beamlines** (Michael Moll, CERN)
WP3: Microelectronics and interconnection technology (Hans-Gunter Moser, MPG, Valerio Re, UNIBG)	**WP6: Transnational access CERN** (Horst Breuker, CERN)	**WP9: Advanced infrastructure for detector R&D** (Marcel Vos, IFIC Valencia, Vincent Boudry, LLR-CNRS)
WP4: Relation with industry (S. Stapnes-→ JM Le Goff)	**WP7: Transnational access European irradiation facilities** (Marko Mikuz, JSI)	

The goals of AIDA WP3

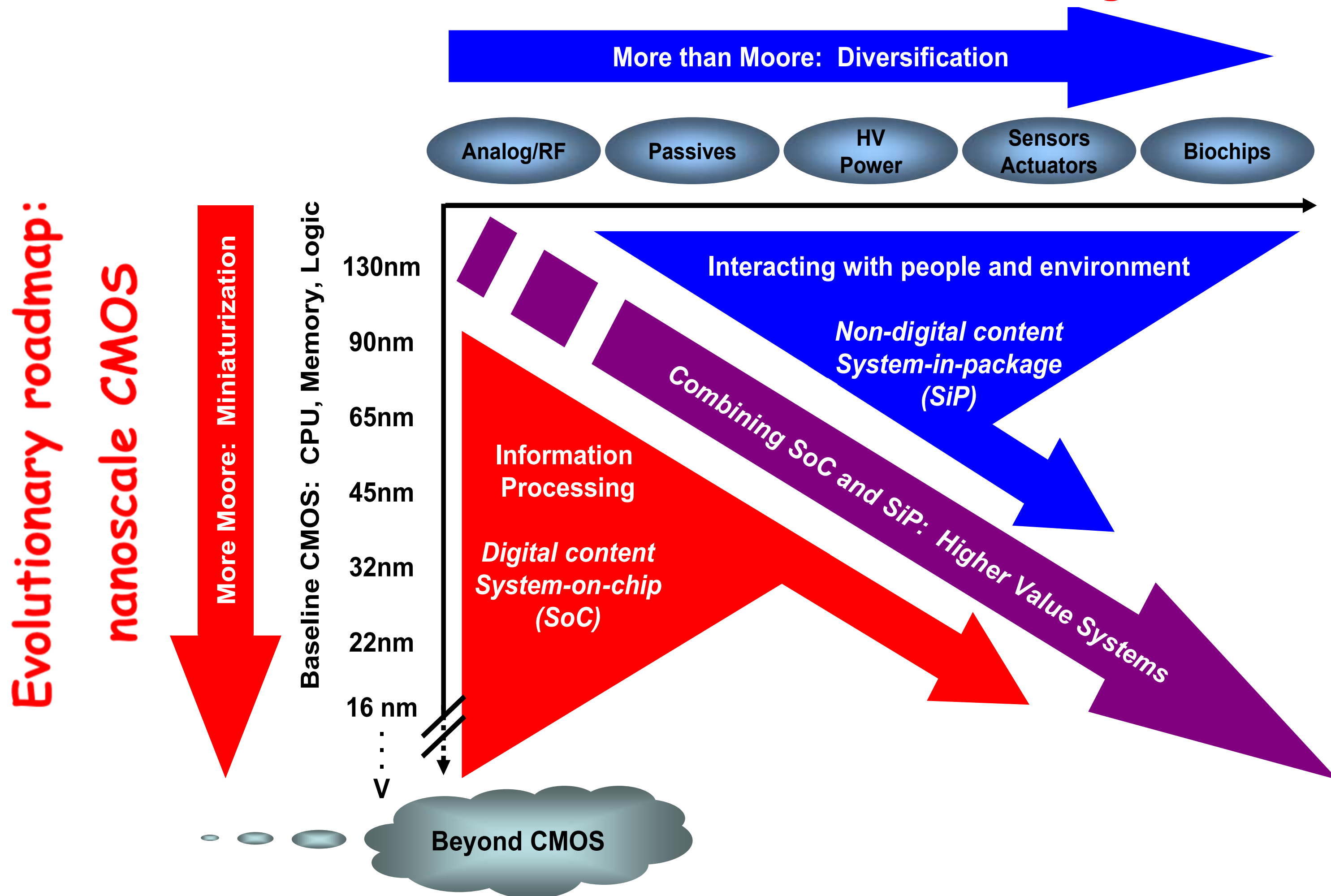
- AIDA WorkPackage3 has the goal of facilitating the access of our community to advanced semiconductor technologies, from nanoscale CMOS to innovative interconnection processes.

- ❑ 3D integration for novel tracking and vertexing detector systems and photon imagers based on high-granularity pixel sensors.

- ❑ 65 nm CMOS and SiGe BiCMOS for new mixed-signal integrated circuits with high density and high performance readout functions

Evolution of microelectronic technologies

No roadmap, room for new ideas: monolithic sensors, 3D integration



Advancing the state of the art of pixel sensors for a next generation of HEP experiments…

New demanding specifications for experiments at new machines (HL-LHC, Linear Colliders,…):

- **Improve resolution ⇒ shrink pixel size and pitch**, down to 20 μm or even less
- **Preserve or even increase pixel-level electronic functions**
  handling of high data rates (hit rates > 10 MHz/mm^2), analog-to digital conversion, sparsification, intelligent data processing…: presently this also contributes to limiting the minimum size of pixel readout cells
- **Decrease amount of material ⇒ thin sensor and electronics** chips, "zero mass" cooling
  - Necessary to reduce errors in track reconstruction due to multiple scatterings of particles in the detector system
  - 50 -100 μm total thickness

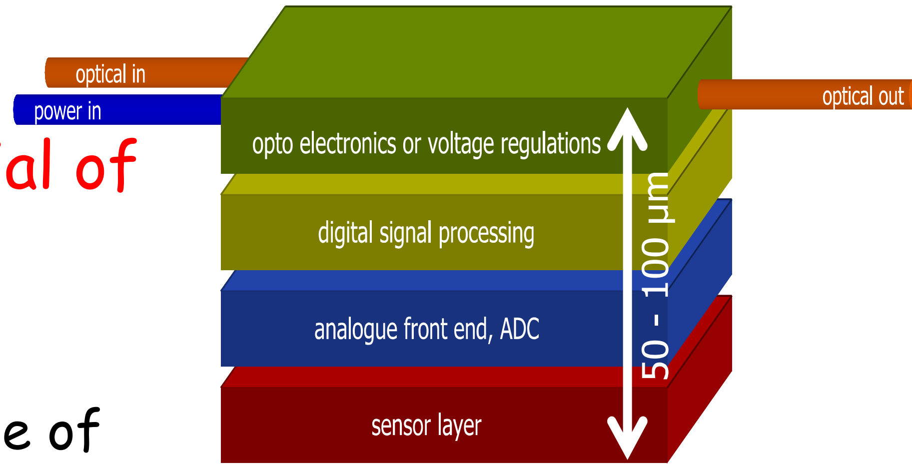
…and photon science

Potential benefits of new microelectronic technologies to future detector systems for X-ray imaging at free electron laser facilities:

- Reduction of pixel size (100x100 μm^2 or even less), presently limited by the need of complex electronic functions in the pixel cell
- Larger memory capacity to store more images
- Advanced pixel-level processing (1 – 10000 photons dynamic range, 10-bit ADC, 5 MHz operation)
- 4-side buttable tiles for a large area detector with minimum or no dead area

What is 3D integration?

- 3D electronics: "the vertical integration of thinned and bonded silicon integrated circuits with vertical interconnects between the IC layers."[1]



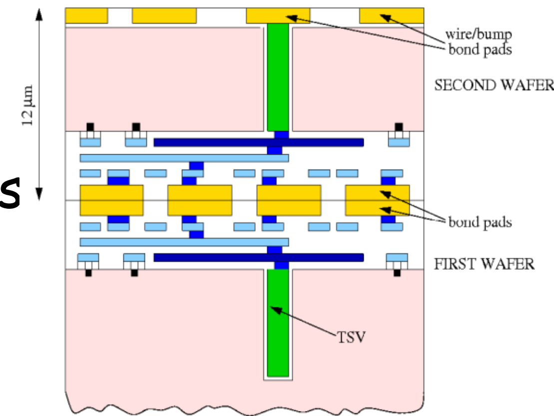
- 3D electronics has the potential of being:
  - Denser (smaller form factor)
  - Faster (reduced delay because of shorter interconnects)
  - Lower power (smaller interconnect capacitance)
  - Lower cost (sizably less expensive than aggressive CMOS scaling)
  - Integration of dissimilar technologies (sensor, analog, digital, optical)

1) Philip Garrou, Christopher Bower, Peter Ramm, Handbook of 3D Integration Technology and Applications of 3D Integrated Circuits, Wiley-VCH, 2008.

The diversity of 3D integration approaches: "via first" vs "via last"

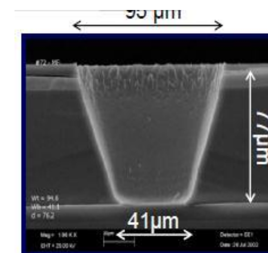
- Different approaches to 3D integration differ in terms of the minimum allowed pitch of bonding pads between different layers and of vertical Through-Silicon Vias (TSVs) across the silicon substrate.
- **Via first, Via middle**: Vias are part of wafer processing at the CMOS foundry, and are inserted before or right after the fabrication of transistors

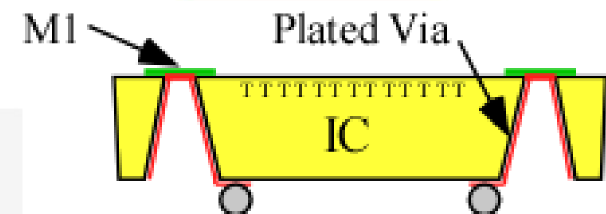
  ➔ **High density TSVs** (few μm pitch) through thinned wafers, allow multiple connections at the cell (pixel) level between transistor layers



- **Via last**: Vias are fabricated on fully processed CMOS wafers, at a facility outside the CMOS foundry

  ➔ **Low density TSVs** (tens of μm pitch) through unthinned wafers or partially thinned wafers, allow connectivity at the pad level in the chip periphery





3D heterogeneous integration and "via last" approach in AIDA WP3

- In our community, widespread interest for 3D integration was triggered thanks to pioneering efforts by Fermilab with 3-layer SOI chips from MIT-LL and (in the 3D-IC Consortium) with 2-layer 130 nm CMOS devices by Tezzaron/GlobalFoundries: both technologies have a high density of TSVs and bonding interconnections
- Even with not so aggressive 3D technologies, sizable performance improvements might be gained by fabricating devices with 2 (or 3…) layers, each optimized for its functions (particle sensing, analog amplification, A/D conversion, data storage…), with additional advantages such as removing dead areas.
- In most cases, only one or two connections are needed between the analog and digital blocks of a single pixel cell, and the digital layer can use low-density peripheral TSVs to reach backside bonding pads for external connection.
- The **"via last"** approach and **3D heterogeneous integration** are being tested by AIDA groups, both for HEP and imaging applications.

The AIDA WP3 task: establish a network for the investigation and qualification of 3D interconnection technologies

- **Explore 3D integration of heterogeneous layers: interconnection of layers fabricated in different technologies, "via last" technique for Through-Silicon Vias.**

- Different options for the pixel sensors (high resistivity fully-depleted detectors and CMOS sensors) and for the readout electronics (130 nm and 65 nm CMOS, 3D integrated circuits)

- Different specifications for the interconnection technologies:

  relatively mature 3D processes for peripheral TSVs and for interconnection:

  high confidence level for the fabrication of demonstrators in the AIDA time span.

  more aggressive 3D processes for a low pitch (< 50 μm) for TSVs and interconnection as required to fully exploit 3D potential: higher level of risk but clear added value in view of future designs of advanced pixels (high resolution and high integration density for an intelligent pixel-level processing)

3D interconnection Sub-Projects

1) Bonn/CPPM:
Interconnection of the ATLAS FEI4 chips to sensors using bump bonding and TSVs from IZM (large diameter TSV, large interconnection pitch).

2) CERN:
Interconnection of MEDIPIX3 chips using the CEA-LETI process

3) INFN/IPHC-IRFU:
Interconnection of chips from Tezzaron/Chartered to edgeless sensors and/or CMOS sensors using an advanced interconnection process (T-MICRO or others)

4) LAL/LAPP/LPNHE/MPP:
Readout ASICs in 65nm technology interconnected using the CEA-LETI or EMFT process.

5) MPP/GLA/LAL/LIV/LPNHE:
Interconnection of ATLAS FEI4 chips to sensors using SLID interconnection and ICV (high density TSVs) from EMFT.

6) Barcelona
use a 2-tier approach to increase the fill factor of APD-sensors (based on Tezzaron/Chartered)

7) RAL/UPPSALA
Integration of a 2-Tier readout ASIC for a CZT pixel sensor using EMFT SLID technology and TSV, including redistribution of I/O connections to the backside for a 4-side buttable device.

The diversity of 3D in the WP3 subprojects

- **LHC (ATLAS) pixel upgrades and high resistivity pixel sensors**

Four-side buttable pixel modules with ATLAS FE-I4 readout chip and via last TSV processing, low-density (IZM) and potentially high-density (EMFT)

New 65 nm pixel readout chips in a 3D assembly with pixel sensors (LETI)

- **Pixels for linear colliders, B-factories,… with CMOS sensors, APDs,…**

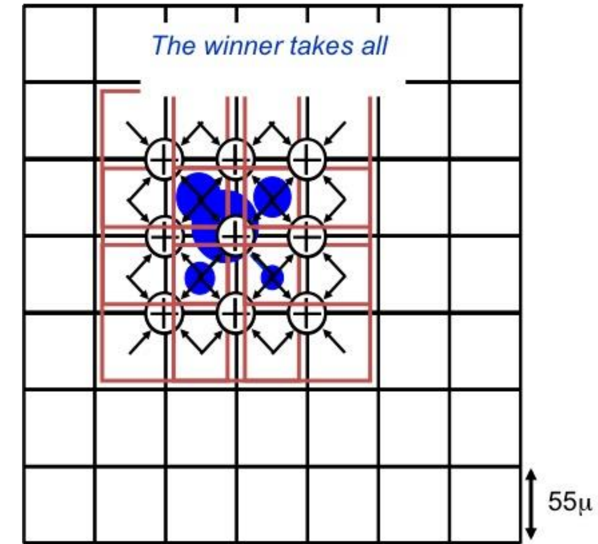
Designs of 3D CMOS chips based on the 3D integration of two 130nm layers (Tezzaron), evaluating alternatives for CMOS (Tower/Jazz) and "via last" TSVs (T-Micro, LETI)

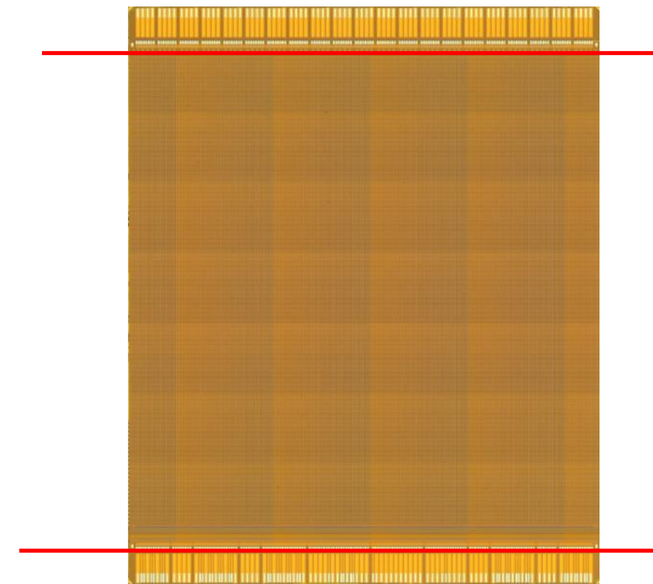
- **Photon science with silicon and High-Z detectors**

4-side buttable imaging sensor tiles (LETI), 3D mixed-signal integrated circuits (T-Micro, EMFT)

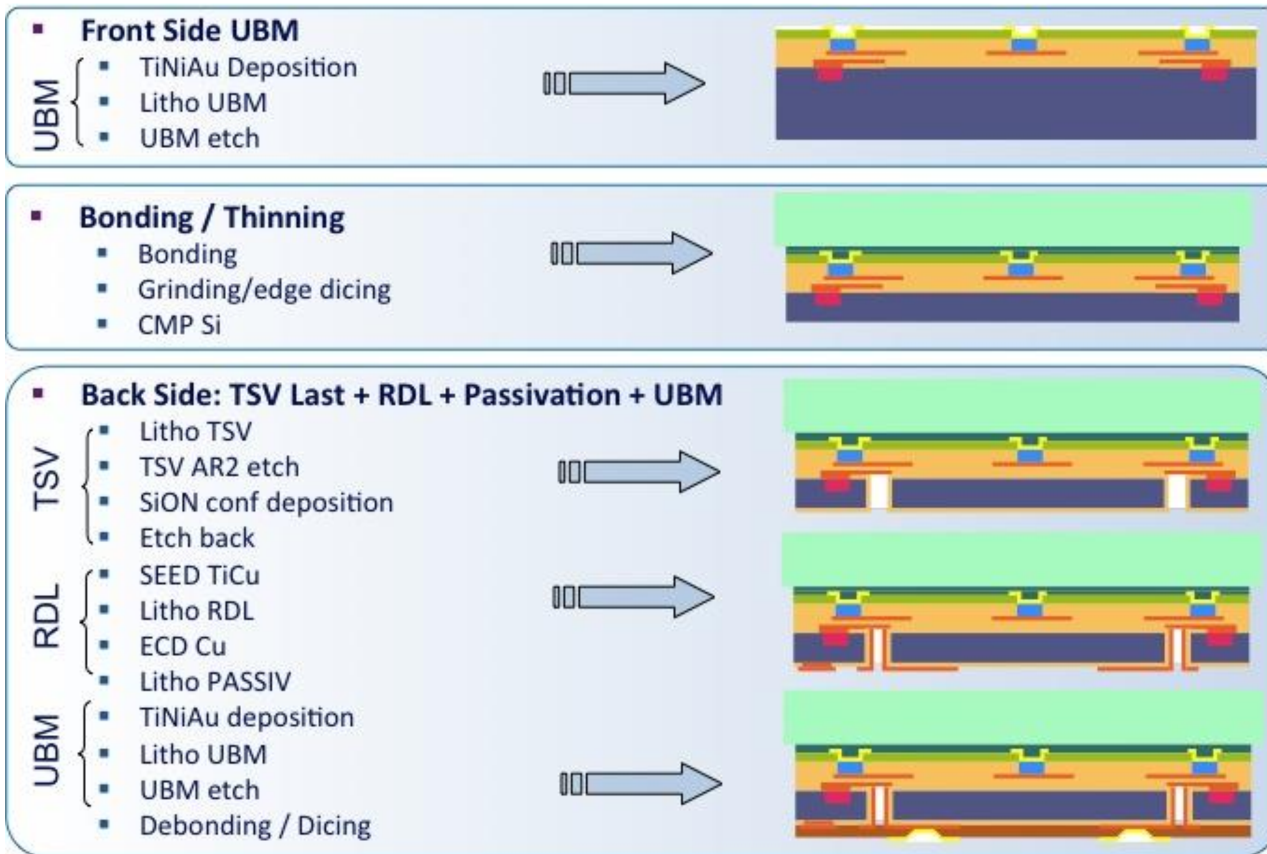
CERN: TSV on MEDIPIX3 for minimal dead area and 4-side butting

- MEDIPIX3: 130 nm CMOS chip for high resolution X-ray spectral imagers based on hybrid pixel detectors (256x256 square pixels of 55 μm size)
- Novel charge summing architecture: charge in 4-pixel cluster added to pixel with largest charge, eliminating spectral distortion due to charge diffusion in the sensor (highly programmable, can operate at 110 μm pitch in spectroscopic mode)
- For 4-side buttable imaging tiles, remove periphery with I/O pads, insert TSVs and backside redistribution layer with BGA pads (CEA-LETI process)





LETI TSV process



- AR (wafer thickness to TSV diameter) max 3:1

- Minimum TSV pitch 80um
- Minimum TSV diameter 40um

- RDL min track width 20um
- RDL min track space 40um
- RDL thickness range 2um to 12um Cu

- Front side UBM min space 30um
- Front side UBM min width 20um
  (For ref MPIX3 25um diameter on 55um pitch)

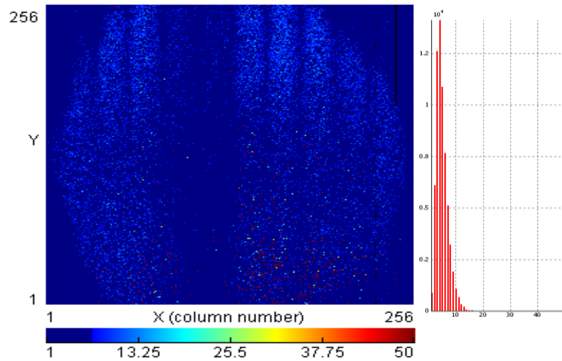
- Back side UBM min space 30um
- Back side UBM min width 20um

- TSV typical resistance 50mohm (60um on 120um thickness)
- TSV typical isolation >= 1Gohm

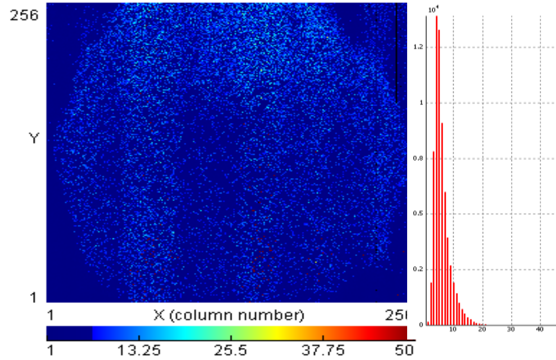
- Resistance UBM to Al pad 150mohm for 25um diameter.

CERN: tests of TSV process on MEDIPIX3

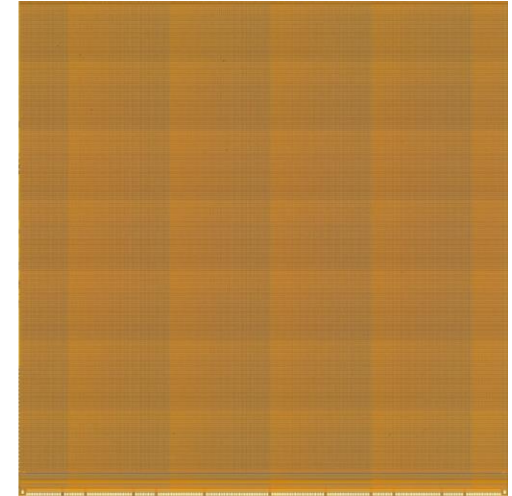
- Phase I: TSV processing on Medipix3 wafers (done , good yield and performance)



Noise floor before TSV



After TSV



All IO logic and pads contained within one strip of 800μm width

- Phase II; Hybridization of the TSV processed chips

  Flip chip interconnection to sensors (first assemblies received from VTT/ADVACAM)

All IO´s have TSV landing pads in place

Permits 4-side butting

- Phase III: Demonstrator Module

  demonstrate multichip module operation

94% sensitive area

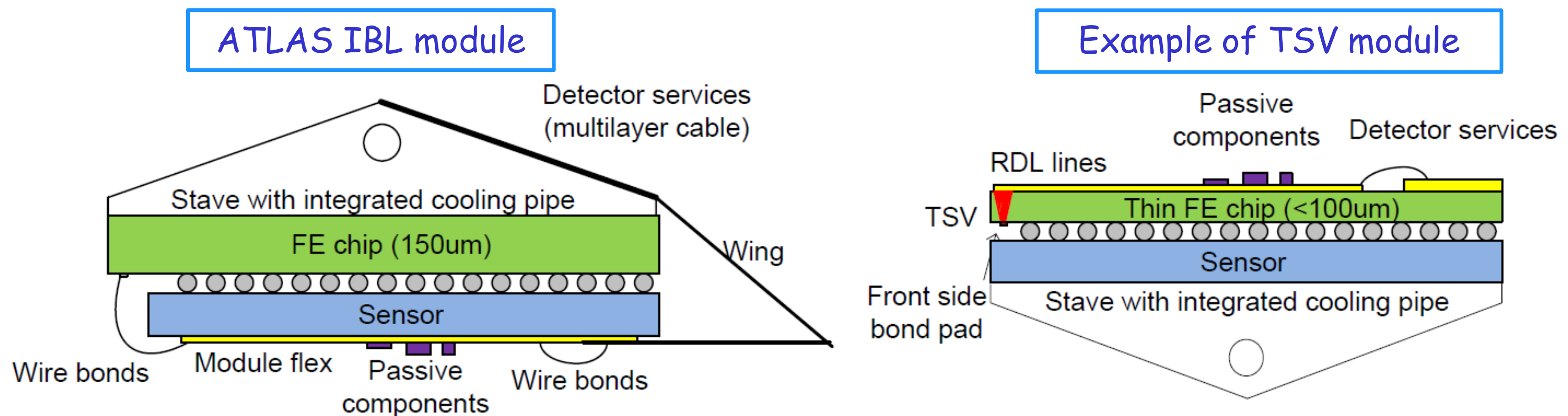
Bonn/CPPM: via last TSV process on ATLAS pixel chips

- The goal of the project is to develop modules for ATLAS pixel detector at the HL-LHC using a via last TSV process
  - Post-processing technology applicable on existing FE electronics
  - Dead area at the chip periphery can be reduced

  → Compact, low mass hybrid pixel modules with minimal modification to the FE layout and using standard CMOS technology

  → Potential for 4 side buttable modules using dedicated sensor layout

- Modules with TSV can be used for the outermost detector layers at the HL-LHC to provide full detector coverage over the large area

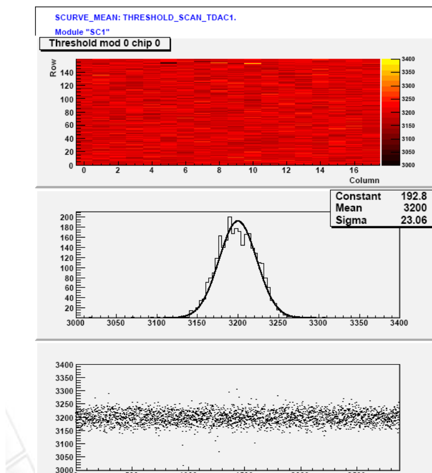


Bonn/CPPM: via last TSV process on FE-I2 chips

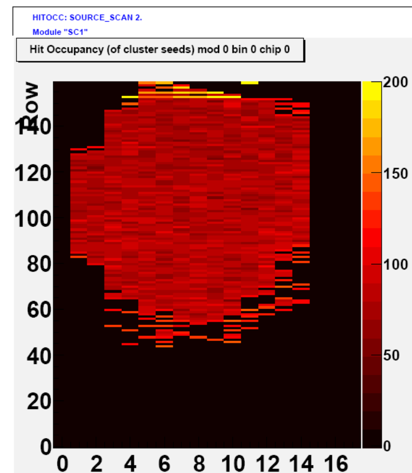
- IZM integrates the TSV process into the bump bonding process (make TSV first and afterwards do BB)
- ultra thin (< 100μm) flip chipping (developed for bumped FE-I4 chips for the ATLAS IBL)

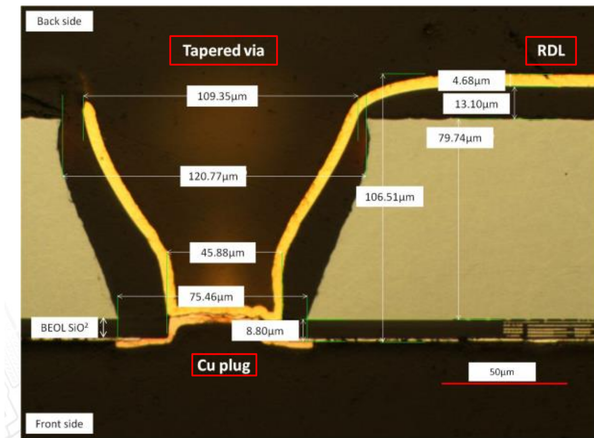
Large tapered sidewall vias were selected, and successfully tested with FEI2-based modules (first HEP demonstration of TSV modules with backside connections)

- Threshold tuning to 3200e



- Source scan with an Am-241 source





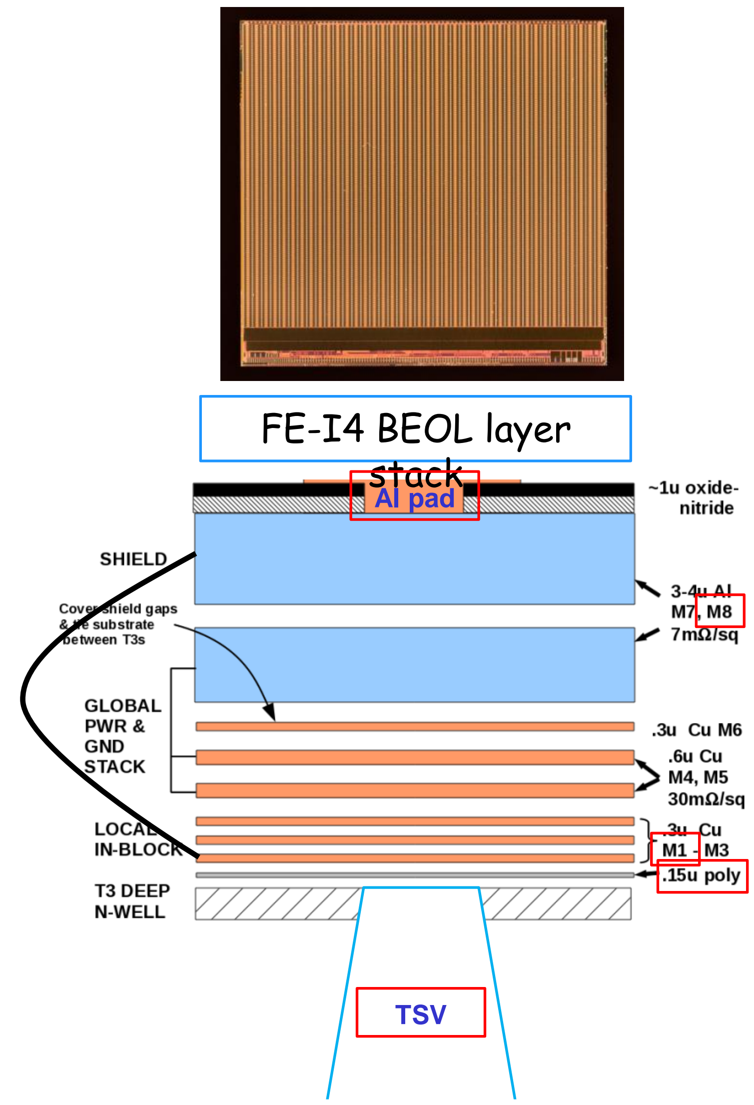
- Front side processing to connect TSV bottom to Al pad → Cu plug
  - No metal layers in the pad
  - ~9 μm thick BEOL SiO_2 stack technically difficult to etch from the back side through the TSV opening on the bottom

Bonn/CPPM: via last TSV process on FE-I4 chips

Next step: FEI4B modules with TSVs: wafers ready for processing, results expected 1Q 2014

- No front side processing needed
  - Metal layers in the pad
  - M8 connected to M1
  - Between silicon and M1 thin layer of BEOL SiO_2 and poly-Si → can be etched from the back side
- Bump bonding of thin (<100µm) FE-I4B with TSV to sensors will use handle wafer
  - FE-I4B area = ~4cm² → prohibitive bending of the FE during reflow
- Method needs to be demonstrated on FE-I4 wafers with TSV and RDL

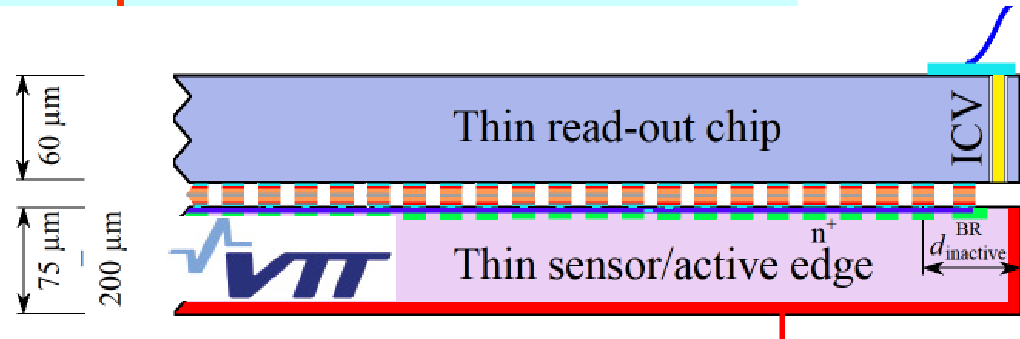
  → constraints on the polymeric glue (connecting handle wafer ond FE wafer) thickness and the uniformity of the deposition



MPP/GLA/LAL/LIV/LPNHE: ICV-SLID process on FE-I4

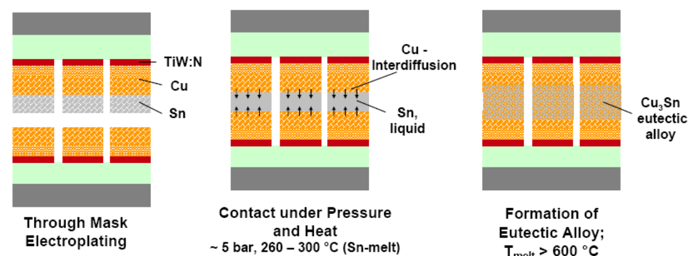
Goal: demonstrator module for SLID and TSV technologies based on ATLAS FE-I4

Similar to Bonn/CPPM project, but more 'aggressive technology
⇒SLID ok for smaller pitch
⇒ potentially, 3μm 1:10 vias



- Project in collaboration with Fraunhofer EMFT, to develop Inter Chip Vias (Via Last approach) to show the feasibility to transport signals and services on the backside using the existing FE-I4 chip
- Inter-Chip-Vias to be etched on each wire bonding pad, cross section ~ 10x30 μm^2
- Chip and sensor connected using SLID technology
- Active edge sensors to remove inactive area associated with Guard Ring structure
- Small pitch possible (~ 20 μm, depending on pick & place precision).
- Stacking possible (next bonding process does not affect previous bond).
- Wafer to wafer and chip to wafer possible.

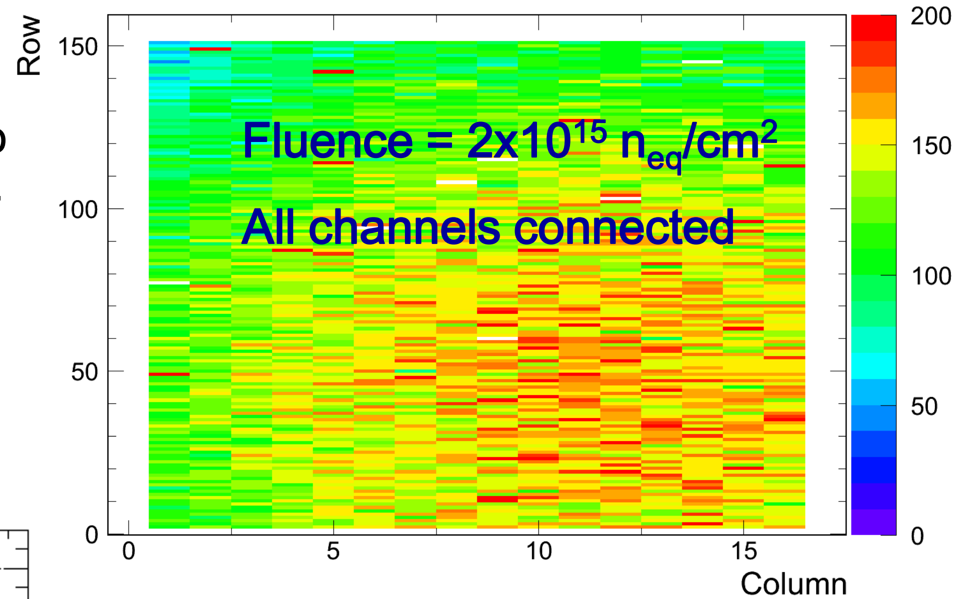
Metallization SLID (Solid Liquid Interdiffusion)

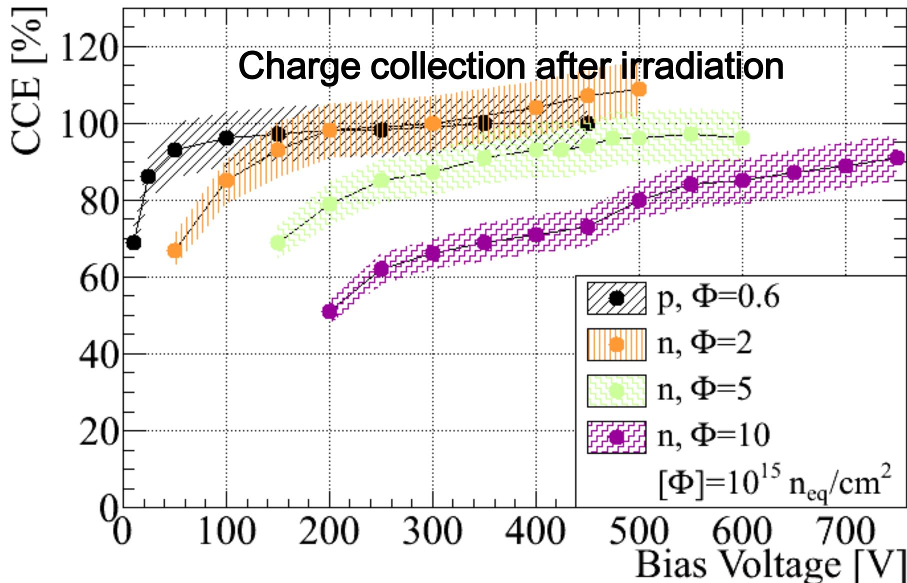


Results with FE-I3 SLID pixel modules

75 μm thick sensors interconnected with SLID to FE-I3 chips, thinned down to 200 μm, at EMFT

- Noise performance comparable to detectors interconnected with bump-bonding
- Stable SLID interconnection after irradiation and thermal cycling





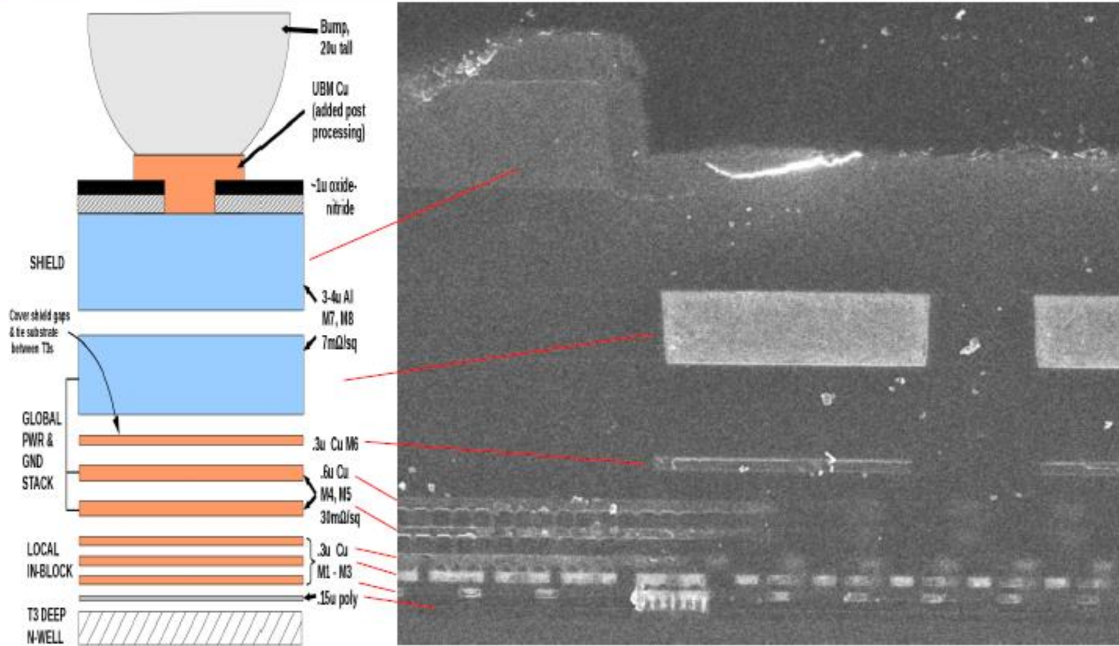
- Good Charge Collection efficiency after irradiation up to 10^{16} n_{eq}/cm^2

SLID interconnection run with FE-I4 sensors (CIS production) and chips foreseen at the end of this year

Inter Chip Vias in the FE-I4 chip

A different technique is needed on FE-I4 because of different metal stacks and filling structures (etching from the backside).

SEM analysis of the FE-I4 wire bonding pad



- FE-I4B IBL wafers are available for TSV trials at EMFT
- Plan is to interconnect FE-I4 to VTT/ADVACAM active edge sensors to build a 4-side buttable demonstrator module.

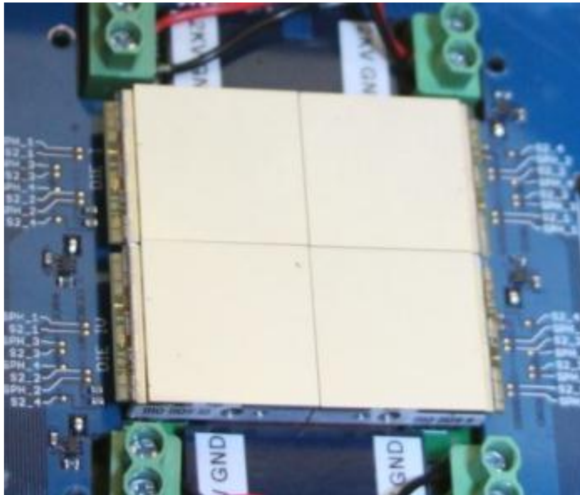
- ❑ Most of the eight FE-I4 metal layers are present in the wire bonding pads → not possible to etch ICV from the front-side
- ❑ Design and test of the ICV layout on test-wafers in on-going: target cross-section 10x30 μm^2 with a global chip thickness of 100-150 μm

RAL/Uppsala:3D integrated circuit for the readout of Cd(Zn)Te detectors for SPECT

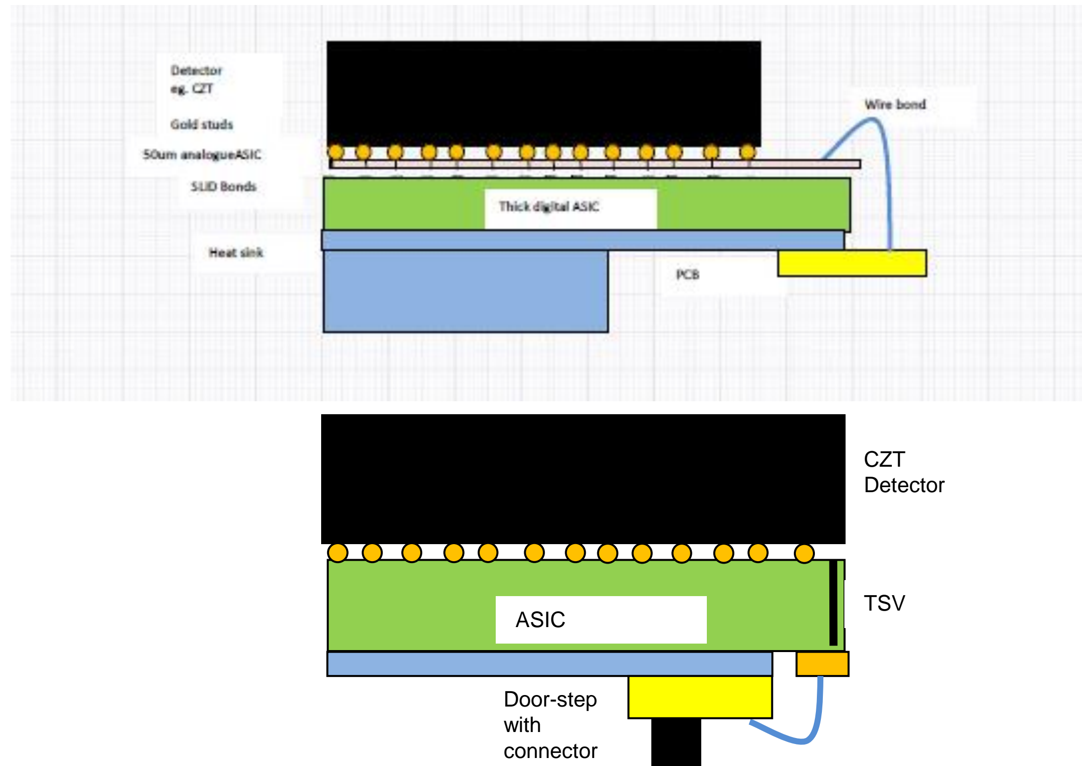
Hexitec CdTe detector to image brain function with dual isotope SPECT

Need of tiling the system bigger than 2x2

New ASIC with TSVs through 100um silicon to allow 4-side butted detectors.



Current 3-Side butted 1mm thick CdTe for dual isotope SPECT.

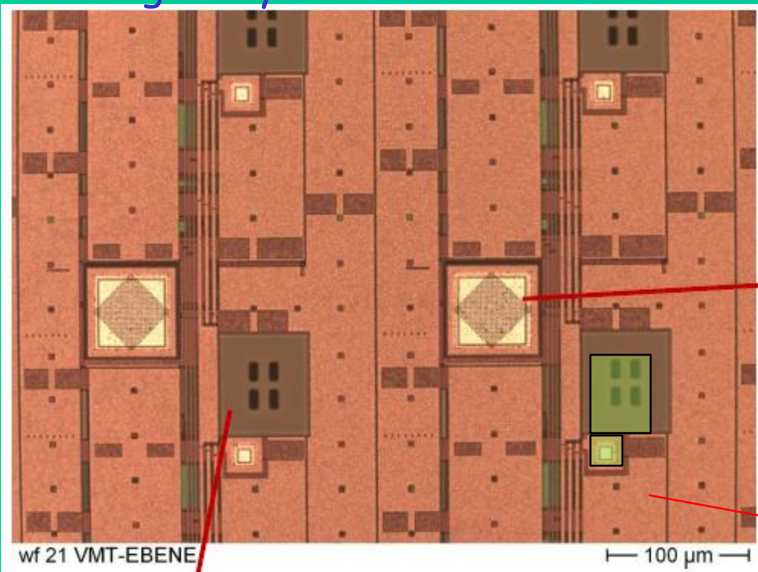


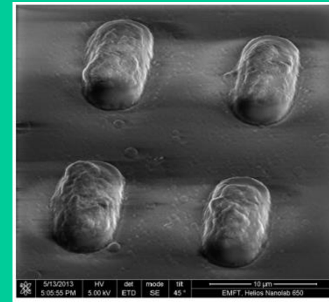
Geometry for 4-side butting and no dead region

RAL/Uppsala: 3D integration of analog and digital chips with EMFT process

I/O TSVs with T-Micro, 3D integration (pixel interconnects between analog and digital layers) with EMFT

Analogue layer





Vias on back of 50um silicon after backgrinding.

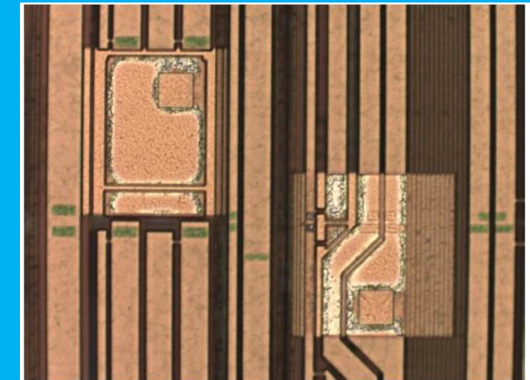
Large bond pad for connection to CdTe detector

Green area is where Al connection from pad to vias is made.

4 tungsten vias in the free silicon area. through 50um silicon.

Digital layer

First trial of SLID patterning onto digital (thick layer). Copper definition not good so reworking this, shows relatively large SLID pads.

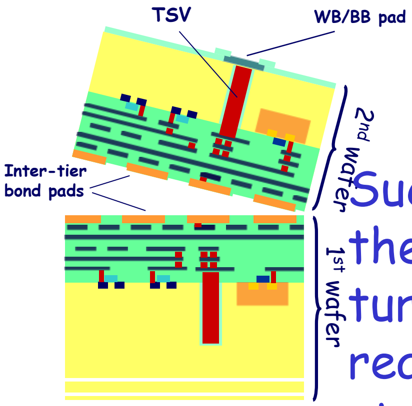


Progress: built 12 wafers of a version of Hexitec with 40x 40 pixels with 250um pitch.

Analogue chip as Hexitec (PA, shaper, peak hold) and a digital layer with a 12 bit ADC in each pixel. These will have TSVs from each analogue pixel through the silicon to the digital pixel. These now work separately and EMFT have processed 3DIC TSVs in the wafers up to SLID level.

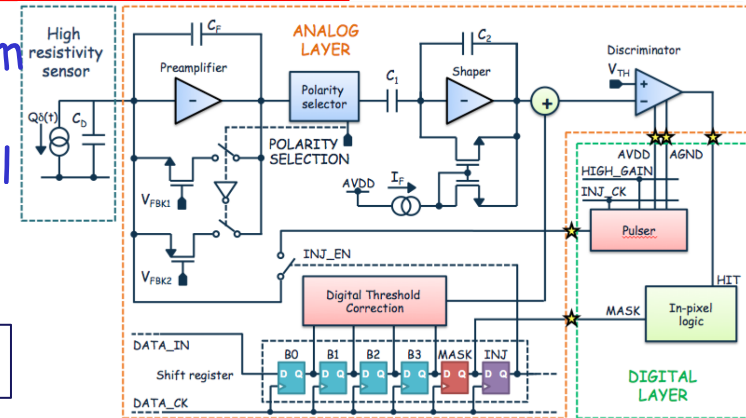
INFN-IPHC: 3D integration of a readout chip with a sensing layer (high-res CMOS sensor or active edge)

- Multi-tier pixel sensor resulting from the 3D integration of a readout chip and of a sensing layer



CMOS readout chip, based on a 130 nm vertically integrated process (Tezzaron/Globalfoundries)

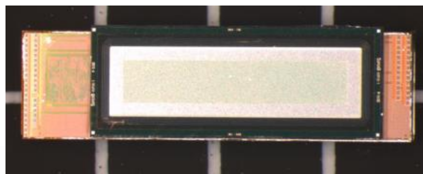
Successful tests on MAPS chips from the first MPW run (but very long turnaround time, low yield); new pixel readout chip at an advanced design stage, submit if process is available

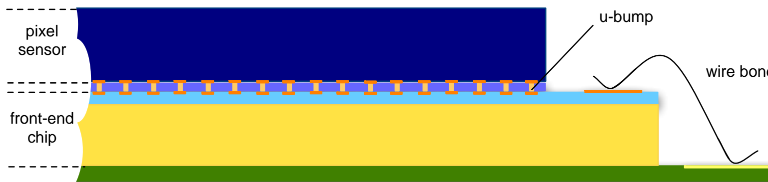


vertical interconnection process (μ-bumps by T-Micro)

Very high interconnect density (15 or 5 μm pitch)

Preliminary tests on 2D 130nm 128x32 readout chip and planar n-on-n pixel sensors





edgeless (or 3D slim edge) fully depleted, planar silicon detector (from FBK, Trento)

Alternative: CMOS sensing layer, with high-resistivity epi or substrate

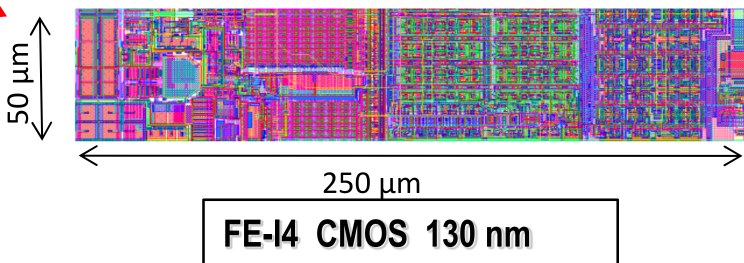
In the four tested samples, respectively 1%, 2%, 8% and 24% of the interconnections were found not to work properly. – would use some improvement also in the other cases

Results on the 3D-IC run with Tezzaron/GlobalFoundries for AIDA groups

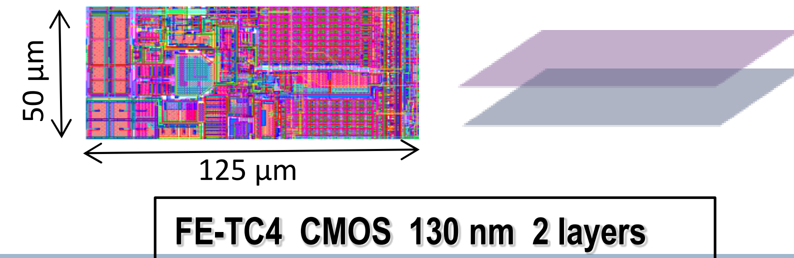
Several chips submitted in 2009/10 in the first 3D-IC MPW run (Bonn/CPPM, LAL, INFN,..)

First fully functional 3D working chips in summer 2012

No degradation of analog, noise and radiation hardness performance with respect to standard 2D 130 nm processes. With appropriate shielding, digital activity does not interfere with the analog front-end.



Next step: bump bonding connection to a planar pixel sensor (FE-TC4, Omegapix). If hybridization on a 12 µm thinned analog tier works, a full demonstration of this 3D process will be achieved.

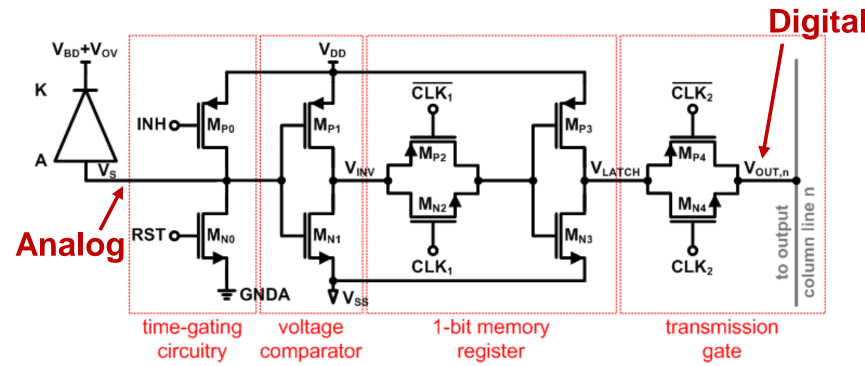


The yield, reliability and turnaround time of this aggressive 3D process still is an issue.

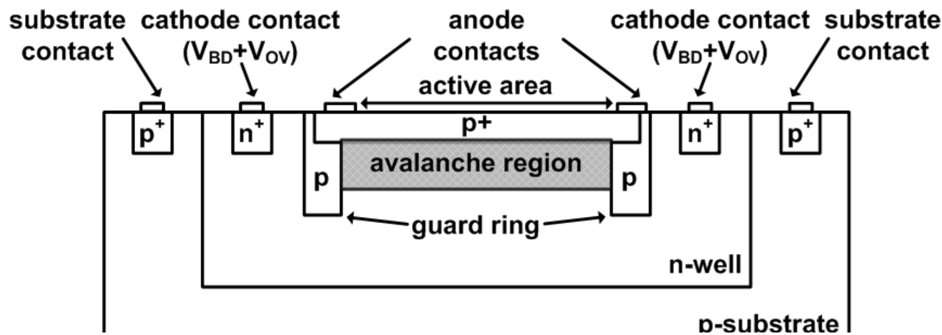
Plans for submitting new 3D chips are pending, waiting for a viable access to the technology (or to a variant of the process used for the first 3D-IC run) .

Univ. Barcelona: Geiger APDs with 2-layer 130 nm CMOS (Tezzaron/GlobalFoundries)

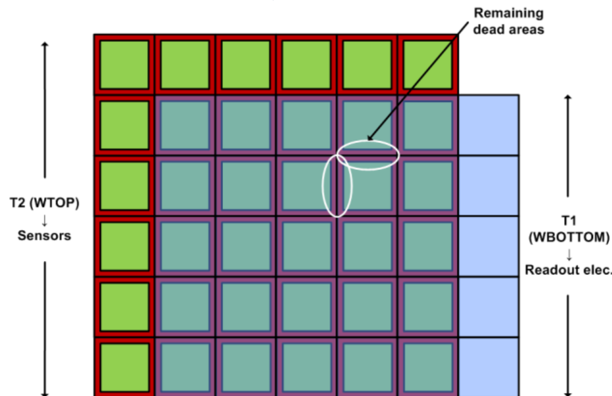
- Tracking sensor based on Geiger APD in 3D-IC CMOS (incl. readout)
- Use 2 tier 3D to increase fill factor (up to 92%) and cure the dark count problem by time-gated operation
- Design ready, waiting for CMP/MOSIS MPW run with Tezzaron

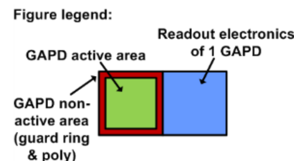


- The GAPD is activated before the BX
- It is deactivated during the interBXs
- The GAPD's ground GNDA allows to use low V_{OV} and further reduce the noise
- The array is read row by row during the interBXs

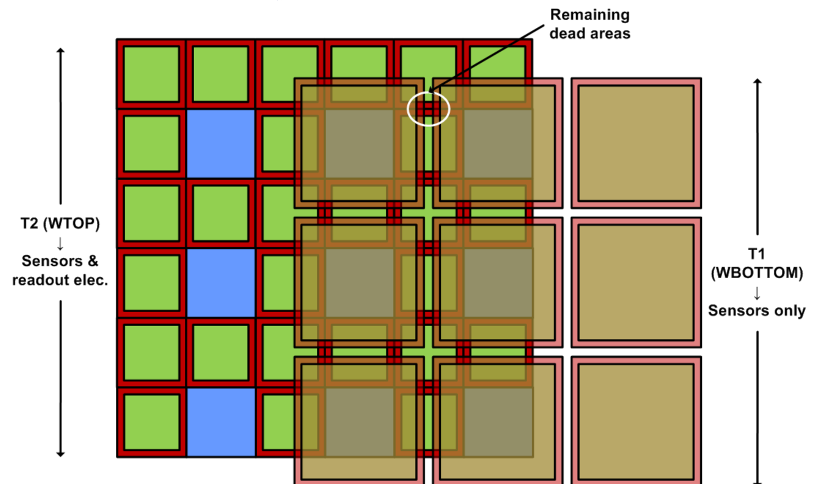


- T1 → electronics;; T2 → sensors



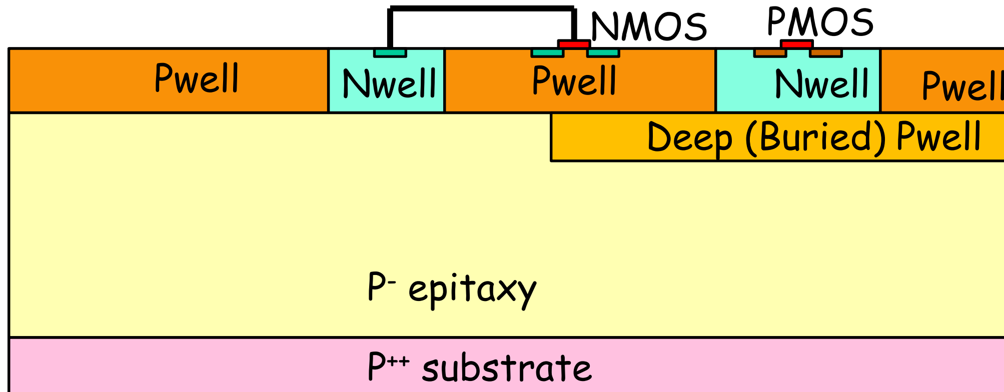


- T1 → sensors;; T2 → sensors & electronics



IPHC: 3D integration of 2 layers in the 180 nm Tower/Jazz process (with thick high-res epi)

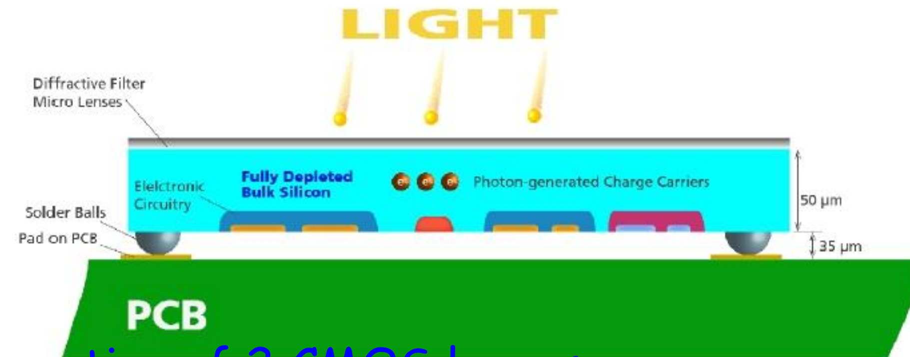
TOWERjazz® CIS 0.18 μm CMOS, 18 μm thick, > 1 kΩ cm epi layer, quadruple well process (both NMOS and PMOS allowed on pixel array)



Wafer Cross Section

Depletion of high-resistivity active layer for higher radiation hardness and thicker sensitive region possible with AC coupling between small pixel diode and front-end amplifier

Alternatives for thick high-resistivity substrate are available (ESPROS: detector grade, n-type,fully depleted 50 μm thick bulk silicon)

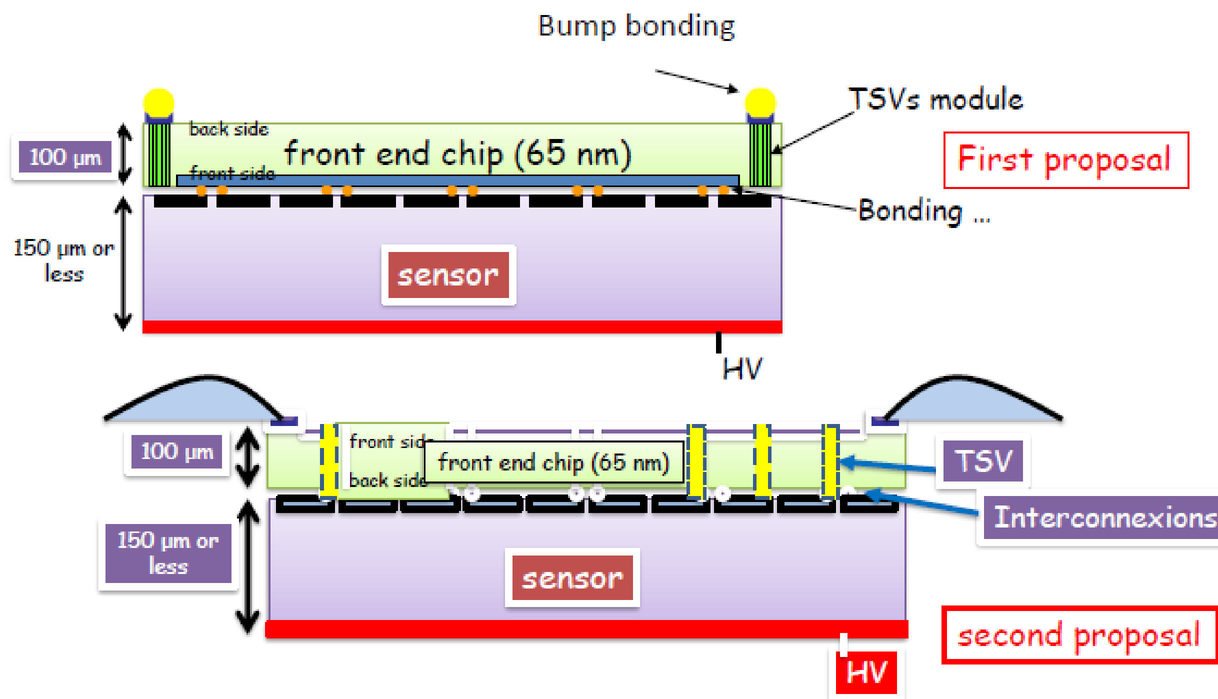


Proposal for the 3D face-to-face interconnection of 2 CMOS layers (sensor/analog front-end + digital readout) from the 180nm TowerJazz process with SLID bonding by Fraunhofer IMS in Duisburg (submission: end of 2013)

LAL/LPNHE: 3D integration of pixel sensors with 65 nm readout chip

Combine major technology advances and evaluate potential benefits of 3D interconnections

- OmegaPix with Tezzaron/Globafoundries
- 65 nm : work in coordination with CERN, goal to design a new pixel readout chip
- Collaborative work with « open » TSV providers in Europe to demonstrate TSVs on functional chips (IPDIA, CEA LETI).



A common library of shareable IP blocks for HEP in AIDA WP3

Goal : provide IP blocks for analog and digital needs in HEP with full documentation and laboratory tests.

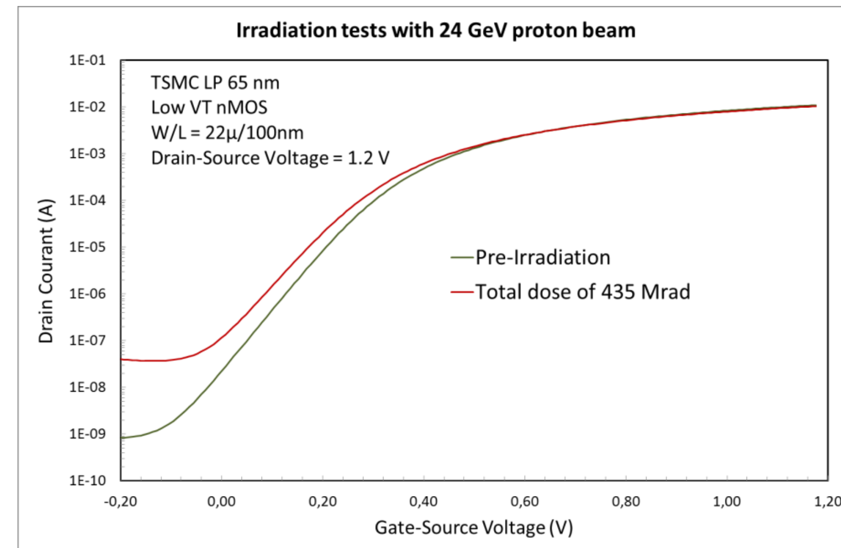
1st set organized by CERN in 65nm. Lot of interest by the community, some work has already started, triggered by the needs of new pixel systems (see ATLAS/CMS RD53), will gain momentum when contract negotiations by CERN with 65 nm foundry are concluded

A 2nd set will be organized by OMEGA for needs in calorimetry, TPC,… (OMEGA/LAL → OMEGA/IN2P3) (large dynamic range, high speed , low noise, low offset, need of precise capacitors and resistors, …).
Technology choice ongoing, based upon an estimation of availability in the future (market needs):

- SiGe or CMOS SOI, HV ….
- 130 nm or 180 nm
- IBM, ST micro, AMS …

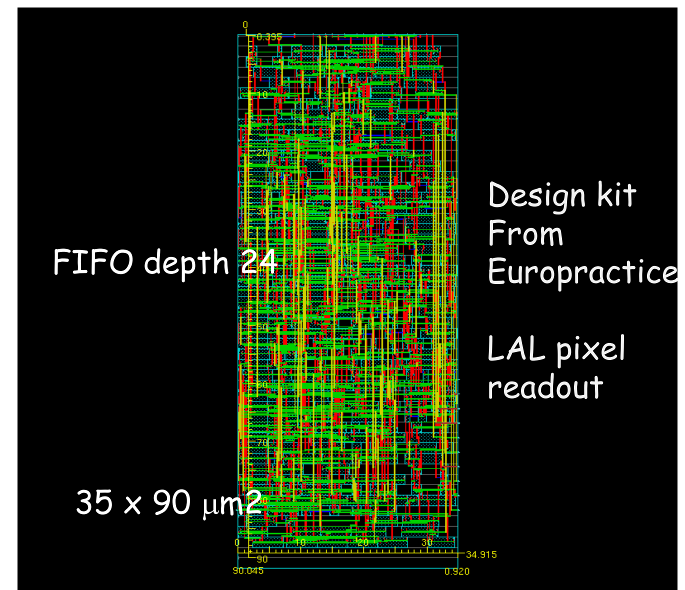
65nm work in AIDA WP3

- Irradiation tests at extreme total ionizing dose (target: 1 Grad) with 24 GeV proton beam (CPPM): some degradation at very high doses, more work on technology characterization is needed



- Design of IP blocks (CPPM, LAL/LAPP/LPNHE, AGH-Krakow, INFN, CERN,…): pixel readout blocks, fast and monitoring ADCs, DACs, OTAs, SEU-tolerant logic, bandgap reference, temperature sensor, PLL, SLVS interfaces,…

- These blocks will be likely used in future 65nm pixel readout chips (HL-LHC detector upgrades and others)



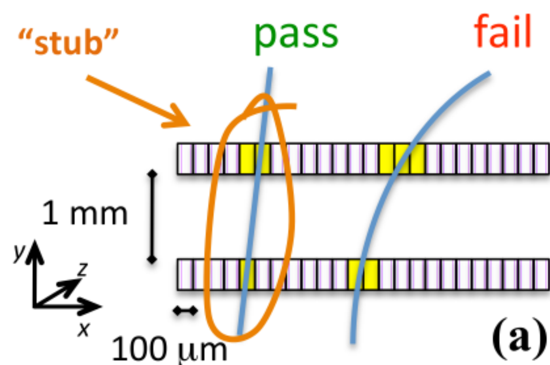
Towards the conclusions: future applications of 3D vertically integrated pixels

- The first 3D-IC run provided demonstrators of 3D CMOS chips, and confirmed potential advantages of 3D integration. The problems associated with this run do not seem to prevent the AIDA community to continue pursuing 3D as a way of devising advanced pixel detectors.

- The "via last" approach is being tested with encouraging results by AIDA groups, both for HEP and imaging applications, and may open the way to new design ideas.

- A few of these new concepts (inside and outside the WP3 network) exploiting 3D integration for particle tracking and vertexing and for X-ray imaging at FELs will be discussed in the following slides: they may combine the key AIDA technologies (3D integration, CMOS 65 nm)

3D techniques in a pixel-strip module for a prompt momentum discriminating tracker at HL-LHC



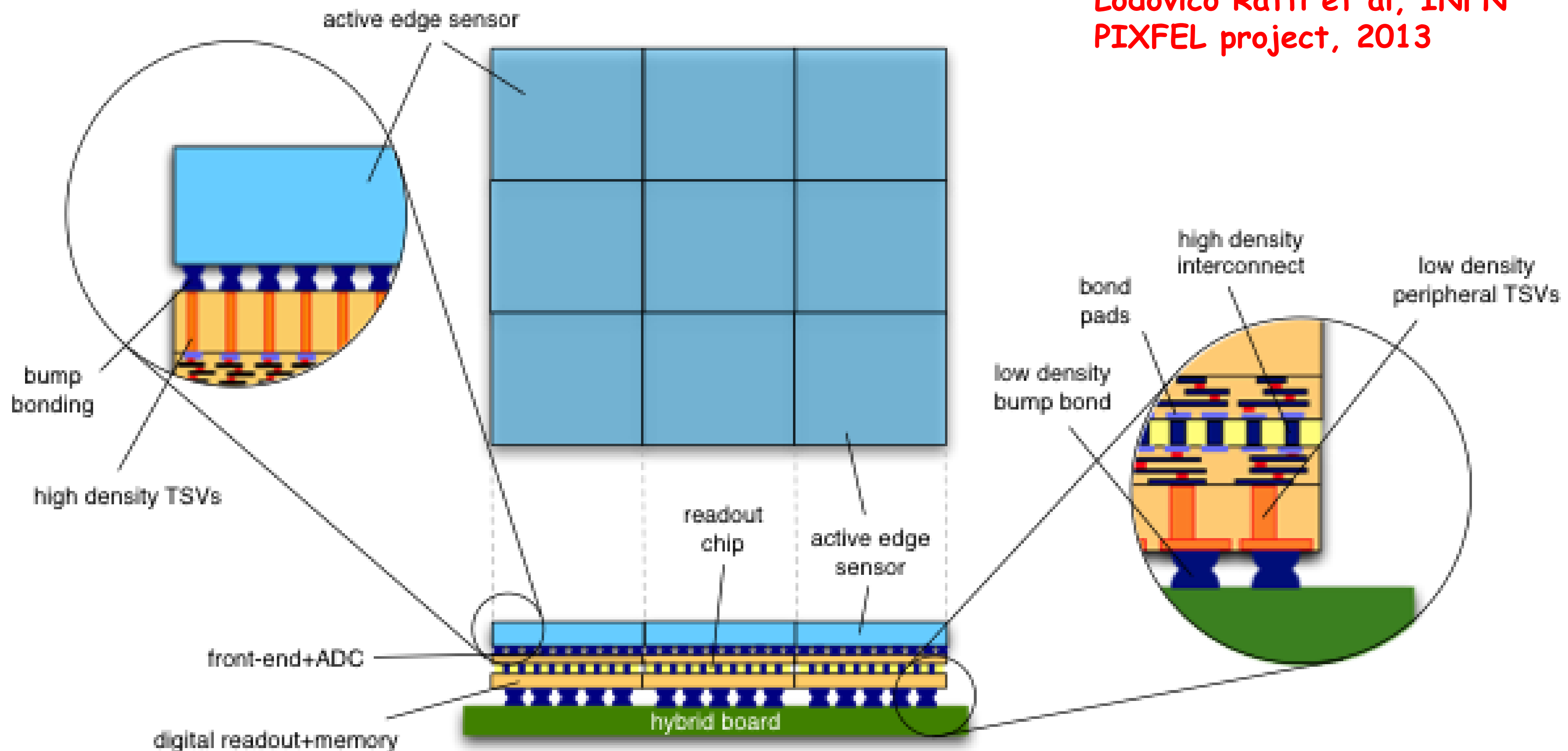
Provide information for Level-1 trigger processing, with local rejection of signals from low-momentum particles. correlating signals in two closely-spaced sensors.

Optimize *pT* cut by tuning sensor spacing and acceptance window.

TSV at the periphery of the pixel ASICs "bridging" two rows of chips in the middle, avoiding regions of stub finding inefficiency

D. Abbaneo, A. Marchioro, A hybrid module architecture for a prompt momentum discriminating tracker at HL-LHC, JINST 7 C09001

Enabling technologies for high-performance 4-side buttable X-ray imaging module: active edge pixel sensors, through-silicon vias, 65 nm CMOS,…



A 3D integrated circuit (AGIPD) for the readout of edgeless pixel sensors for X-ray imaging at XFEL

> mid term: "logic – on - memory"

1) bump-bond to the detector

2) amplification & double sampling

5) digital signal readout

tech #1 (CMOS Low Pow)

tech #2 (CMOS High Perf)

3) ADConversion

tech #3 (DRAM)

4) store the digitalized signal in a digital memory cell

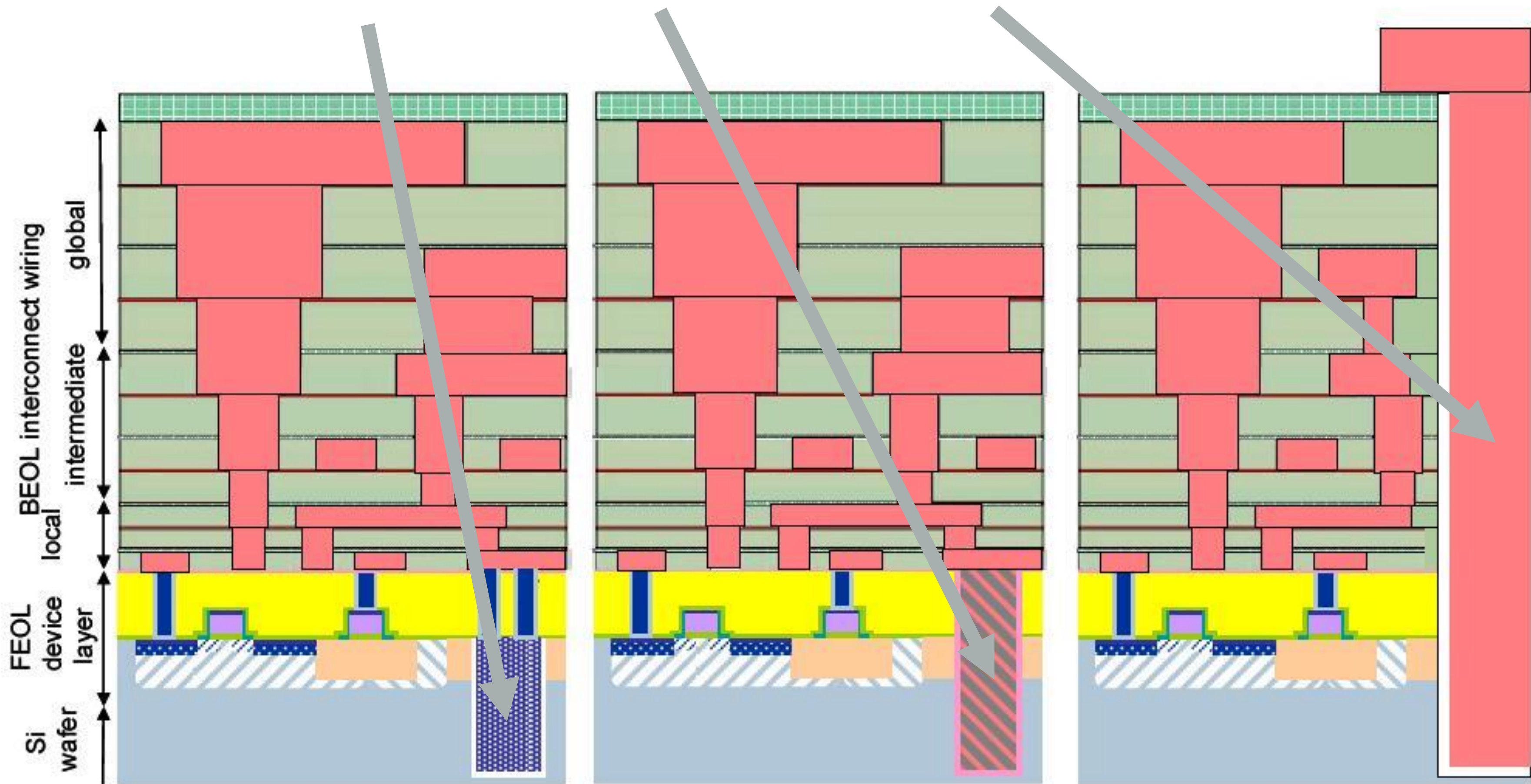
Heinz Graafsma, 532.WE-Heraeus Seminar, May 2013

Conclusions

- The AIDA WP3 subprojects are exploring various flavors of 3D integration; the progress is largely depending on the different level of maturity of the 3D processes ("via last" vs. "via middle", high vs. low interconnection density, etc.)
- Some subprojects (e.g. CERN/MEDIPIX) are already very close to their goal of implementing 3D pixel demonstrator modules
- New concepts exploiting advanced microelectronic technologies are being developed inside and outside the AIDA community, and will likely play a key role in future detector systems

Backup slides

Via First, Middle and Last Process Flows



Semiconductor Industry Association,
“The International Technology Roadmap for Semiconductors”,
2011 Edition.SEMATECH:Austin, TX, 2011