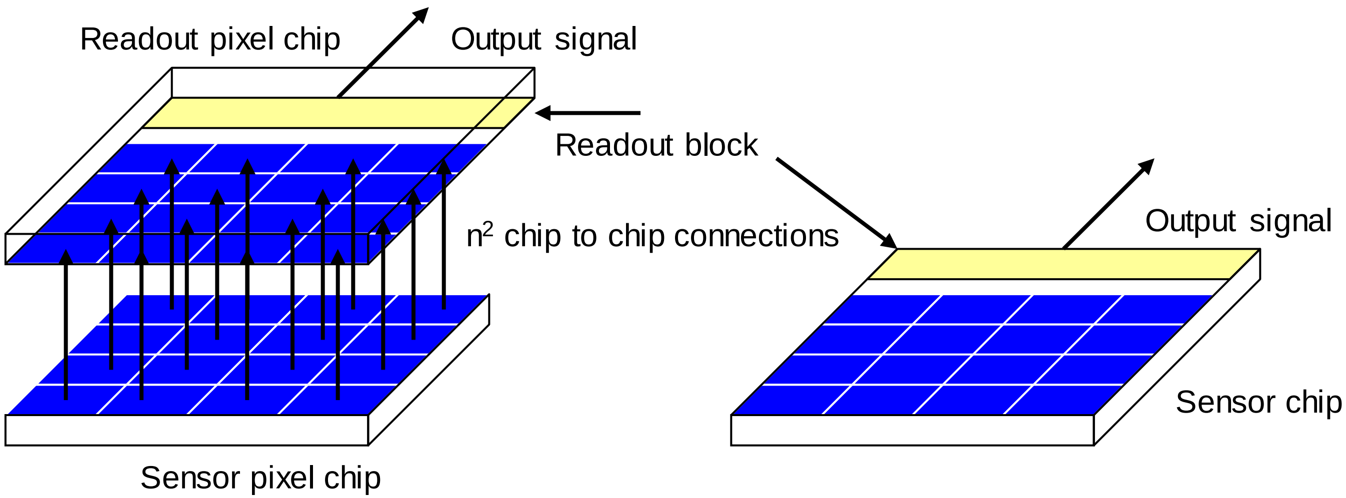
Monolithic pixel sensors

Ivan Perić

- Monolithic pixel sensor
- Monolithic - formed from a single crystal
- Pixel sensor - segmented detector of visible light or radiation



Hybrid detector

Monolithic detector

Overview of monolithic sensors

- Monolithic pixel sensors – three classes
- 1) Pixel sensors implemented in commercial CMOS technologies
- 2) Special monolithic technologies (DEPFETs, SOI-detectors)
- 3) Monolithic sensors obtained by 3D integration

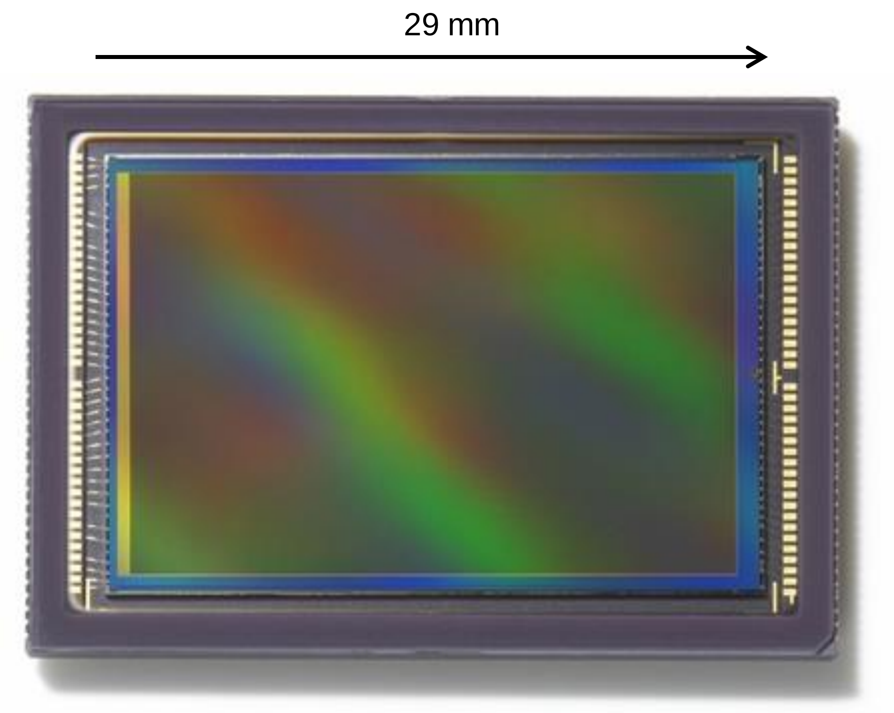
Commercial (C)MOS monolithic pixel sensors

(C)MOS monolithic sensors

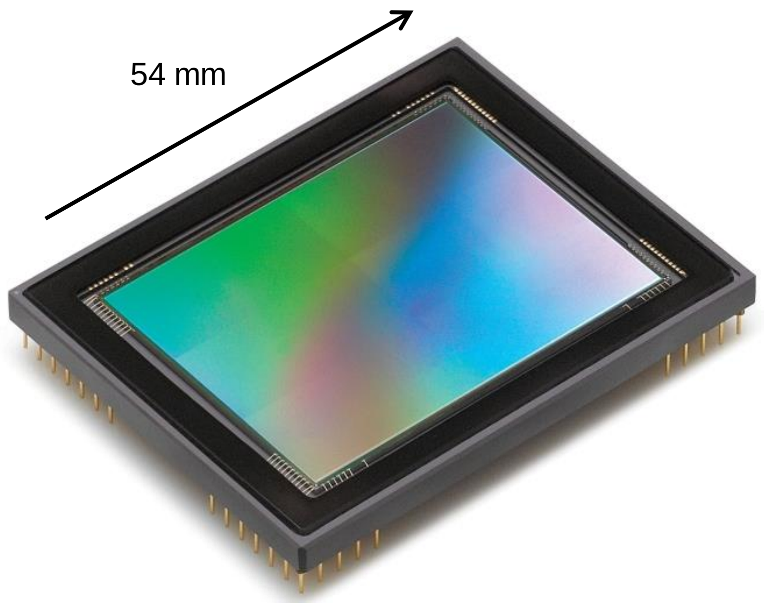
- The original application of CMOS sensors – consumer electronics
- Imaging sensors for digital cameras and mobile phones
- Such sensors be used for particle tracking, however…
- certain improvements are necessary
- Epi layer, hi-resistivity substrate, deep-n-well, use of *true* CMOS pixels
- Although implemented in CMOS technologies commercial imagers use only one type of transistor in pixels – (C)MOS

Phone with 41 M pixel sensor, 1.4um pixel size

- Imaging sensors for digital cameras and mobile phones
- Two basic types CMOS sensor and CCD

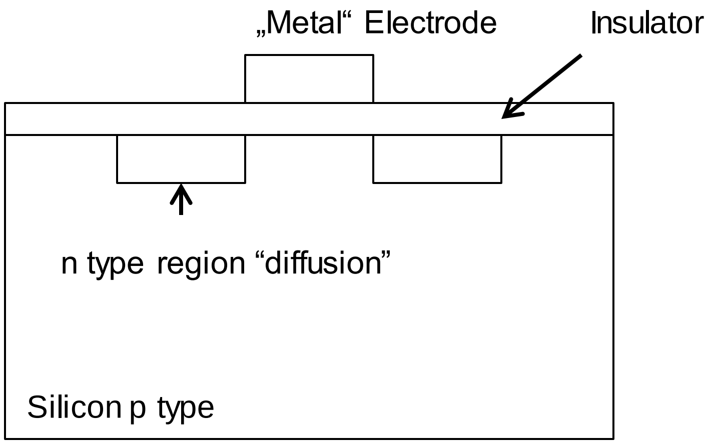


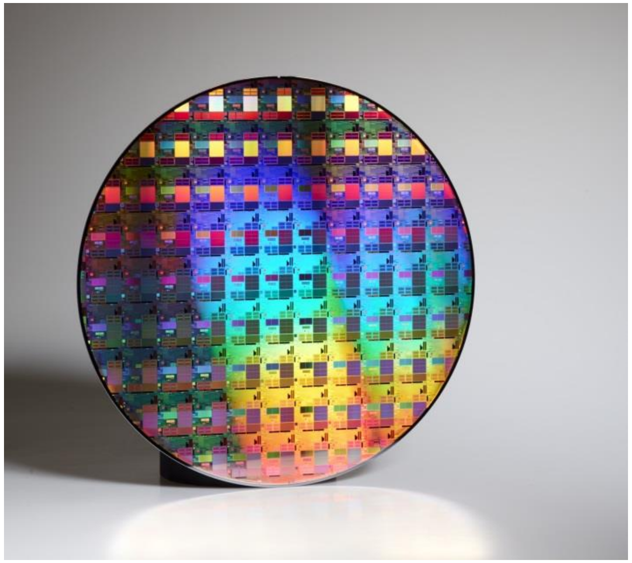
Canon 120 M pixels, 2um pixel size



Teledyne DALSA 60 M pixels CCD, 6um pixel size

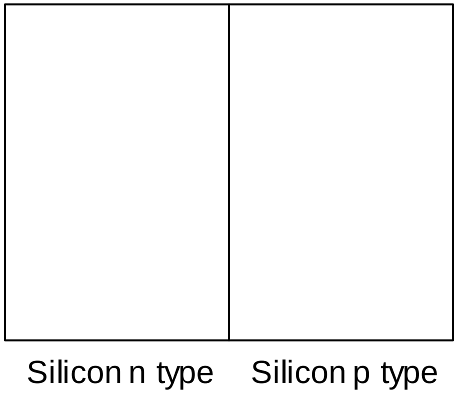
- MOS Technology – Integrated circuit technology based on Metal Oxide Semiconductor field effect transistors
- Field effect transistor invented in 1925 by Julius Lilienfeld
- Finally realized in 1960s

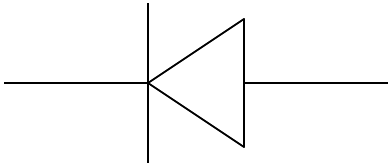


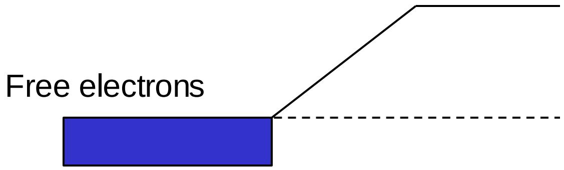


Samsung 32nm process

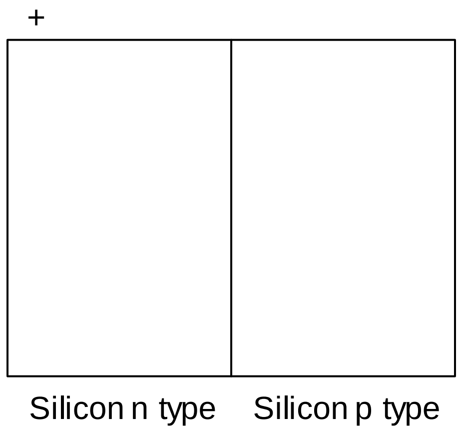
- The simplest building element – PN junction
- N-diffusion – potential valley for electrons
- P-substrate – potential barrier for electrons

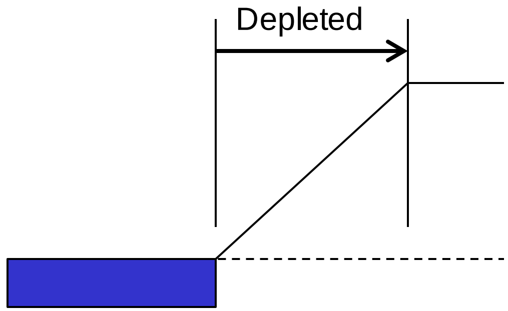




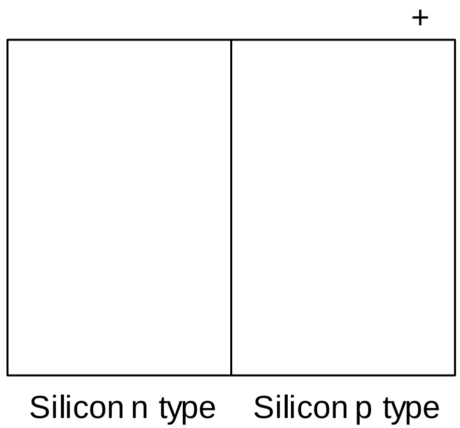


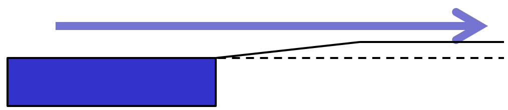
- Reversely biased – large depleted layer
- Detector mode





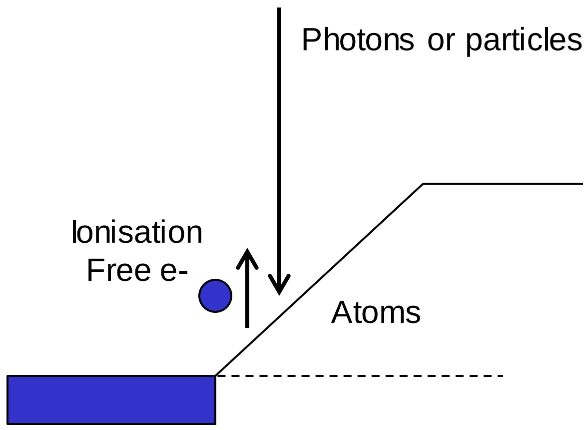
- Directly biased – current flow
- Not used in MOS circuits



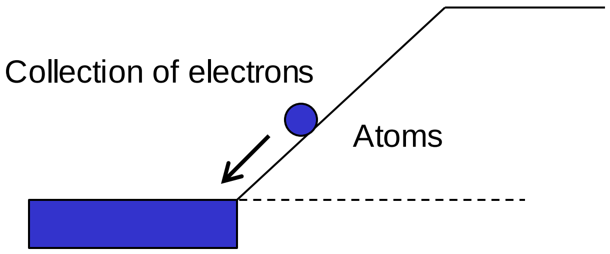


PN junction as sensor of radiation

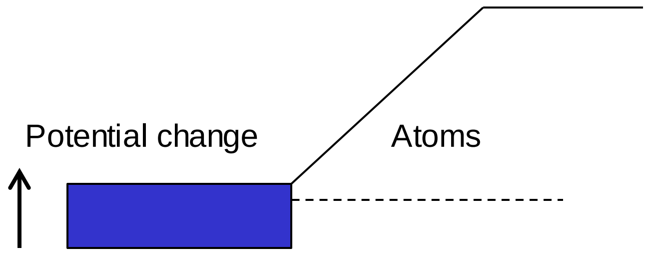
- PN junction as sensor
- 1. step - ionization



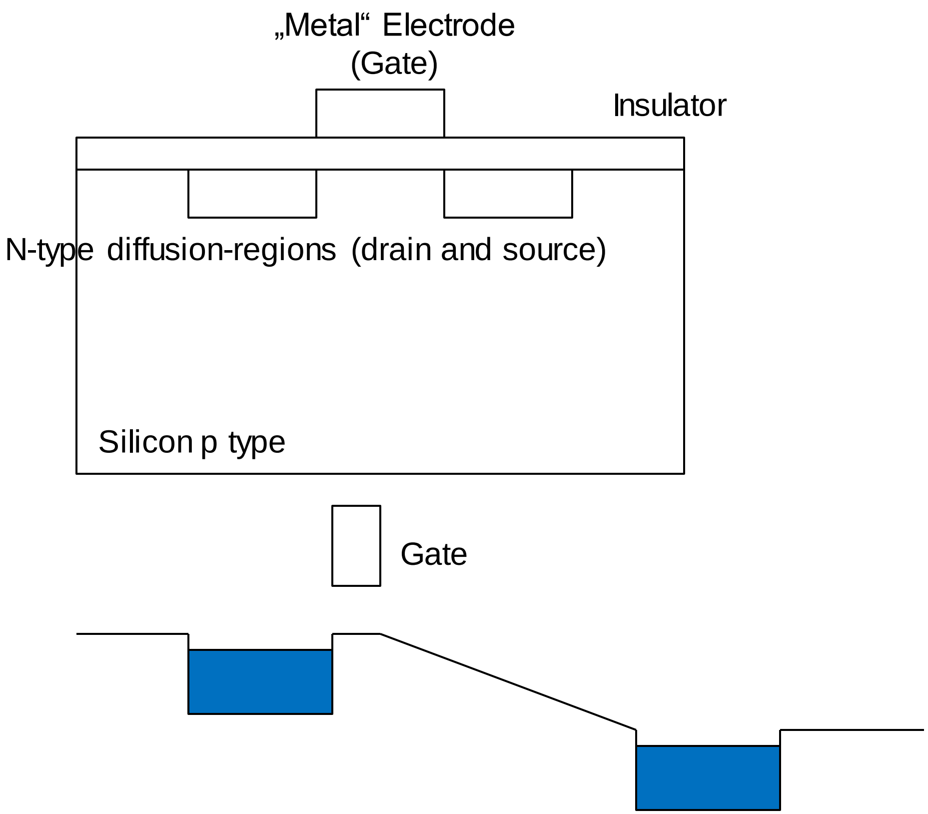
- PN junction as sensor
- 2. step – charge collection
- Two possibilities for charge collection – drift (through E-force) and by diffusion (density gradient)



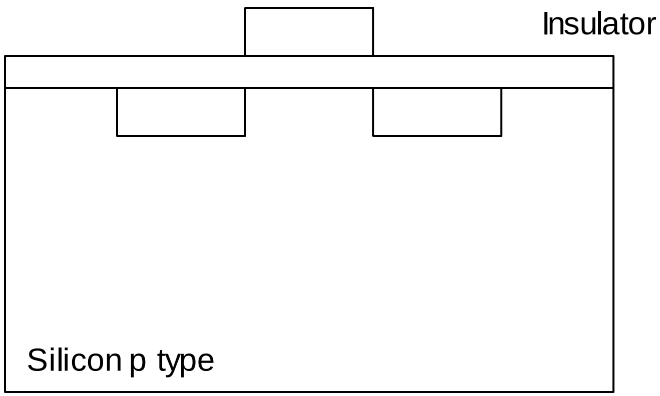
- PN junction as sensor
- 3. step – charge to voltage conversion
- Collection of the charge signal leads to the potential change

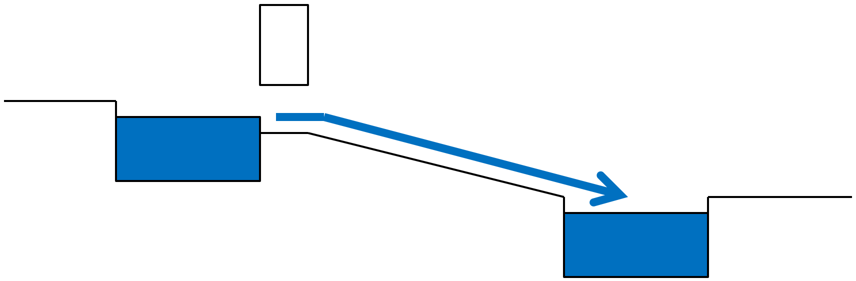


- The basic element – MOS field effect transistor
- Potential barrier between the transistor contacts can be controlled by the voltage applied at gate electrode
- N-channel MOS - NMOS

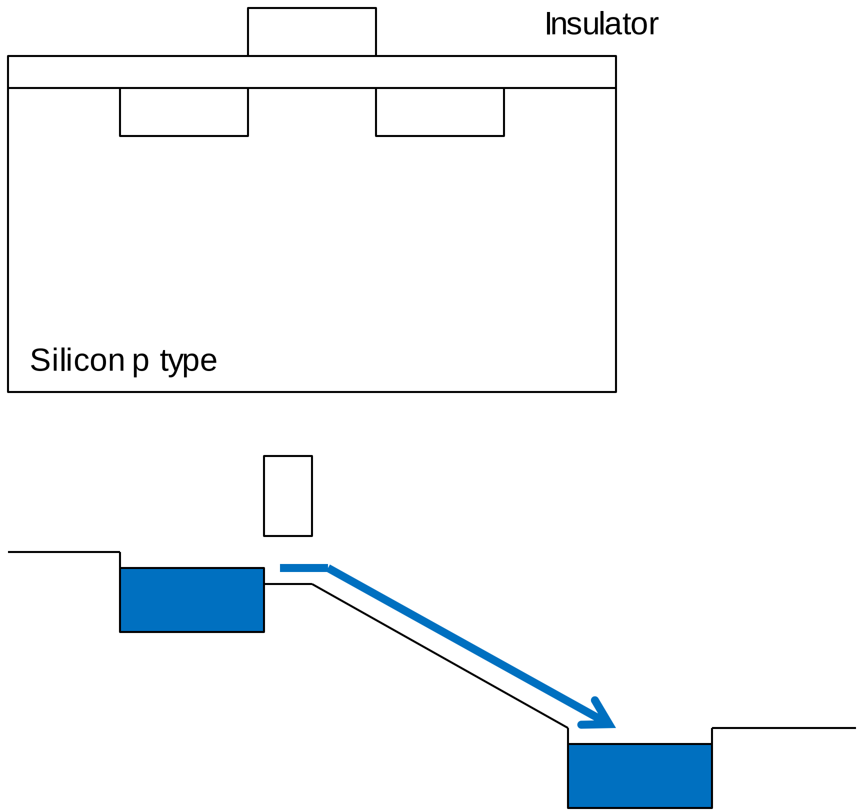


- Current flow controlled by gate-bulk voltage

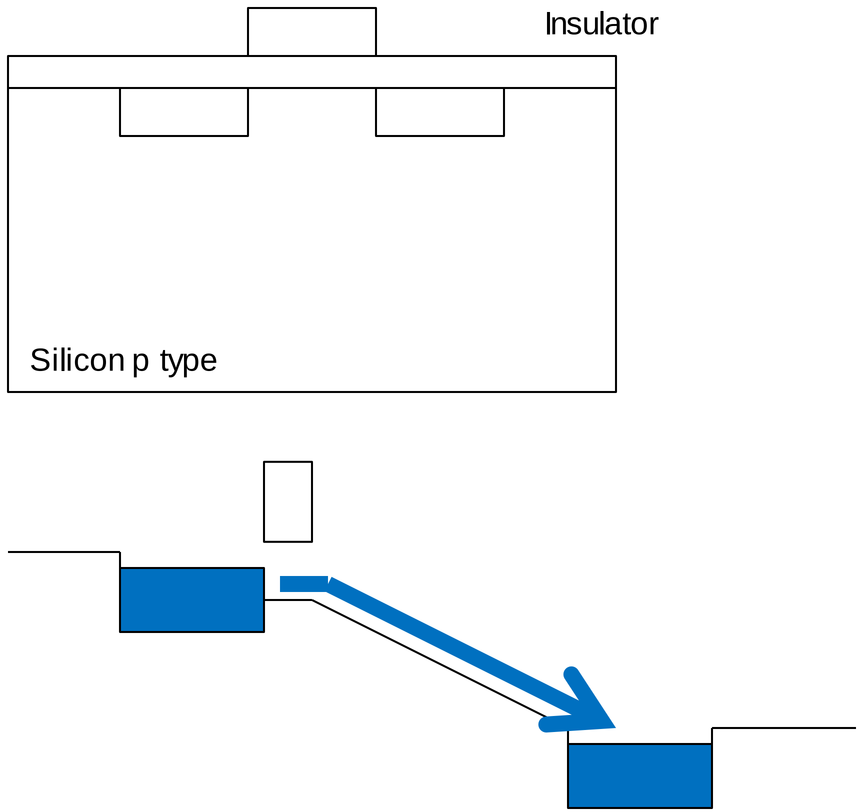




- Interesting: Current flow does not depend on drain voltage

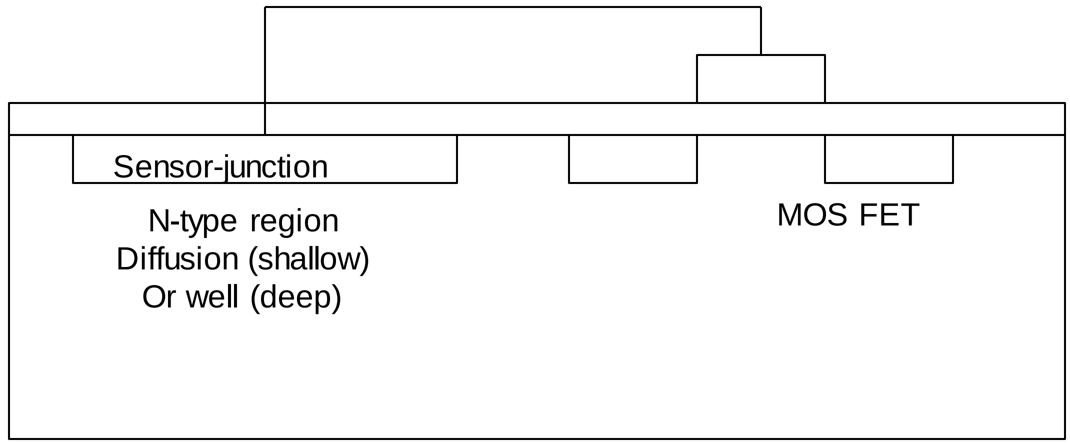


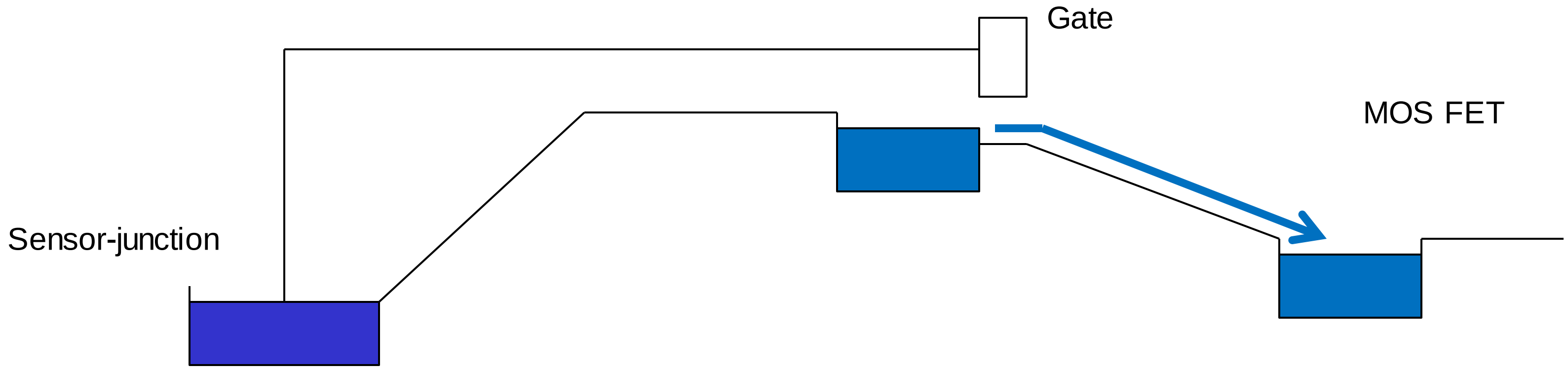
- Current flow controlled *only* by gate-bulk voltage



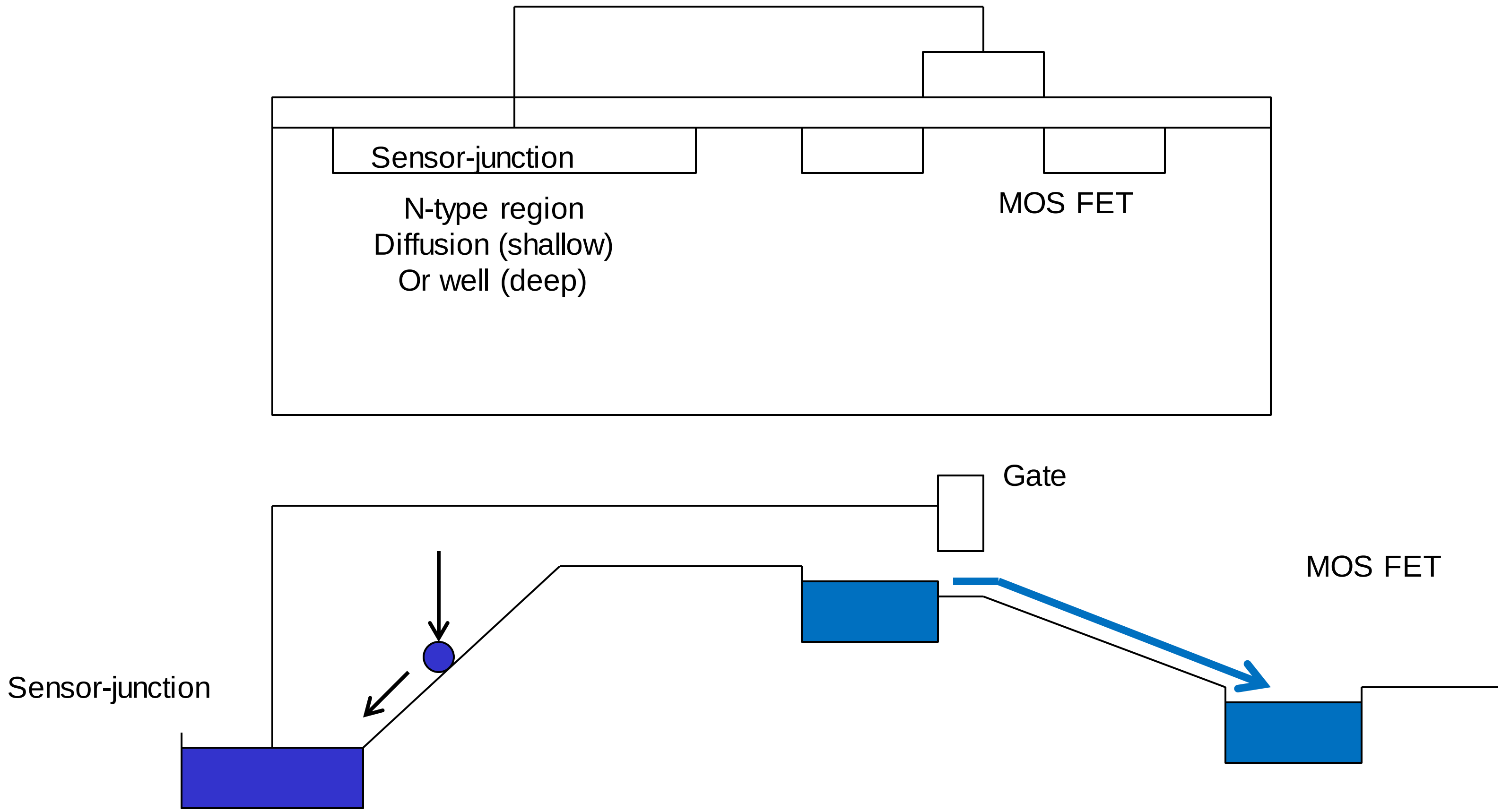
CMOS pixel

- Pixel sensor in MOS technology

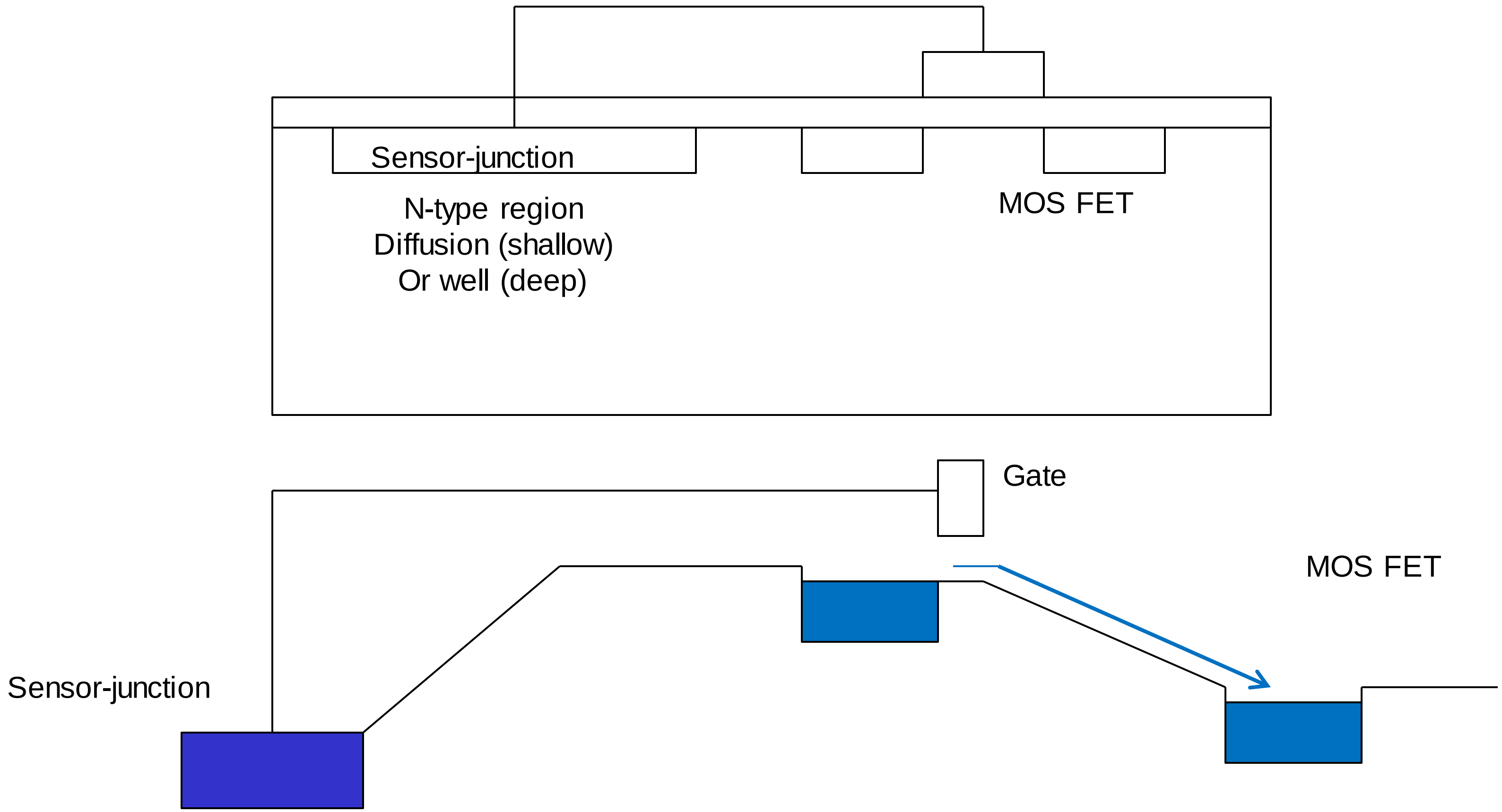




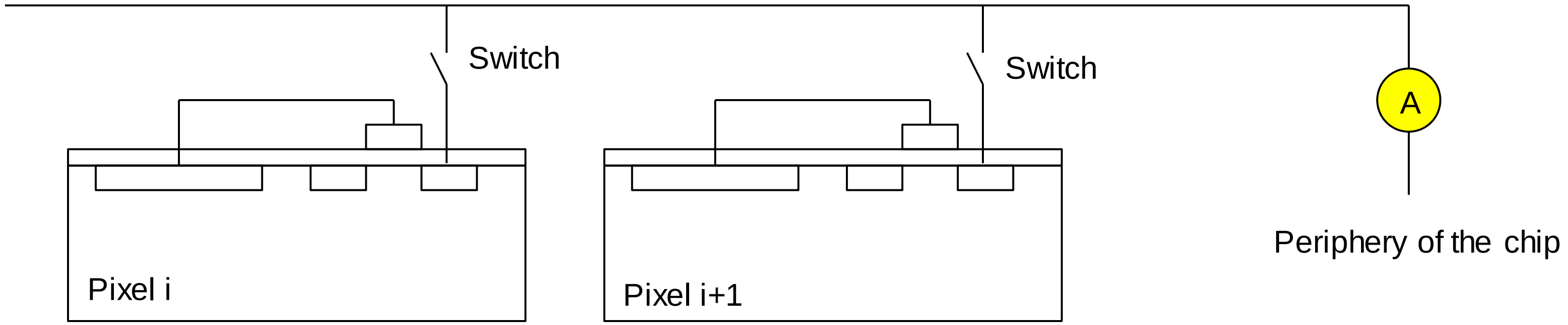
- N in P diode acts as sensor element – signal collection electrode

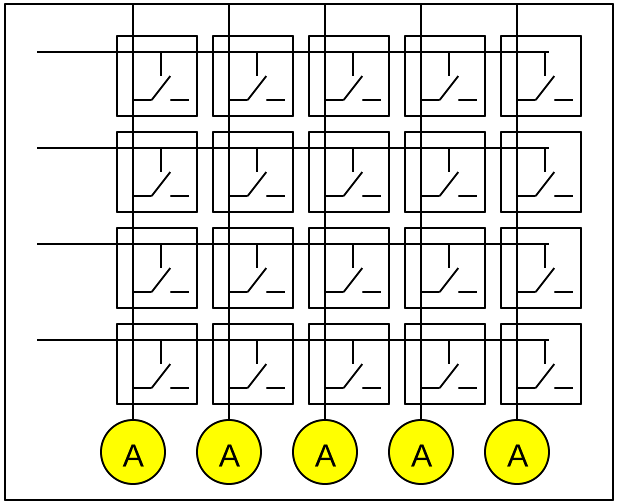


- Charge generated by ionization is collected by the N-diffusion
- This leads to the potential change of the N-diffusion
- The potential change is transferred to transistor gate – it modulates the transistor current



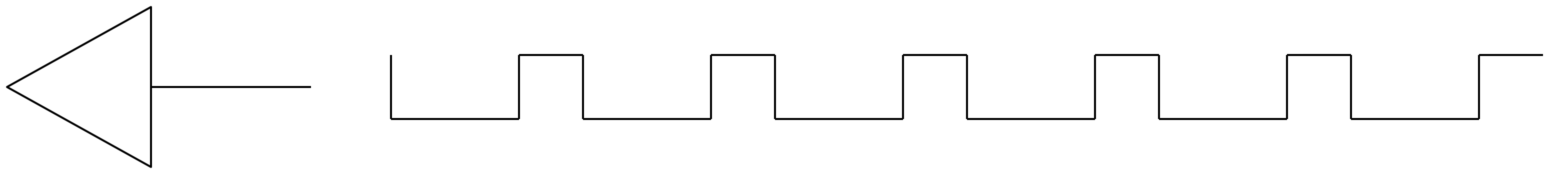
- Readout principle: Many pixels (usually one row) share one readout line
- Additional MOSFET used as switch
- The readout lines lead to the electronics at the chip periphery that does signal processing
- Monolithic detector – signal processing on the chip - fast



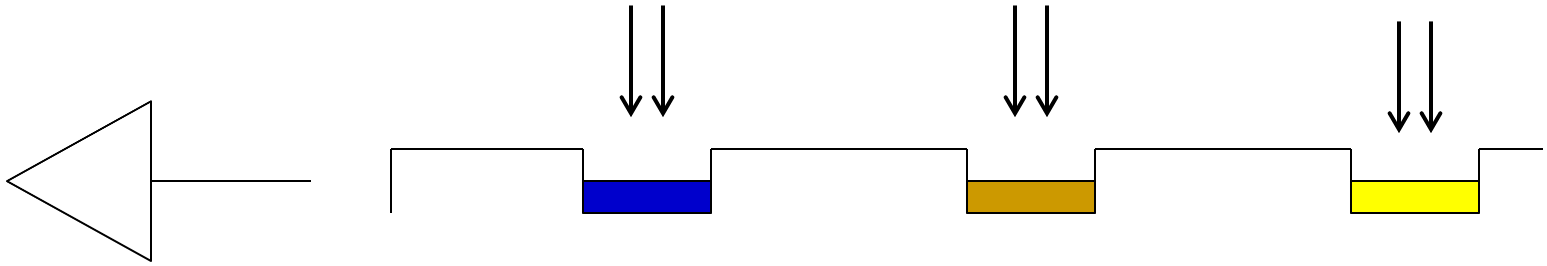


CCD principle

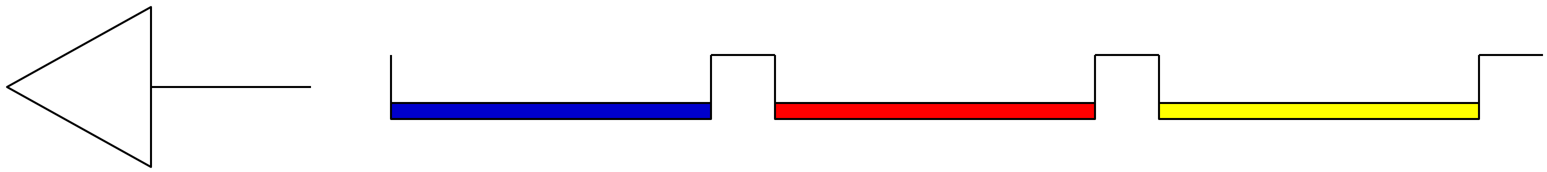
- CCD principle as comparison
- Potential valleys and barriers in silicon formed by proper doping.
- They are controlled applying voltages on metal electrodes



- Illumination, ionization and charge collection

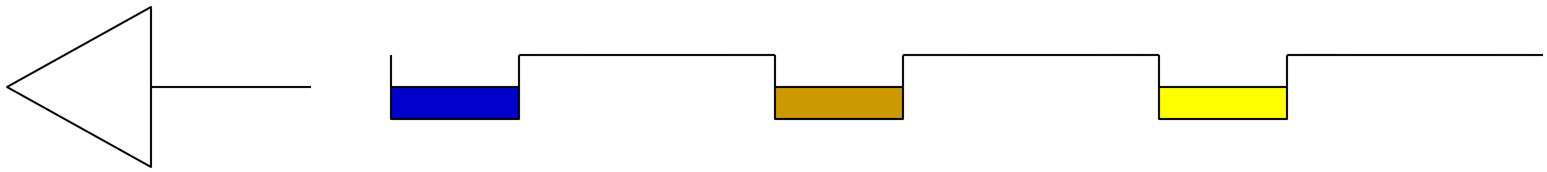


- Shifting of the charge
- Two voltage pulses are used to raise and lower the barriers

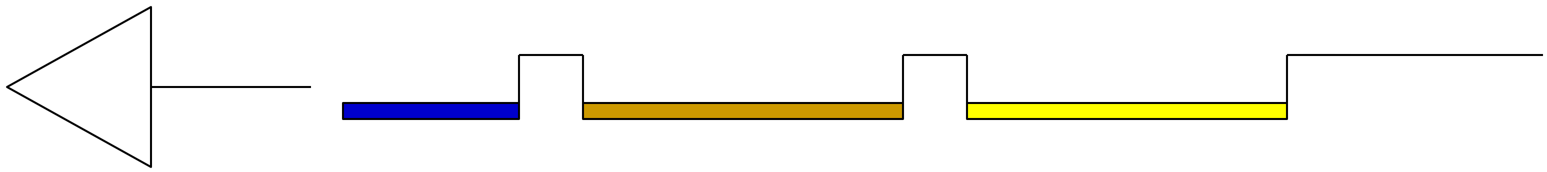


CCD principle

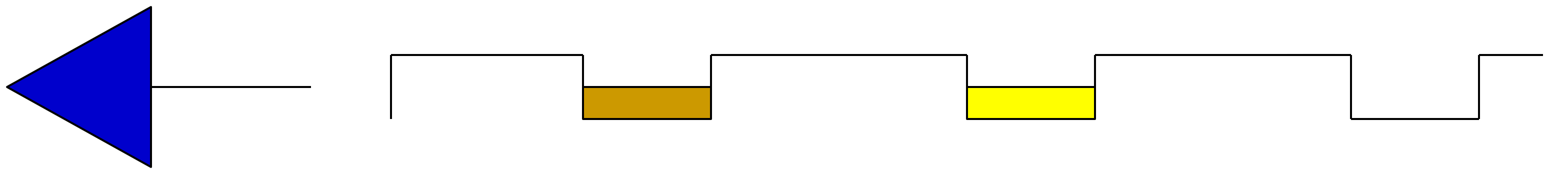
- Shifting of the charge

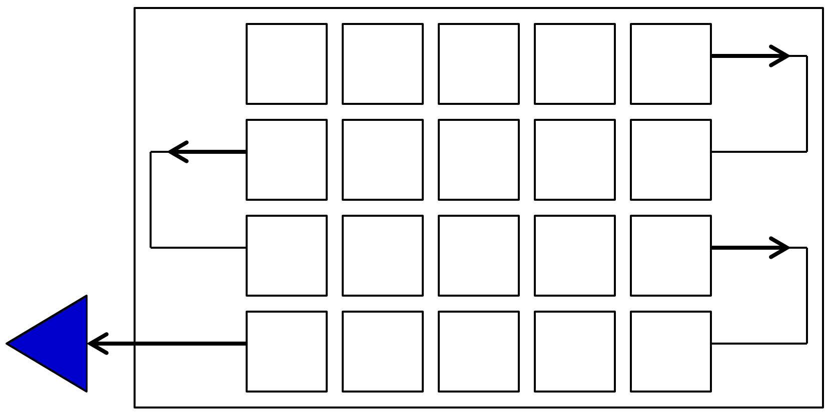


- Shifting of the charge



- Charge signals are shifted to the external amplifier
- No conversion to voltage occurs
- Amplification and signal processing on separated chip
- Slow readout

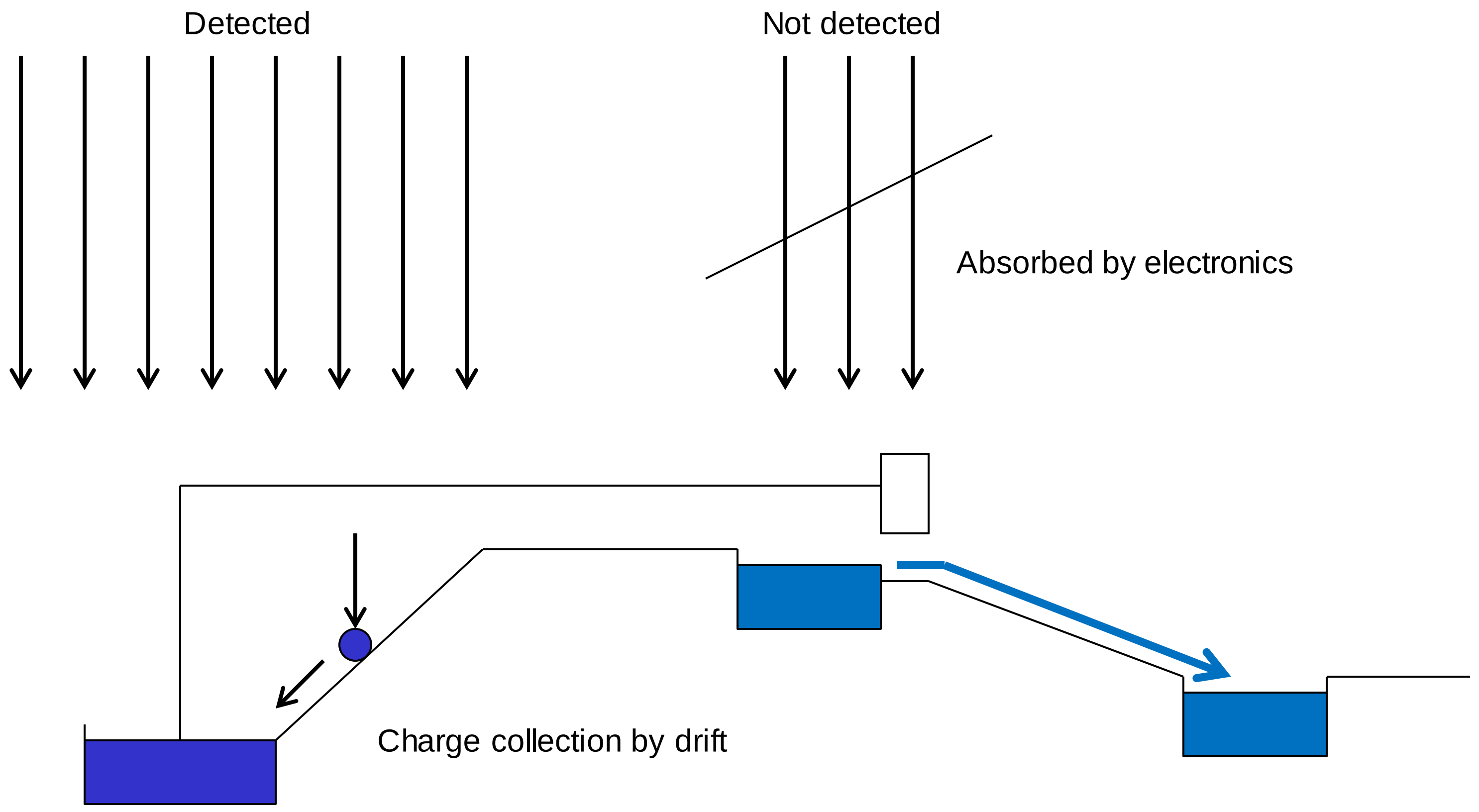




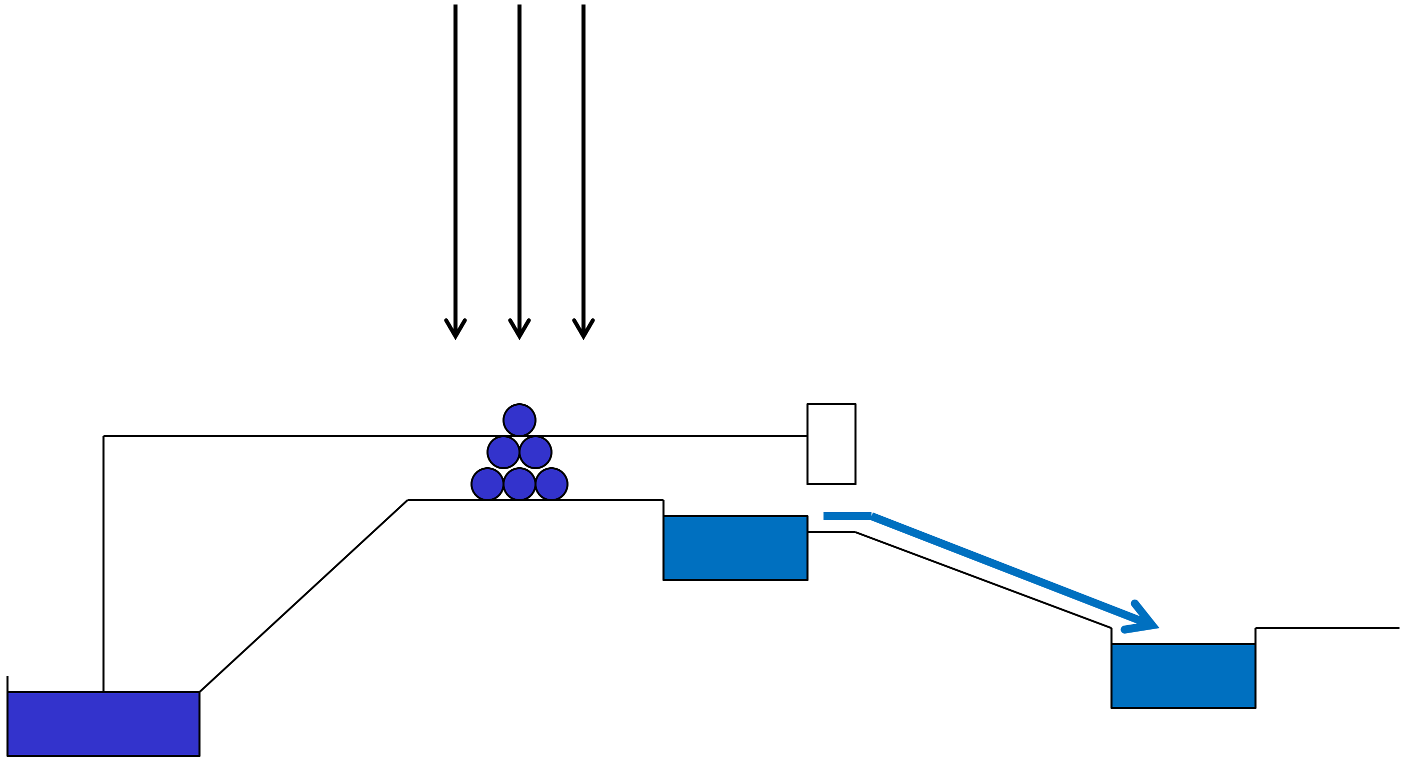
(C)MOS monolithic pixel sensors for particle tracking

CMOS sensors for particle tracking

- Can CMOS structure be used for detection of high energy particles in particle tracking?
- Yes, but fill factor is an issue – ratio of the sensitive versus insensitive area

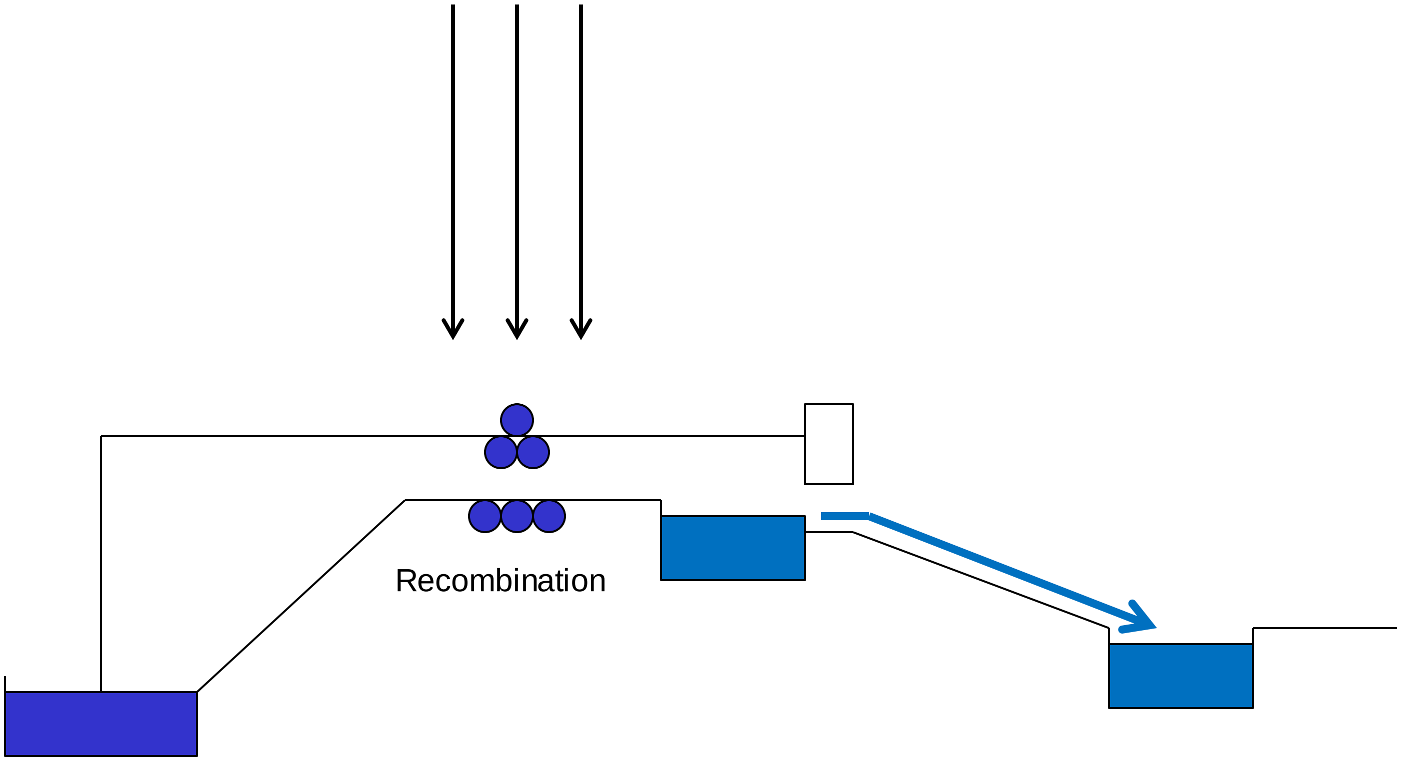


- Partial signal collection in the regions without E-field

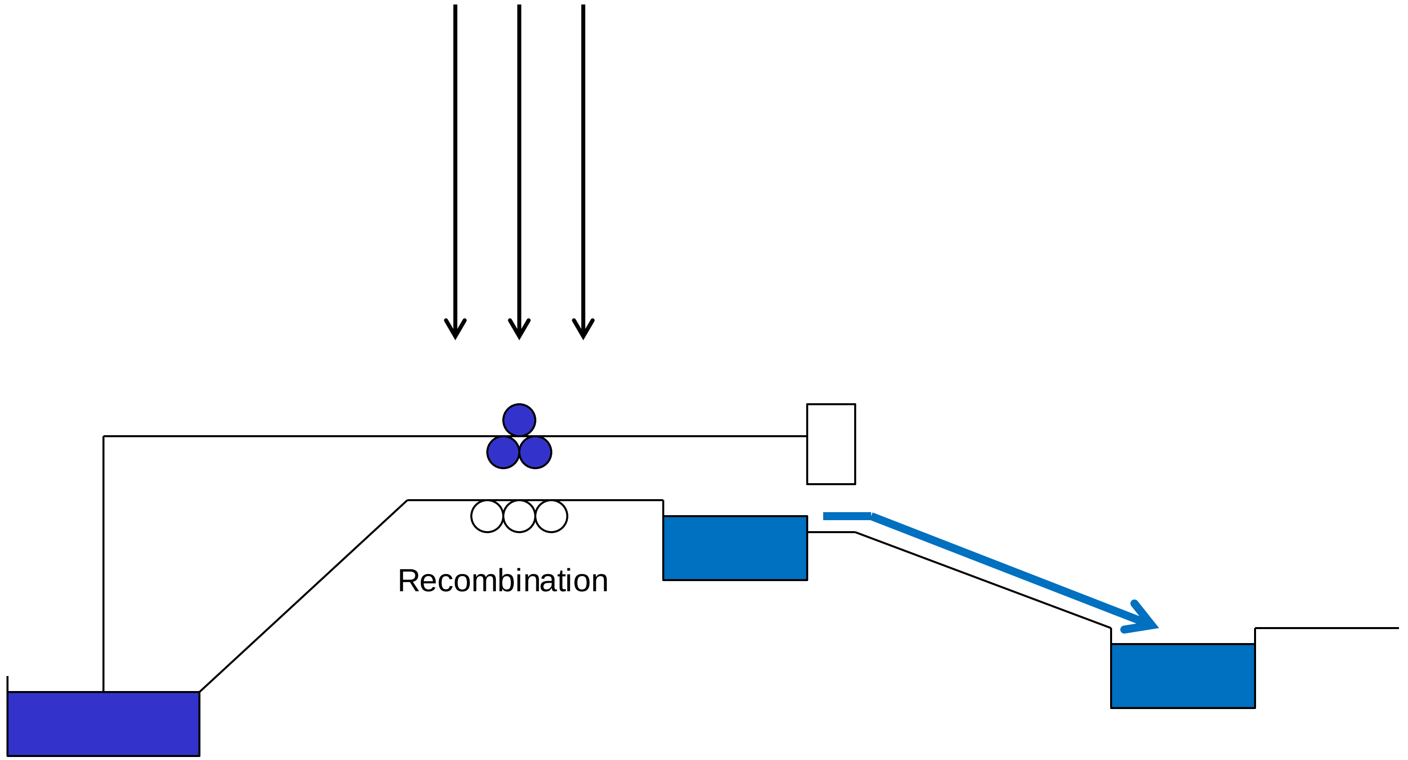


Fill-factor

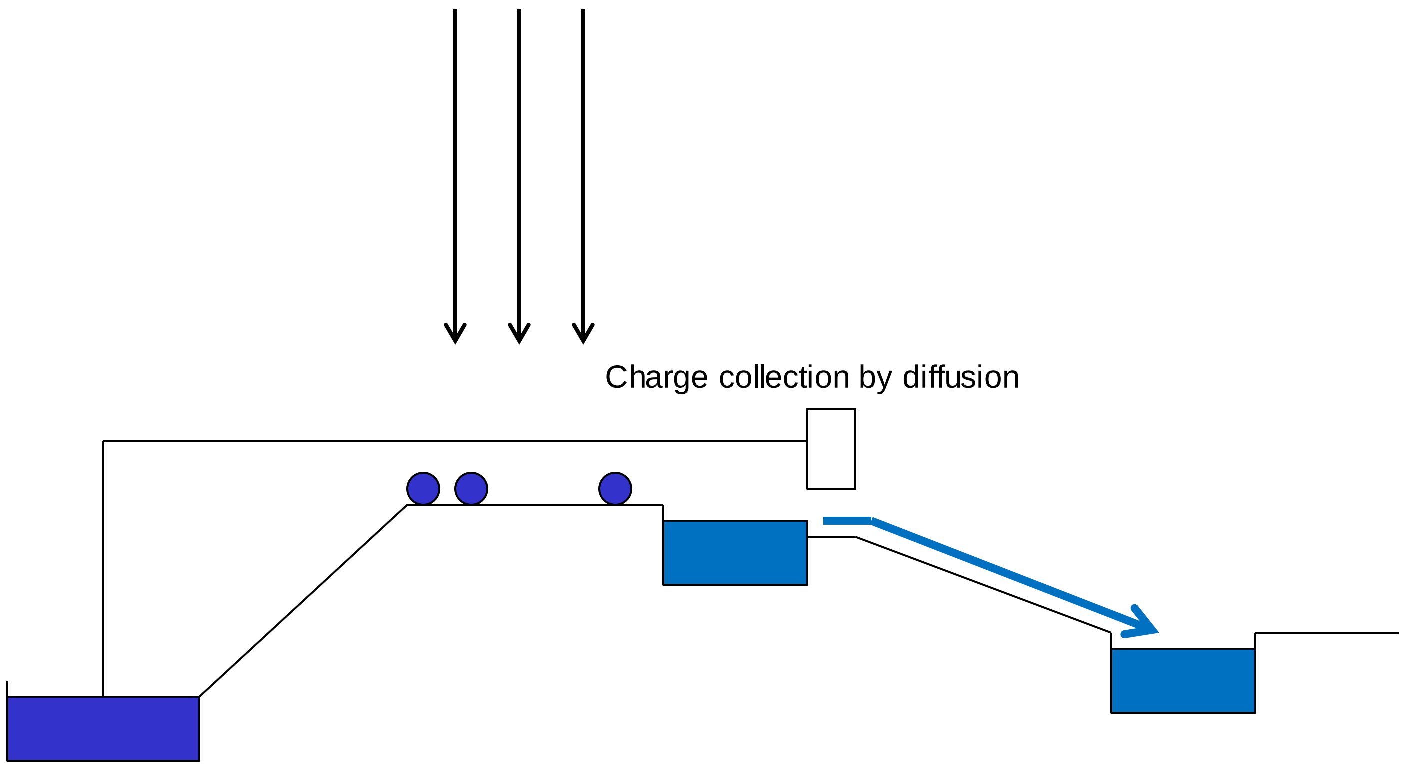
- Partial signal collection in the regions without E-field



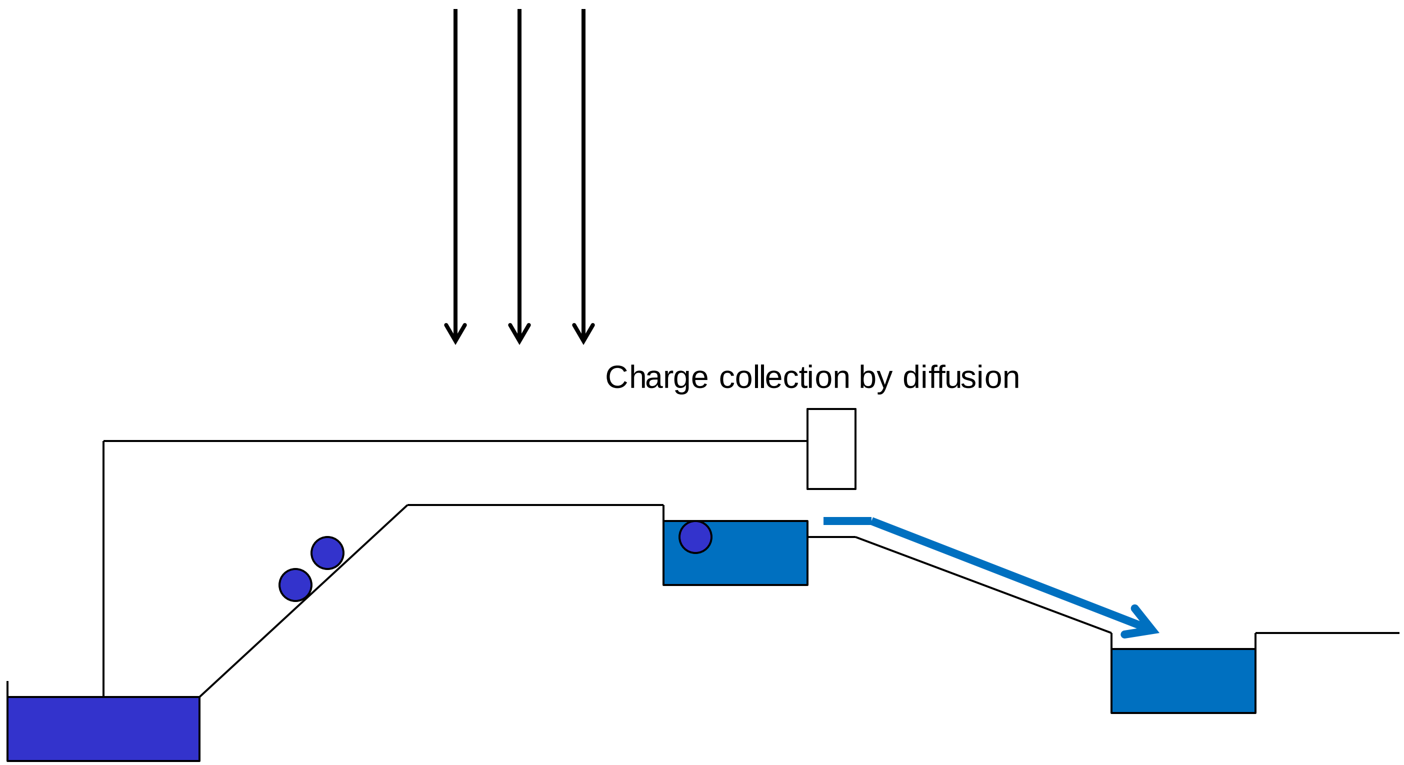
- Partial signal collection in the regions without E-field



- Partial signal collection in the regions without E-field

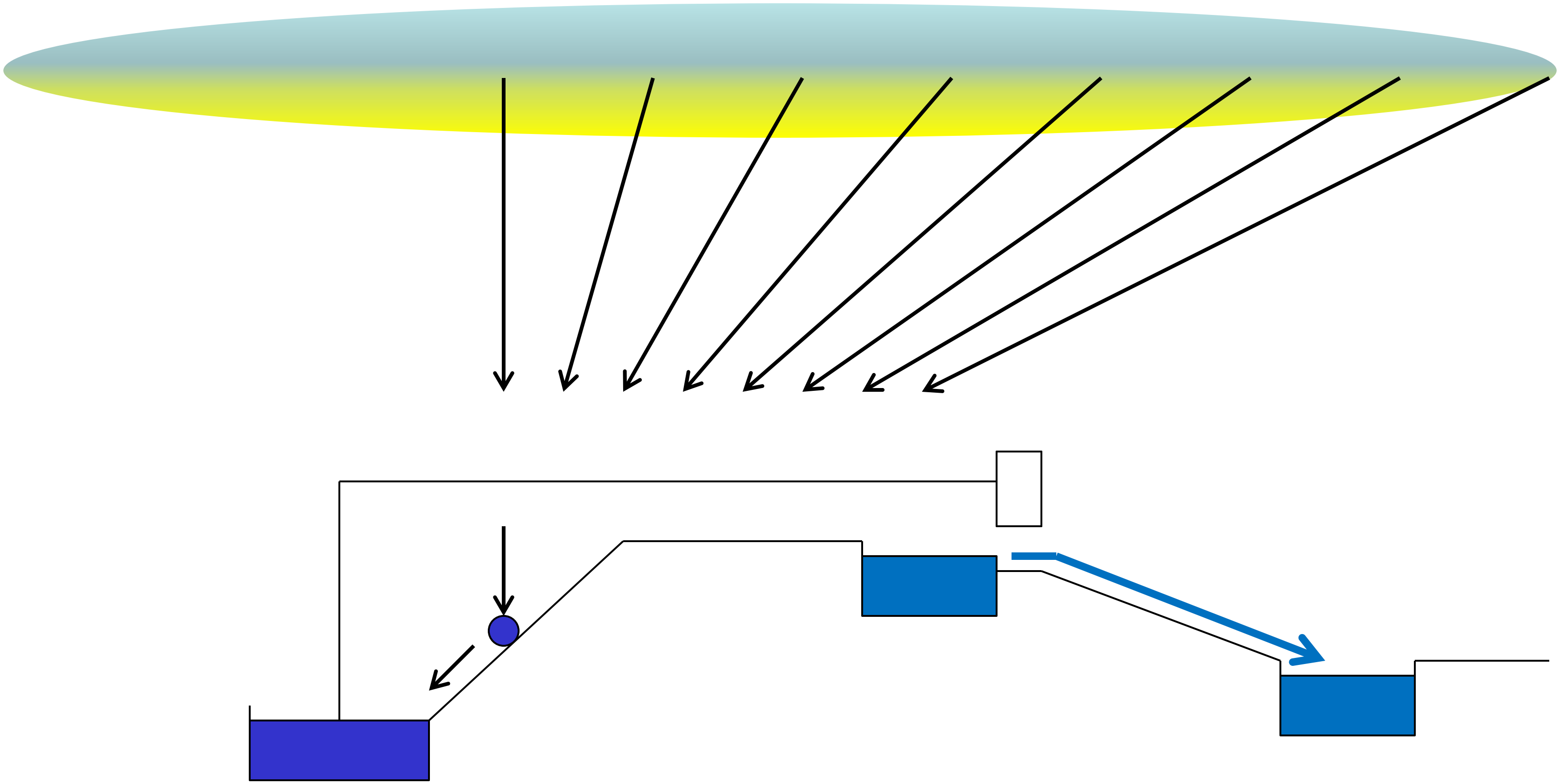


- Partial signal collection in the regions without E-field



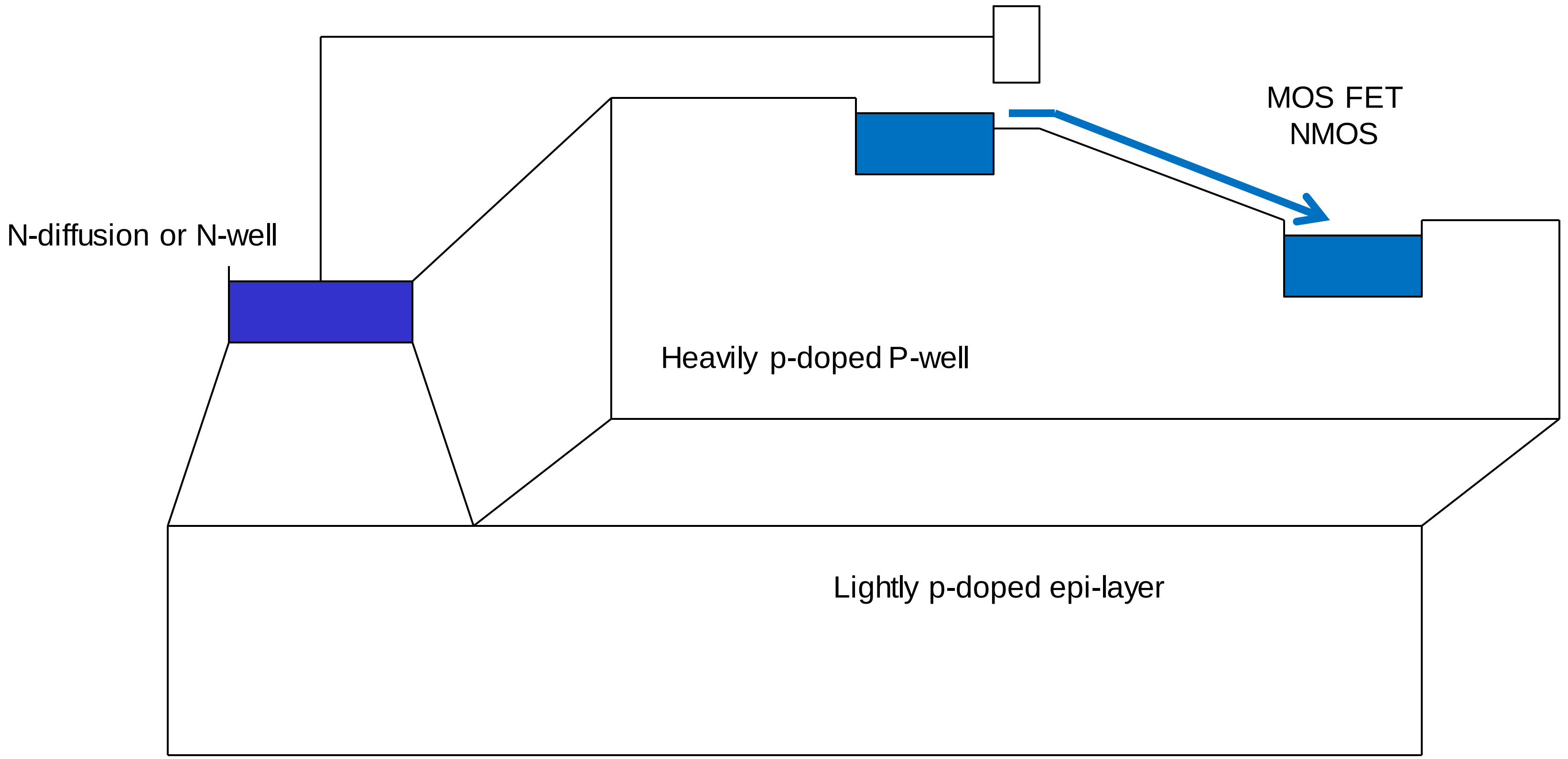
Fill-factor

- In the case visible light imaging, the insensitive regions do not impose a serious problem
- Light can be focused by lenses
- Exposure time can be increased
- In the case of particle tracking, any insensitive region should be avoided

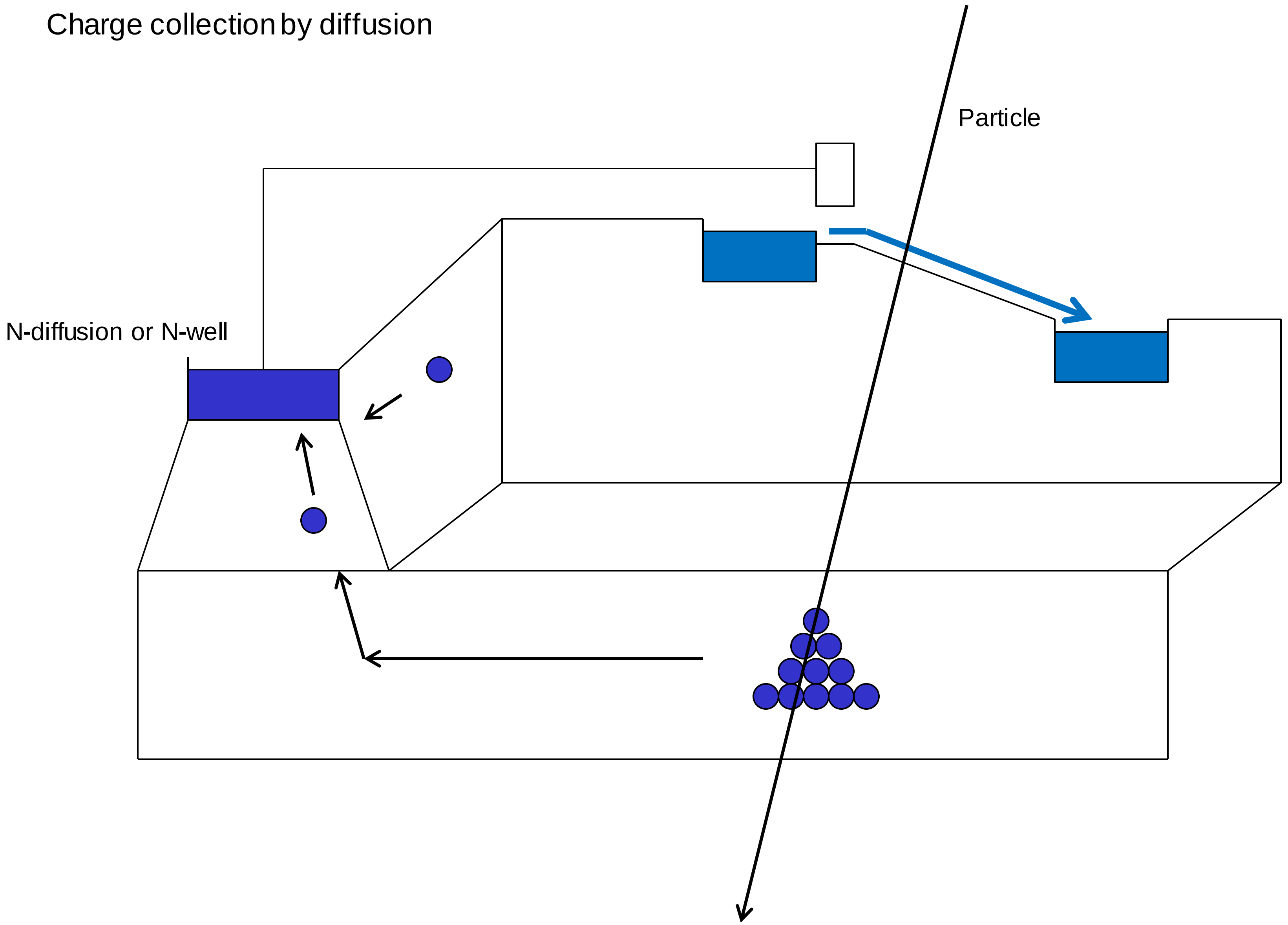


MOS pixel sensor with 100% fill factor

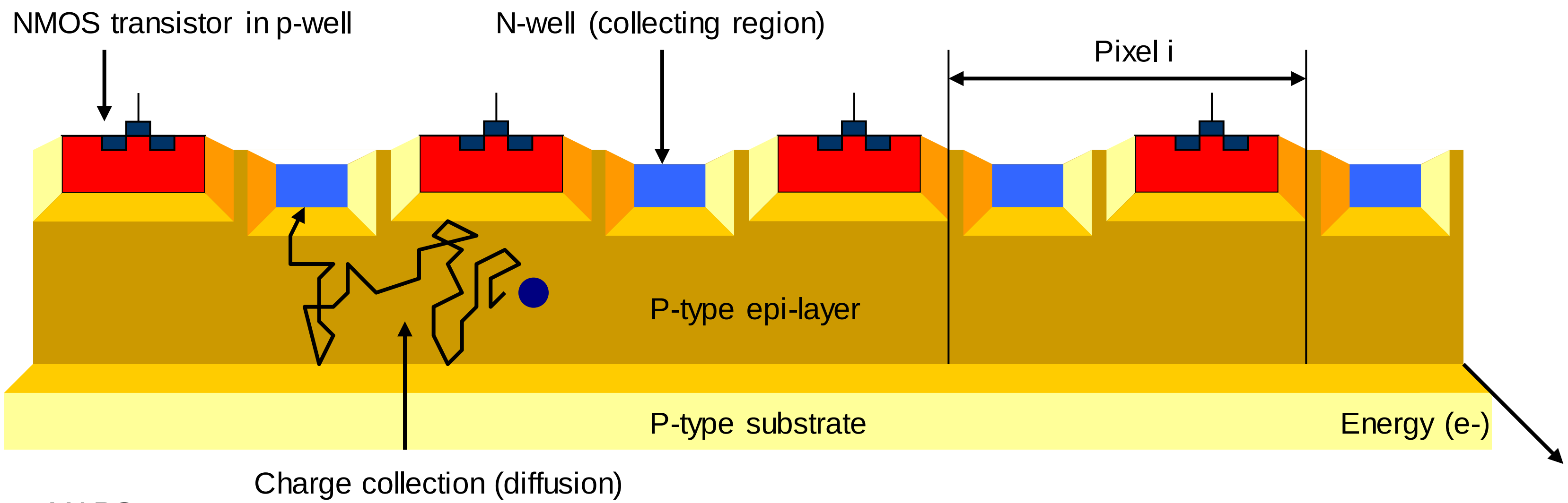
- MOS sensor with 100% fill-factor
- Based on epi-layer
- Monolithic active pixel sensor - “MAPS”



- Ionization in the epi-layer
- Charge collection by diffusion



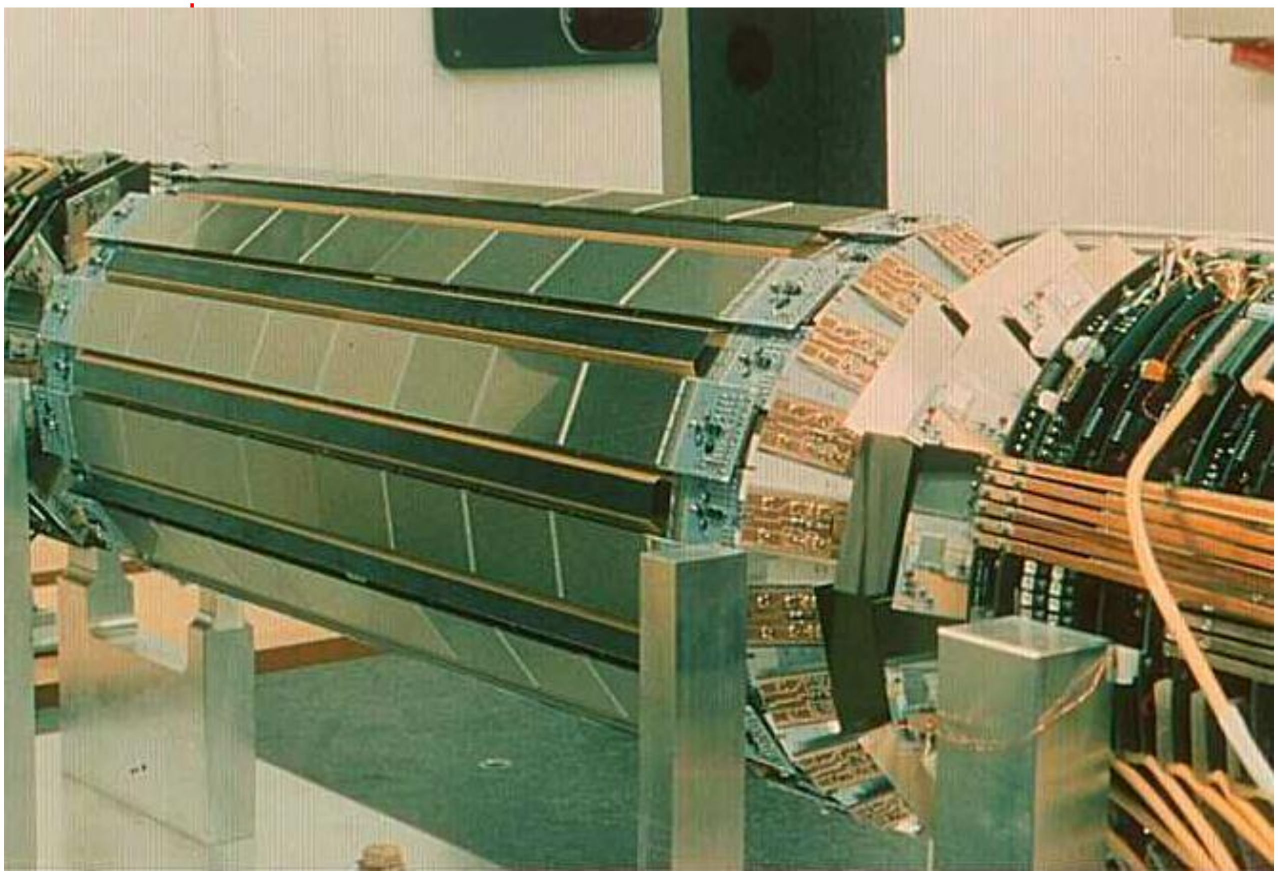
MAPS


NMOS transistor in p-well
N-well (collecting region)
Pixel i
P-type epi-layer
P-type substrate
Energy (e-)
Charge collection (diffusion)

MAPS

MAPS

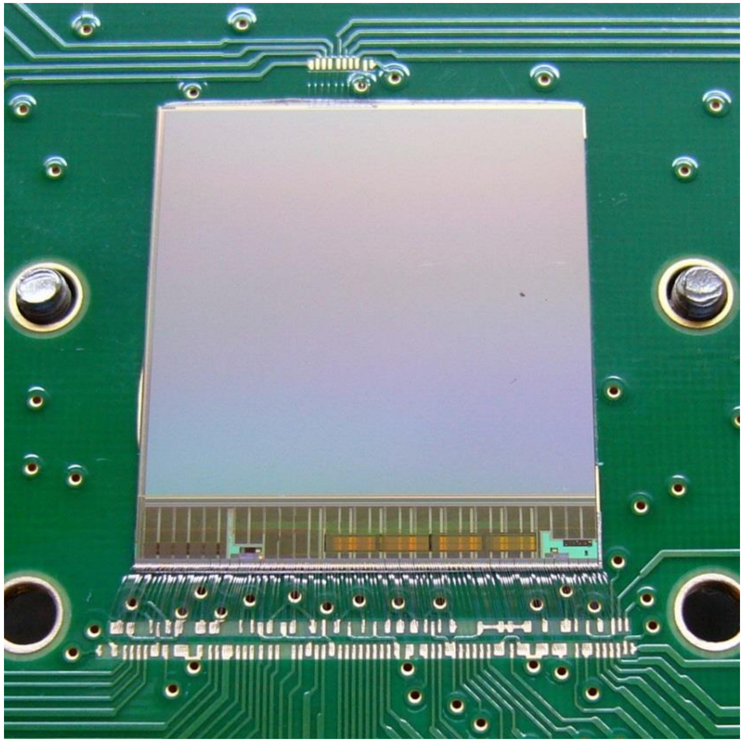
- Many institutes are developing MAPS, for instance: IPHC Strasbourg (PICSEL group)
- Family of MIMOSA chips
- Applications:, STAR-detector (RHIC Brookhaven), Eudet beam-telescope and ALICE inner tracker



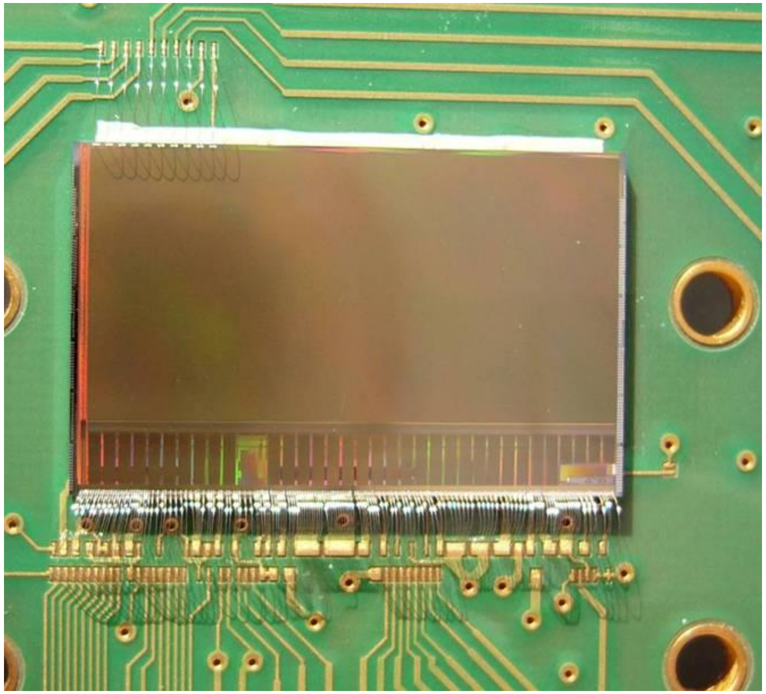
http://www.iphc.cnrs.fr/Monolithic-Active-Pixel-Sensors.html

MAPS

- Although based on simple MAPS principle – epi layer and NMOS electronics – MIMOSA chips use more complex pixel electronics
- Continuous reset and double correlated sampling



Ultimate chip for STAR



MIMOSA 26 for Eudet telescope

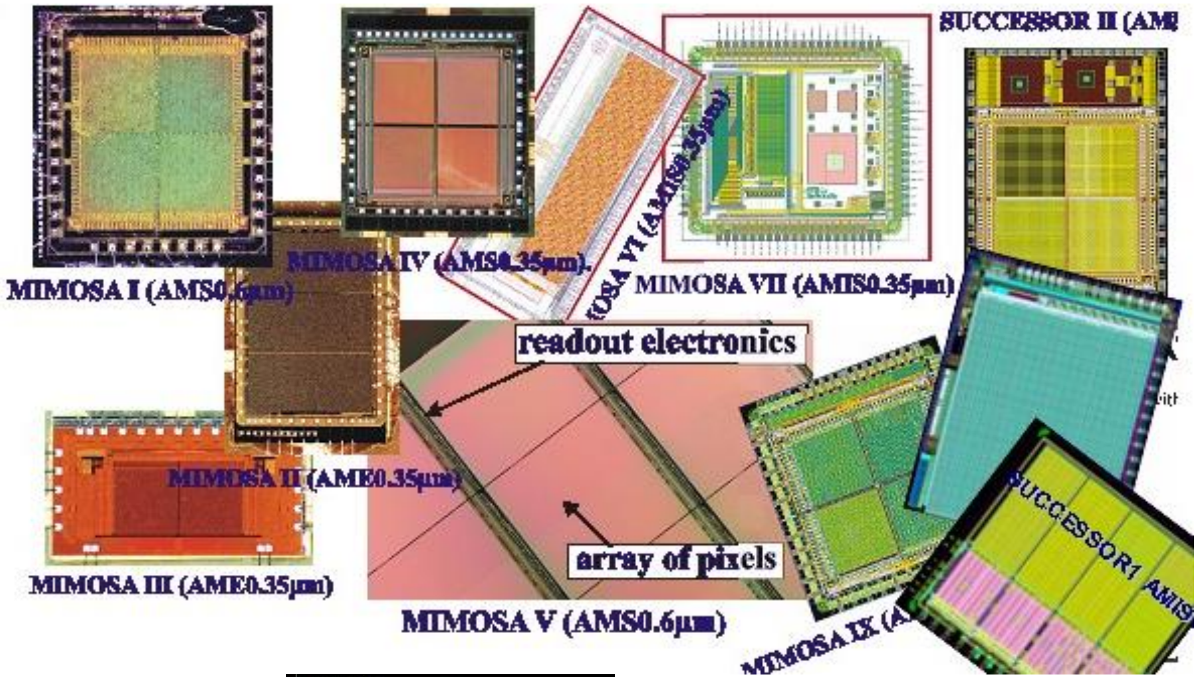
http://www.iphc.cnrs.fr/Monolithic-Active-Pixel-Sensors.html

MAPS

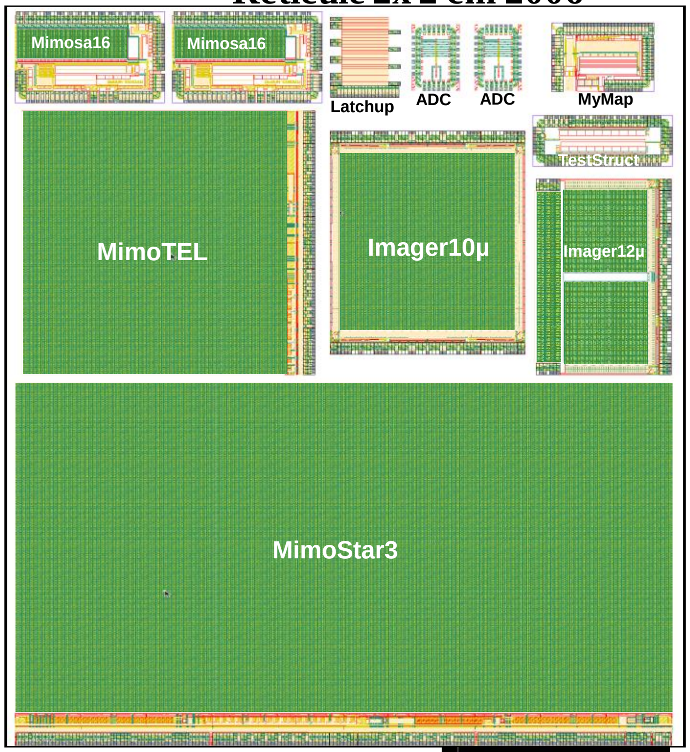
Charge collection & technology studies – simple demonstrators

Real size prototype - yield studies

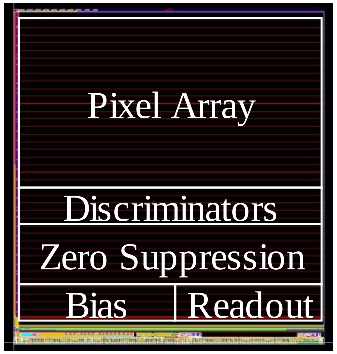
1999

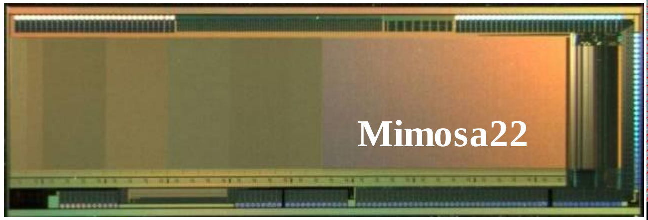


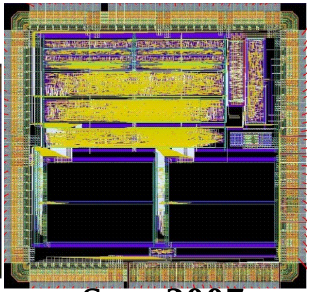
Reticule 2x 2 cm 2006



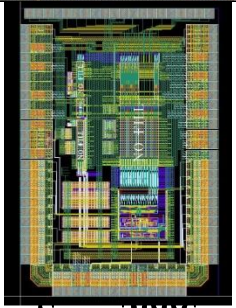
Production







Suze 2007



Sara 2006

2008

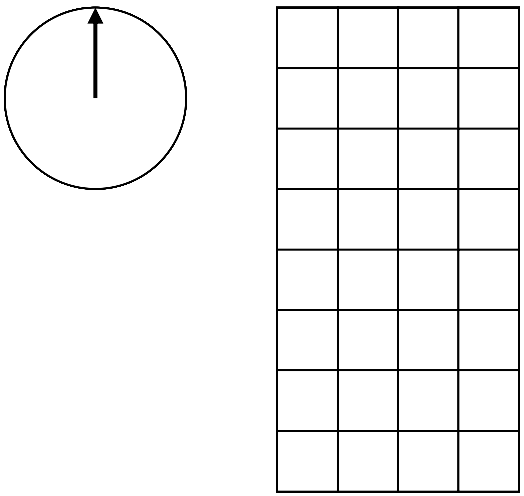
2007

Final circuits – sub-blocs integration

Data compression - digitization

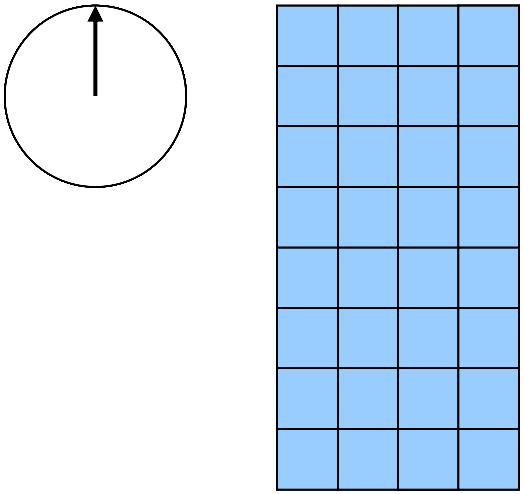
Advanced CMOS pixel sensors with intelligent pixels

Frame readout



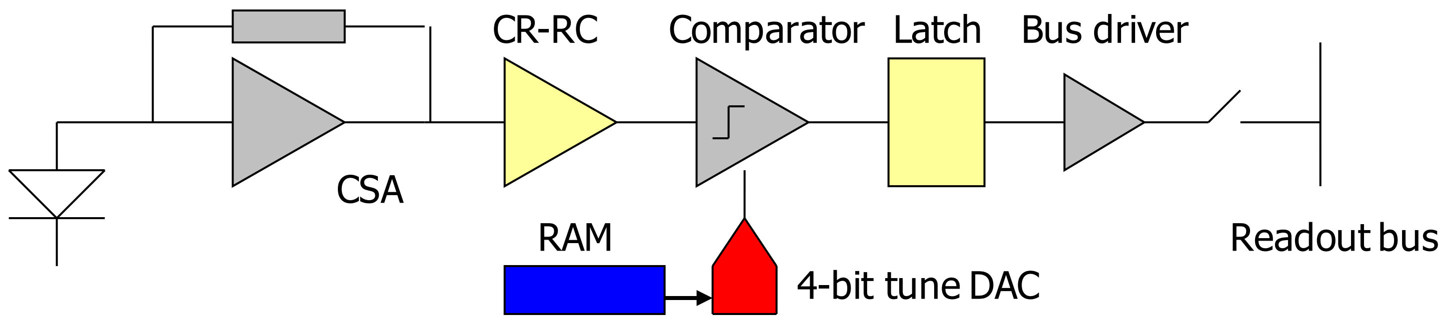
- Simple pixels
- Signal and leakage current is collected
- No time information is attached to hits
- The whole frames are readout

☺ Small pixels
☺ Low power consumption
☺ Slow readout

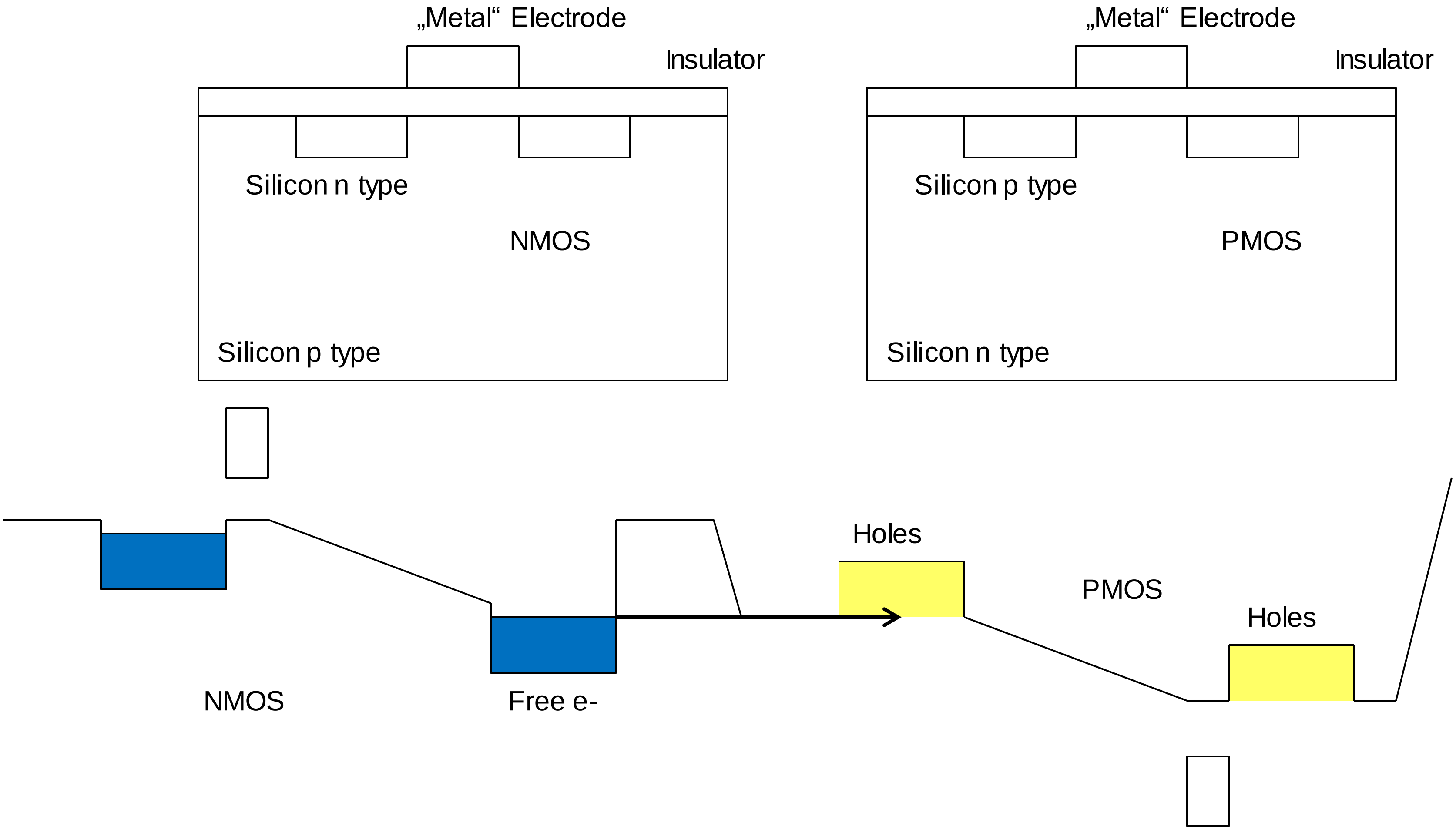


- Intelligent pixels
- FPN is tuned inside pixels
- Leakage current is compensated
- Hit detection on pixel level
- Time information is attached to hits

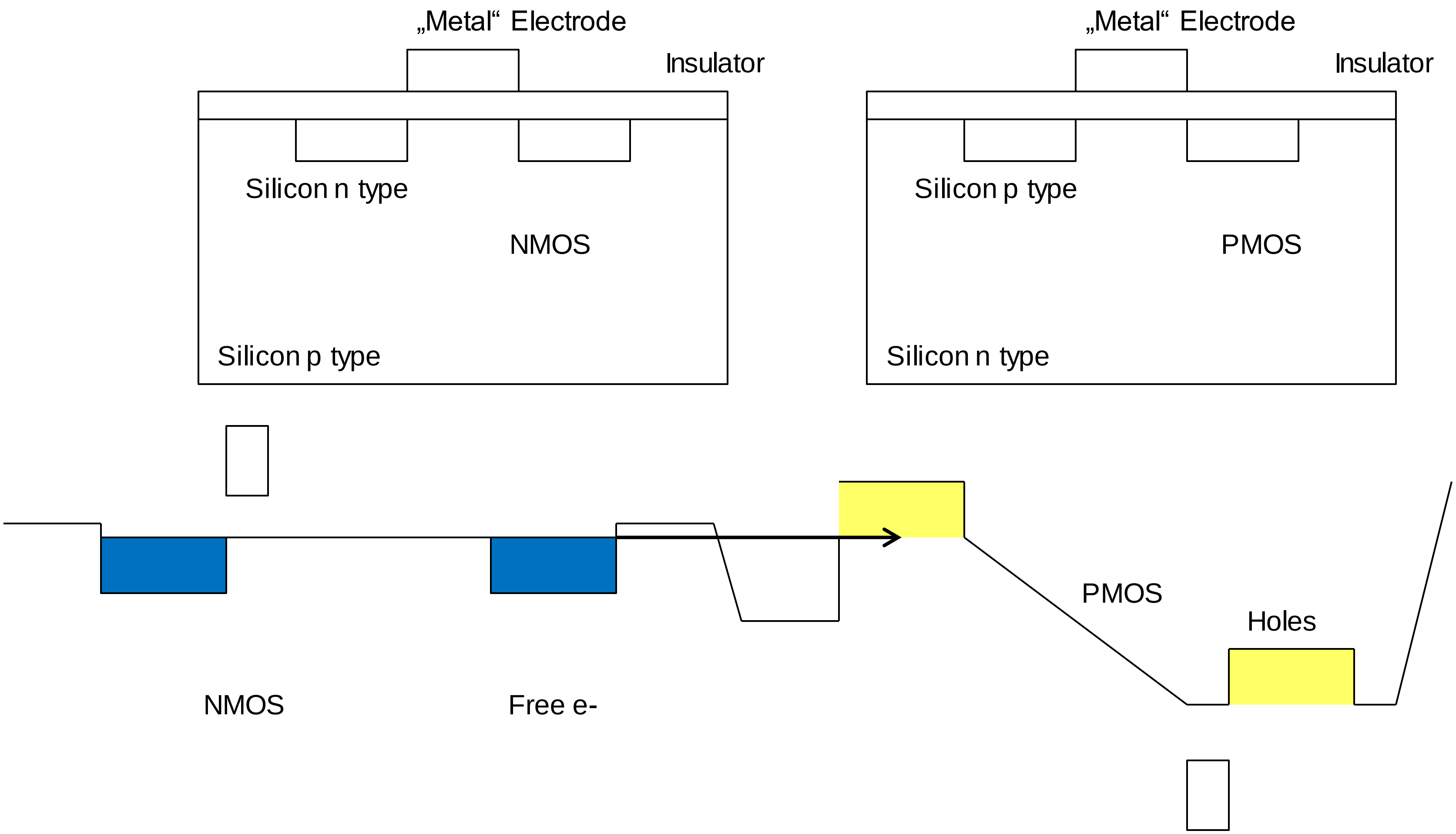
☹ Larger pixels
☹ Larger power consumption
☺ Fast (trigger based) readout


CR-RC
Comparator
Latch
Bus driver
CSA
RAM
4-bit tune DAC
Readout bus

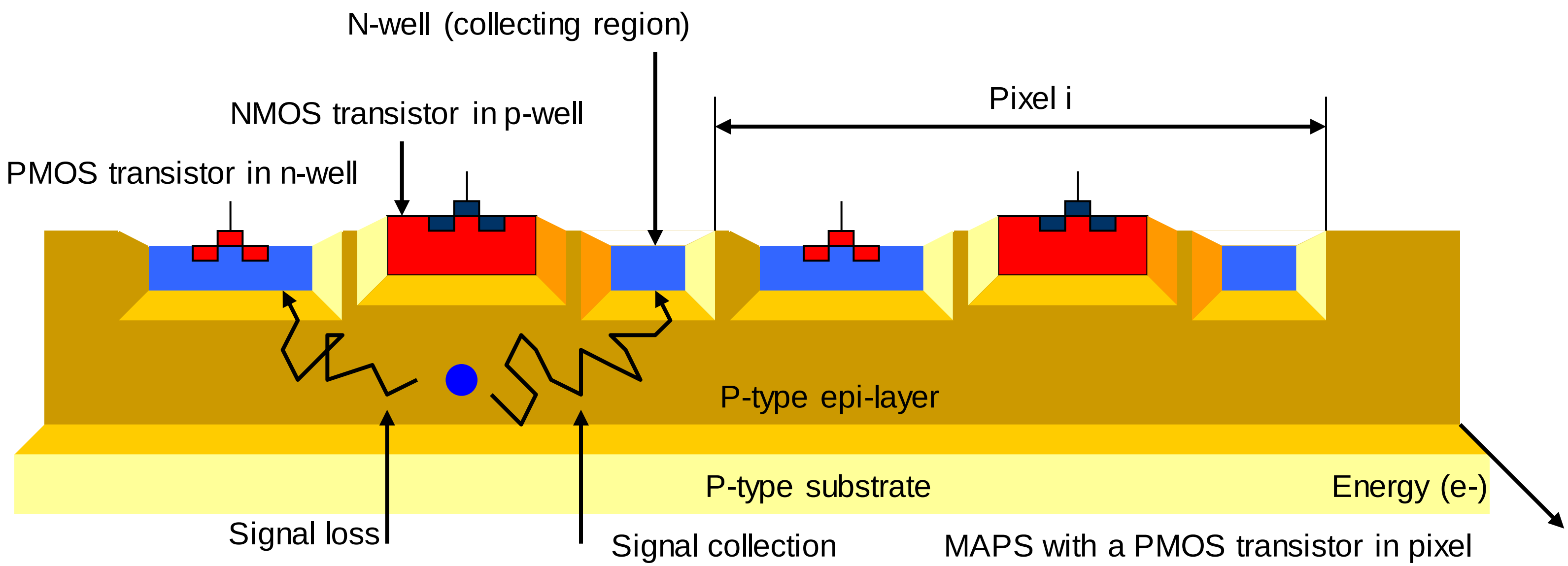
- Two transistor types n-channel NMOS and p-channel PMOS are needed for the realization of complex circuits



- Example: A good voltage amplifier can only be realized with CMOS

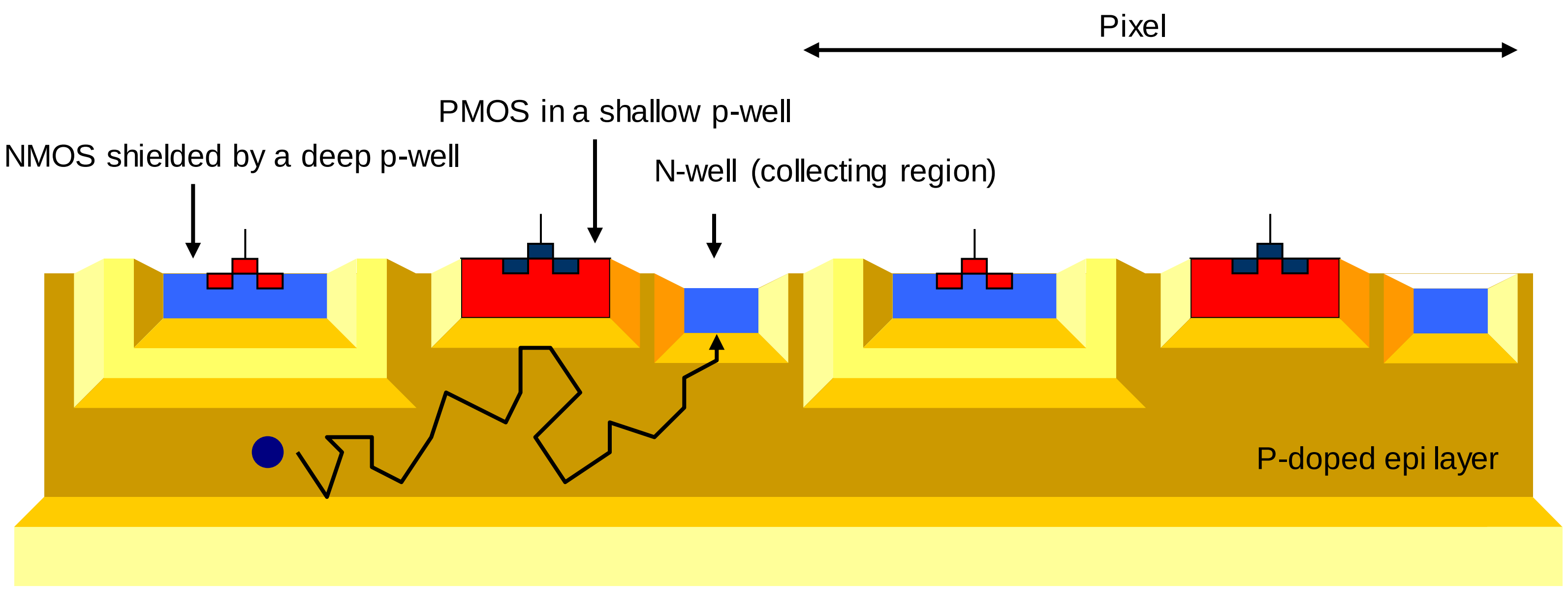


- If PMOS transistors are introduced, signal loss can happen



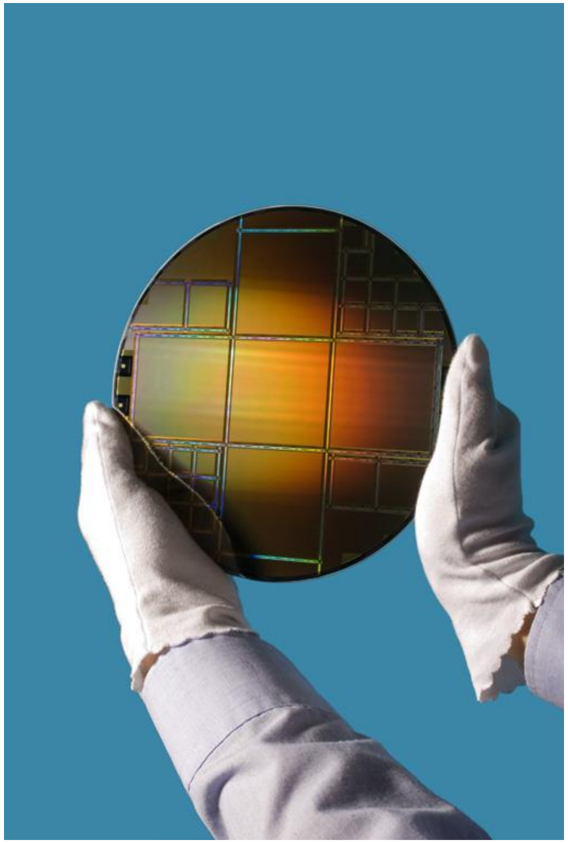
Advanced structures: INMAPS

- Deep P-layer is introduced to shield the PMOS transistors from epi layer
- No charge loss occurs
- This is not a CMOS standard process
- Only one producer so far: Tower Jazz



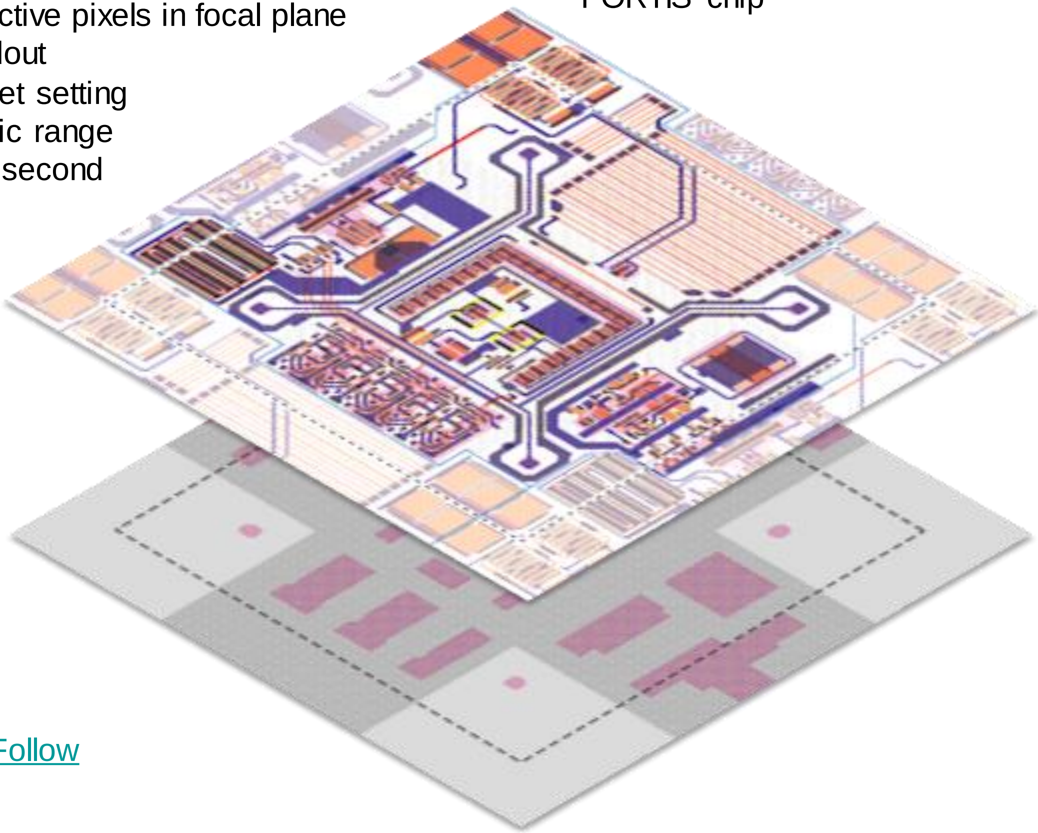
INMAPS

- INMAPS Tower Jazz process is gaining popularity in particle physics community
- It was originally developed by the foundry and the *Detector Systems Centre*, Rutherford Appleton Laboratory



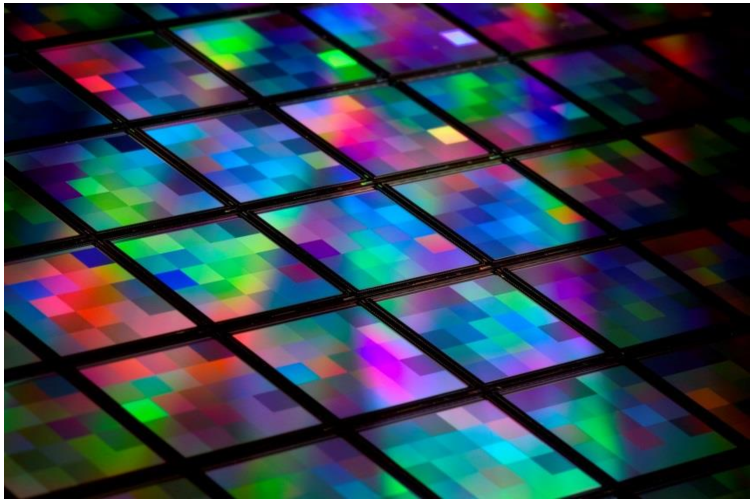
2 Megapixels, large area sensor
Designed for high-dynamic range X-ray imaging
40 µm pixel pitch
1350 x 1350 active pixels in focal plane
Analogue readout
Region-of-Reset setting
140 dB dynamic range
20 frames per second

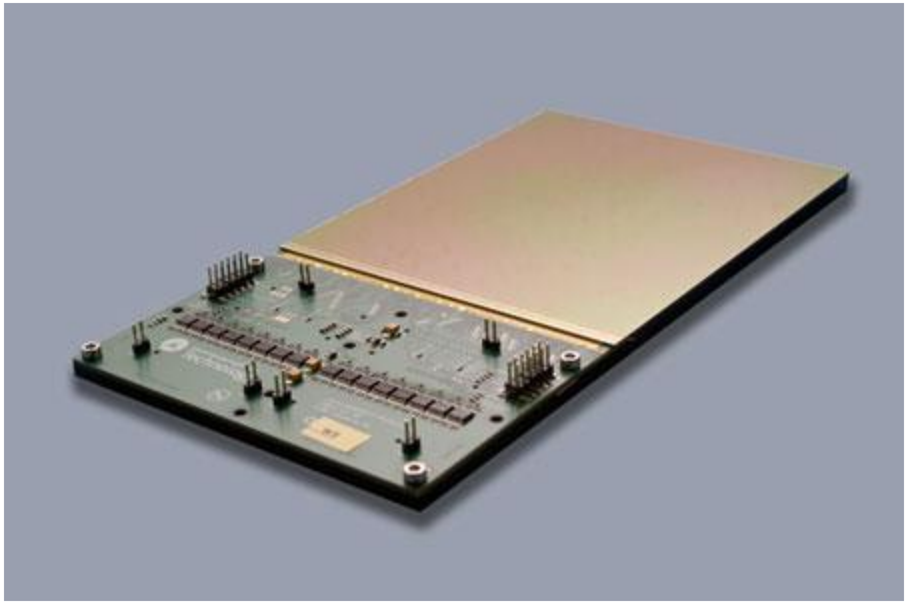
FORTIS chip



http://dsc.stfc.ac.uk/Capabilities/CMOS+Sensors+Design/Follow+us/19816.aspx

- Detector Systems Centre, Rutherford Appleton Laboratory – some examples





Wafer scale 120 x 145 mm chip for medical imaging

http://dsc.stfc.ac.uk/Capabilities/CMOS+Sensors+Design/Follow+us/19816.aspx

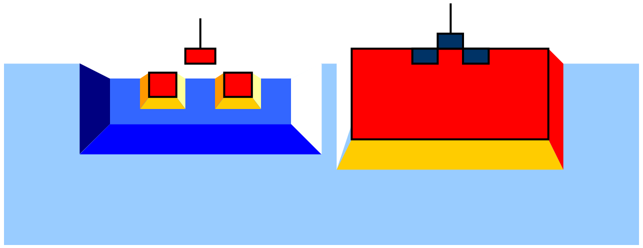
Fast CMOS detectors based on drift charge collection: detectors in HVCMOS-processes and the CMOS processes with a high resistive wafer

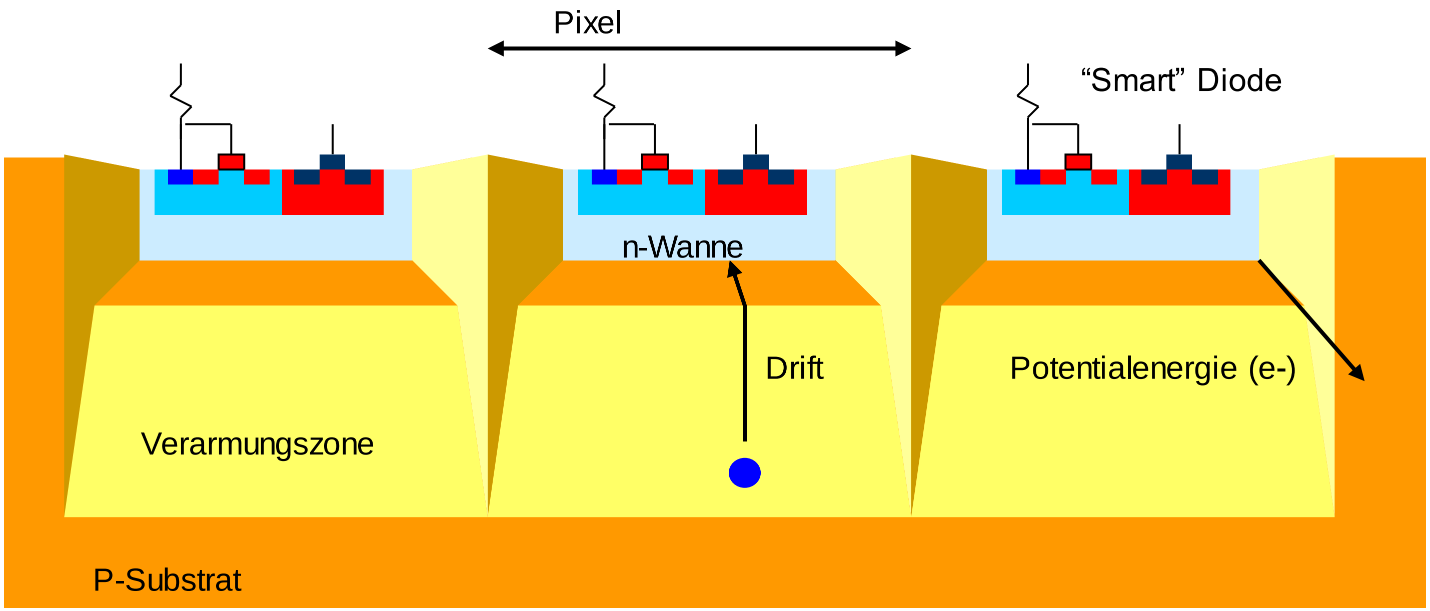
Drift based detector: HVMAPS

- HVMAPS rely on the charge collection by *drift*
- Fast charge collection – high radiation tolerance
- The key is the use of a high voltage n-well in a relatively highly doped substrate
- Pixel electronics is embedded in the n-well
- Two concepts:
- High Ohmic Monolithic Pixels - LePIX – relies on a special CMOS process with high resistive substrate (CERN, Geneve)
- HVCMOS (or smart diode arrays - SDAs) – use a commercial HVCMOS process (CPPM, CERN, Bonn, LBNL, Geneve, Göttingen, Manchester and Heidelberg)

HVCMOS detectors (smart diode arrays)

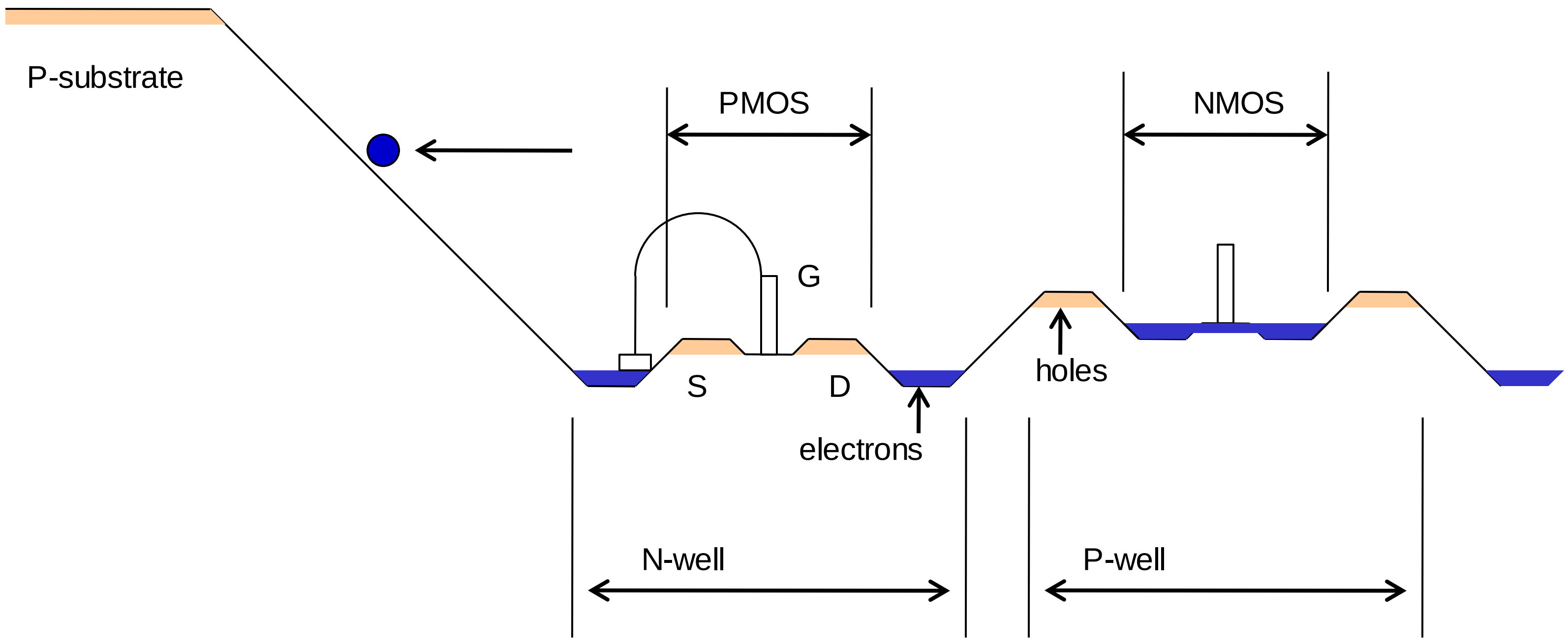
- Smart diode array





"Smart diode" Detector

- Collected charge causes a voltage change in the n-well.
- This signal is sensed by the amplifier – placed in the n-well.



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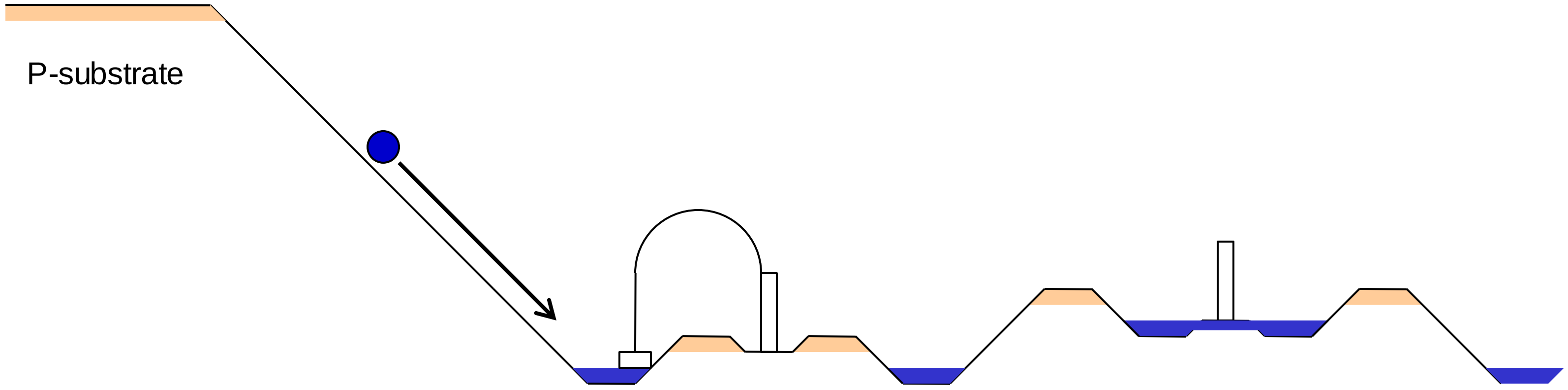

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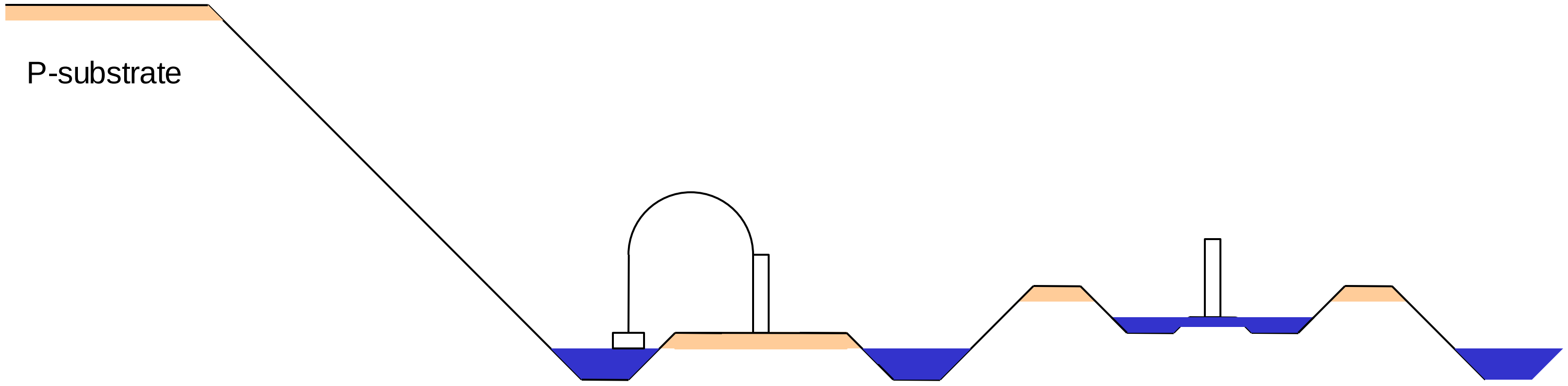
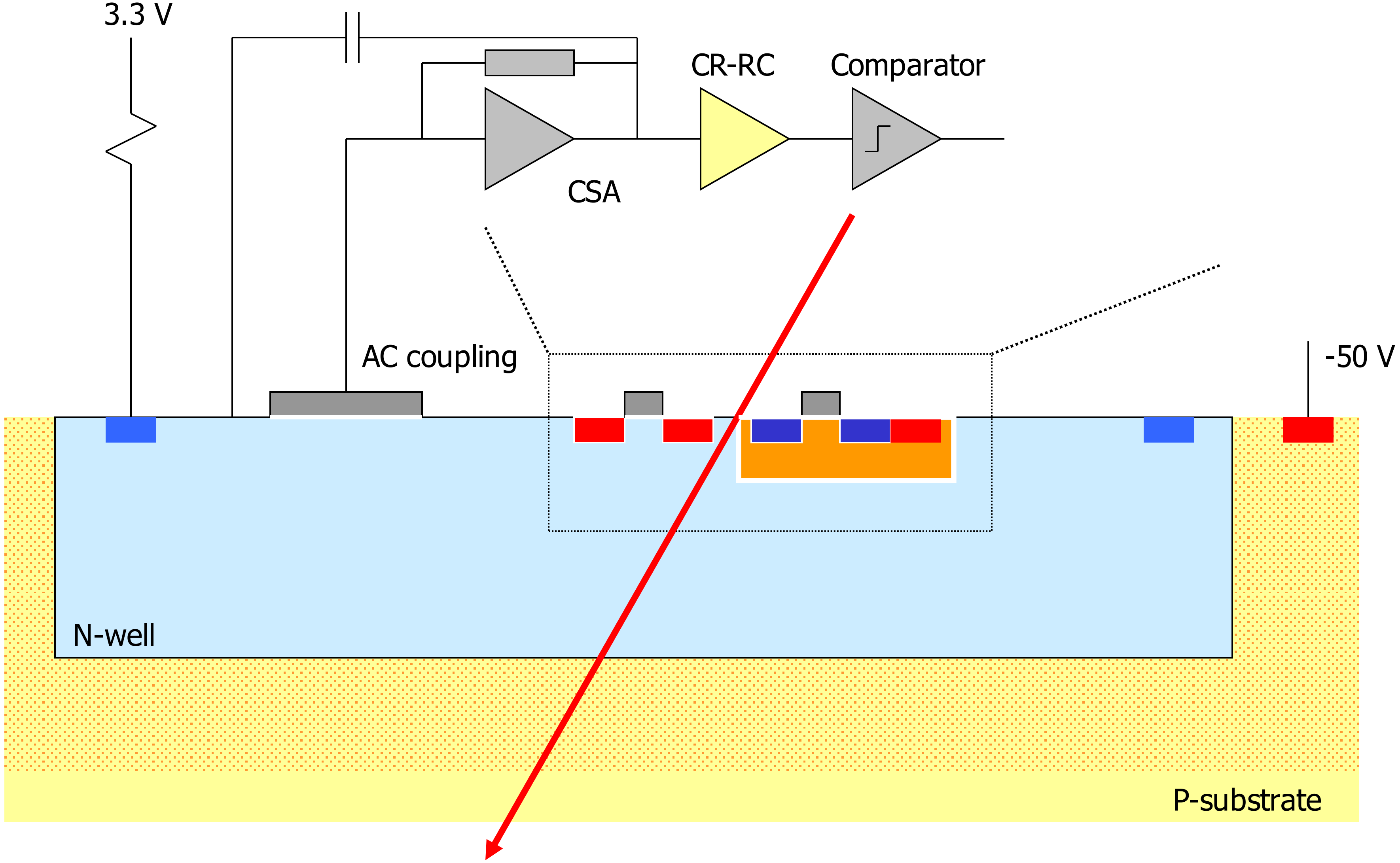
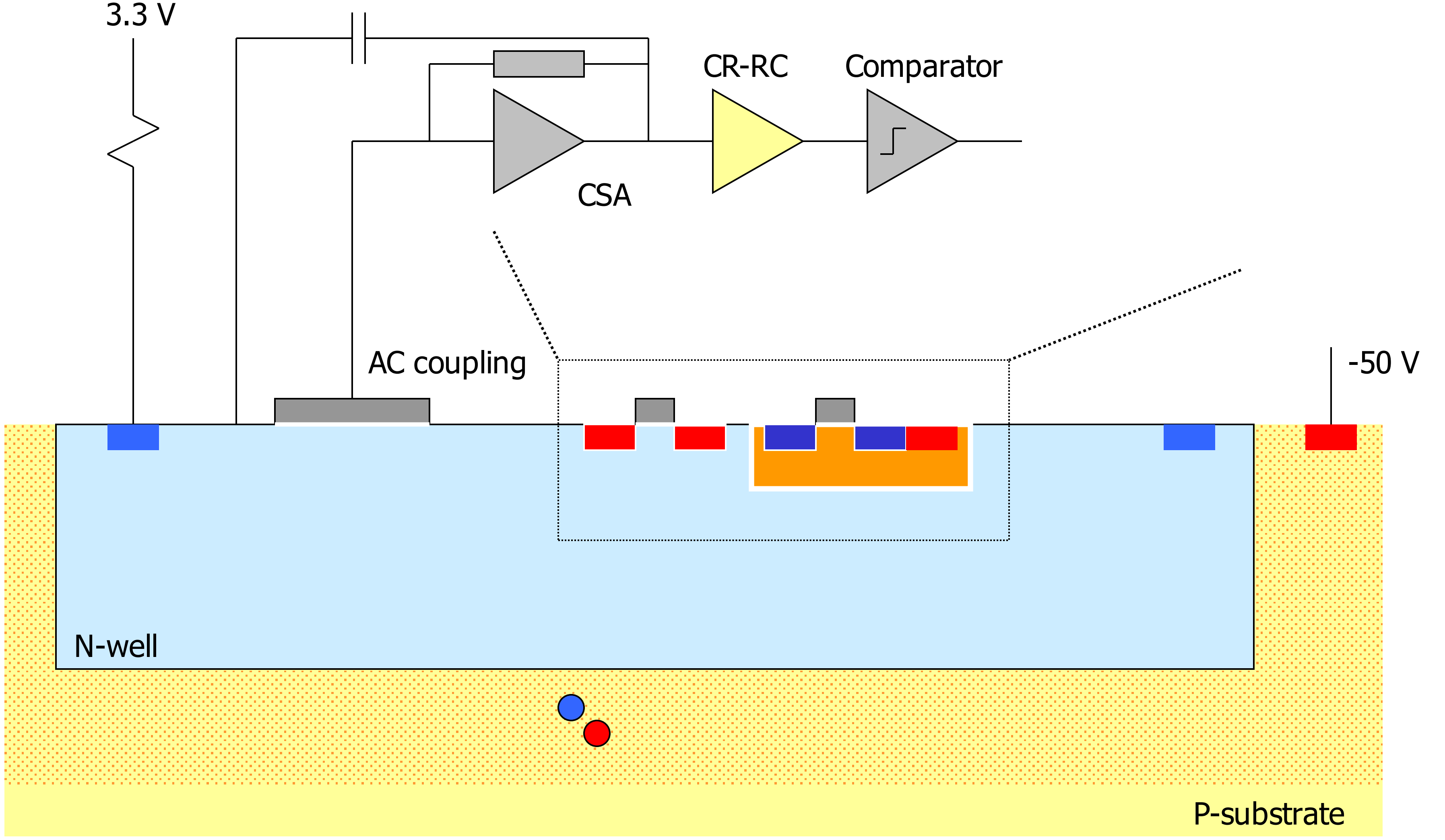



3.3 V
CR-RC
Comparator
CSA
AC coupling
-50 V
N-well
P-substrate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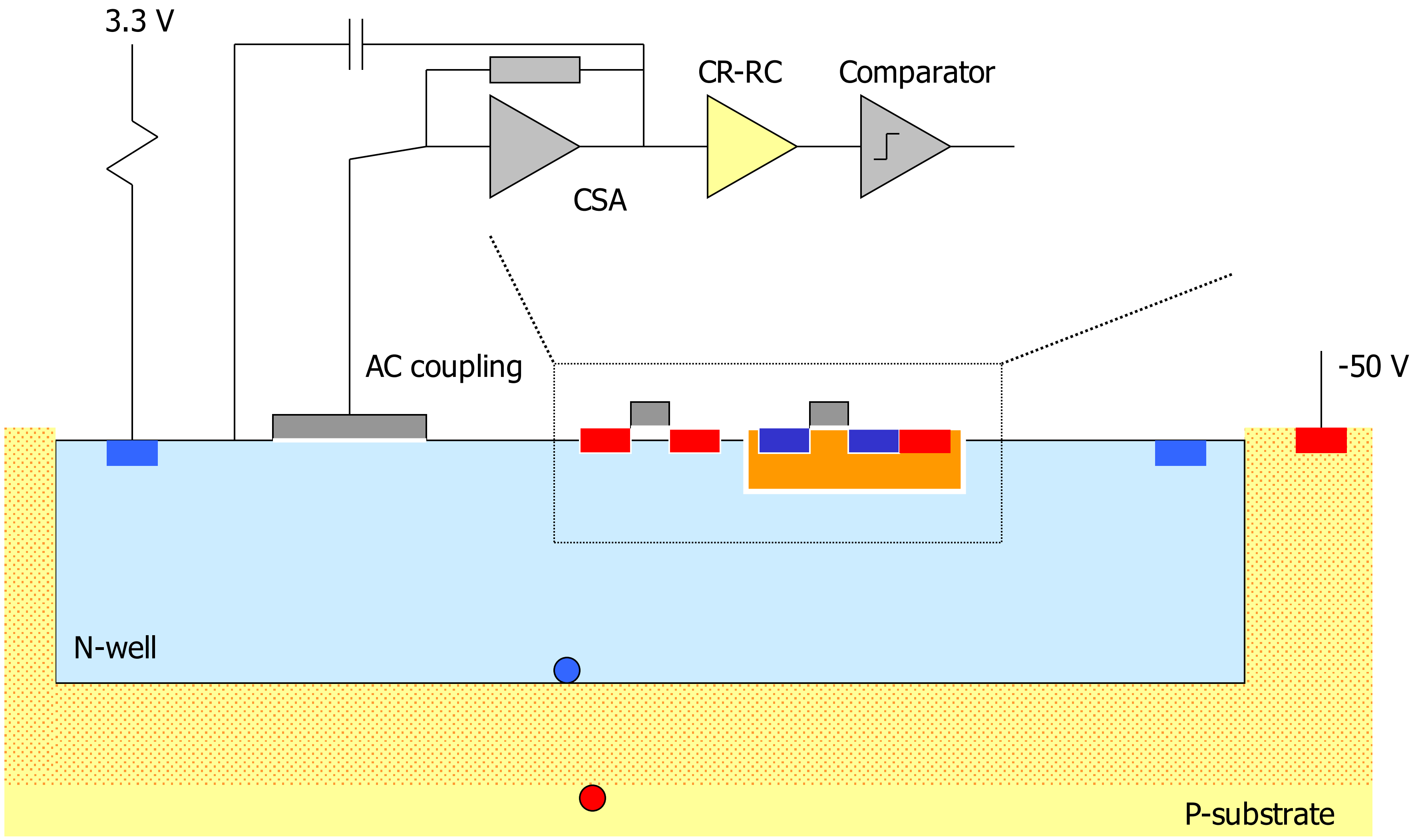
3.3 V
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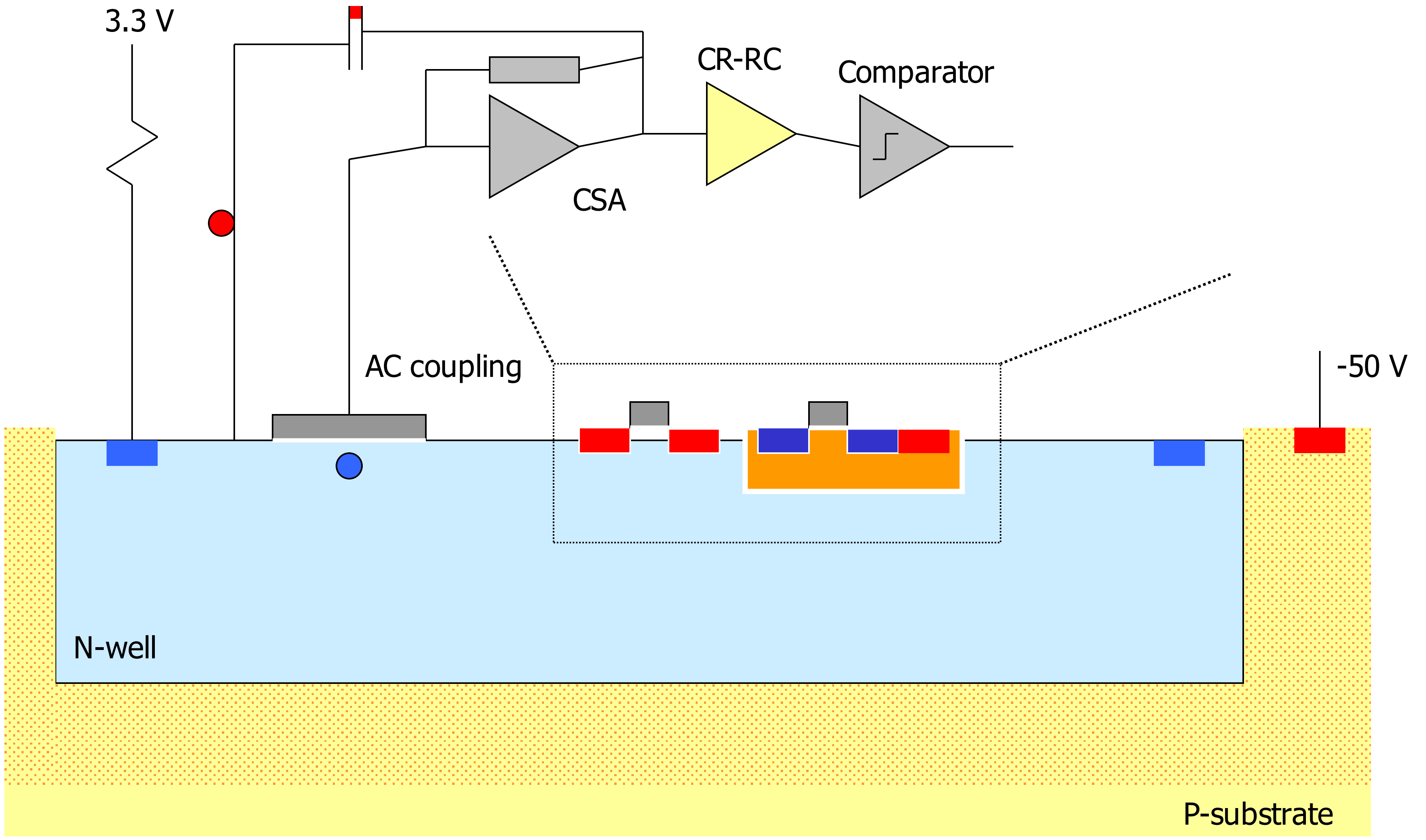
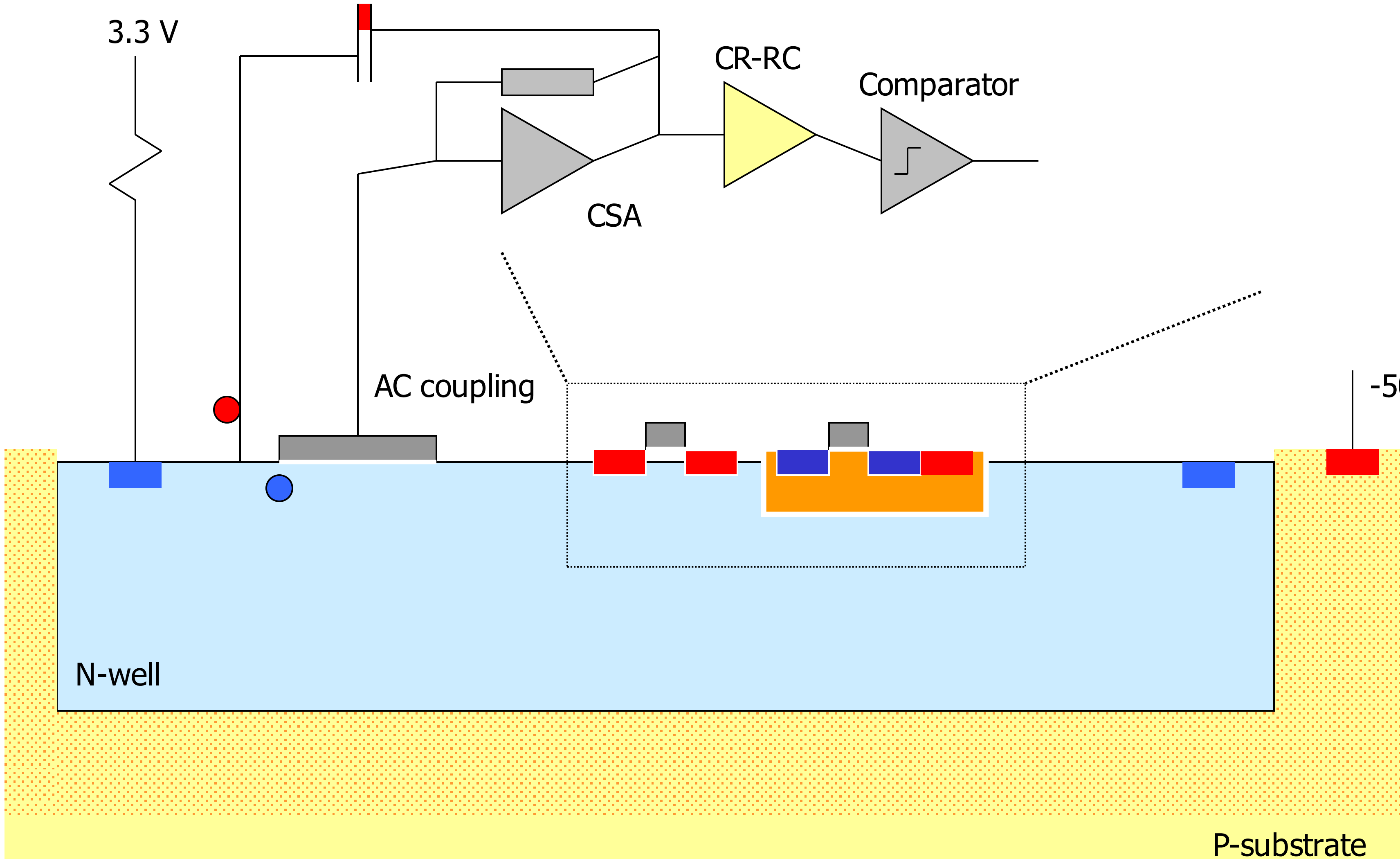
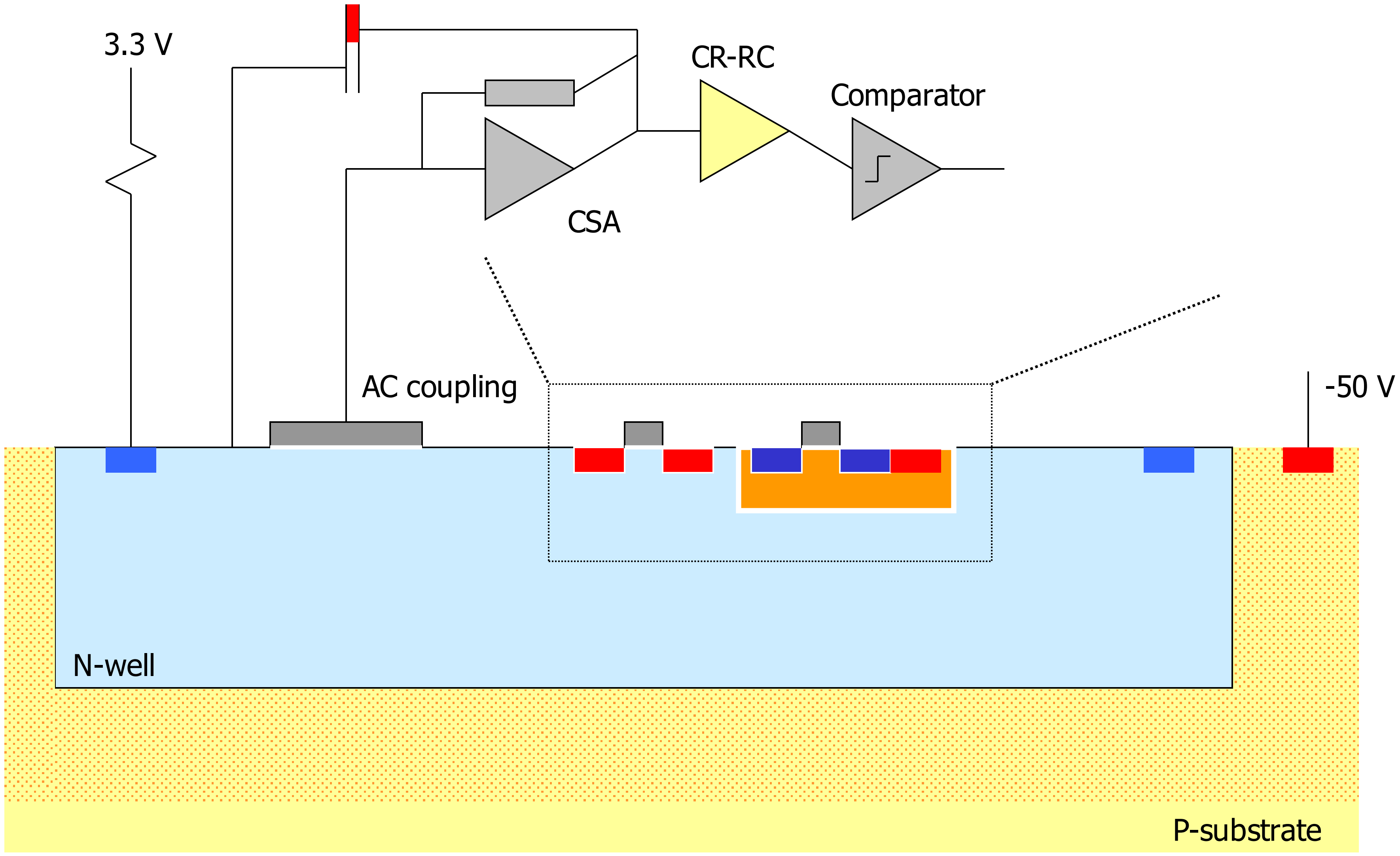
Intelligent pixel

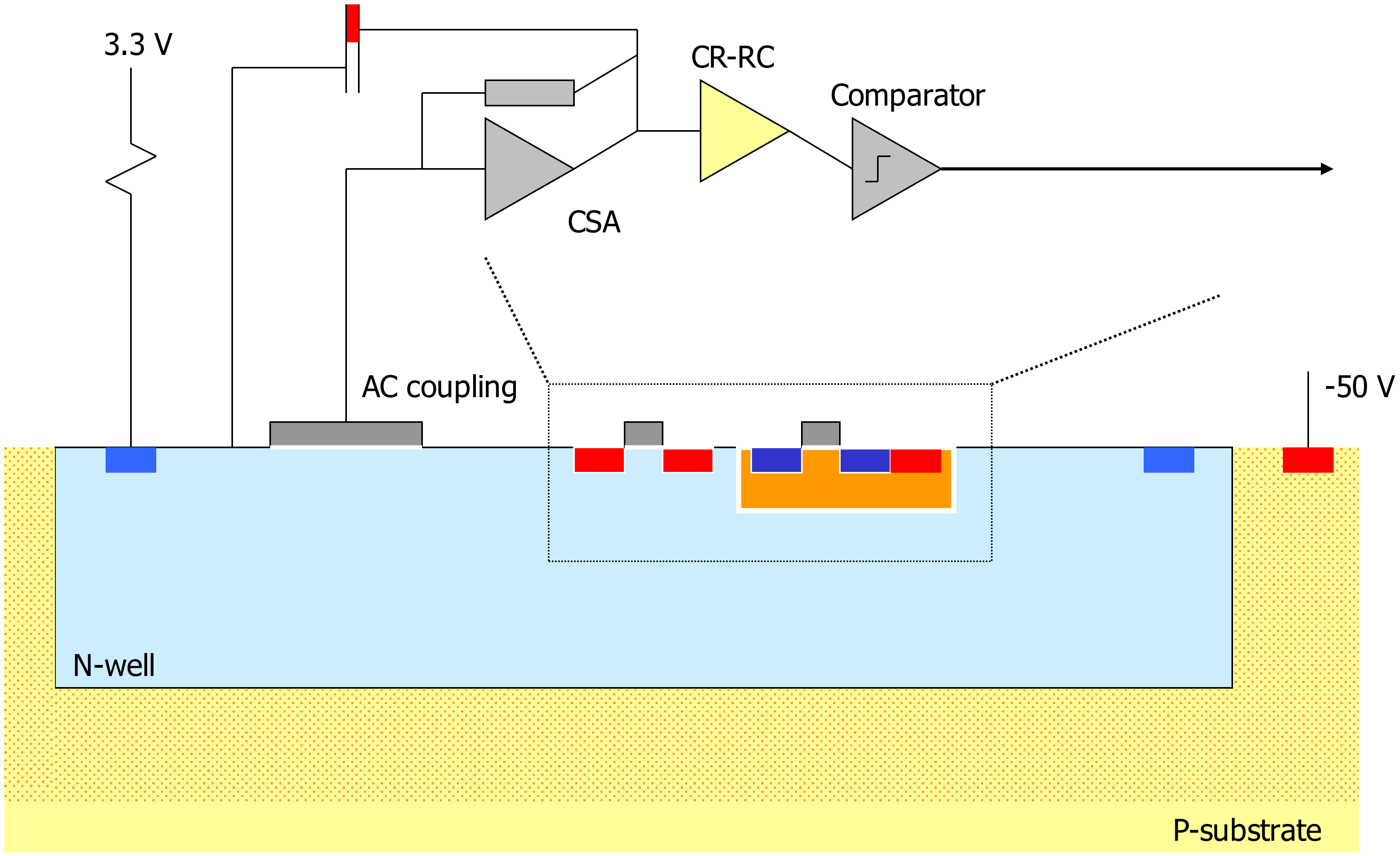


Intelligent pixel

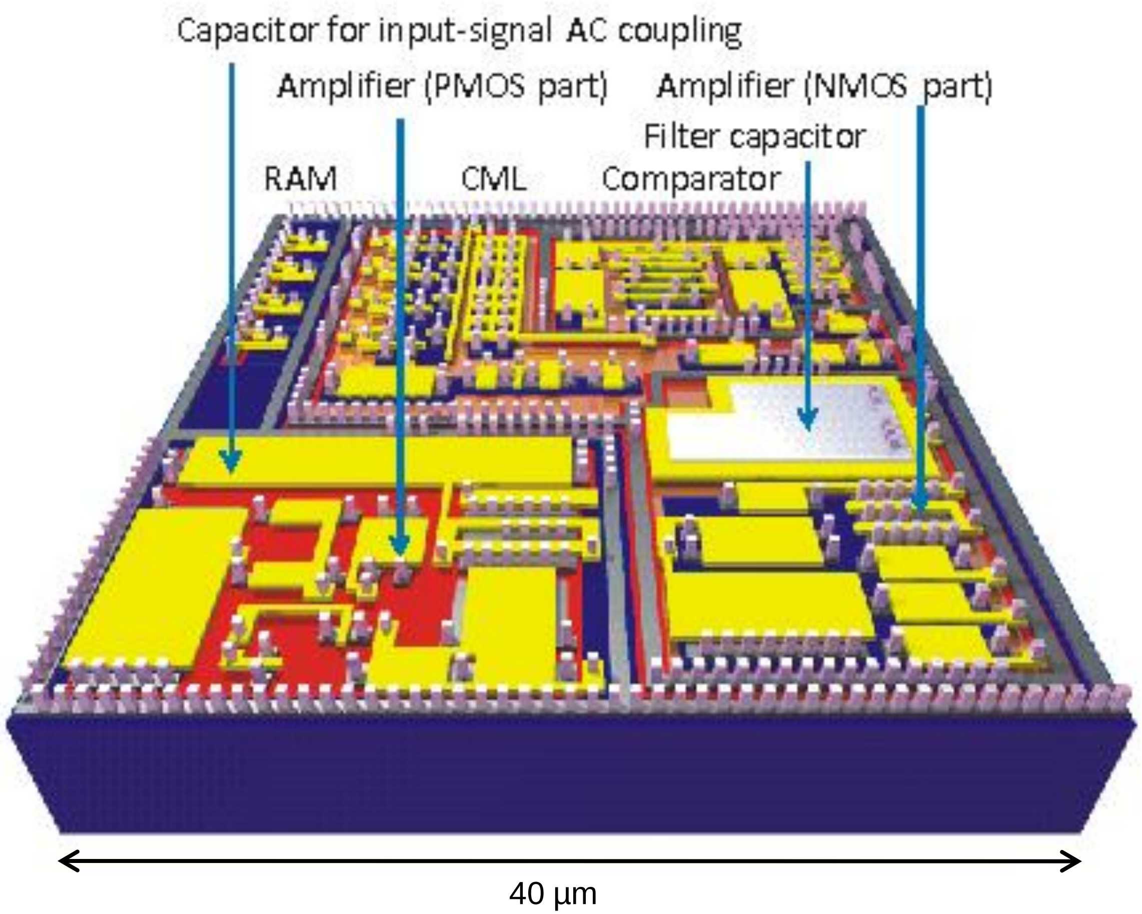


Intelligent pixel



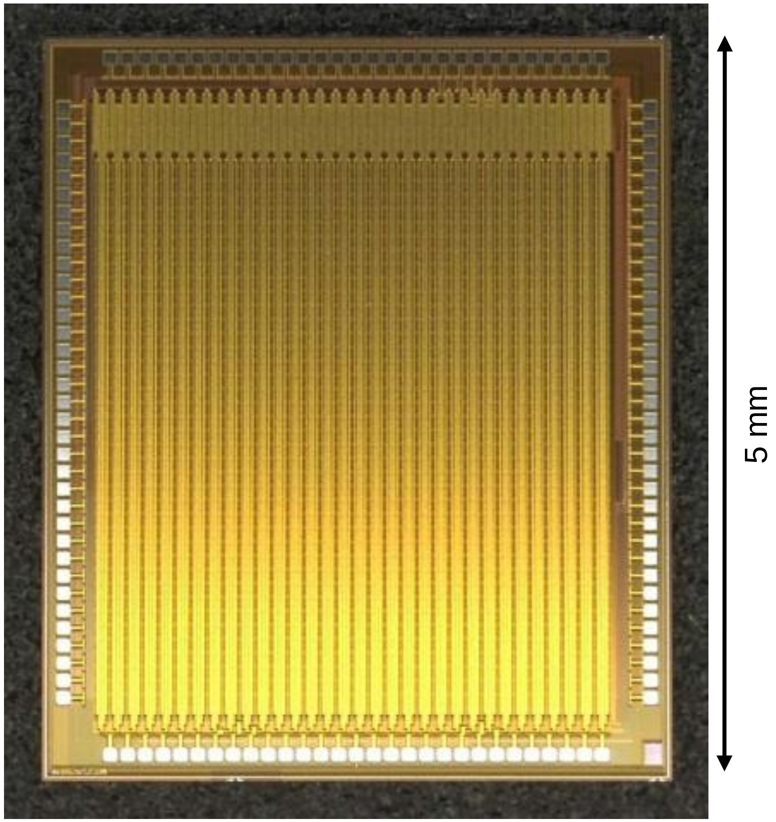

3.3 V
CR-RC
Comparator
CSA
AC coupling
-50 V
N-well
P-substrate

3D layout of a "smart diode"

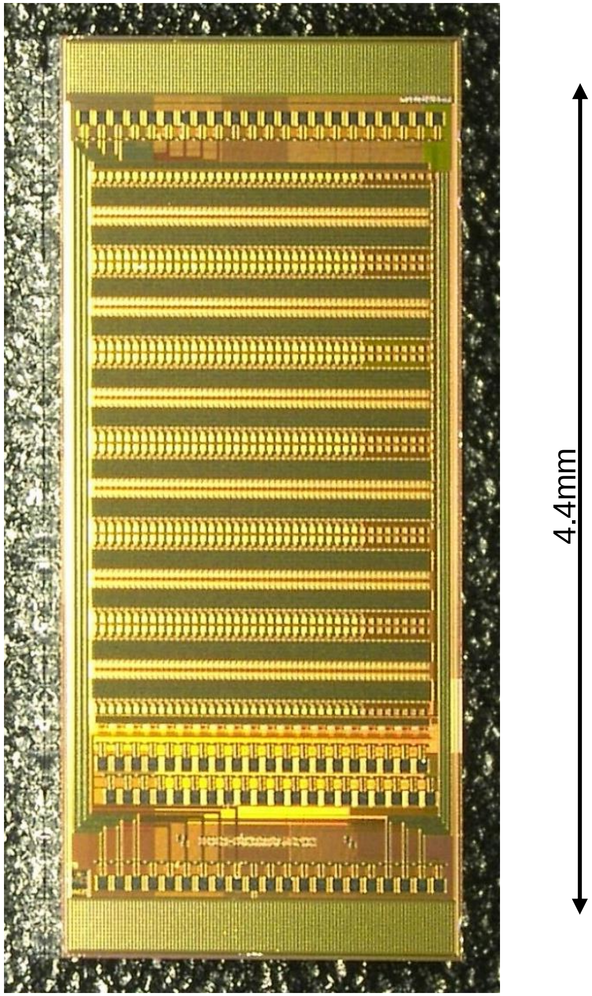


3D layout generated by GDS2POV software

- Mu3e experiment at PSI and ATLAS upgrade option



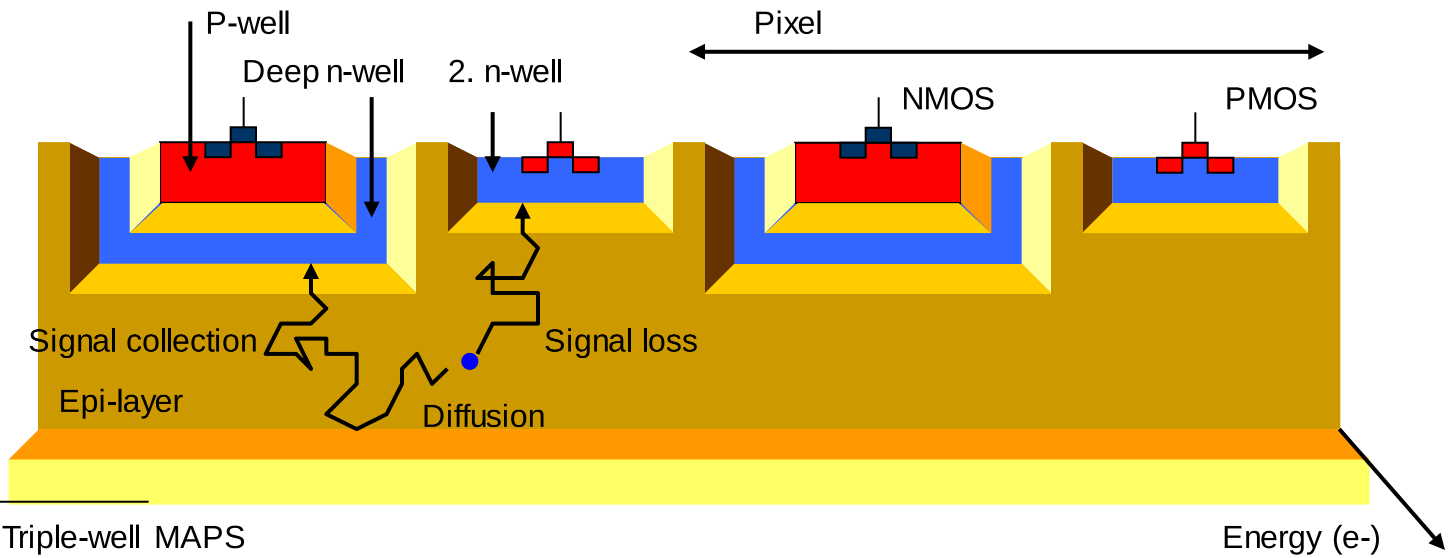
Mu3e prototype chip



ATLAS prototype chip

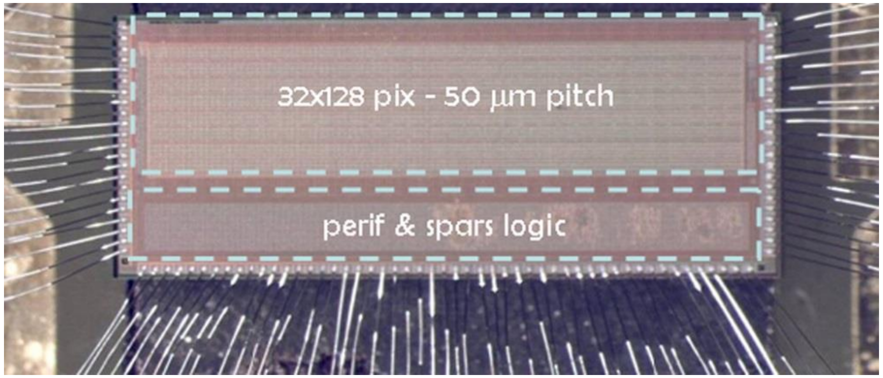
TWELL - MAPS

- Collection electrode is a deep n-well
- To avoid crosstalk, secondary n-well is used for digital electronics
- Rely on diffusion, implemented in low voltage CMOS processes
- Collaboration: INFN Pisa, Pavia, Trieste, Padova, Torino, Bologna

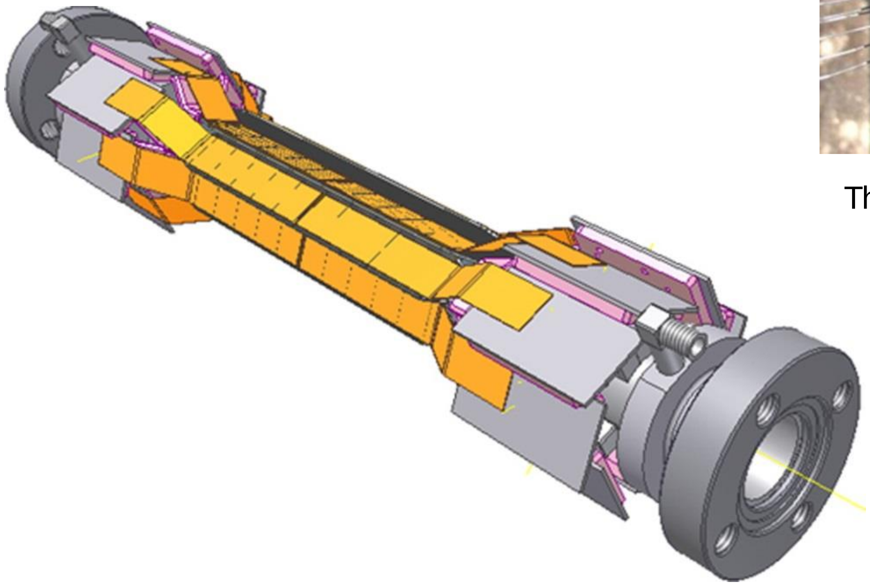


Triple-well MAPS

- APSEL Chips for B-factories



The APSEL4D MAPS chip bonded to the chip carrier.



Schematic drawing of the full Layer0 made of 8 pixel modules mounted around the beam pipe with a pinwheel arrangement.

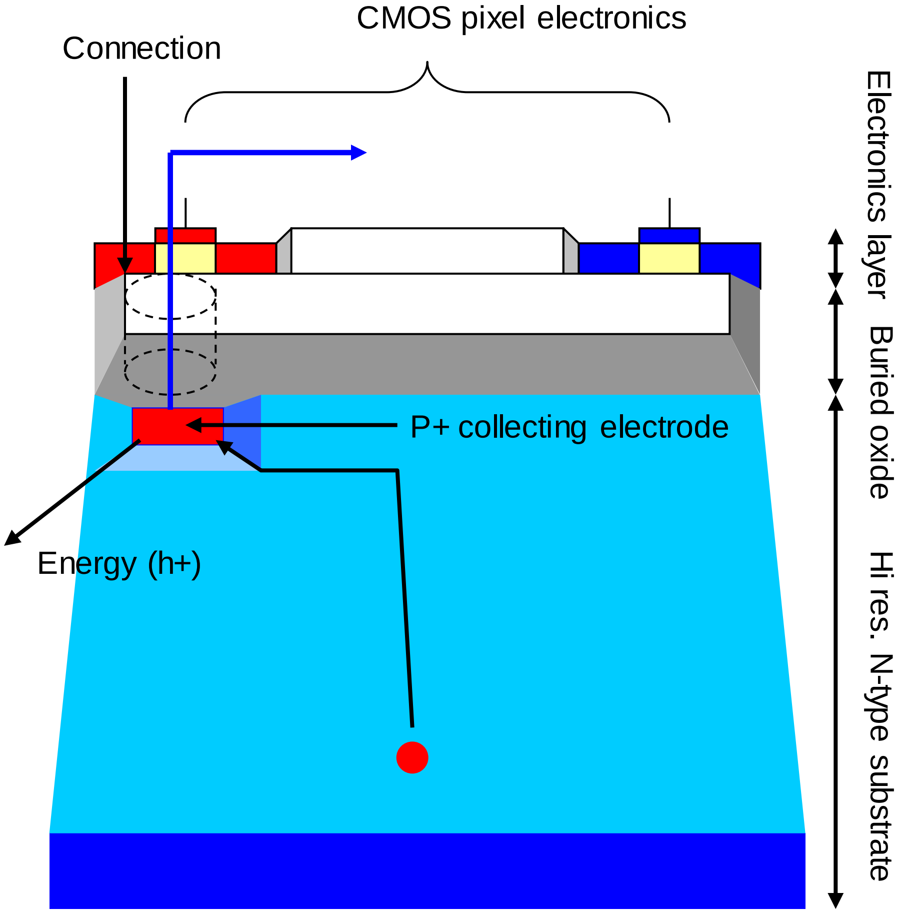
“Thin pixel development for the SuperB silicon vertex tracker”, NIMA vol. 650, 2011

Special monolithic technologies

SOI

SOI technology

- Originally developed at University of Krakow
- The development continued in collaboration with industry (OKI and Lapis)
- The collaboration is now led by KEK, Japan

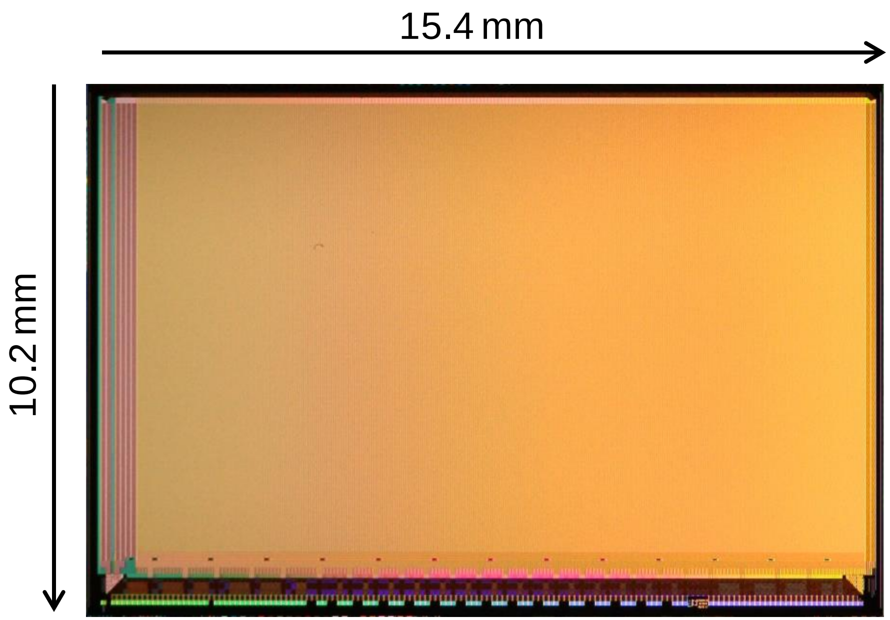


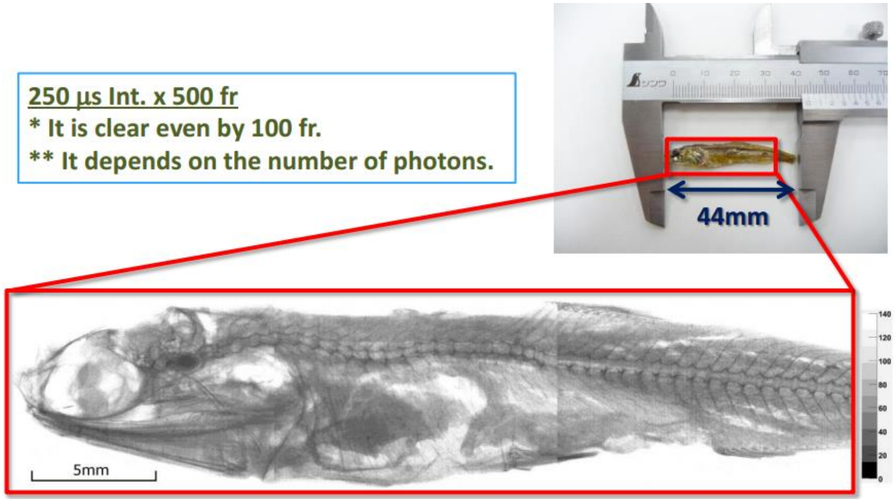
- An SOI detector consists of a typically micrometer-thick electronics layer, an insulation silicon-dioxide layer (called buried oxide) and a high resistance substrate. (In our case ~500μm thick, 7.1kΩcm, n-type FZ substrate.)
- The sensor has the form of a matrix of pn junctions, the collecting regions are p-type diffusion implants in the n-substrate.
- A connection through the buried oxide is made to connect the readout electronics with electrodes
- The industrial SOI detector technology based on Lapis semiconductor (formerly OKI) 200nm (or 150nm) CMOS fully depleted process has been developed within a collaboration between industry and institutes

MPW (Multi Project Wafer) run

~Twice per Year

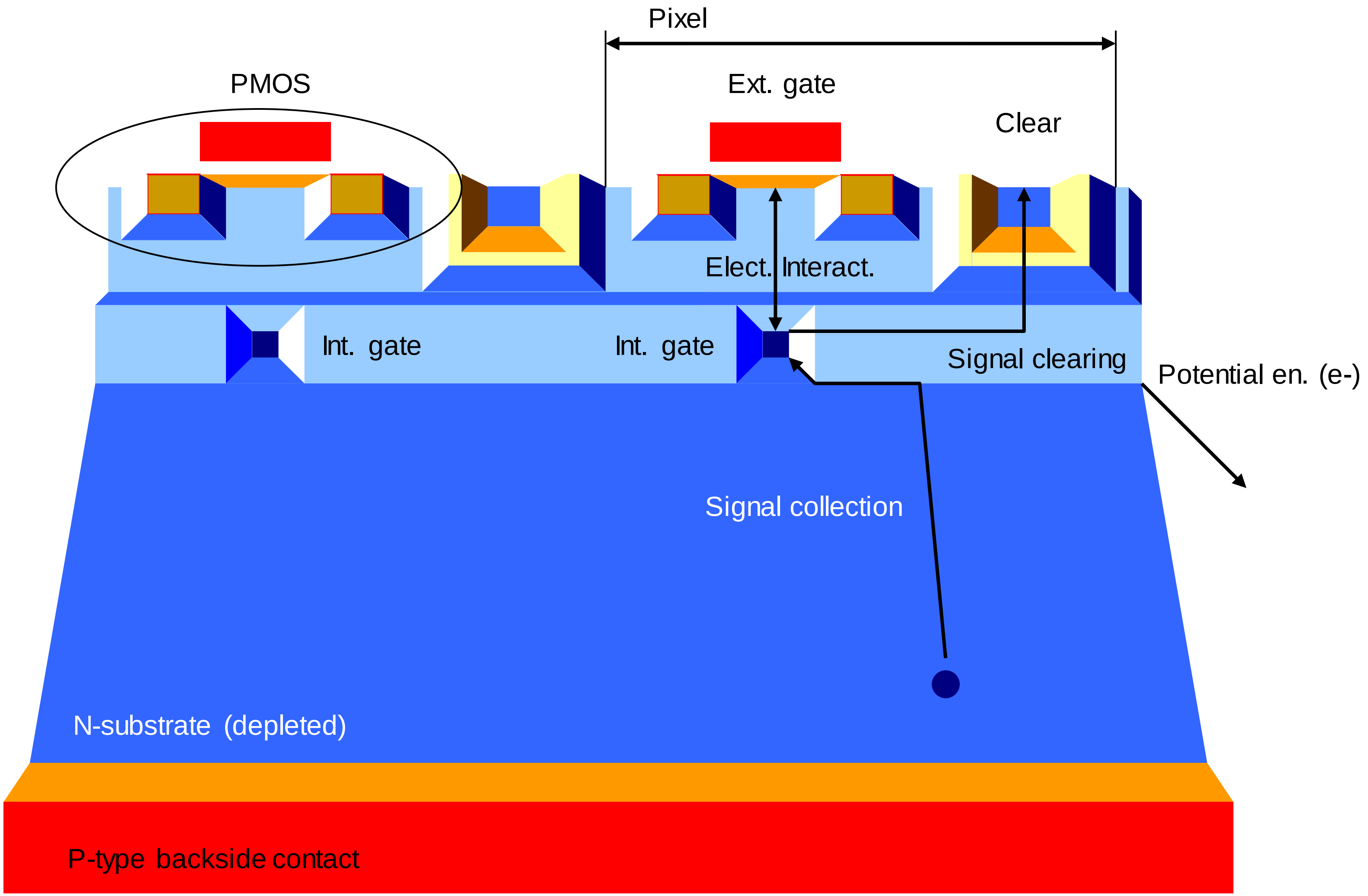
- SOI technology can be used for x-ray detection thanks to its thick sensitive region
- Example of an x-ray detector: INTPIX4





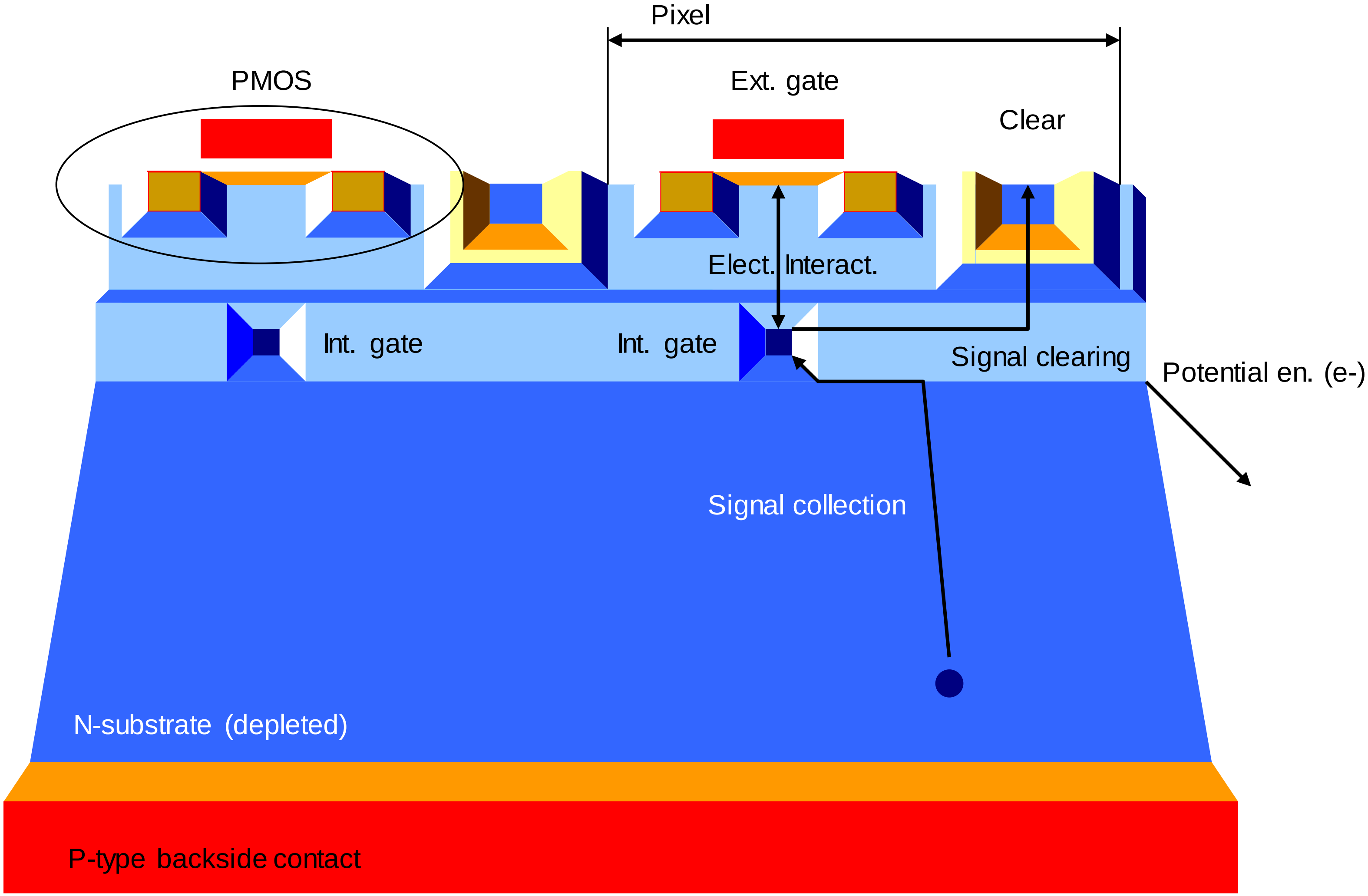
DEPFET

- DEPFET is a special MOS-based monolithic detector produced at Semiconductor Laboratory (MPI) Munich



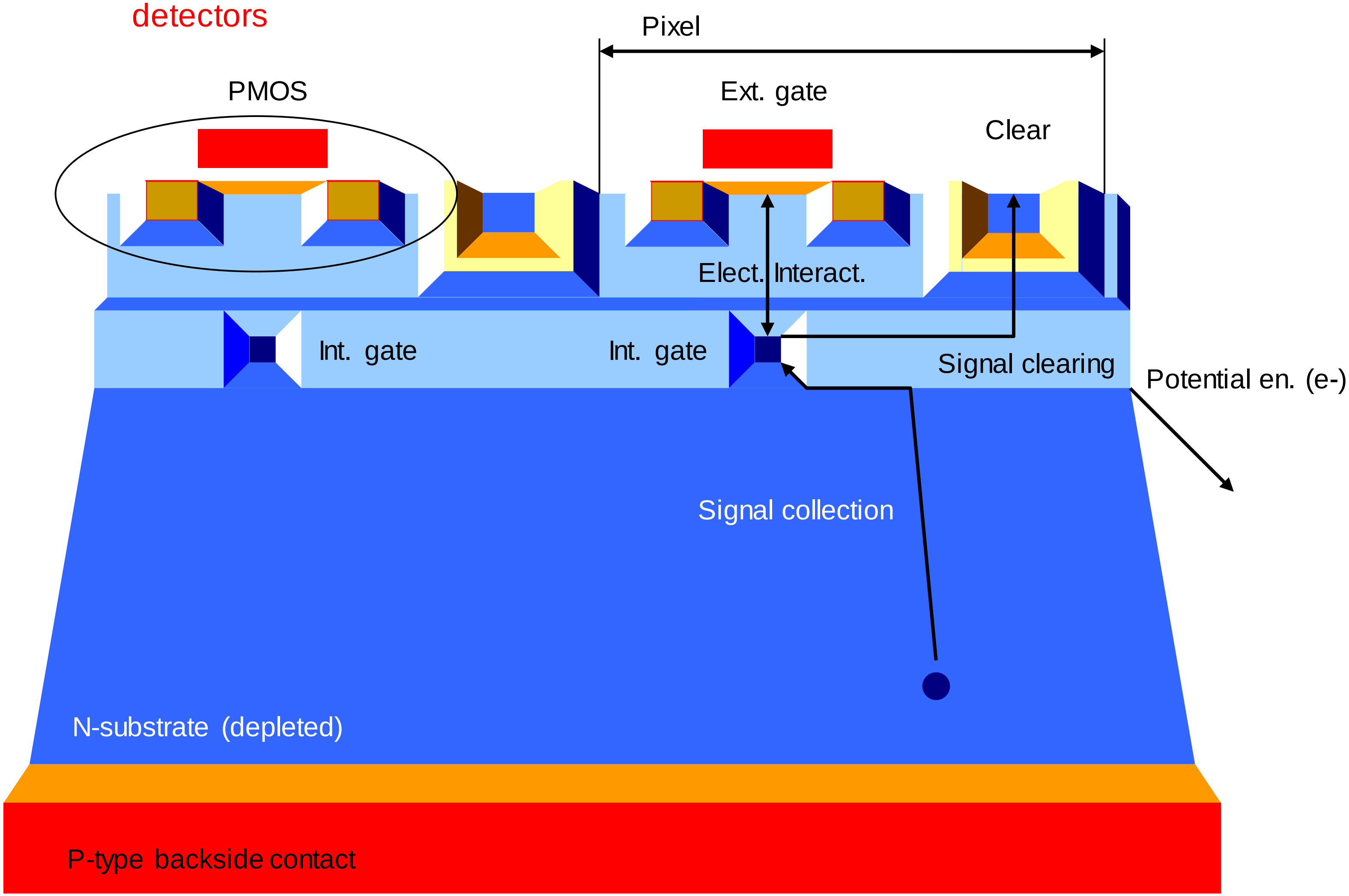
DEPFET

- DEPFET uses high resistive substrate with depleted layers up to 600 um – very high signal to noise ratio



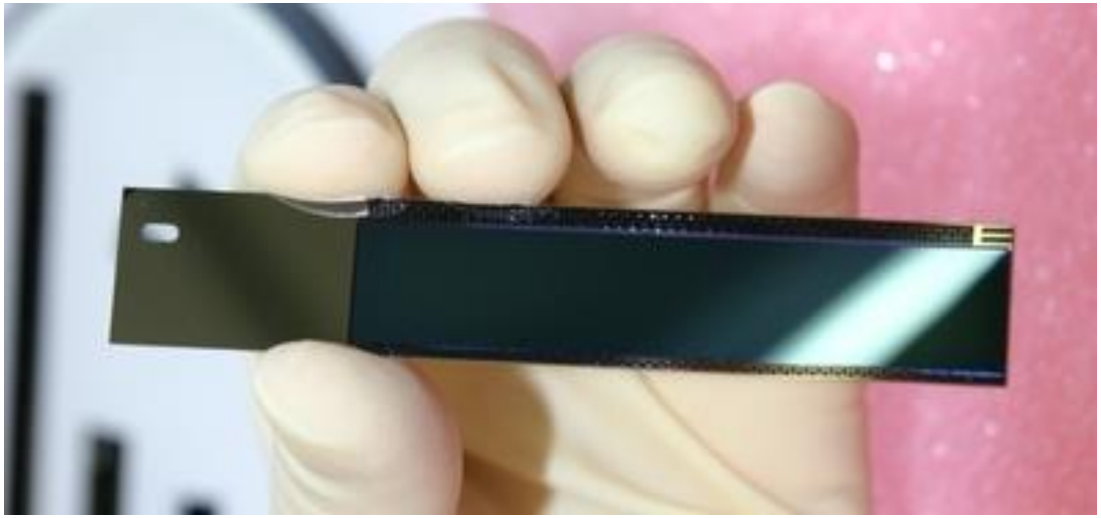
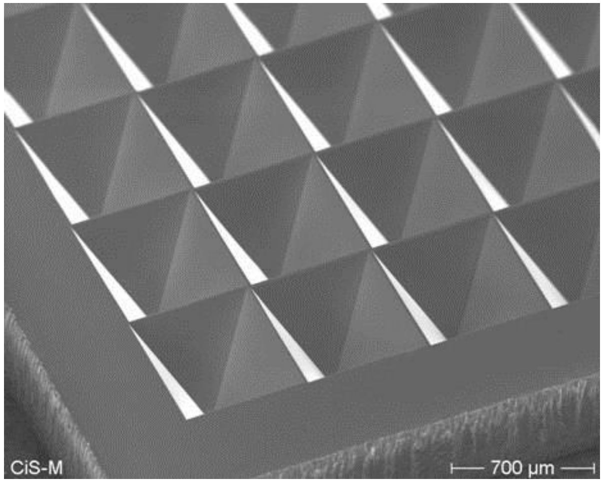
DEPFET

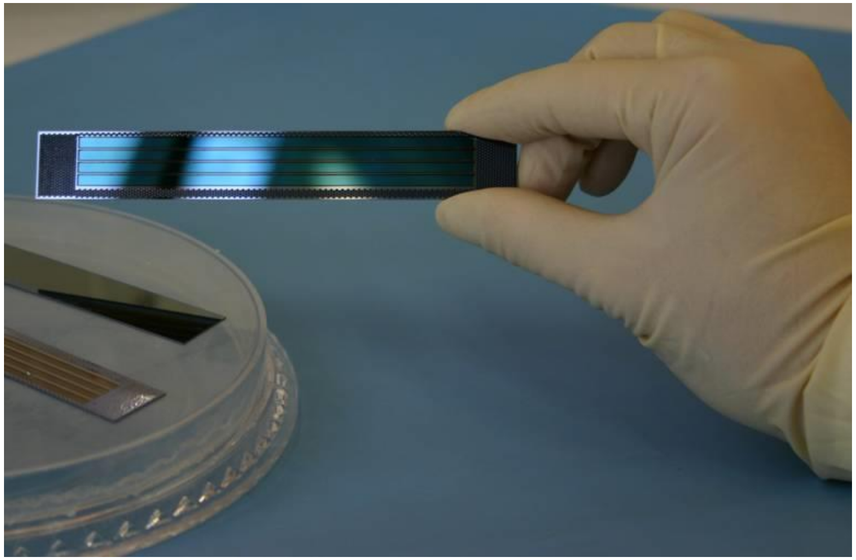
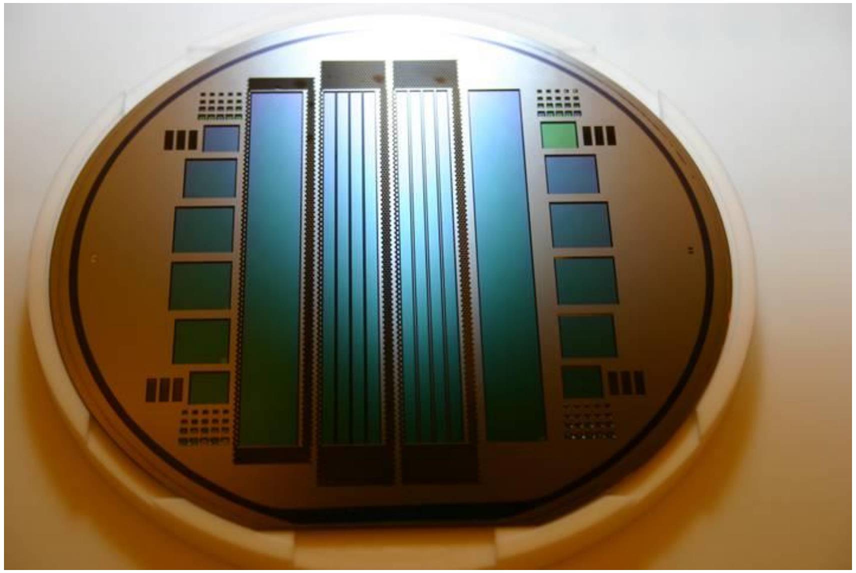
- DEPFET structure is very innovative – the signals are collected in internal gates
- Strong points: small “capacitance” of internal gate – high signal amplification
- Absence of reset noise, special thinning technique assures mechanical stability of the thin detectors



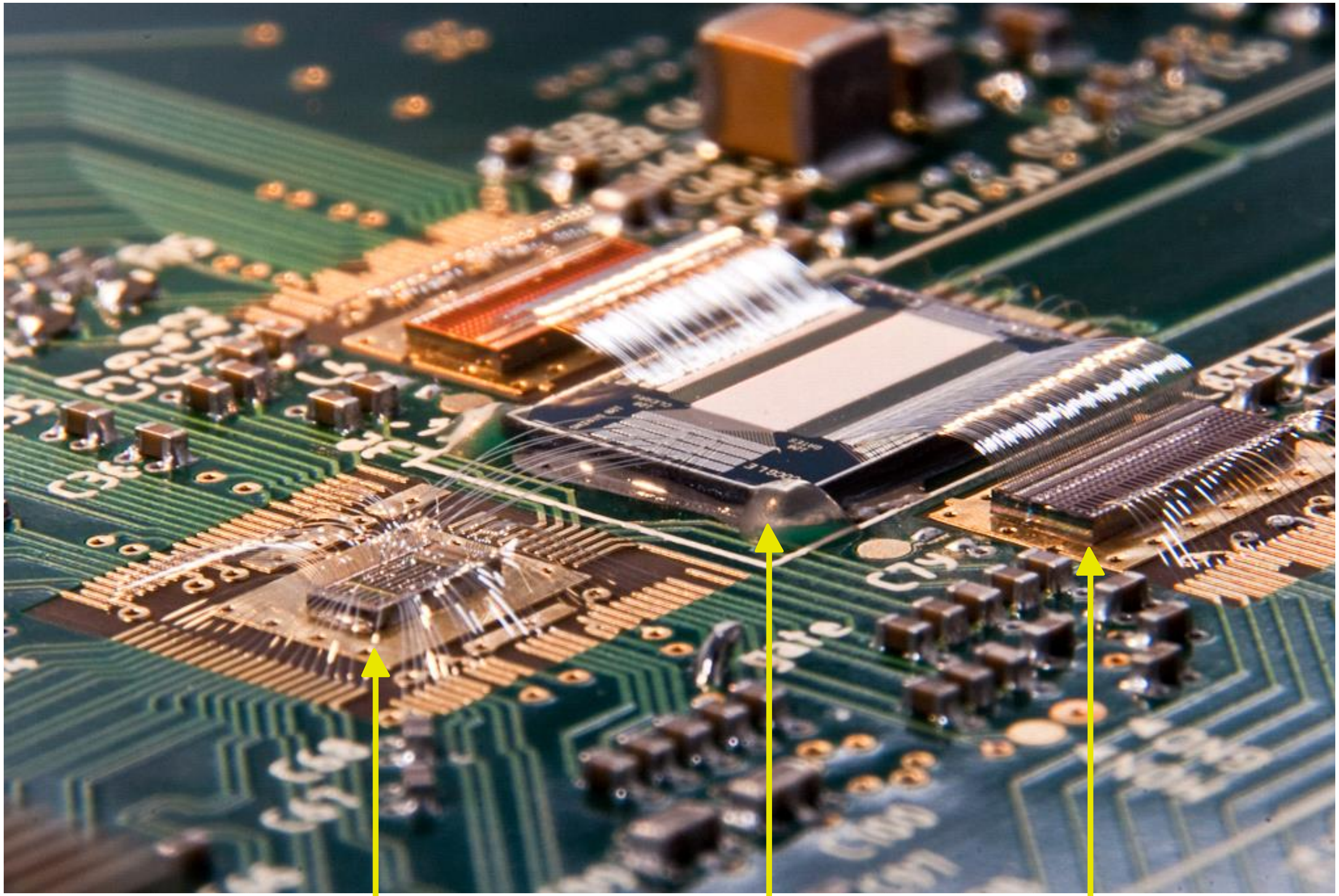
- Application in high energy physics: Belle II pixel detector at KEK
- 10 cm long detector modules fixed at the edges without any other supporting structure

- Only silicon modules

- Since pixel electronics is very simple (only one transistor) and no periphery circuits can be realized at the detector substrate, external ASICs needed for the readout
- Semi-Monolithic concept



DCD DEPFET SWITCHER

- Thank you!