Radiation hard front-end electronics

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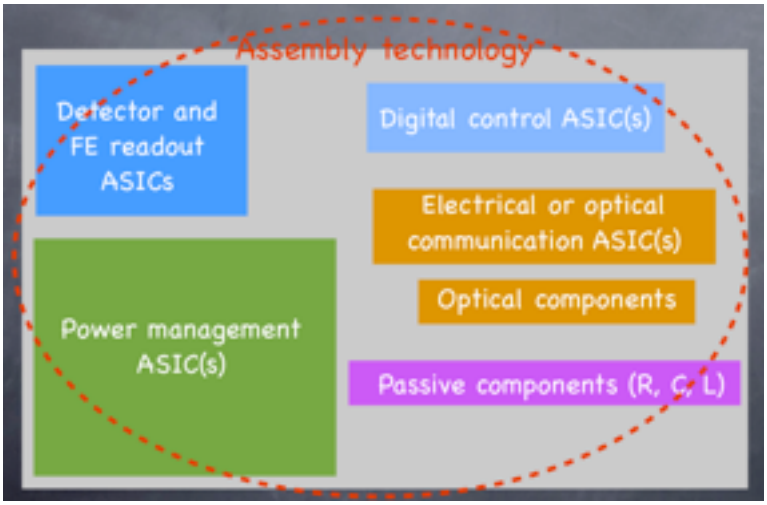
These are the notes accompanying the 1-hour lecture given at the CERN TALENT summer school (June 2013). They cover electronics typically used in silicon tracking detectors such as pixels or strips, which are used in the very central part of HEP experiments.
It is instructive to compare the radiation requirements for the 'typical' HL-LHC projected application in trackers with those for a Space mission, being it a satellite or a deep space probe. The levels of radiation are several orders of magnitude larger for HEP trackers, in terms of total ionizing dose (TID) and displacement damage (DD). However, Space is a more difficult environment for Single Event Effects (SEE) because of the presence of energetic Heavy Ions (HI), which are not directly present in the particle environment of physics experiments.

To specifically address the electronics used in trackers, it is useful to have an image of a conceptual detector module summarizing the architectures in discussion (and development) for LHC upgrades.



The module contains a number of electronics functions which are executed by Application-Specific Integrated Circuits (ASICs). Moreover, some commercial-grade electronics or optoelectronics components are used, such as passives (R, L, C), PiN diodes, light emitters (VCSELs, Lasers). Ensuring radiation hardness of the module hence implies mainly the development of radiation hard ASICs, which our community has been doing for the past 20 years. However, technology changes and its natural resilience to radiation effects, which is often deeply related to process details, also evolves. We therefore need to keep the expertise on how to design radiation hard ASICs, and keep updated with radiation effects in present-day (and near-future) technologies. It should also be noted that all present developments of ASICs for tracker upgrades use CMOS technologies only (no bipolar or BiCMOS): this article will only cover CMOS.

The main radiation effects in ASICs manufactured in CMOS technologies are summarized below. Their relevance, as indicated in the table, must not be taken in absolute terms: it expresses the likelihood of the effect to strongly affect the functionality of the ASICs in

future tracker detectors (based on technologies and design strategies planned to be used as of today).

			Relevance
Cumulative effects	Total Ionizing Dose (TID)		++
	Displacement damage		--
Single Event Effects (SEE)	Temporary effects	Single Event Upset (SEU)	++
		Single Event Transient (SET)	+
	Permanent effects	Single Event Latchup (SEL)	-

Cumulative effects include manifestations of electrical parameter variations due to the continual exposure of the device to radiation. Damage accumulates in time (with the integral of the radiation) and affects the functionality. A pre-characterization of the device can help determine the failure level, which can reliably help predicting at which time the device will fail in the real application.

- TID are due to the energy deposited in the electronics device by radiation via ionization. It is very relevant for tracker applications, since CMOS technologies are typically vulnerable to TID.
- Displacement Damage (DD) effects are instead due to the displacement of atoms in the lattice of the semiconductors used for the construction of the electronic circuits, which happens because of ‘collisions’ of radiation (particles) with the atoms. The displacement leads to a deformation of the lattice, which can electrically be seen as a defect (or group of defects) affecting electrical performance. It is of little relevance for low-voltage CMOS technologies (used for almost all ASICs in the tracker), which are insensitive to this effect up to even the large radiation levels of HL-LHC, hence it has been labelled as generally little relevant - but there are important exceptions!

Single Event Effects are instead due to the instantaneous interaction of radiation with the device - often traceable to the transit of a single particle. Not every particle (radiation) crossing the device will lead to the same macroscopic malfunction, hence SEEs have to be treated in a statistical manner. For this reason, it is possible to express the sensitivity of a circuit in terms of cross-section, but it is not possible to foresee exactly if and when a failure will happen in the real application: only a probability can be quoted.

- Temporary effects instantaneously affect the correct functionality, but can be recovered. They are due to the charge deposited locally by radiation, which affect either the state of a logic bit of information, or induce a current/voltage spike in the circuit. Their effect might be transparent (no effect, for instance when the information bit corrupted was not used by the circuit), or can be a temporary loss of functionality of the whole circuit (Functional Interrupt, SEFI, for instance when the circuit experiences a reset or switches to a test mode and remains stuck in such state until an external reset is sent).
- Permanent effects are destructive event that actually break something fundamental in the device. The circuit can not recover functionality.

Characterization of the radiation environment in LHC

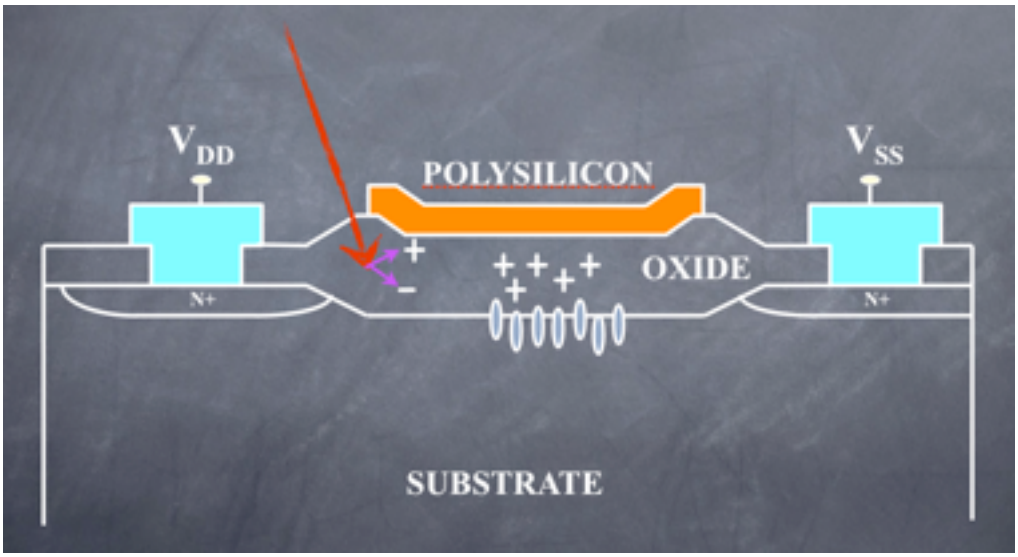
Given the different classes of radiation effects, how is a radiation environment described to enable setting some specifications for the radiation qualification of the electronics components?

- Total Ionizing Dose is due to the energy loss via ionization, and it is very easy to quantify because the radiation effect is known to be very similar regardless the particle that has deposited the dose. If the dose in SiO2 is the same, then the effect is considered the same (this is true to a reasonably good approximation). The environment for TID can hence be described in terms of the energy deposited by all ionizing particles in the unit mass (of Si or SiO2). The unit in SI is the Gray, but the radiation effects community still widely use the former unit called rad. Luckily, the conversion between the two units is straightforward (1Gy=100rad). TID in HL-LHC trackers might reach, according to present estimates, even 800Mrad for the pixel detector and 200Mrad for the strip detector.
- Displacement damage is due to non-ionizing energy loss (NIEL) and is complicated by the fact that the effect depends both on the NIEL of the specific particle (dependent on its type and energy) and on its cross-section for interaction. For this reason, NIEL is often expressed for DD in terms of MeVmb where the MeV is the indication of the NIEL of each interaction while the mb is the indication of the cross-section. It has been experimentally found that DD scales normally rather well, for silicon devices, with NIEL. Therefore, one needs to define a 'reference' particle and energy to describe any radiation environment: damage can then be scaled to that 'reference' environment by applying the correction on the NIEL based on available data. It is common practice to describe the environment in terms of "1MeV equivalent neutrons" (for which a definition of the NIEL has been made). The radiation environment of the LHC experiments is hence made available by simulation studies in this unit, as the fluence of particles with such NIEL over the lifetime of the LHC. This is expected to reach about 5e15 cm^{-2} in the HL-LHC trackers.
- Single Event Effects are due to local deposition of energy via ionization by a single particle. In the LHC environment, the particle environment is dominated by neutrons (and pions in the tracker). In very good approximation, the effect of all hadrons above about 20MeV can be considered as equal for SEUs. Therefore, the environment is well described by the flux of hadrons above 20MeV (10MeV if one wishes to be conservative). This flux could be of the order of 1e7 $cm^{-2}s^{-1}$ in HL-LHV trackers.

Radiation effect	Origin of the effect	Description of the environment
TID	Energy loss via ionization in unit mass	"Gray" (GY) in SI "rad" is still used (1Gy=100rad)
Displacement Damage	Non-Ionizing Energy Loss (NIEL)	particle fluence (= integral of flux in time) in 1MeV neutron equivalent
SEEs	Ionization along a single particle track	particle flux including all hadrons above 10-20MeV

TID effects in CMOS technologies: basic effects on SiO2

TID effects are due to the energy deposited via ionization by radiation in the oxides (SiO2) present in CMOS integrated circuits. Via ionization electron-holes pairs are formed in SiO2. In the absence of immediate recombination, electrons quickly move in the material and leave the oxide, while holes migrate slowly and can be trapped in some pre-existing trapping centre. This creates a net positive charge trapped in the oxide, which affects the electric field across it (for instance, in the case of a MOS structure, it can change the effective threshold of the transistor). This positive charge can be annealed if the hole is de-trapped, which can happen via thermal processes. Migration of holes and other positive species to the Si-SiO2 interface (MOSFET channel) can give origin to the activation of interface states, states available for charge to be trapped at the interface. These trap centers, by trapping some charge, also affect the threshold voltage of the MOS transistor (but might also affect the mobility of charges in the channel).



How much a MOSFET is affected by TID depends on a number of parameters and irradiation conditions, the main of which are:

- Characteristics of oxide: thickness of the oxide, quality, growing method, sintering method, etc. This will have a direct impact on the density of defects and on their energy level (are they easily accessible for free charge to anneal them at low temperature?).
- Electric field in the oxide: at the time of creating the electron-hole pair, this can more easily recombine in case of small electric field. An immediate recombination removes the main origin of TID effects. The electric field strongly influences the migration of charges in the oxide, which is directly related to the evolution of trapping (and interface state creation) during irradiation.
- Temperature: annealing, or detrapping and release of trapped holes in the oxide, is often a thermally activated process. Temperature strongly affects the annealing rate. This is true to some extent also for the interface states, but they require much higher energy to be neutralized.
- Dose rate: for CMOS technologies, the dose rate (or how much ionizing energy is deposited per unit time) is relevant because the higher it is the shorter the time to reach a given TID level. Since annealing is often active already at room T, a high dose rate experiment does not allow annealing enough time to influence the final irradiation result. The same TID accumulated in 1day or in 10years most likely leads to different effect on a MOS device: during the 10years annealing of trapped

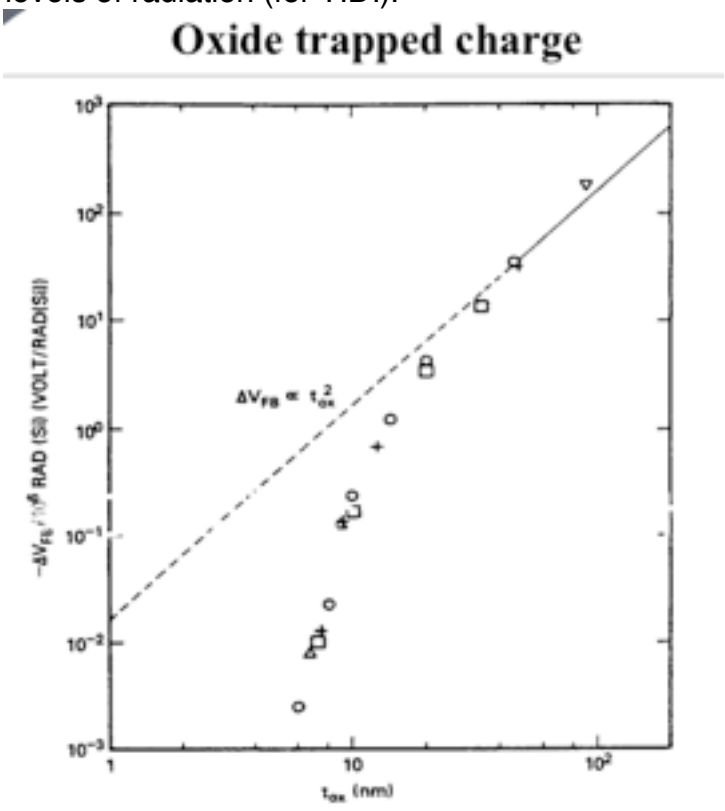
charge has the time to happen, during 1day most likely not. The result will hence be much worst (all radiation-induced charge is still trapped) at high dose rate.

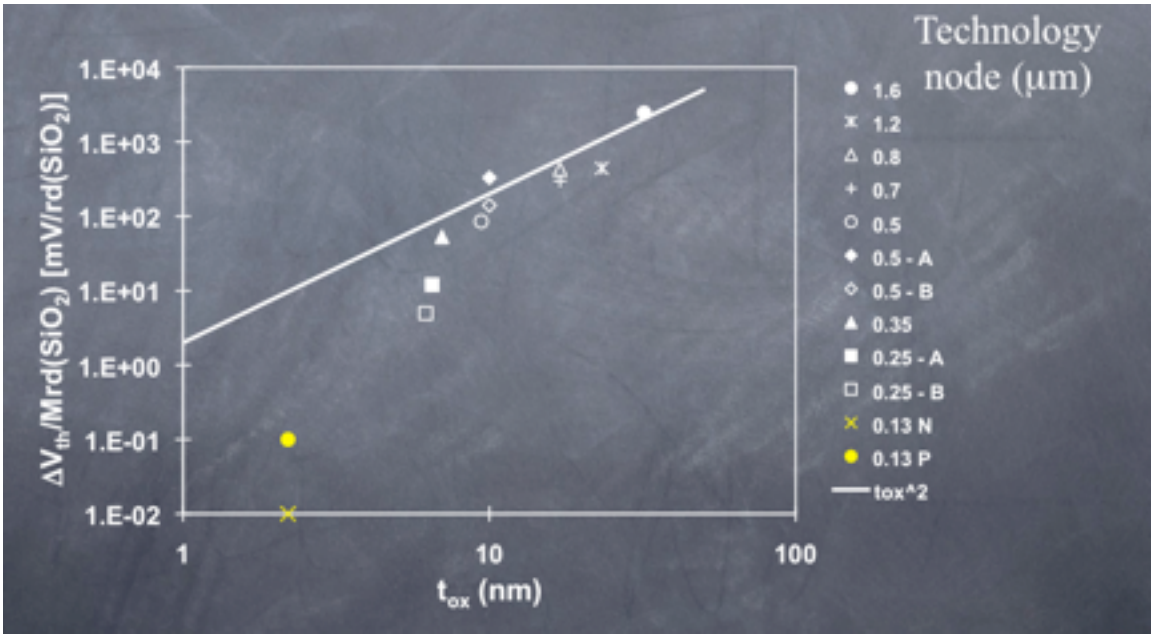
Because of all these dependences, it is important to know precisely what the experimenter wants to evaluate with an irradiation test. If the wrong combination of parameters is chosen, or the interpretation of the results does not keep into account the precise irradiation conditions (and the final application), then this can easily lead to wrong conclusions about the radiation tolerance of a circuit.

TID effects in CMOS technologies: consequences at the circuit level

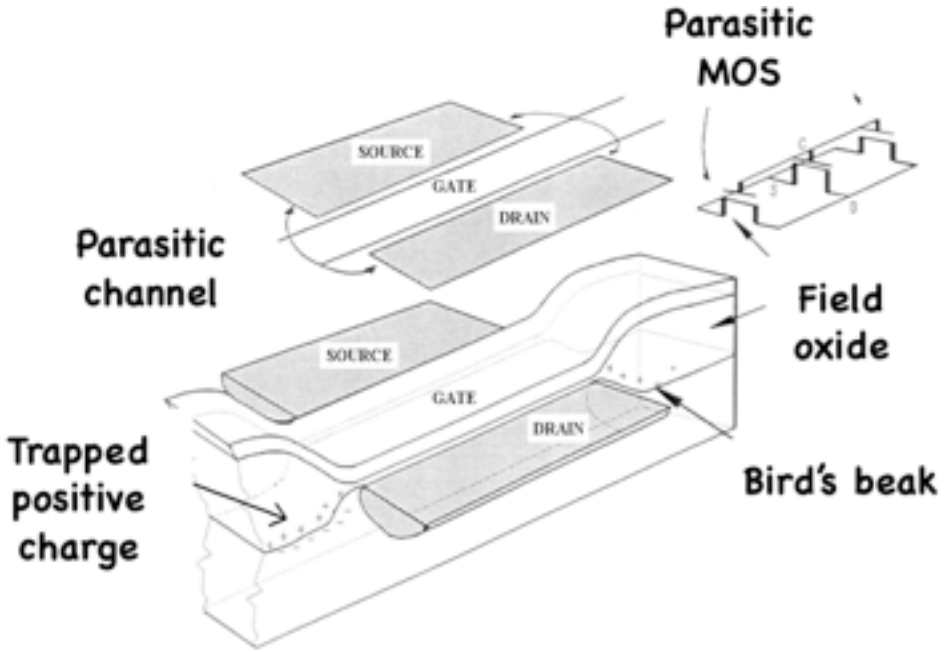
Given that TID influences the oxide used in CMOS technologies, let us see where this can happen and what are the consequences at the circuit level.

First, the NMOS and PMOS transistors used as main building blocks in CMOS technologies rely on a gate oxide for their correct behavior. The gate oxide determines the electrical performance of the transistors to a large extent. Radiation can strongly affect the properties of this oxide, hence impacting the performance of the transistor. This has historically been the case for several decades, and the main limit to the TID resilience of a CMOS technology has been set by radiation effects on the gate oxide. However, already in the middle of the 1980s some experiment run at the American Naval Research Lab showed that the accumulation of defects in an oxide depends strongly on its thickness. As shown in the following picture for the oxide trapped charge (a similar chart exists for interface states), charge accumulation in the oxide drops with the square of the oxide thickness and even more rapidly for tox below about 10nm. This was measured at the time on laboratory-grade oxides, but has been confirmed on commercial-grade oxides later on (see following image with gray background, compiled by the CERN Microelectronics group). It can be concluded that very thin oxides of modern deep-submicron technologies are very resilient to TID effects, and in principle the main MOSFETs can survive very large levels of radiation (for TID!).



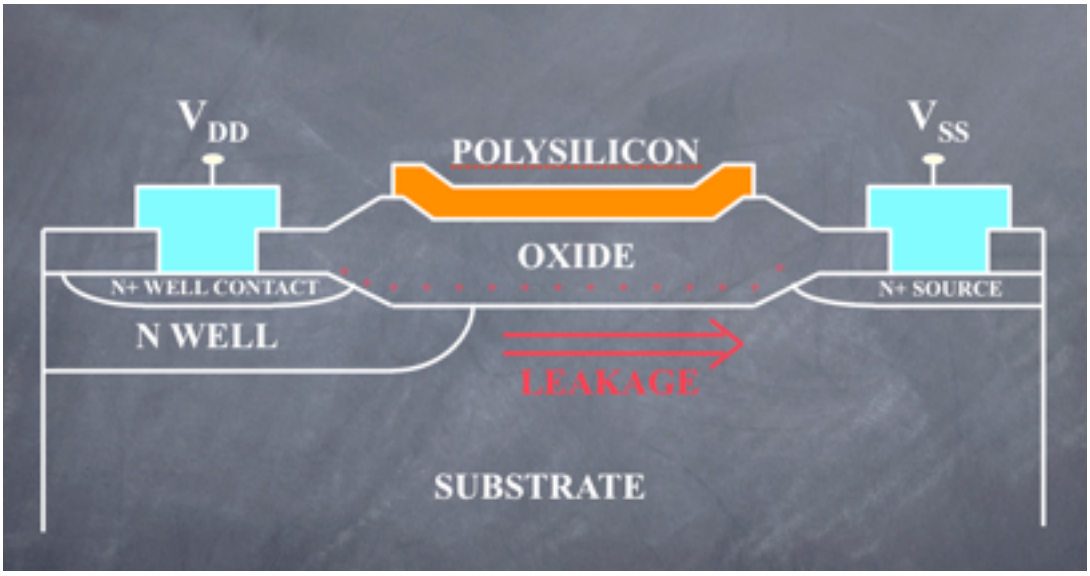


However, this is not the end of the story. Other oxides exist in a CMOS technology and their thickness does not necessarily scale with time. The isolation oxide, LOCOS in the old days and STI today, still make use of rather thick oxides manufactured with processes very different than those used for the gate oxide (thermally grown). Trapping in the thick STI oxide still happens in relevant quantity, and this might have a strong impact on some parasitic structures inherent to the CMOS technologies. For instance, at the edge of a MOSFET transistor the STI oxide is directly in contact with the channel (this region is called bird's beak in the following picture: this was the case in the old LOCOS technology which has been replaced by STI, but the situation has not changed with STI).



Trapping of positive charge in the STI can change the threshold of the parasitic lateral edge transistor, and induce an equivalent leakage current between source and drain (only in NMOS transistors, since the trapped charge is always positive). This current flows beyond the control of the gate.
Leakage current can also flow, for a similar mechanism, between adjacent n+ diffusions (or wells) at different potential. In the example below, an n-well biased at Vdd leaks current

towards the source of an NMOS transistor connected to Vss. The parasitic transistor turning on is under the isolation oxide (STI), where a sizable amount of holes accumulate with TID. The presence of an electric field, due to a polysilicon routing connection in the figure, worsens the situation.



Overall, while the gate oxide is getting thinner with newer technology nodes the main N and P-channel FETs gate more resilient to TID but this is not sufficient to render a circuit radiation tolerant. The weak point is now the radiation-induced leakage current in NMOS transistors, and between n+ diffusions. Typically, this will lead first to an increase of the current consumption of the circuit, and possibly to its failure. The level at which this happens is strongly technology dependent.

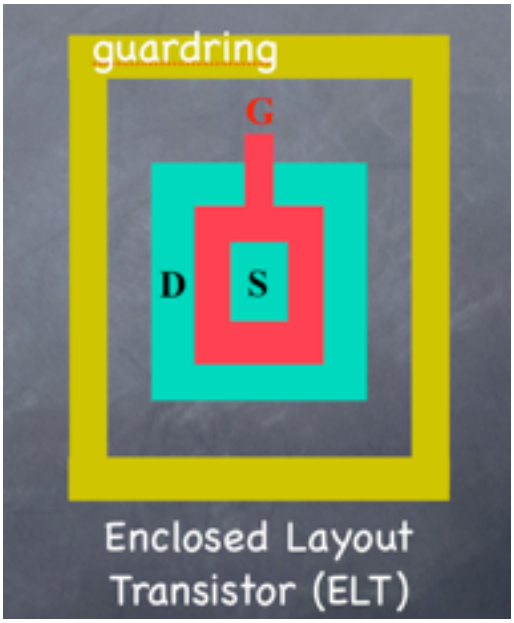
How to mitigate TID-induced failure mechanisms in CMOS

In order to mitigate TID effects, it is sufficient to avoid leakage current to flow between source and drain, and between n+ diffusion. The former leakage path can be suppressed by eliminating the edge of the NMOS transistors, where thick STI enters in contact with the transistor's channel. The most straightforward way of doing so is by 'enclosing' the drain (or source) of the transistor with the polysilicon gate, as shown in the figure below. This transistor has been called ELT, Enclosed Layout Transistor, and it has been shown to eliminate the source-drain leakage induced by TID (verification done in a large number of technologies in different nodes between 0.7 and 0.065um node).

To prevent the formation of leakage current paths between adjacent n+ diffusions (or wells), it is possible to systematically enclose diffusions to be isolated with a p+ guardring. This guarding is so heavily doped that the charge trapped in the overlaying oxide can not invert it, hence it can not form a conduction channel between n+ diffusions. Also this method has been verified in a number of technology nodes.

The combination of ELT NMOS transistors and guardrings, which is a technique to obtain Hardness By Design (HBD), has however some inconveniences, or at least imposes some constraints to the designer wishing to use this approach. First, the SPICE transistor models provided by the foundries are not valid for the ELT design, and a way to compensate for that has to be found (the minimum precaution is to have a model to compute an 'equivalent' transistor size, or W and L, so that the standard geometry SPICE model can reproduce the current of the ELT). Digital libraries made available from the foundry do not use HBD, and hence can not be used: a digital library with custom ELT transistors and guardrings has to be developed for even small complexity digital design to

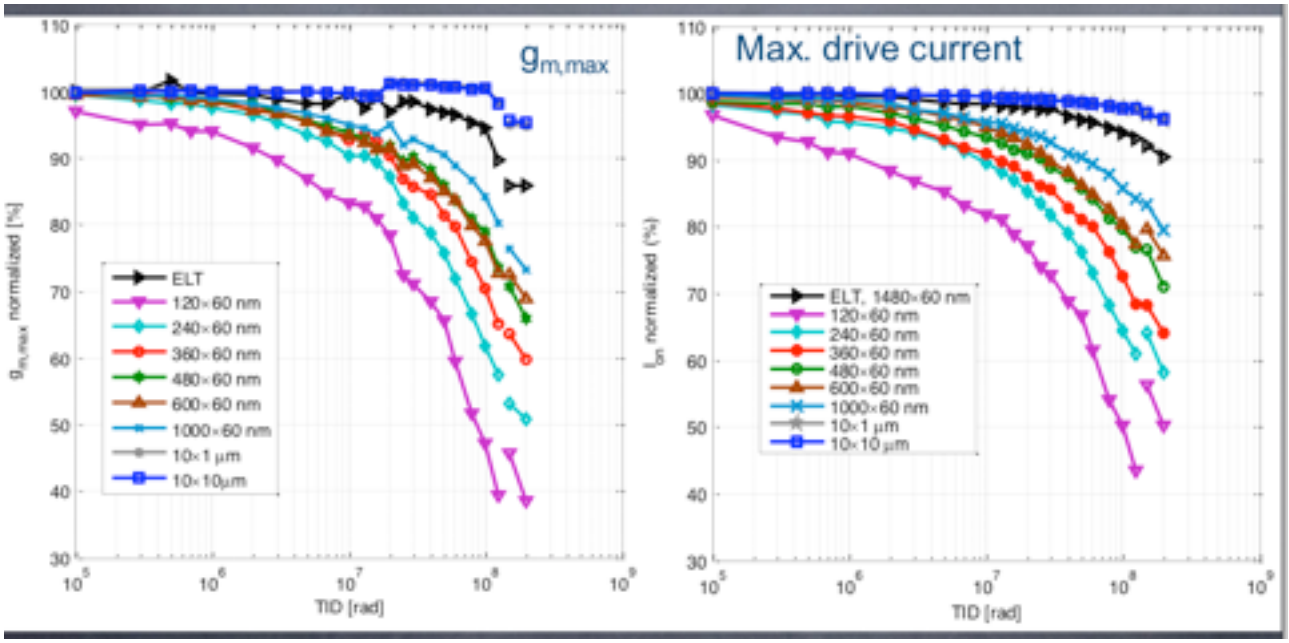
be possible. Compared with standard layout, this HBD approach leads to a relevant loss in achievable density, which translates in higher cost and smaller integration capabilities. Despite these drawbacks, the approach has been extensively used to design ASICs for the LHC experiments (in a quarter micron technology) in what is still today the larges application ever of HBD. About 3000 wafers with more than 50 different designs have been produced this way, and circuits are running today in the LHC experiments in almost any location.



In preparation of LHC detector upgrades, the HEP community is today looking at more advanced technologies in the 130 and 65nm nodes for the development of the ASICs to be employed in tracker modules. Is it possible to find technologies that do not require HDB techniques to be used, still obtaining the required TID tolerance?

The 130nm technology node has been studied for TID effects first, starting from about 2001. As expected, the gate oxide tolerance is very large: threshold voltage shifts of tens of mV are observed at TID levels of 100Mrad or more - only the PMOS transistor seem to have a significant Vth shift at very large TID levels (400Mrad or more). While this is a general behavior of all probed processes (from 3 manufacturers), the radiation effects in STI appear to vary considerably. A source-drain leakage current is observed in some technologies, while being almost negligible in others. Trapping in the lateral STI also affects, for narrow channel transistors, the apparent Vth of the main FET (this effect has been called Radiation-Induced Narrow Channel Effect, RINCE). Also the annealing impact on the final irradiation result varies with the probed CMOS process. As a consequence, we concluded that - in a chosen technology - it is possible to avoid the systematic use of HBD techniques provided narrow channel transistors are not used. The chosen technology requires however to be probed regularly for possible changes in the radiation resilience due to process modifications - which might not be announced by the manufacturer.
The 65nm technology node has been studied for TID much later, and still requires some additional exploratory work (results can be found in the linked paper by S.Bonacini et al., http://iopscience.iop.org/1748-0221/7/01/P01015/). However, the process we studied (from a single manufacturer) looks to be even more resilient than the 130nm. The Vth shift of the NMOS is negligible up to 200Mrad at least, with leakage being evident (but rather small) only for the very narrow channels. For PMOS, the Vth shift is small but observable (50-60mV for narrow channel at 200Mrad). The largest impact on the electrical parameters

of the transistors is observed for the transconductance (gm) and current drive of the PMOS at large TID levels (see figures below).



The same conclusion about the need for HBD can hence be drawn for the 65nm. In both 130 and 65nm nodes, it is important to consider that the above conclusion holds for core transistors, while I/O transistors rated for larger Vgs and Vds might still require HBD to satisfy the TID requirements of the trackers.

Displacement Damage in CMOS

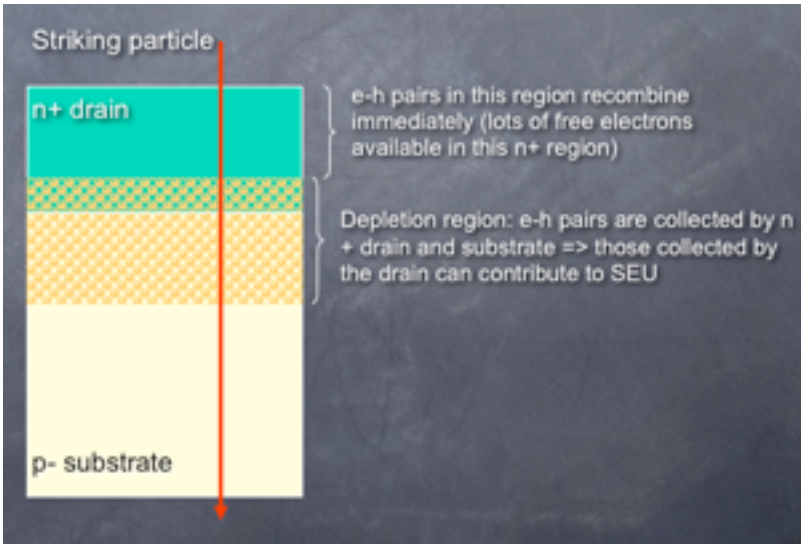
As already mentioned, CMOS FETs are known not to be sensitive to DD even at the large particle fluence of LHC trackers. However, some of the circuits developed in standard CMOS, or in specialized versions of it, might still be sensitive. The main example concerns the LDMOS transistors (Lateral Diffusion MOS) used for increasing the Vds rating of CMOS transistors in technologies developed on purpose for Power Management. These technologies are used in developing devices used in power distribution schemes attractive for use in upgraded LHC detectors, such as DCDC converters. LDMOS transistors have recently been observed to decrease considerably their current capability with displacement damage, and this technology-dependent effect might limit the maximum radiation hardness of power management circuits in the future.

Another device that is possibly affected by displacement damage, and that is extensively used in HEP front-end circuits, is the diode used in bandgap reference voltage generators. This basic circuit block is needed to provide a stable reference voltage on-chip, and is used in practically all large circuits as a reference whenever a relatively prices current or voltage has to be generated on-chip. Some recent data suggest that, in some implementations of the bandgap reference circuit and in some technologies, displacement damage in the diode can induce a large shift in the bandgap reference voltage. This has still to be confirmed, and appears to be largely technology dependent.

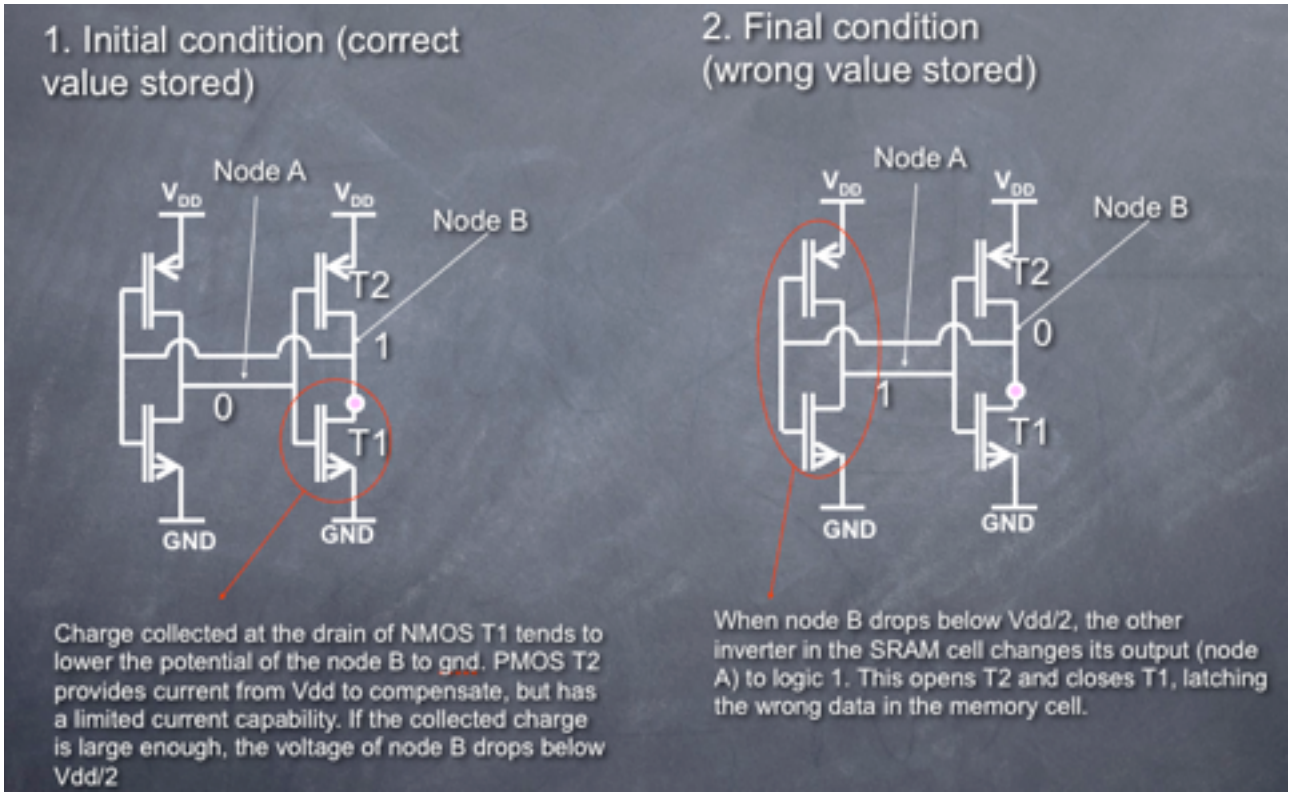
A similar problem also affects, possibly in even larger measure, parasitic bipolar transistors made available in some CMOS processes for some specific application (in particular, often for bandgap reference voltage generators). Also in this case, sensitivity of the bipolar to DD might render the CMOS circuit using it very sensitive as well.

Single Event Effects
As already explained above, these are traceable to the instantaneous release of charge in the electronics device, typically by the interaction of a single particle. Their consequences might be temporary or permanent.

Temporary Single Event Effects: SEU (Upset)
SEU happens in digital circuits when a node collects charge from a particle strike and changes its logic state as a consequence. This requires that the ionizing particle crosses the depletion region of a node which is storing a logic value, typically the drain of a transistor (either PMOS or NMOS). In the image below, this is shown for the drain of an NMOS transistor. A particle transits and ionizes along its path in the semiconductor: the particle needs to have a relatively large dE/dx (linear energy transfer) to induce sufficient electron-hole pairs to be created along its path. In the highly doped drain, density of charges is so large that all e-h pairs practically recombine. However, in the depletion region electron and holes migrate following the electric field, and a net charge is collected at the drain (current). Depending on the doping concentration in the substrate, the charge collection region can extend beyond the depletion region: in fact the depletion region is modified instantaneously by the high density of charge deposited by the particle (mechanism that is known as funneling). All the charge collected at the drain, if not quickly removed, will induce a voltage spike at this circuit node.



How this leads to an SEU is explained now for the specific case of a cross-coupled pair of inverters, similar to the configuration in a basic SRAM cell, but can be extended easily to other memory architectures or to registers (DFF, latches).
In the figure below, node B is storing a logic 1: its potential is Vdd. The drain of the NMOS T1 is biased at Vdd and its junction to the substrate is biased (depletion region). In this condition, a particle must deposit charge in the drain of T1 for an SEU to be possible. The charge collection is an instantaneous current at the drain that, if not removed by T2 (which has a limited current capability), will decrease temporarily the potential of node B. SEU happens because of the feedback mechanism in the memory cell: in the absence of this feedback the circuit will experience a transient (SET) that can propagate to the next logic gate. Because of the feedback, the voltage fall of node B - the input of the other inverter - determines also the change of node A, which in fact opens T2 and closes T1 and ‘latches’ the transient in the memory cell. This can be seen as a competition between the current capability of T2, trying to remove the charge, and the other inverter which tries to latch the transient voltage drop.

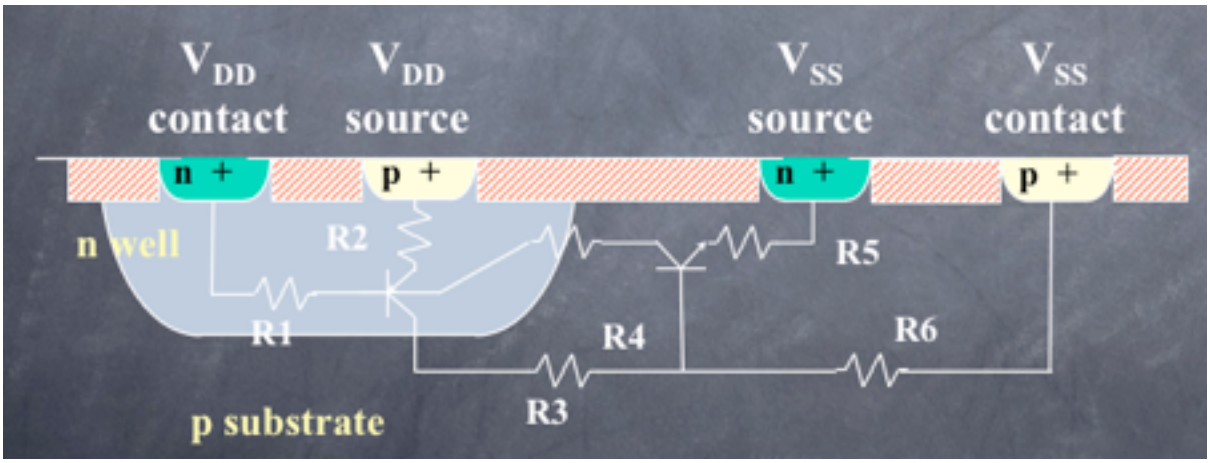


Once the cell has changed state, the consequences of this SEU on the full circuit functionality depends on the specific memory bit (or register) that has been affected. In some cases, this could be an unused memory bit: this will be transparent to the user. In other cases, one bit of information is corrupt and leads to an error in a computation. In the worst case, this could be a bit of information determining the program running on an FPGA, or determining if the circuit is in test mode. In these cases, the full functionality of the circuit might be lost until the user intervenes to re-establish the correct value (reset). This latter case is labelled as a functional interrupt (SEFI).

Temporary Single Event Effects: SET (Transient)
The same charge collection mechanism explained above, when happening in an analog circuit, might induce a voltage-current transient of variable duration. In OTAs or other amplifiers, for instance, this could translate in a rail-to-rail transient at the output. The consequences on the analog circuit depends strictly on its function and on the hit node.
A SET happening in a combinatorial logic gate gives origin to a Digital SET (or DSET). The voltage spike might propagate through the combinatorial logic, and eventually reach the input of a register: if this happens during sampling (in sync with the clock), then the transient can be latched in the register. Increasing the frequency of the clock, the probability of latching a transient increases and in some experiments the observed error rate is linearly dependent on the frequency.
Propagation of DSET in combinatorial logic was not a major problem in the past: the voltage spike typically lasted 1ns or less, and was filtered by the RC of the gates, so it could not propagate. Today, the time delay of the gates is so short that even 100ps pulses can easily propagate - actually in some experiments they even widen their time duration during propagation, reaching or exceeding 1ns.

Permanent Single Event Effects: SEL (Latch-up)
Amongst the different permanent SEEs susceptible of destroying electronics devices/ circuits, the only relevant one for low-voltage CMOS is SEL. This is the turning-on of a

parasitic thyristor structure inherently present in all CMOS technology. The thyristor is composed by two bipolar transistors - an NPN and a PNP - connected so that the emitter of the first is the base of the second (and the other way round). The following figure shows the structure: it is composed by the nwell hosting the PMOS transistor (with its own n+ diffusion to contact the well), the p+ source of the PMOS, the substrate contact (p+ doped in a p-doped substrate) and the n+ source of a NMOS transistor. The first two diffusions are connected to Vdd, the latter two to Vss. A vertical PNP transistor is formed by the p+ source, the nwell and the substrate. A lateral NPN is formed by the n+ source, the substrate and the nwell. The collector of the PNP, the substrate, is also the base of the NPN while the collector of the NPN, the nwell, is also the base of the PNP. However, for this structure to be detrimental we have to consider also the resistance between the effective electrodes of the parasitic bipolars and the n+ or p+ diffusions that try to keep their potential steady. When charge is deposited by a particle, this is collected by the existing electric fields and gives origin to currents which, along the relatively large parasitic resistances, will determine locally large voltage spikes.
For instance, a particle hit in the nwell-substrate depletion region creates a transient current to the Vss p+ substrate contact. Along R3 and R6 this current locally increases the voltage of the substrate in the region between the n+ source and the nwell, which is the base of the parasitic NPN. If this voltage spike exceeds about 0.7V, the bipolar turns on and inject current in its collector (nwell). This current has to be collected by the nwell contact, and through R1 increases the local voltage of the well under the p+ source. This is the base of the vertical PNP bipolar. If this voltage exceeds about 0.7V, this bipolar injects more current in the base of the NPN. This mechanism can continue until both bipolar transistors remain in the on state and a large current flows between their emitters (Vss and Vdd). The latch is active and will remain so until the power supply is interrupt (power cycle); if the power is not interrupt quickly this current might exceed the capability of metal lines to carry it and create excessive heat, ultimately leading to the destruction of something (metal line, bonding wire, ...).



SEL is probably getting less likely in modern technologies, although the designer should be careful not to increase this probability by inappropriate design. The decrease in the Vdd gives less space for the series of two bipolar transistors to keep on (at least two base-emitter junctions have to be forward biased). Also, modern technologies use triple wells with retrograde profile which decrease considerably the parasitic resistances to the base of the parasitic bipolars. However, a bad design practice (excessive distance between well contacts and any point in the well) might still expose the circuit to SEL susceptibility: it is important that the designer maximizes the density of well and substrate contacts, in particular in the frontier between the well and the substrate.

Susceptibility of 130 and 65nm technologies to SEEs

Recent experiments on the 130 and 65nm technologies used for LHC tracker upgrades have allowed to measure their sensitivity to SEU (results can be found in the paper from S.Bonacini et al. in the following link: http://iopscience.iop.org/1748-0221/7/01/P01015/). These experiments are based on D-Flip-Flop (DFF) and/or SRAM circuits, and have been conducted using Heavy Ions (particles with very large and well known dE/dx, allowing to estimate precisely how much charge they deposit in the depletion region of the sensitive nodes, and to change it at wish by changing the ion species used in the test).

Since any particle hitting an integrated circuit has a given probability of provoking an SEE, the experiment aims at evaluating this probability: the total number of observed events is counted and its ratio with the total number of particles hitting the device is computed. This parameter, called 'cross-section' (sigma) contains the information on the sensitivity of the circuit. Once the sensitivity is known, it is possible to estimate the rate of SEE in the real radiation environment by multiplying sigma by the flux of particles in the application. This requires that the same particles (with the same energy spectrum) are present in the experiment and in the real radiation environment, which is almost never possible. It is however possible, thanks to the approximate validity of some hypothesis on nuclear interaction probabilities, to use the available irradiation facilities (proton or Heavy Ion beams) to measure sigma and then estimate the error rate in the more complex environment of the LHC experiments. The full methodology to do so is presented in the paper: M.Huhtinen, F.Faccio, "Computational method to estimate Single Event Upset rates in an accelerator environment", Nucl. Inst. and Meth. in Physics Research A 450 (2000) 155-172).

$$\sigma = \frac{\text{N of SEEs}}{\text{integrated flux during the experiment}}$$

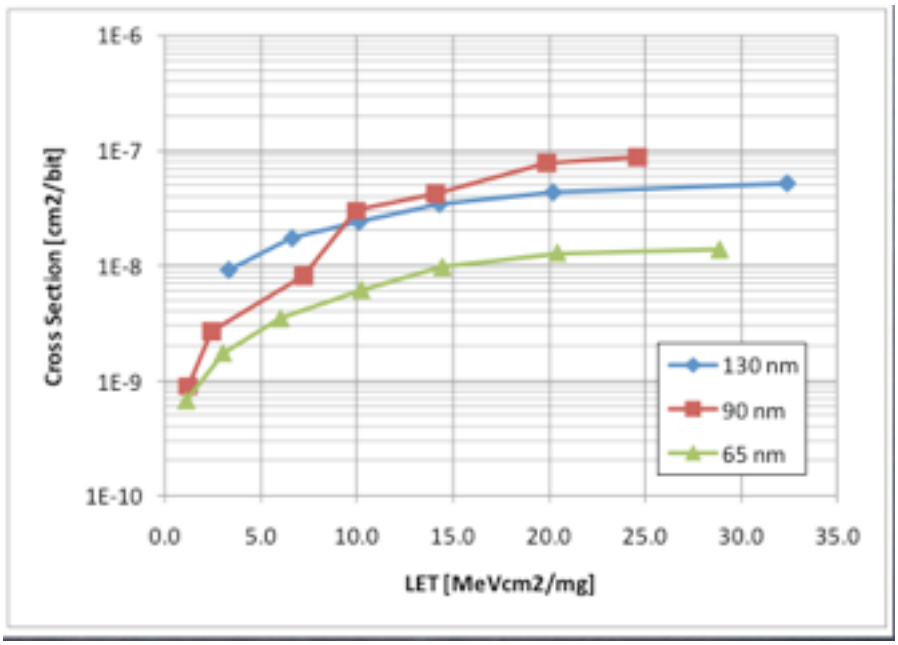
General considerations can be made on the sensitivity of the 130 and 65nm technologies to the different classes of SEEs that have been described above. Because of the small Vdd and capacitance of the nodes storing the logic information, memories and registers in these technologies are expected to have a rather large sensitivity to SEU (very little charge needs to be collected to change the logic state of a node). Also sensitivity of combinatorial logic to DSET is expected to be large: due to the rapidity of logic gates there could be no filtration of the DSET which can easily propagate along even long chains of gates. However, the nodes are small in size and hence the individual sensitive node presents a smaller target area to the incoming particles, which could decreases somewhat the sensitivity of individual nodes to SEU and DSET. Design methods to protect the logic cells from these effects will be described later.

The sensitivity of analog circuits to SET is difficult to generalize, since it is very heavily circuit dependent. In general, this sensitivity can be important in 130 and 65nm technologies which are fast (no filtering of SETs) and have small node capacitance: analog designer should hence systematically try to address the possible sensitivity by analyzing which node is critical for SET and protecting it or the rest of the circuit from the possible consequences of SET.

SEL should not be an excessive worry in these technologies and for application in LHC trackers. Due to the reduced Vdd and to the high well doping, these technologies are well armed against SEL, but again designers should be careful to avoid increasing the sensitivity by improper layout: frequent and well distributed substrate and well contacts have to be used across the circuit.

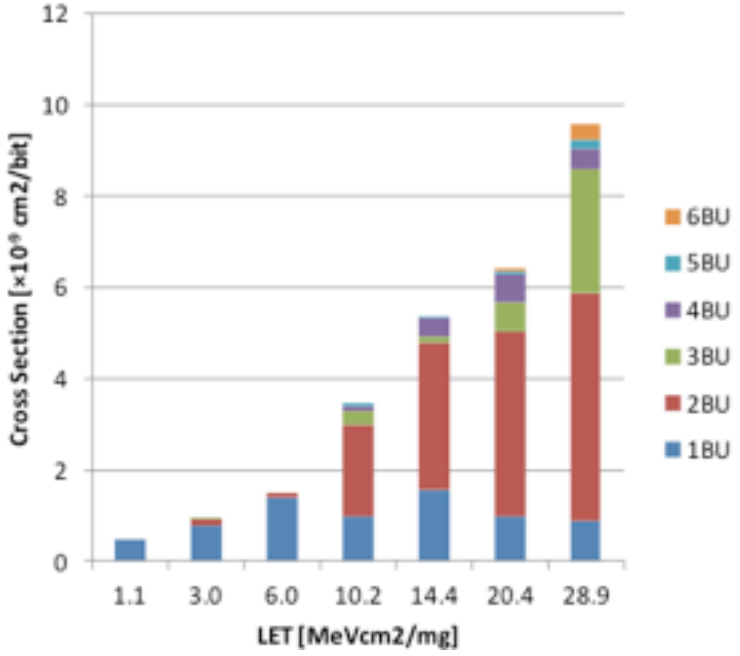
	Probability	Prevention
SEU, DSET	Large (small charge needed for SEU because of small Vdd)	Hardened cells; triplication and voting; redundancy
Analog SET	Very dependent on circuit configuration	Increase the capacitance of crucial nodes, or current in the circuit; limit consequences on core circuit functions
SEL	Small (because of small Vdd and higher doping in wells)	Use frequent well and substrate contacts

We can now leave the generalizations and look the results from the characterization of 130 and 65nm technologies DFF and memories, which has been done using a Heavy Ion beam. In this experiment, sigma for SEU is measured for different species of Ions which have different and well known dE/dx: the result is hence a curve where the cross-section is plotted against linear energy transfer (normalized to the silicon density, hence expressed in $MeVcm^2mg^{-1}$). The figure below shows the available results for DFF in three technology nodes (standard cells from commercial libraries have been used for 65 and 130nm, while for the 90nm a custom cell has been developed). To estimate SEUs in the LHC environment, the interesting portion of the curve is the one up to an LET of 15. For all technologies, the threshold LET (below which no SEU is observed) could not be measured, since all designs had SEUs for all used ions. This sensitivity is considerably larger than the one observed for the quarter-micron DFF used in the design of ASIC presently installed in the LHC experiments, and we can expect hence a larger error rate in these newer technologies. However, it looks like the error rate per bit could be smaller for the 65nm technologies than for the 130nm.



One additional and very relevant consideration to be added when comparing the estimated SEU sensitivity with the one observed today in our quarter-micron ASICs concerns the occurrence of multiple bit errors (MBU). The size of the individual memory cell is so small

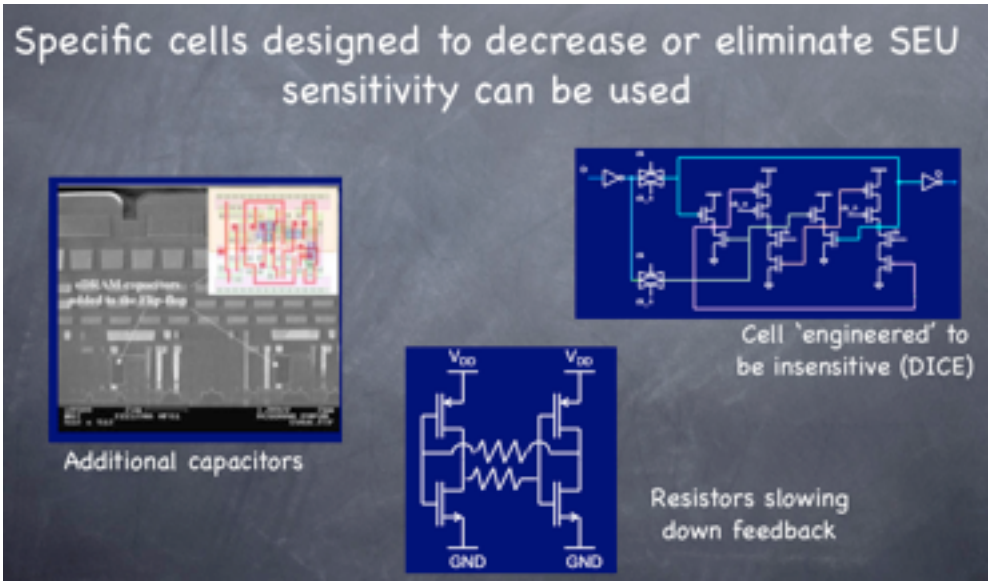
in these technologies that several adjacent cells might collect the charge deposited by a single incoming particle. Since the charge required for SEU is small, the fraction collected by every cell can be sufficient to upset the cell: in that case, several cells can get their content corrupted by a single particle hit (MBU). The sensitivity to this even increases for denser technologies, and the following chart obtained for the 65nm technology (SRAM) is very eloquent. Already at an LET of 10 most of the observed SEUs occur in pairs - in two neighbor cells.



Hardening techniques against SEU

SEU being such a relevant problem in these advanced technologies, it is important to be aware that some remedies are available to the designers. The aim, it must be remembered, is to lower the system unavailability or unreliability, so some of the approaches are based on system-level redundancy rather than on modifications of the memory cell itself. However it is certainly possible, and it is a used solution, to harden the cell by modifying it. Techniques used in this direction include the increase of the capacitance of the storage nodes, slowing down of the feedback path via additional resistors, or complete modification of the working principle of the memory cell (the most commonly used cell in this sense is the DICE). The latter approach normally relies on a duplication of the information within the cell where the feedback mechanism is only active during the cell writing. However, this is getting less efficient in modern technologies where the cell is so small that it is difficult to prevent charge collection from the same particle strike in both nodes.

Another approach very frequently used is the triplication of the information in the form of real triplication of the memory cell. The three cells have to be positioned sufficiently far apart to prevent that two of them are corrupted by a single particle strike. The output of the three cells is then voted before passing the value to the next logic stage. Since the voter itself could be affected (by an SET), in some cases the voter is triplicated as well. To prevent accumulation of errors in time, it is necessary to regularly refresh the contempt of the cells, which could be done by a feedback mechanism from the voters. Finally, in some applications it is possible to combine the cell and the voter in one only and more compact cell, especially when dynamic logic is used (we had this need when designing a fast circuit whose speed specifications could not be met by static logic).



The triplication and voting can be implemented also while designing logic circuit with the help of synthesizers (functional description of the circuit in some behavioral language followed by automatic place & route): in this case one should check that the optimizer will not remove the redundancy which in this case is a desired feature.
An alternative hardening technique, more at the system level, is to limit the redundancy to only the addition of a few bits rather than triplicating each bit. This is more efficient in terms of memory space, but requires encoding and decoding - which are rather complicated logic functions needing themselves to be protected. While encoding, each data word is extended by a number of bits (parity is the simples example) that help the system understand if some of the word bits have been corrupted. Depending on the complexity of the coding algorithm, the system might be capable of only detection or also of correction of a variable number of bits. This technique is used for memories and, in the upgrade of LHC detectors, for optical data transmission.

Conclusion

In view of ASIC design for LHC tracker upgrades, 130 and 65nm CMOS technologies are the favorite candidates today. The chosen manufacturers for ASIC fabrication in these 2 technology nodes provide devices which are naturally rather insensitive to TID: we can today plan not to systematically need HBD design against TID effects. This means that, with respect to the work done in the past in the quarter micron technology, a simpler design methodology will be affordable - with some important exceptions.
On the other hand, designers have to be aware that SEU and SET sensitivity in these technologies is rather large, and that MBUs are a real threat. Techniques to moderate the SEU rate have to be qualified and used, while attention has to be devoted to avoid designs enhancing possible SEL vulnerability.
It should be reminded, however, that the cost profile for the development and production of ASICs in this technology is different than the one typical of the quarter micron process used 10 years ago. Today, and in particular for the 65nm node, the dominant cost for the typical ASIC to be used in LHC upgrade is represented by the non-recurrent engineering charges (NRE) rather than the mass production. The HEP community has therefore to expand and maintain its knowledge on circuit design and radiation effect in order to limit the prototyping cycles to just 1 or 2 iterations, and produce working silicon qualified to the specified radiation effects without the need for a large number of redesigns.