

Open Hardware at CERN

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BE-CO Hardware and Timing section
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Outline

- 1 Introduction to Open Hardware
- 2 The Open Hardware Repository
- 3 Legal Aspects
- 4 Economics
 - Case studies
 - Experience with Industry
- 5 FOSS for Open Hardware
- 6 Conclusions

There is an OSHW definition!

Check out <http://www.oshwa.org/definition/>

- Inspired by the Open Source definition for software.
- Focuses on ensuring freedom to study, modify, distribute, make and sell designs or hardware based on those designs.
- Now we know exactly what we mean when we say OSHW!

Dispelling the commercial vs open myth

	Commercial	Non-commercial
Open	Winning combination. Best of both worlds.	Whole support burden falls on developers. Not scalable.
Proprietary	Vendor lock-in.	Dedicated non-reusable projects.

Why we use Open Hardware 1/2

Get a design just the way we want it

We specify fully the design.

Peer review

Get your design reviewed by experts all around the world, including companies!

Design re-use

When it's Open, people are more likely to re-use it.

Healthier relationship with companies

No vendor-locked situations. Companies selected solely on the basis of technical excellence, good support and price.

Why we use Open Hardware 2/2

Dissemination of Knowledge

One of CERN's key missions!

Spend money where you or your funding agencies want

- Makes life easier for public institutions
- Opens the door to smaller companies with good local support

Open Hardware Repository – ohwr.org

A web-based collaborative tool for electronics designers

- Wiki, News
- File repository
- Issues management
- Mailing list

Fully open access

- All information readable by everyone, without registration

Platform made itself of open software

- ChiliProject (a fork of Redmine)
- SVN/GIT for version management, integrated in OHR
- Sympa mailing list manager

Example of an OHR project

[HOME](#) [MY PAGE](#) [PROJECTS](#)

Logged in as erikval

FMC PROJECTS » SIMPLE PCIE FMC CARRIER (SPEC)

[OVERVIEW](#)[ACTIVITY](#)[MAILING LIST](#)[ROADMAP](#)[ISSUES](#)[NEW ISSUE](#)[NEWS](#)[DOCUMENTS](#)[WIKI](#)[FILES](#)[REPOSITORY](#)[SETTINGS](#)

OVERVIEW



A simple 4-lane PCIe carrier for FPGA Mezzanine Cards (VITA 57). It has memory and clocking resources and supports the White Rabbit timing and control network.

- **Detailed project information**
- Subprojects: **Software support for the SPEC board**
- Status: Beta
- Licence: CERN OHL

OHR Status

June 2013

Projects

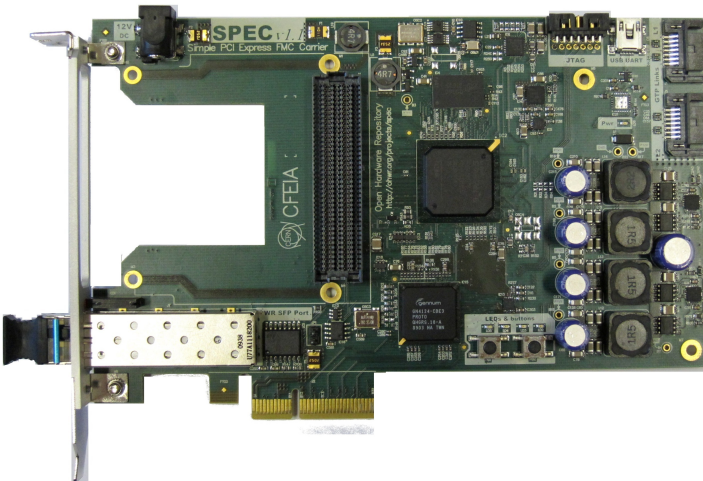
- 123 projects
 - 70 initiated by CERN groups, 53 by other institutes
- 165 active developers, many more users

Types of designs

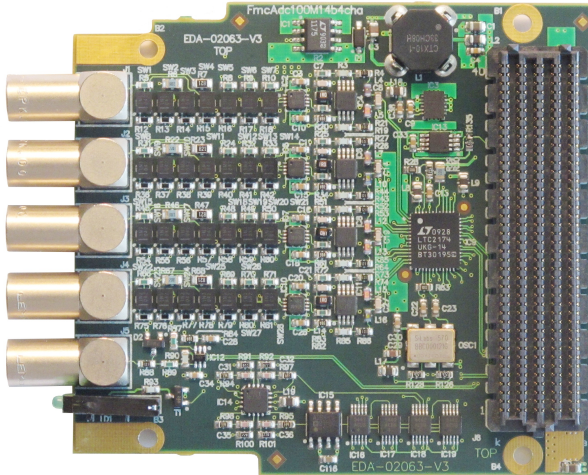
- Around 60 hardware designs
- Around 20 re-usable HDL cores
- General tools like
 - Production test environment (Python based)
 - ADC performance test

Designs are fully documented: OHR is a great place to learn electronics!

PCIe FMC carrier



FMC mezzanine: 100 MSPS 14-bit 4-channel ADC



CERN Open Hardware License – ohwr.org/cernohl

Provides a solid legal basis

- Developed by Knowledge Transfer Group at CERN.
- Better suited than non-HW licenses (GPL, Creative Commons. . .)
- Defines conditions for using and modifying licensed material.

Provides a clear legal environment

- Written in a clear, concise style.
- Easy for licensors to evaluate if this is good for them.

CERN Open Hardware License – ohwr.org/cernohl

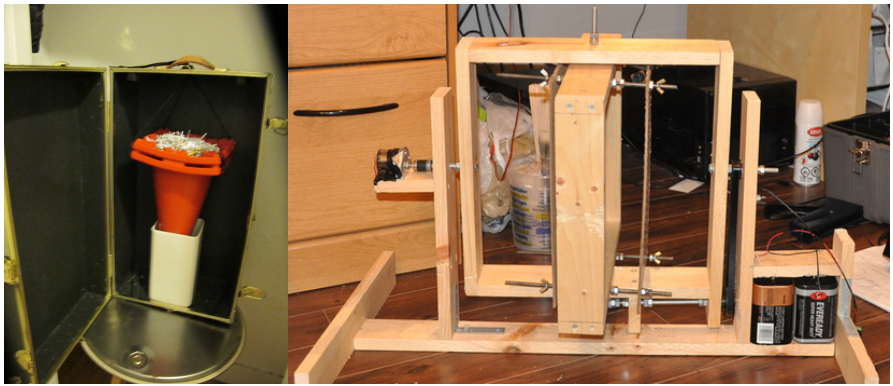
Inspired by FOSS licenses

- Anyone can see the source (design documentation).
- Anyone is free to study, modify, manufacture and share.
- Any modification and distribution must happen under same license.
- Persistence makes everyone profit from improvements.

Takes into account hardware production and distribution

- When producing and distributing licensee is invited to inform the licensor.
- Distributed HW must come with documentation.

Example of mechanics licensed with the CERN OHL



Worm farm and rotocaster

Some key ideas 1/2

It's about Free as in "Freedom"

- People need to make a living!
- Most successful FOSS projects have paid developers.
- Companies help ensure projects are not based on unpaid work (good for scalability).

We live in a world of creative abundance

- Some business models are incompatible with OSHW. So be it.
- Find a good company that suits your needs without compromising openness.
- Buy design, hardware and support.

Some key ideas 2/2

OSHW forces you to design better

- Other people will commercialize what you design.
- Lots of documentation needed.
- Testing gear and (automated) procedure is a must.
- Using standards is very important.

When in doubt, look at FOSS!

- Software people have worked many things out through the years.
- Most of the arguments, business models, etc. apply directly to OSHW.

Case study – SPEC – Simple PCI Express Carrier

We started with a complex design

- Our first FMC carrier design
- Wanted to have lots of timing things on it
- Wanted it to be very flexible: one design does it all

And got results

- We built a few prototypes
- Actually a bit overdesigned, too complex and expensive

Case study – SPEC



PCIe FMC Carrier (PFC)

Case study – SPEC

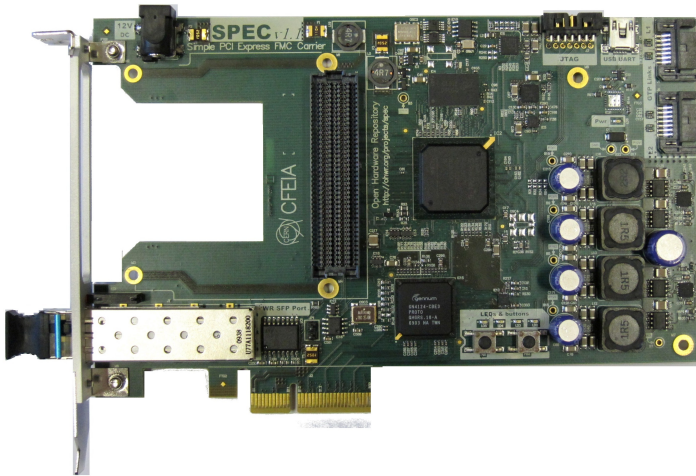
Too complex, so we wanted to have a simpler board

- Simple PCI Express Carrier (SPEC)
- Basically remove components from old design
- Optimize with new knowledge and re-layout

Industry got in

- We didn't have time to do the work
- Hired a small company (<15 persons)
- Review, review, review (specifications, schematics, PCB)
- CERN's design office generated final production files
- Used ohwr.org for all documentation

Case study – SPEC: Simple PCI Express FMC carrier



6-layer PCB instead of 12 on the PFC

Case study – SPEC

Make it a testable product

- Developed an FMC connector test card
- Developed a re-usable test environment (using Python)
- Developed go/no-go test suite

Redesign: V1, V1.1, V2, (V3,) V4

- 65 Issues registered and tracked in ohwr!

First series of 70 boards (production, guarantee)

- Solid specification, IPC norms for PCB fab and assembly
- Price Enquiry to 7 companies *having already PCIe products*. Boards received at CERN June 2012.

Case study – 100 MSPS 14-bit 4-channel ADC

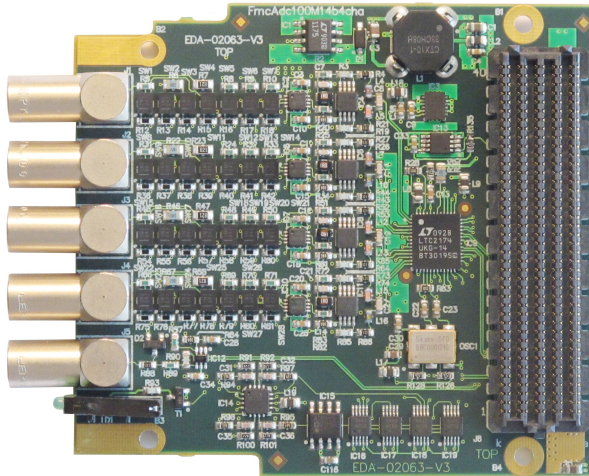
Design

- Designed by a CERN student.
- A small specialist firm designed the front-end.
- Review, review, review.
- Design process well documented (mails, documents).
- 56 Issues documented.
- 4 prototype versions, produce V5.

CERN Price Enquiry for 40 boards (production, guarantee)

- Price Enquiry to five companies *that produce ADC boards*
- Useful design feedback (schematics and PCB layout) from winning company. Boards delivered in January 2012.

Case study – 100 MSPS 14-bit 4-channel ADC



Case study – 100 MSPS 14-bit 4-channel ADC

Potential users who contacted us

- BPM Linac4 (CERN BE/BI)
- Frame grabber for BSRT emittance meter (CERN BE/BI)
- PSB pick-ups (CERN BE/BI)
- Septum. Booster Trajectory Measurement (CERN TE/ABT)
- OASIS general purpose (CERN BE/CO)
- Italian Hadron Therapy Center, BPM system (CNAO)
- Agata experiment (INFN, PH/UCM)
- Culham Center for Fusion Energy (CCFE)
- Advanced Photon Source (Argonne National Laboratory)
- Radio Telescope (Oregon State University)

Experience with Industry

Product Design

- Needs additional effort to make CERN designs a Product.
- Particular effort in reducing Bill of Material.
- Automated test bench.
- Precise production documentation.

Industry and the OH concept

- Open Hardware is new and not always understood.
- Need to explain to firms the opportunities and risks.
- Companies think they compete with assembly houses. We ask only firms that can also support (guarantee, repair, improve).

Experience with Industry

June 2013

Companies

- 15 European, 1 US.
- 60 projects.

Types of work

- Hardware: PCB development, production, HDL development.
- Software: device drivers.
- Usually small projects (<2 months work), speeds up projects, gets in specialist knowledge.
- Small firms can play a large role.

Experience with Industry

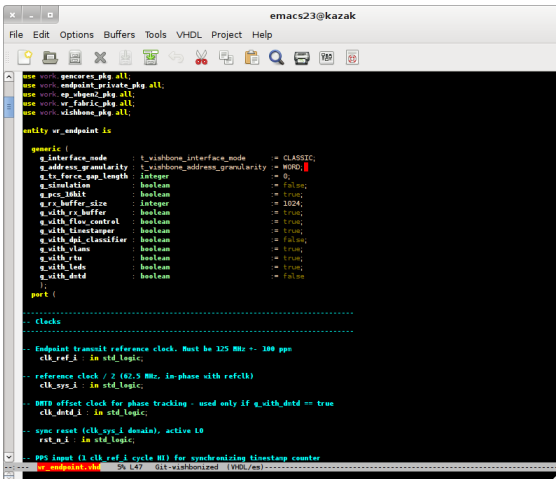
Examples of re-use of work

- Two companies modified SPEC carrier design.
 - larger FPGA (for software radio DSP).
 - PXIe bus instead of PCIe.
- A company re-uses White Rabbit spec for own product.
- Another one used nanoFIP VHDL for renovating trains.

Generates interaction

- One company helps another with product development.
- Firms work together in mutualistic symbiosis:
 - One sells a carrier, others sell mezzanines.
 - One sells a WR switch, others sell WR nodes.

HDL simulation flow 1/2: HDL entry



```
emacs23@kazak
File Edit Options Buffers Tools VHDL Project Help
[Icons]
use work_generates_pkg all;
use work_endpoint_private_pkg all;
use work_ep_vhgen2_pkg all;
use work_wr_fabric_pkg all;
use work_vishbone_pkg all;

entity wr_endpoint is
generic (
  g_interface_mode      : t_vishbone_interface_mode := CLASSIC;
  g_address_granularity : t_vishbone_address_granularity := WORD;
  g_tx_force_gap_length : integer := 0;
  g_simulation          : boolean := false;
  g_pcc_10bit          : boolean := true;
  g_rx_buffer_size     : integer := 1024;
  g_with_rx_buffer     : boolean := true;
  g_with_flow_control  : boolean := true;
  g_with_timestamper   : boolean := true;
  g_with_dpt_classifier : boolean := false;
  g_with_clans         : boolean := true;
  g_with_rtu           : boolean := true;
  g_with_leds          : boolean := true;
  g_with_dtdt         : boolean := false;
);
port (
-----
-- Clacks
-----
-- Endpoint transmit reference clock. Must be 325 Mhz +/- 100 ppm
clk_ref_i : in std_logic;

-- reference clock / 2 (62.5 Mhz, in-phase with refclk)
clk_sys_i : in std_logic;

-- DTDt offset clock for phase tracking - used only if g_with_dtdt == true
clk_dtdt_i : in std_logic;

-- sync reset (clk_sys_i domain), active L0
rst_n_i : in std_logic;

-- PPS input (1 clk_ref_i cycle HI) for synchronizing timestamp counter
or_endpoint.vhd 5% L47 Git-vishbonized [VHDL/es]
```

HDL simulation flow 2/2: HDL simulator

The screenshot displays the ModelSim SE 10.0 interface. The top window shows a digital waveform simulation. The left pane lists the signals being monitored, including memory locations (0000-001F) and registers (reg_1, reg_full_0, rsp_0, and registers 17-12). The main window shows the timing diagram with a vertical cursor at 12988.63429 ns. The bottom window shows the transcript, which includes a memory dump and simulation control messages.

Transcript:

```

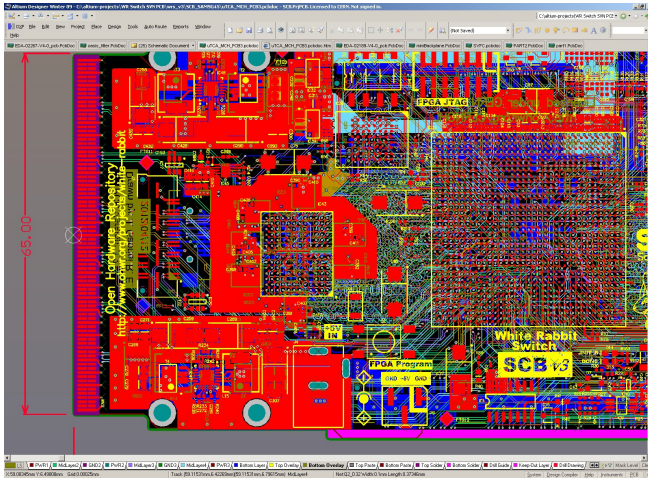
# *010: 12 13 08 09 16 17 18 19-1a 1b 1c 1d 1e 1f 14 15
# *020: 22 23 24 25 26 27 28 29-2a 2b 2c 2d 2e 2f 30 31
# *030: 32 33 34 35 36 37 38 39-3a 3b 3c 3d 3e 3f 40 41
# *040: 42 43 38 39 46 47 48 49-4a 4b 4c 4d 4e 4f 44 45
# *050: 52 53 54 55 56 57 58 59-5a 5b 5c 5d 5e 5f 60 61
# *060: 62 63 64 65 66 67 68 69-6a 6b 6c 6d 6e 6f 70 71
# *070: 72 73 68 69 76 77 78 79-7a 7b 7c 7d 7e 7f 74 75
# *080: 82 83 84 85 86 87 88 89-8a 8b 8c 8d 8e 8f 90 91
# *090: 92 93 94 95 96 97 98 99-9a 9b 9c 9d 9e 9f a0 a1
# *0a0: a2 a3 99 99 a6 a7 a8 a9-aa ab ac ad ae af a4 a5
# *0b0: b2 b3 b4 b5 b6 b7 b8 b9-ba bb bc bd be bf
# [port 6] tx 75
# [port 5] tx 75
# break key hit
# Simulation stop requested.
# Simulation Breakpoint: Simulation stop requested.
# MACRO ./run.do PASSED at Line 9
V$IM(pausd>)
Now: 159.496 ns Delta: 2 sim/main/OUT/genbkt[0]*ASSIGN#ptry_ref_clr_[]#192
  
```

PCB design flow 1/5: schematics entry

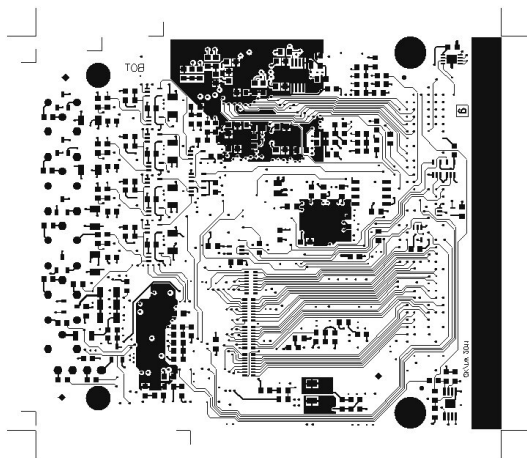
The screenshot displays the Altium Designer interface for a PCB schematic. The main workspace shows a detailed circuit diagram with numerous components and their interconnections. A legend in the bottom-left corner lists various components and their values. The bottom-right corner features a title block with the following information:

Project Name		File Delay FMC (FMC_TDC) ap450	
DocName	PCB.DOC	DocDate	15/05/2012
DocPath	C:\Users\j.serrano\Documents\EDA-02267-V4-0	DocUser	J.Serrano
DocType	PCB Project	DocVersion	1.0
DocAuthor	J.Serrano	DocStatus	Not Released
DocDate	15/05/2012	DocScale	1:1
DocUser	J.Serrano	DocSheet	1 of 10
DocVersion	1.0	DocTitle	EDA-02267-V4-0
DocStatus	Not Released	DocPart	1 of 1
DocScale	1:1	DocSheet	1 of 10
DocTitle	EDA-02267-V4-0	DocPart	1 of 1

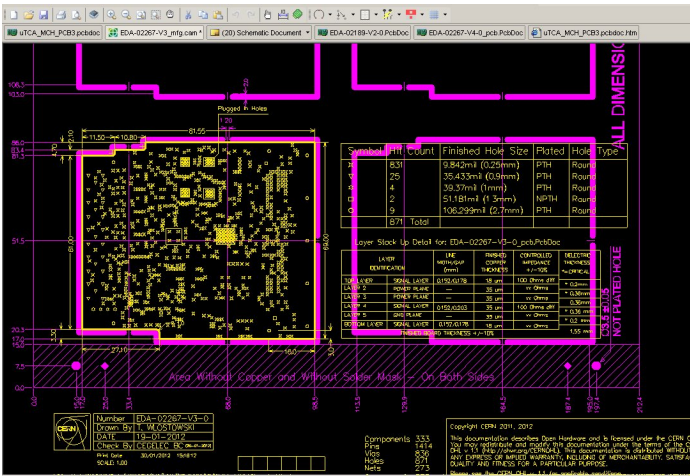
PCB design flow 2/5: PCB layout



PCB design flow 3/5: artwork



PCB design flow 4/5: drilling



PCB design flow 5/5: pick and place

A1												
Designator												
A	B	C	D	E	F	G	H	I	J	K		
1	Designator	Footprint	Center-X(mm)	Center-Y(mm)	Ref-X(mm)	Ref-Y(mm)	Pad-X(mm)	Pad-Y(mm)	Layer	Rotation	Comment	
2	IC16	SOIC127P600X175-8N	67.82	-86.66	67.82	-86.66	70.52	-47.73	Top	180	24LC024H-VSN	
3	J1	3M_5607-4200-SH	161.71	-9.42	160.53	-9.42	160.53	42.28	Top	90	3M_5607-4200-SH (SATA)	
4	J5	3M_5607-4200-SH	161.76	-30.02	160.58	-30.02	160.58	42.33	Top	90	3M_5607-4200-SH (SATA)	
5	L19	L_WUERTH_74407	72.28	-5.56	68.43	-5.56	68.43	-49.82	Top	270	4.7uH	
6	L5	L_WUERTH_74407	81.53	-16.02	81.53	-12.17	81.53	-36.72	Top	180	4.7uH	
7	IC3	SOP65P490X110-8N	96.16	-2.73	96.16	-2.73	93.96	-24.29	Top	0	AD5662BRMZ-1	
8	IC7	SOP65P490X110-8N	96.24	-6.29	96.24	-6.29	94.04	-24.21	Top	0	AD5662BRMZ-1	
9	T1	SOT95P230X110-3N	21.72	-74.22	21.72	-74.22	22.87	-95.38	Bottom	180	BSH103	
10	T2	SOT95P230X110-3N	21.69	-78.38	21.69	-78.38	22.84	-95.41	Bottom	180	BSH103	
11	T7	SOT95P230X110-3N	83.06	-56.65	83.06	-56.65	82.11	-36.14	Top	90	BSH103	
12	T9	SOT95P230X110-3N	87.73	-19.53	87.73	-19.53	86.58	-31.67	Top	0	BSH103	
13	C100	CAPC1005X56N	101.58	-31.18	101.58	-31.18	101.58	-16.67	Top	270	CC0402_100NF_16V_10%_X7R	
14	C101	CAPC1005X56N	93.48	-31.13	93.48	-31.13	93.48	-24.77	Top	270	CC0402_100NF_16V_10%_X7R	
15	C102	CAPC1005X56N	108.51	-21.79	108.51	-21.79	108.96	-9.29	Bottom	180	CC0402_100NF_16V_10%_X7R	
16	C103	CAPC1005X56N	107.93	-15.63	107.93	-15.63	108.38	-9.87	Top	180	CC0402_100NF_16V_10%_X7R	
17	C104	CAPC1005X56N	98.55	-17.85	98.55	-17.85	98.55	-19.69	Bottom	90	CC0402_100NF_16V_10%_X7R	
18	C105	CAPC1005X56N	94.46	-18.05	94.46	-18.05	94.46	-23.79	Bottom	270	CC0402_100NF_16V_10%_X7R	
19	C106	CAPC1005X56N	107.82	-25.37	107.82	-25.37	108.27	-9.98	Bottom	180	CC0402_100NF_16V_10%_X7R	
20	C107	CAPC1005X56N	103.91	-23.73	103.91	-23.73	104.36	-13.89	Bottom	180	CC0402_100NF_16V_10%_X7R	
21	C108	CAPC1005X56N	96.65	-17.15	96.65	-17.15	96.2	-22.05	Bottom	0	CC0402_100NF_16V_10%_X7R	
22	C109	CAPC1005X56N	105.99	-25.37	105.99	-25.37	106.44	-11.81	Bottom	180	CC0402_100NF_16V_10%_X7R	
23	C112	CAPC1005X56N	110.23	-24.2	110.23	-24.2	110.23	-8.02	Top	90	CC0402_100NF_16V_10%_X7R	
24	C113	CAPC1005X56N	109.77	-20.9	109.77	-20.9	110.22	-8.03	Bottom	180	CC0402_100NF_16V_10%_X7R	
25	C114	CAPC1005X56N	99.51	-16.31	99.51	-16.31	99.51	-18.74	Bottom	270	CC0402_100NF_16V_10%_X7R	
26	C115	CAPC1005X56N	109.8	-17.88	109.8	-17.88	110.25	-7.99	Bottom	180	CC0402_100NF_16V_10%_X7R	
27	C116	CAPC1005X56N	98.18	-31.13	98.18	-31.13	98.18	-20.07	Top	270	CC0402_100NF_16V_10%_X7R	
28	C117	CAPC1005X56N	105.55	-15.15	105.55	-15.15	105.55	-12.69	Top	270	CC0402_100NF_16V_10%_X7R	
29	C118	CAPC1005X56N	97.95	-19.68	97.95	-19.68	97.95	-20.29	Bottom	270	CC0402_100NF_16V_10%_X7R	
30	C123	CAPC1005X56N	101.01	-35.18	101.01	-35.18	100.56	-17.69	Bottom	0	CC0402_100NF_16V_10%_X7R	
31	C124	CAPC1005X56N	98.53	-39.38	98.53	-39.38	98.08	-20.17	Bottom	0	CC0402_100NF_16V_10%_X7R	
32	C125	CAPC1005X56N	97.69	-36.99	97.69	-36.99	97.69	-20.56	Bottom	90	CC0402_100NF_16V_10%_X7R	
33	C126	CAPC1005X56N	106.7	-35.71	106.7	-35.71	107.15	-11.1	Bottom	180	CC0402_100NF_16V_10%_X7R	
34	C127	CAPC1005X56N	106.43	-37.85	106.43	-37.85	105.98	-12.27	Bottom	0	CC0402_100NF_16V_10%_X7R	
35	C131	CAPC1005X56N	100.04	-51.81	100.04	-51.81	100.04	-18.21	Bottom	270	CC0402_100NF_16V_10%_X7R	

Try to use FOSS tools for development

Tools: the last hurdle to sharing

- We already have a forge and a license.
- Current proprietary CAD tools make it hard to share designs.

Current efforts

- Icarus Verilog: help in adding VHDL and SystemVerilog support.
- Kicad: help bring it on par with proprietary tools in terms of features and quality. See <http://www.ohwr.org/projects/cern-kicad/wiki>.
- Your help is *very* welcome!

Regarding public research institutions

OSHW is good for the labs

- Develop technology, avoid maintenance burden
- Reduce development costs and avoid vendor lock-in
- Return benefits to society
 - Feed into local and global economy
 - Make results quickly available
 - Communicate results widely to citizenship

OSHW is good for the companies

- Further develop and support technology, making a profit
- Negligible upfront costs, easy entry into market

Why we use Open Hardware

Does it hold its promises?

Get a design just the way we want it – Yes

With own designers and with outside help (industry, institutes).

Peer review – Yes

From different groups. Also by industry.

Design re-use – Yes

- SPEC and ADC100M have users and lots of interest.
- SPEC design is being copied and re-used in other designs.

Healthier relationship with companies – Yes

- We are much more free to work with small companies.
- Not tied to any single one.

Why we use Open Hardware

Does it hold its promises?

Dissemination of knowledge – Yes

Lots of interaction with other institutes, universities and companies, much more than before.

Spend money where you or your funding agencies want – Yes

Many projects spread among CERN member states.

Conclusions

- The electronics that we support cannot be black boxes.
- Open Hardware has many advantages.
 - Anyone can help in developments and make improvements.
 - Allows to work differently with industry (design work, smaller companies).
 - Not tied to a single company for production and support.
- CERN Open Hardware License provides a legal basis.
- OHR site is practical, stimulating and fun for engineers.
- Good FOSS tools needed: help us make it happen!
- Many designs being developed and several are already produced by industry.
- Four years of experience show it works!

Questions?

