DFM analysis

BB ELECTRONICS
EMS – from idea to solution

Customer	XX	Product Name	XX
EAQ	XX	BOM number	XX
Report Date	11/5-2010	Report by	Claus E. Nielsen & Peter Riis

1. Introduction

The aim of this document is to identify potential problems foreseen to occur during production, enabling proper remedies to be taken prior to a production run.

1.1 Standards

The following assessments, suggestions and recommendations regarding component and PCB design are based on the following standards in the newest revision.

1.1.1 Acceptance

- IPC-A-610, Acceptability for Electronic Assemblies

1.1.2 Advanced

- J-STD 013, Implementation of Ball Grid Array and Other High Density Technology
- IPC-SM-784, Guidelines for Chip-on-Board Technology Implementation

1.1.3 Assembly

- J-STD 001, Requirements for Soldered Electrical and Electronic Assemblies
- IPC-HBD-001, Handbook and Guide to Supplement J-STD-001
- IPC-D-279, Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies
- IPC-7351, Surface Mount Design and Land Pattern Standard

1.1.4 Assembly Support

- IPC-CM-770, Guidelines for Printed Board Component Mounting
- IPC-SM-780, Component Packaging With Emphasis on Surface Mounting
- IPC-7095, Design and Assembly Process Implementation for BGA’s
- IPC-7525, Stencil Design Guidelines
- IPC-7530, Guidelines for Temperature Profiling for Mass Soldering Processes (Reflow & Wave)

1.1.5 Components

- J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
- J-STD-033, Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

1.1.6 Laminate

1.1.6.1 Rigid

- IPC-4101, Specification for Base Materials for Rigid and Multilayer Printed Boards

1.1.7 Other

- IPC-7251, Generic Requirements for Through-Hole Design and Land Pattern Standard

1.1.8 Printed Board

- IPC-2221, Generic Standard for Printed Board Design
- IPC-2222, Sectional Design Standard for Rigid Organic Printed Boards

1.1.9 Printed Board Acceptance

- IPC-A-600, Acceptability of Printed Boards
- IPC-6011, Generic Performance Specification for Printed Boards
- IPC-6012, Qualification and Performance Specification for Rigid Printed Boards
- IPC-6013, Qualification and Performance Specification for Flexible Printed Boards
- IPC-6015, Qualification and Performance Specification for Organic Multichip Module (MCM-L) Mounting and Interconnecting Structures
- IPC-6016, Qualification and Performance Specification for High Density Interconnect (HDI) Layers or Boards
- IPC-6018, Microwave End Product Board Inspection and Test

1.2 Definitions of categories.

Design improvements and suggestions are categorized in the following manner:

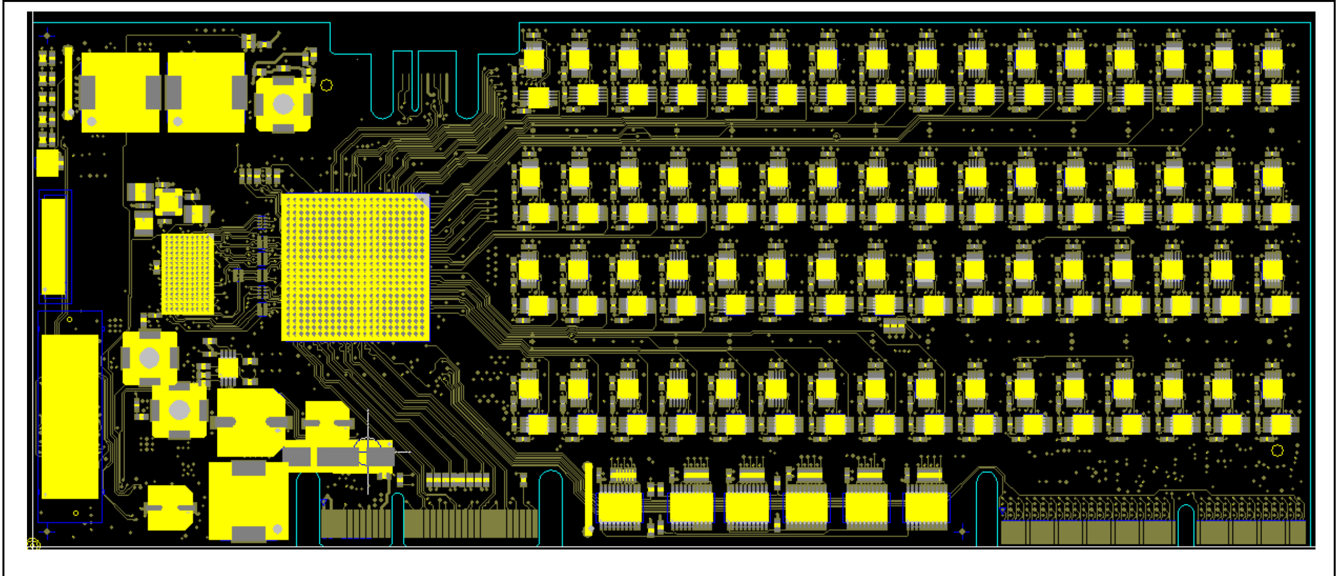
A	Major error / problem which must be altered before next revision.
B	Process improvement / cost saving suggestion.
C	Minor issue.
X	BB Electronics internal issue
OK	Issue checked and found okay.
NA	Not Applicable: Issue is not possible / relevant to check.

1.3 Sources used in the analysis.

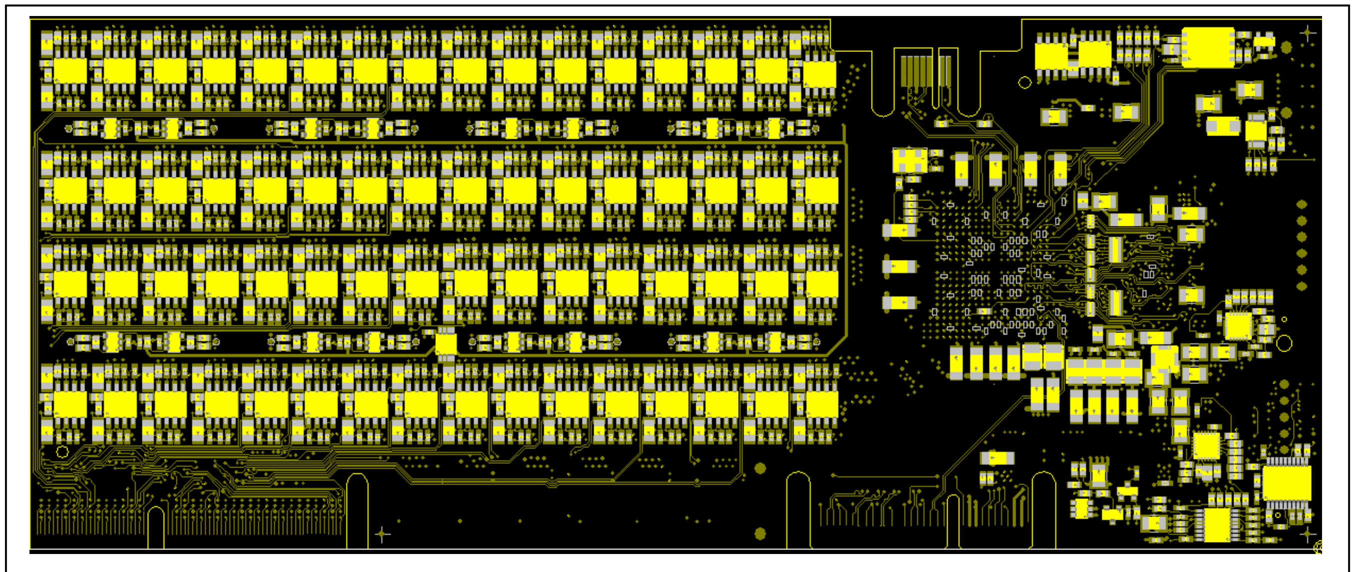
- Cad data: GenCad data-file provided by customer created 19th of February 2010.
- Gerber data in 274x format provided by customer created 19th of February 2010.
- BOM provided by customer: XX.pdf.
- Component placement drawing provided by customer: XX.pdf, created 21st of February 2010.
- Additional information provided by Mats Persson, BB Electronics.

2. Drawing of product

2.1 Topside



2.2 Bottom side



3. Contents

1. Introduction ... 1
1.1 Standards ... 1
1.1.1 Acceptance ... 1
1.1.2 Advanced ... 1
1.1.3 Assembly ... 1
1.1.4 Assembly Support ... 1
1.1.5 Components ... 1
1.1.6 Laminate ... 2
1.1.7 Other ... 2
1.1.8 Printed Board ... 2
1.1.9 Printed Board Acceptance ... 2
1.2 Definitions of categories. ... 2
1.3 Sources used in the analysis. ... 2
2. Drawing of product ... 3
2.1 Topside ... 3
2.2 Bottom side ... 3
3. Contents ... 4
4. Proposed manufacturing processes. ... 5
4.1 Suggested test setup ... 5
5. PCB Layout ... 6
6. SMT process ... 22
7. Through hole components ... 29
8. Reflow soldering ... 30
9. Reflow/adhesive ... 31
10. Wave soldering ... 31
11. Selective soldering ... 31
12. Summary ... 32

4. Proposed manufacturing processes.

The following processes are recommended in connection with production of the PCB.

Single sided PCB		Double sided PCB	
SMT		SMT	
Process	Suggested	Process	Suggested
Reflow		Reflow/reflow	X
Pin in paste		Pin in paste	
		Reflow/adhesive	
THT		THT	
Process	Suggested	Process	Suggested
Wave soldering		Wave soldering	
Selective soldering		Selective soldering	X
Hand soldering		Hand soldering	

Instead of lead free hand soldering or lead free wave pallet soldering of the components JTP1, JTP2, J3 (center ground pins) and J4, it is recommended to use lead free selective soldering.

The main argument being that you insure a consistent high level of quality and repeatability.

Further you avoid the costs of design and fabrication of expensive special solder pallets for wave soldering.

4.1 Suggested test setup

Not considered.

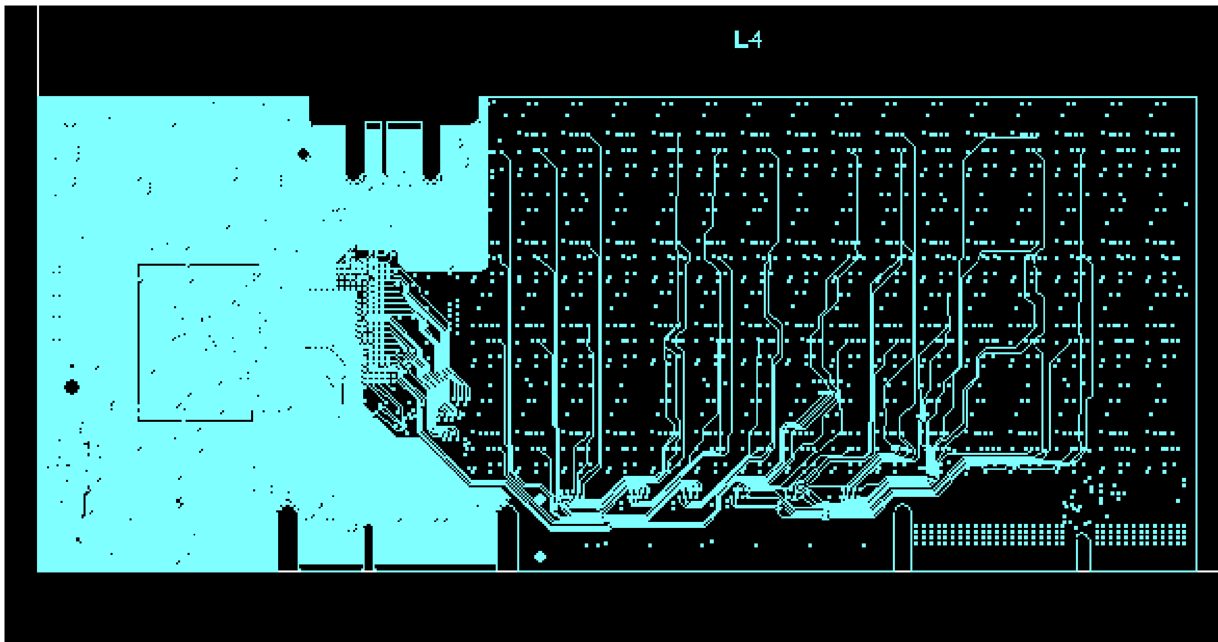
5. PCB Layout

No.	Issue	Result	[Position:] Comments
5.01	Optimal Board size, and shape [>100 x 110 mm, <300 x 200mm, square or rectangle.] Largest size allowed 460 x 460mm.	OK	200mm x 82mm
5.02	Proper Panelization [optimal < 300 mm x 200 mm],(Largest size allowed 460 x 460mm) .minimum material waste, optimal transport efficiency.	NA	No panelization data available. Due to the current PCB outline, it is recommended to apply a break off frame of 10mm on the long sides of the PCB for optimal transport efficiency.
5.03	Breakout tab. Type: shear/score/router/mouse-bite, V-groove, and the location. Keep away from ceramic caps min. 5mm. Smooth edges vs. rough edges.	NA	No panelization data available.
5.04	Break-offs have cut outs and no break points under protruding Connectors to be wave soldered or selectively soldered	NA	No panelization data available.
5.05	Board thickness [0.8 – 4 mm] rigidity	OK	1.6mm specified.
5.06	Board warpage	OK	See comment below.
5.07	Specified silkscreen width not less than 0.2mm	A	Error in silkscreen layer for bottom side of PCB. See comment below.
5.08	Specified silkscreen height not less than 0.1mm	A	Error in silkscreen layer for bottom side of PCB. See comment below.
5.09	Via hole. 0.250mm min diameter. Min location from pads 0.254mm incl. trace. Min edge-to-edge 0.381mm if not masked. No underneath part (wave or adhesive). No mask if used for test. Tented/Capped when wave-soldered.	A	Numerous occasions, where vias are placed under pads. See comments below.
5.10	Via hole minimum 0.5mm from PCB edge.	OK	
5.11	Ground planes where possible. Crosshatched copper to fill in gaps. Evenly distributed copper throughout entire board to avoid bow & twist.	OK	See comment for 5.06
5.12	Solder Mask Webbing min. 0.1mm Solder mask between fine pitch 0.5mm or smaller is not necessary. Soldermask Clearance min. 0.1mm, BGA 0.15mm	A	Numerous occasions of too small solder mask webbing. IC222, IC223 & IC802 solder mask present between fine pitch. See comment below.

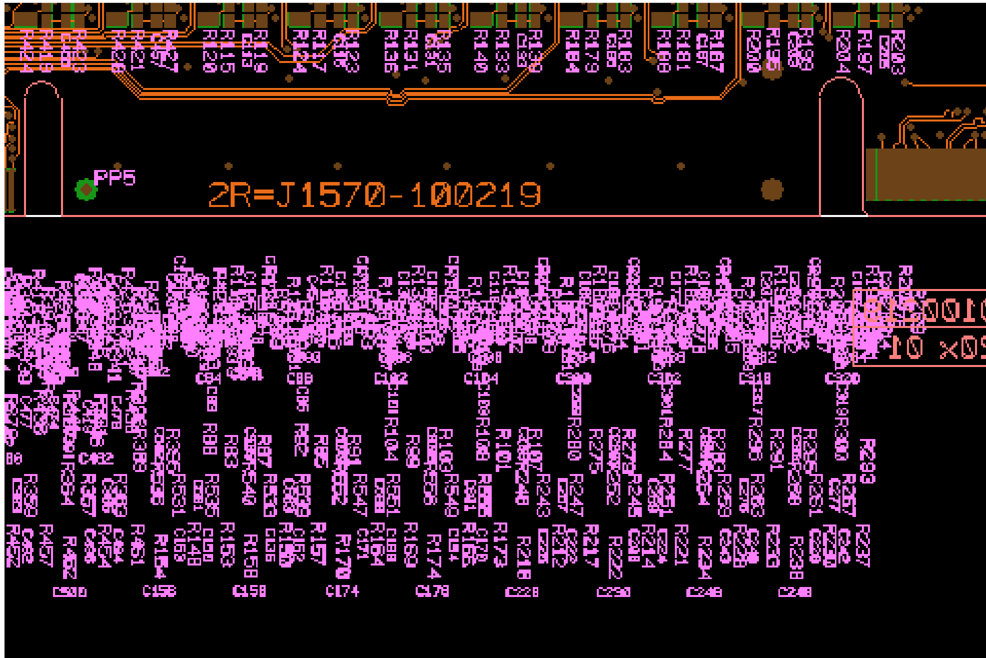
5.13	No solder mask between 0402 or 0201 solder pads	A	Numerous occasions of solder mask present between pads for 0402 components. See comment below.
5.14	Optimal PCB surface finish. HASL not to be used with fine pitch, CSP or smaller, 0402, or 0201 technology, or PCB thinner than 0.8mm.	NA	Due to no PCB specification presented.
5.15	IPC-7351 land patterns used for general SMT design	A	Numerous occasions where the recommendations listed in IPC-7351 has not been adhered to. See comments below.
5.16	Fine pitch land patterns set to 60% of lead pitch. E.g. 0.5mm pitch = 0.3mm land width.	A	IC222, IC223, IC802; see comment below.
5.17	No natural bridges on fine pitch, networks or other areas.	OK	
5.18	Non-solder mask defined (NSMD) pads on CSP's, QFN's, LLC's, BGAs and flip chips.	A	IC202, IC222, IC223, IC802; see comment below.
5.19	BGA land pattern, pad geometry & location. Keep away from press-fit areas and other attachments. BGA vias must include a sufficient solder dam or completely covered. Solder mask relief around Land >=0.10mm. Oval shape lands preferred.	C	Round shape apertures used in BGA design is acceptable. Numerous occasions where solder mask relief around land is below 0.1mm. See comment below
5.20	Documentation, drawings, data with acceptable quality	A	No PCB specification available, see comment below.
5.21	Min etch distance from PCB edge 0.5mm	A	IC104; see comment below.
5.22	Min Etch width (0.1mm) and Etch to Etch spacing (0.1mm)	OK	
5.23	Critical apertures optimized for solder paste screening.	OK	
5.24	Rework process feasible with regards to space and thermal load.	C	JTP1; see comment below.
5.25	General orientation of polarized components.	C	Tantalum and IC's OK, CANCAP components have random orientation.
5.26	Fine pitch devices are limited in numbers. BGA type used where possible.	OK	
5.27	Any heat sensitive components identified	C	C730: Max peak. 240°C, IC201: Max peak: 245°C.

5.28	Other issues related to PCB	B	Se comments below.

5.06:
We do not suspect any problems related to warpage. All though the copper is unevenly distributed in layer 4 (see picture below), the even distribution of copper in the other layers will overrule any tendency of warpage related to this layer. As no PCB specification has been presented, please observe that the laminate used in the PCB construction has not been taken into account when making this judgment.



5.07 & 5.08:
Error in silkscreen specification in gerber data for bottom layer (sno.gdo), see picture below.

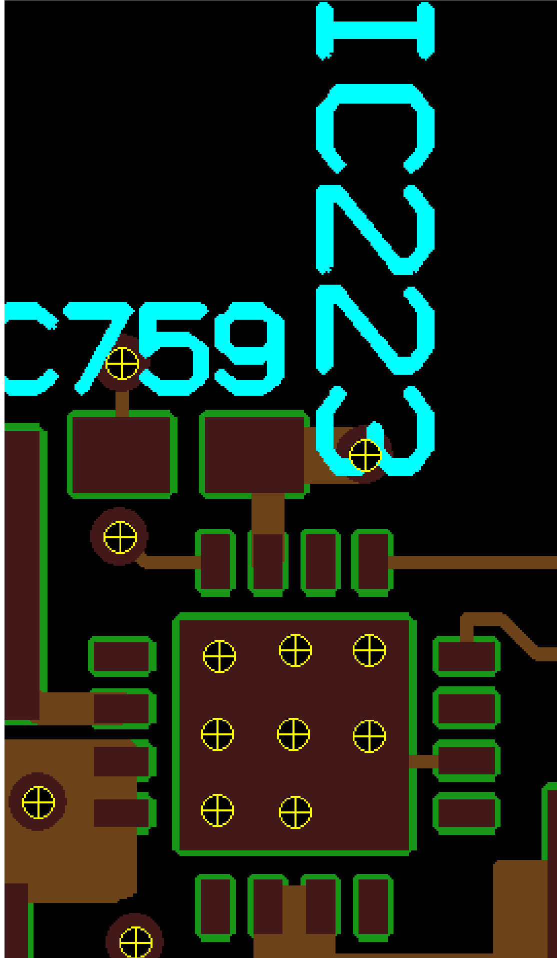


As can be seen from above, a large amount of the silkscreen text is present outside the PCB. As no print specification has been presented to us, we are not aware, whether silkscreen is desired on the final product. From a production point of view, we would not recommend the use of silkscreen.

5.09:
Numerous occasions with via in pad;

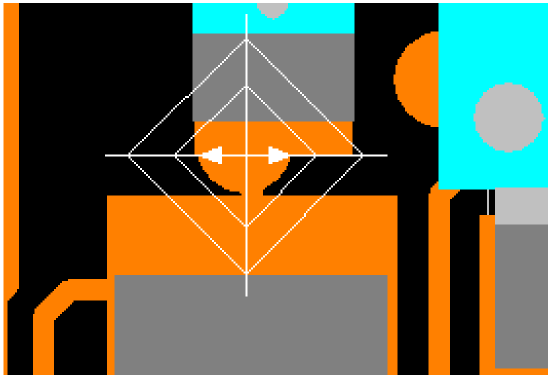
IC206, IC221, IC222, IC223 & IC802 all have vias in ground pad. Where this is considered necessary due to thermal relief, we recommend, that the vias should be plugged according to IPC-4761.

IC223: Via in ground pad.



For the other occurrences of vias in pad, it is recommended to move the via outside the pad.

C445: Via in SMD-pad.



A via in pad is considered a problem since it makes it very hard to control the solder amount on the pad. Further air is very easily trapped underneath the solder paste on the pad, which in turn can lead to voids during the soldering process.

5.12:
The solder mask webbing has been observed as small as 51µm. Such small webbings are impossible to manufacture; attempting to do so, could very well lead to small pieces of solder mask polluting the PCB.

IC222, IC223, IC802:
IC222, IC223, IC802 are fine pitch components (pitch equal or less than 0.5mm). Nevertheless solder mask has been specified, probably due to the fact, that some of the pads are solder mask defined. Using solder mask for fine pitch components can result in irregular screening of solder paste on the pads, due to the fact, that the height of the solder mask can obstruct the screening process.

5.13:
Specifying solder mask between pads for such small components can lead to the components "riding" on top of the solder mask webbing. We recommend that the solder mask is removed between the pads for the 0402-components. Please bear in mind also to remove any ghost traces (i.e. traces between 0402-pads), that otherwise will be exposed, when the solder mask is removed.

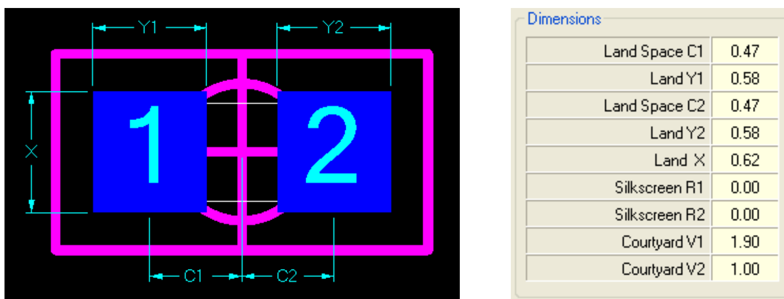
5.15:

0402 chip resistor layout, general:

3111800550	Res 1,5k 1% 50V 0402	130	PCS	R47
CRCW04021K50FKED	Vishay			

The current 0402 chip resistor layout does not comply with the IPC-7351 recommended pad layout for this component type regarding the pad to pad distance.

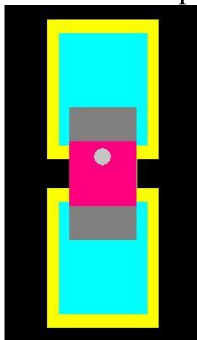
The IPC-7351 suggests the following nominal pad layout dimensions for a standard 0402 chip resistor:



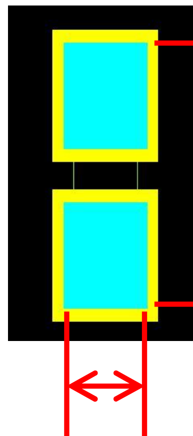
Land Space C1	0.47
Land Y1	0.58
Land Space C2	0.47
Land Y2	0.58
Land X	0.62
Silkscreen R1	0.00
Silkscreen R2	0.00
Courtyard V1	1.90
Courtyard V2	1.00

The current PCB layout for the 0402 chip resistor has been measured to the following dimensions:

With 0402 chip resistor:



Pads shown only:



Outline pad to pad distance is measured to 2.12mm where IPC-7351 LP Calculator denotes an optimal distance of 1.32 to 1.72mm. (Least to most value).

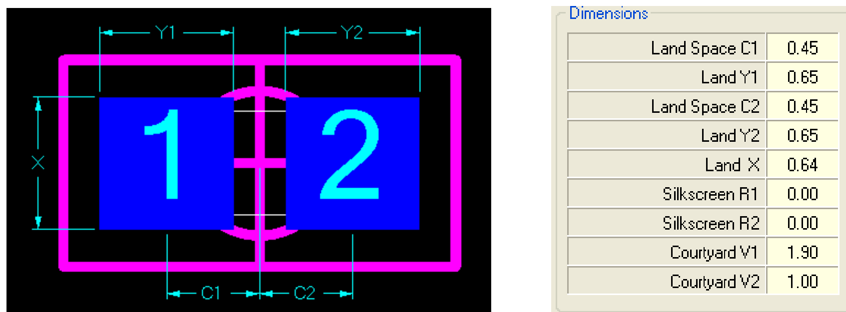
Pad width is measured to 0.67mm where IPC-7351 LP Calculator denotes an optimal distance of 0.52 to 0.72mm. (Least to most value).

<u>0402 chip capacitor layout, general:</u>

3130900040	Cap 4,7pF 50V 5A4R7CAT2A cer SMD 0402 NPO	128	PCS	C41
04025A4R7CAT2A	AVX			

The current 0402 chip capacitor layout does not comply with the IPC-7351 recommended pad layout for this component type regarding the outline pad to pad distance.

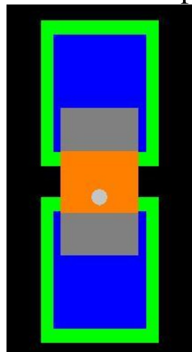
The IPC-7351 suggests the following nominal pad layout dimensions for at standard 0402 chip capacitor:



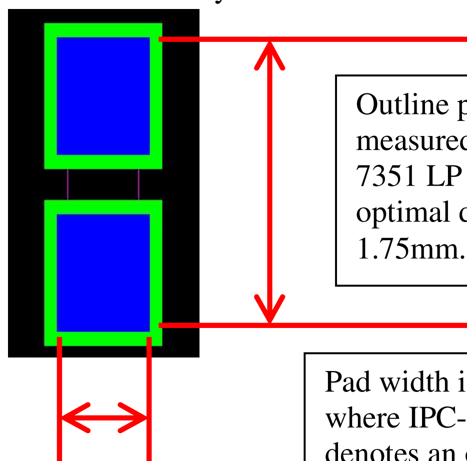
Dimensions	
Land Space C1	0.45
Land Y1	0.65
Land Space C2	0.45
Land Y2	0.65
Land X	0.64
Silkscreen R1	0.00
Silkscreen R2	0.00
Courtyard V1	1.90
Courtyard V2	1.00

The current PCB layout for the 0402 chip capacitor has been measured to the following dimensions:

With 0402 chip capacitor:



Pads shown only:



Outline pad to pad distance is measured to 2.12mm where IPC-7351 LP Calculator denotes an optimal distance of 1.35 to 1.75mm. (Least to most value).

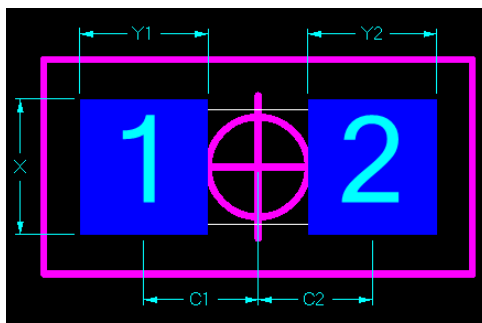
Pad width is measured to 0.67mm where IPC-7351 LP Calculator denotes an optimal distance of 0.52 to 0.72mm. (Least to most value).

0603 chip resistor layout, general:

3111700740	R 10K Ohm, 1%1/10W, SMD 0603	45	PCS	R561
RK73H1JTTD1002F	KOA			

The current 0603 chip resistor layout does comply with the IPC-7351 recommended pad layout for this component type, but it could be optimized to fit the nominal IPC layout since the current layout is quite close to the "least" IPC layout recommendation regarding the pad width.

The IPC-7351 suggests the following pad layout dimensions for at standard 0603 chip resistor:

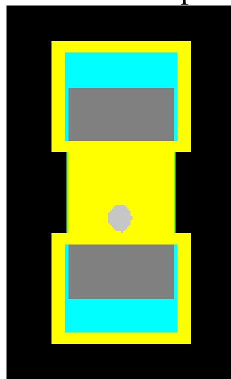


Dimensions

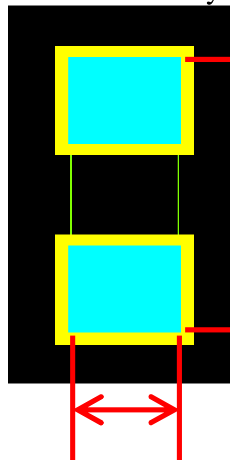
Land Space C1	0.80
Land Y1	0.90
Land Space C2	0.80
Land Y2	0.90
Land X	0.95
Silkscreen R1	0.00
Silkscreen R2	0.00
Courtyard V1	3.00
Courtyard V2	1.50

The current PCB layout for the 0603 chip resistor has been measured to the following dimensions:

With 0603 chip resistor:



Pads shown only:



Outline pad to pad distance is measured to 2.30mm where IPC-7351 LP Calculator denotes an optimal distance of 2.10 to 2.90mm. (Least to most value).

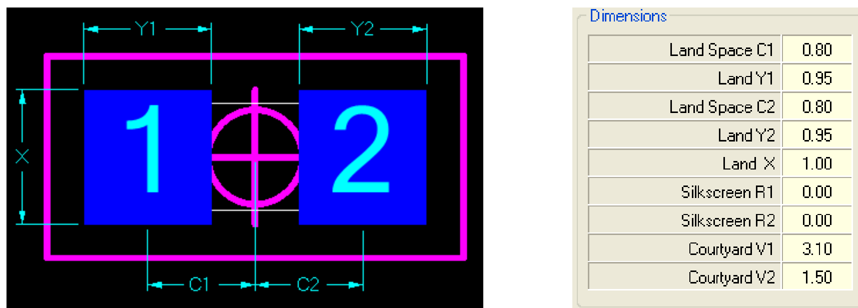
Pad width is measured to 0.85mm where IPC-7351 LP Calculator denotes an optimal distance of 0.85 to 1.05mm. (Least to most value).

0603 chip capacitor layout, general:

3131000420 C 4,7nF 50 V cer.SMD 0603 X7R 16 PCS C5
CD0603C472K5RAC Kemet

The current 0603 chip capacitor layout barely complies with the IPC-7351 recommended pad layout for this component type, but it could be optimized to fit the nominal IPC layout since the current layout is less than the “least” IPC layout recommendation regarding both the outline pad to pad distance and the pad width.

The IPC-7351 suggests the following nominal pad layout dimensions for at standard 0603 chip capacitor:

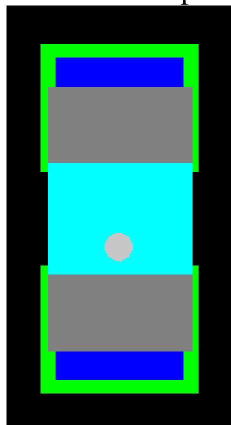


Dimensions

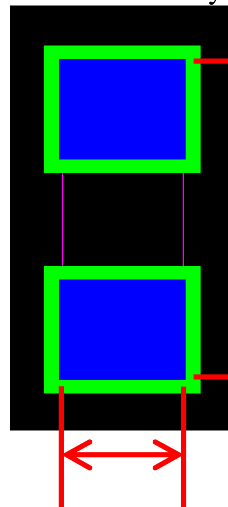
Land Space C1	0.80
Land Y1	0.95
Land Space C2	0.80
Land Y2	0.95
Land X	1.00
Silkscreen R1	0.00
Silkscreen R2	0.00
Courtyard V1	3.10
Courtyard V2	1.50

The current PCB layout for the 0603 chip resistor has been measured to the following dimensions:

With 0603 chip capacitor:



Pads shown only:



Outline pad to pad distance is measured to 2.14mm where IPC-7351 LP Calculator denotes an optimal distance of 2.15 to 2.95mm. (Least to most value).

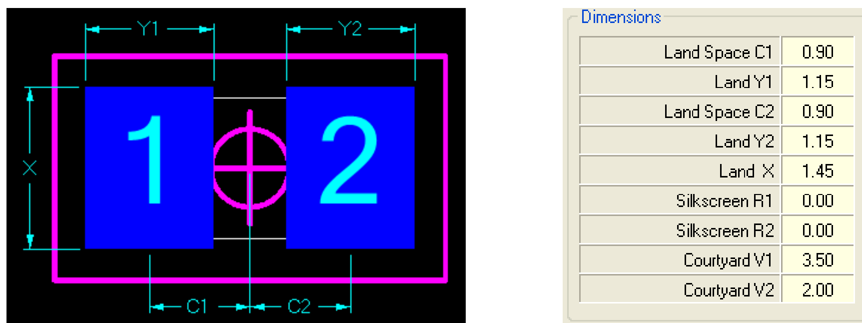
Pad width is measured to 0.84mm where IPC-7351 LP Calculator denotes an optimal distance of 0.90 to 1.10mm. (Least to most value).

<u>0805 chip capacitor layout, general:</u>

3131100100	C 1µF 10 V cer.SMD 0805 X7R	6	PCS	C615
0805ZC105KAT2A	AVX			

The current 0805 chip capacitor layout barely complies with the IPC-7351 recommended pad layout for this component type, but it could be optimized to fit the nominal IPC layout since the current layout is less than the “least” IPC layout recommendation regarding the pad width.

The IPC-7351 suggests the following nominal pad layout dimensions for at standard 0805 chip capacitor:

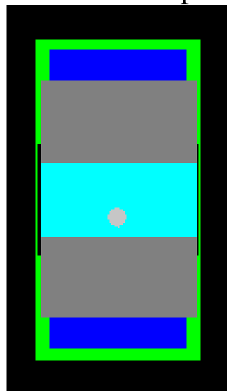


Dimensions

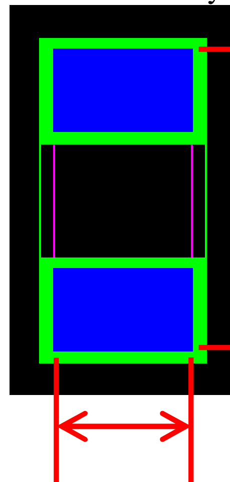
Land Space C1	0.90
Land Y1	1.15
Land Space C2	0.90
Land Y2	1.15
Land X	1.45
Silkscreen R1	0.00
Silkscreen R2	0.00
Courtyard V1	3.50
Courtyard V2	2.00

The current PCB layout for the 0805 chip capacitor has been measured to the following dimensions:

With 0805 chip capacitor:



Pads shown only:



Outline pad to pad distance is measured to 2.79mm where IPC-7351 LP Calculator denotes an optimal distance of 2.55 to 3.35mm. (Least to most value).

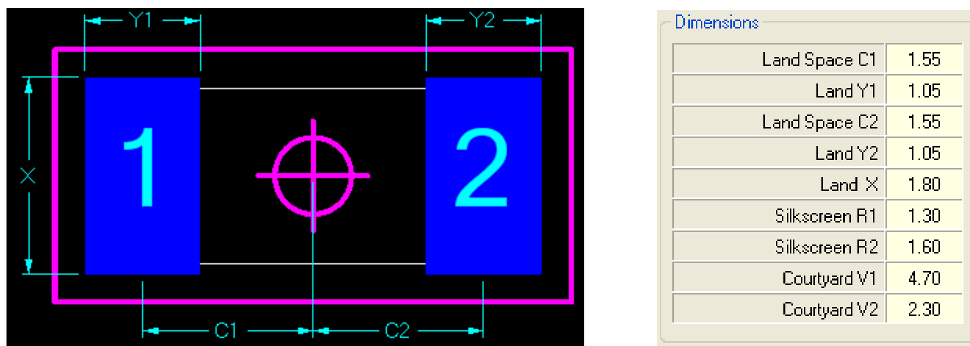
Pad width is measured to 1.28mm where IPC-7351 LP Calculator denotes an optimal distance of 1.35 to 1.55mm. (Least to most value).

<u>1206 chip resistor layout, general:</u>

3113100250	R 470, 1% 0,25W, SMD 1206	128	PCS	R56
60-194-18	Elfa AB			

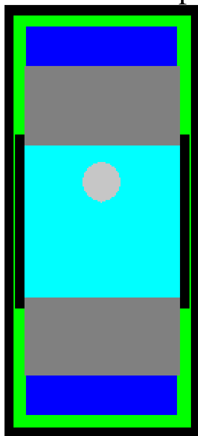
The current 1206 chip resistor layout barely complies with the IPC-7351 recommended pad layout for this component type, but it could be optimized to fit the nominal IPC layout since the current layout is quite close to the "least" IPC layout recommendation regarding the pad width.

The IPC-7351 suggests the following nominal pad layout dimensions for at standard 1206 chip resistor:

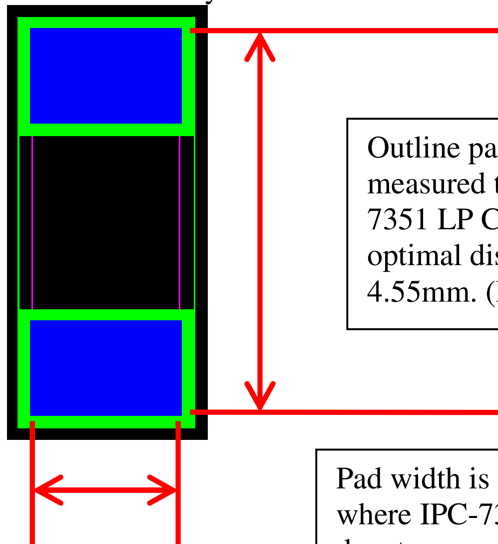


The current PCB layout for the 1206 chip resistor has been measured to the following dimensions:

With 1206 chip resistor:



Pads shown only:



Outline pad to pad distance is measured to 4.00mm where IPC-7351 LP Calculator denotes an optimal distance of 3.75 to 4.55mm. (Least to most value).

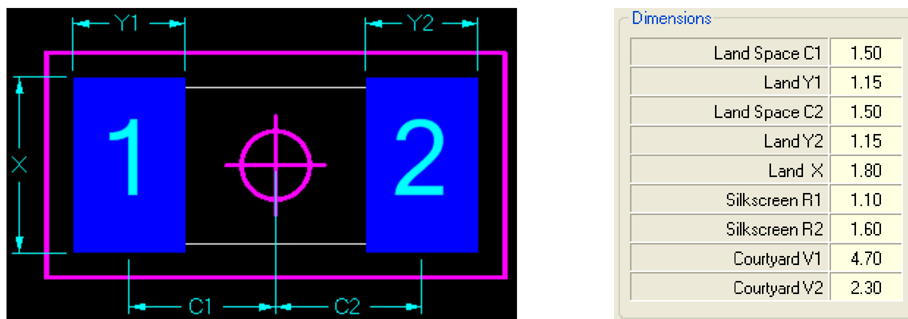
Pad width is measured to 1.55mm where IPC-7351 LP Calculator denotes an optimal distance of 1.70 to 1.90mm. (Least to most value).

1206 chip capacitor layout, general:

3131200120 Cap 22µF 6V3 10% cer SMD 1206 X5R 5 PCS C610
C1206C226K9PACTU Kemet

The current 1206 chip capacitor layout barely complies with the IPC-7351 recommended pad layout for this component type, but it could be optimized to fit the nominal IPC layout since the current layout exceeds the "most" IPC layout recommendation regarding the pad width.

The IPC-7351 suggests the following nominal pad layout dimensions for at standard 1206 chip capacitor:

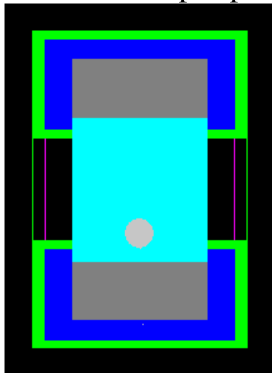


Dimensions

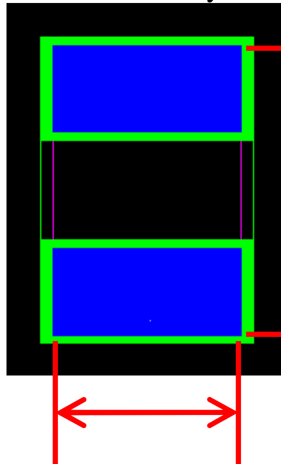
Land Space C1	1.50
Land Y1	1.15
Land Space C2	1.50
Land Y2	1.15
Land X	1.80
Silkscreen R1	1.10
Silkscreen R2	1.60
Courtyard V1	4.70
Courtyard V2	2.30

The current PCB layout for the 1206 chip capacitor has been measured to the following dimensions:

With 1206 chip capacitor:



Pads shown only:



Outline pad to pad distance is measured to 3.90mm where IPC-7351 LP Calculator denotes an optimal distance of 3.75 to 4.55mm. (Least to most value).

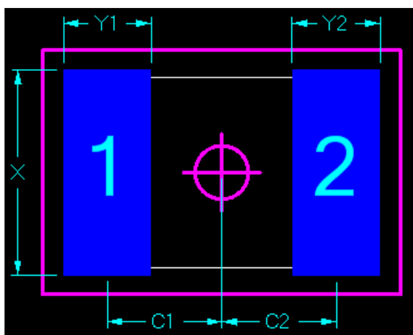
Pad width is measured to 2.55mm where IPC-7351 LP Calculator denotes an optimal distance of 1.70 to 1.90mm. (Least to most value).

<u>1210 chip capacitor layout, general:</u>

3133000120	Cap 47uF 6V3 10% cer SMD 1210 X5R	7	PCS	C748
12106D476KAT2A	AVX			

The current 1210 chip capacitor layout barely complies with the IPC-7351 recommended pad layout for this component type, but it could be optimized to fit the nominal IPC layout since the current layout is less than the “least” IPC layout recommendation regarding the pad width.

The IPC-7351 suggests the following nominal pad layout dimensions for at standard 1210 chip capacitor:

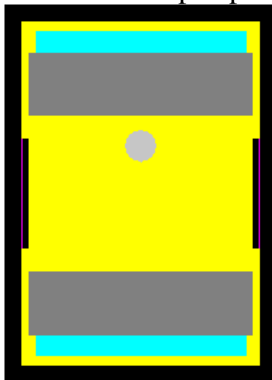


Dimensions

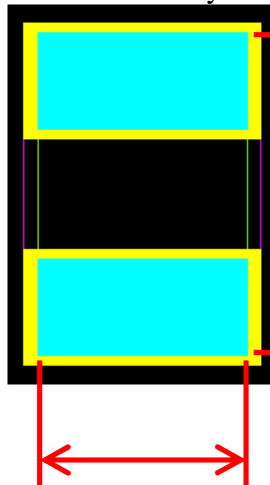
Land Space C1	1.50
Land Y1	1.15
Land Space C2	1.50
Land Y2	1.15
Land X	2.70
Silkscreen R1	1.10
Silkscreen R2	2.50
Courtyard V1	4.70
Courtyard V2	3.20

The current PCB layout for the 1210 chip capacitor has been measured to the following dimensions:

With 1210 chip capacitor:



Pads shown only:



Outline pad to pad distance is measured to 3.90mm where IPC-7351 LP Calculator denotes an optimal distance of 3.75 to 4.55mm. (Least to most value).

Pad width is measured to 2.55mm where IPC-7351 LP Calculator denotes an optimal distance of 2.60 to 2.80mm. (Least to most value).

5.16:

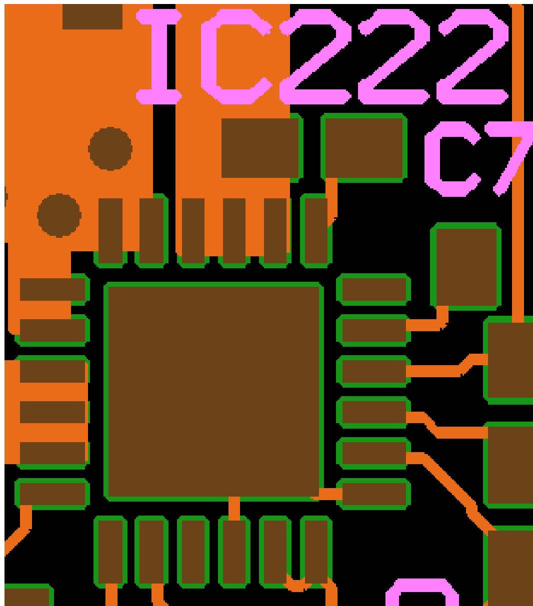
IC222, IC223, IC802:

For these components only 0.25mm wide pads has been defined, all though the pad pitch is 0.5mm, hence a pad width of 0.3mm would have been optimal.

5.18:

IC202, IC222, IC223, IC802:

All these components have non solder mask defined pads. This is not recommendable, as the pads purely defined by the solder mask will extend to a larger area, than those defined by copper, leading to an uneven soldering of the pads for the component. Below is shown a picture IC222.



5.19:

Solder mask relief around land is measured to be between 0.05mm and 0.07mm on numerous occasions which is below our recommendation of 0.10mm. Some PCB manufacturers will be able to provide an accurate solder mark registration with an opening of 0.05mm to 0.07mm but in order to widen/increase the process window at the PCB manufacturer we recommend the solder mask relief around land to be at least 0.10mm.

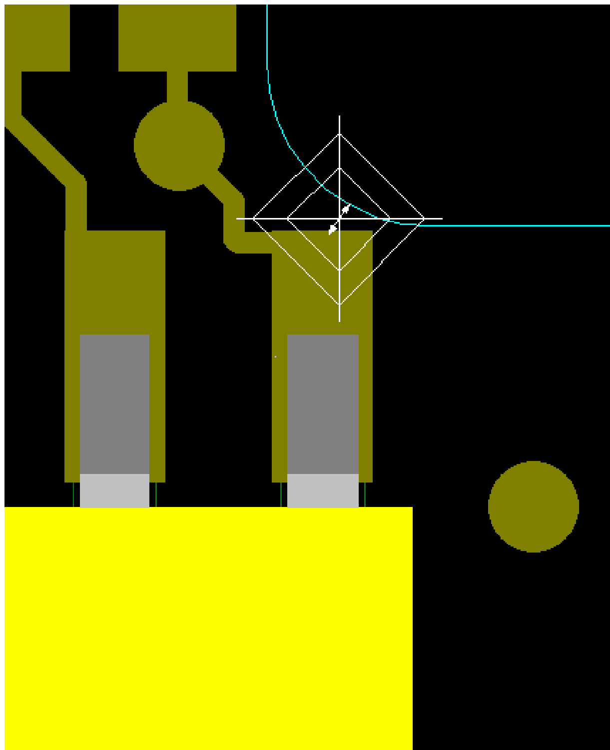
5.20:

A readme_pcb.txt file exists in gerber data. It has some information regarding the PCB, but information regarding the laminate and a drawing or description of the stack-up layer is missing. Further we miss information regarding the PCB surface.

5.21:

IC104:

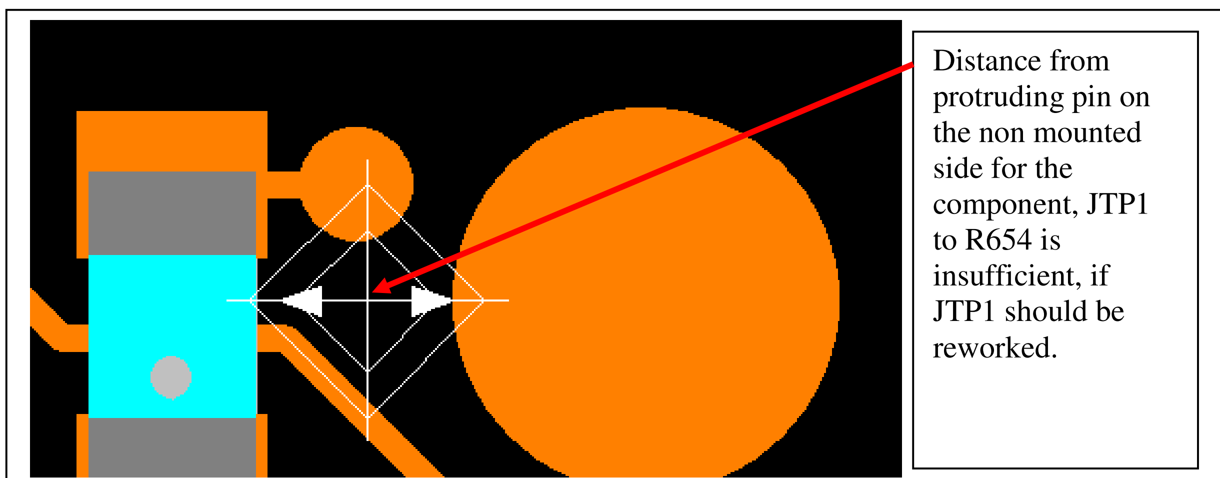
There is too little distance from one of the pads to the PCB edge. Such a small distance can be difficult for the PCB-manufacturer to manufacture; a potential risk exists, that the bare copper can be exposed during the milling process. See picture below.



5.24:

JTP1:

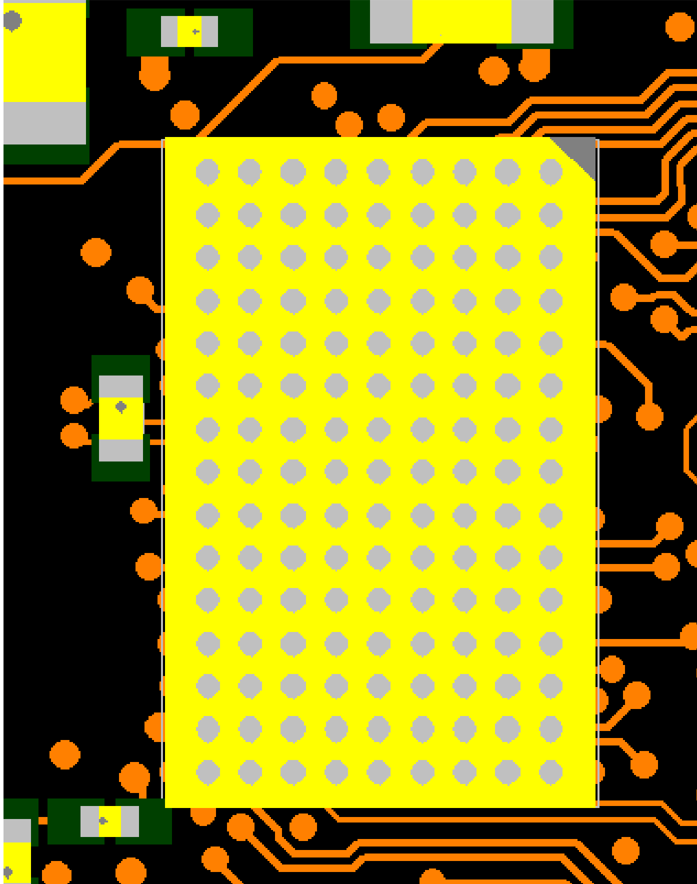
Too little space around through holes on the non mounted side for this component (less than 2mm). See picture below:



6. SMT process

No.	Issue	Result	[Position:] Comments
6.01	Global & local fiducial marks. 1.0 - 2.0mm in diameter, mask free area = 3.0mm in diameter. Preferable doughnut pattern or round. Both sides of PCB need marks. On opposite diagonal corners. Min clearance from PCB edge 4.0mm.	OK	Local fiducial marks exist; as no panelization data exist global fiducial marks has not been evaluated.
6.02	Min of 3-5mm free space around BGA type to allow for microscope inspection, rework possibility and mechanical fixtures for heatsinks.	A	IC202, see comment below.
6.03	Component to component body spacing. Min 0.3mm	A	C680, C684, C686, C689, C732 & IC219. See comment below.
6.04	Component board edge clearance. Top side min 3mm, Bottom side min 5mm. If panelized >= 0.5mm from edge. Special considerations for ceramics	A	R301, See comment below.
6.05	Max component height 18mm.	OK	
6.06	Max component weight 25g	OK	
6.07	No heavy / large components on bottom side of double reflow boards.	OK	
6.08	SMD component optimized for automation.	OK	
6.09	Component has right size for layout.	A	IC206, IC209, IC224, D6, F1, F2
6.10	Any other component issue.	A	C730, C989, C991; See comment below.

6.02:
IC202:
Several components obstruct inspection and rework possibilities for this BGA-component. See illustration below.

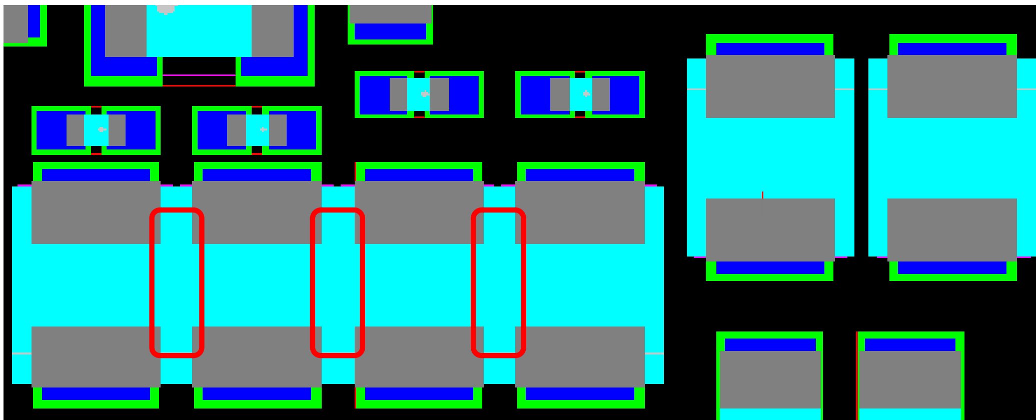


6.03:
C680, C684, C686, C689, C706, C707:

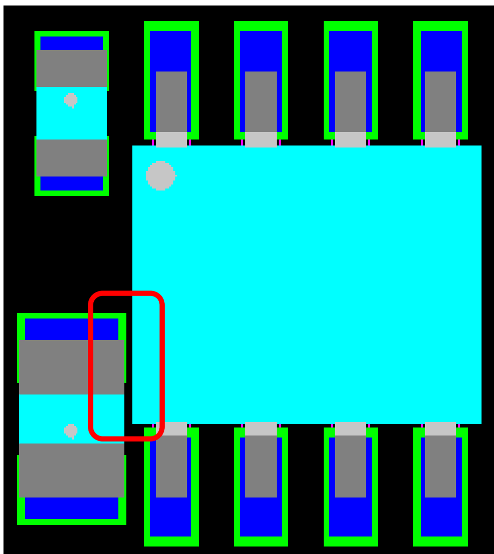
3145200230	C 10uF Ttal, T494,16V, B-case	6	PCS	C680
T494B106M016AT	Kemet			

Insufficient distance between 4 of the 6 components has been detected. In case of the usage of a tantalum B-size component batch with maximum physical outline (2.80+0.20 =3.00mm), the individual distances between C680, C684, C686 and C689 are too small and there is a great risk of the components touching each other during SMT placement causing both misplacement and misalignment and missing solder joints.

The individual distance between C706 and C707 is adequate and it is therefore recommended to increase the individual distances between C680, C684, C686 and C689 to the same distance as in between C706 and C707.

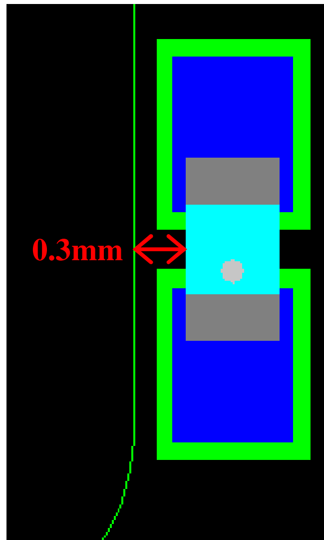


C732 & IC219:
Insufficient distance between C732 and IC219 has been detected. The distance is measured to 0.115mm and is therefore below the recommended distance of 0.3mm. There is a potentional risk of the components touching each other during SMT placement causing both misplacement and misalignment and missing solder joints.



6.04:
R301:
The distance from component to board edge is measured to 0.3mm which is below the recommended distance of 0.5mm for panelized boards. (Break-off frame for transportation).

Due to the current oversized pad layout for R301, there is a risk of the component "floating" even further towards the board edge and hereby reducing the distance to less than 0.3mm.

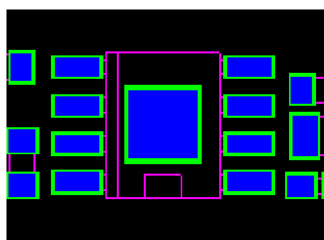


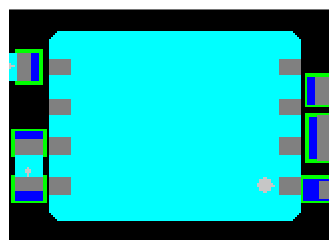
6.09:
IC206:

The physical dimensions of this component have a different size than the CAD layout.

3010200070	IC M25P64 64Mbit Serial Flash 75MHz 8-VDFPN	1	PCS	IC206
M25P64-VME6TG	Numonyx			

The CAD layout is too narrow and the component pins just barely touches the pads on the PCB causing a high risk of poor quality yields due to missing solder joints. Inner distance between pin rows is measured to 6.8mm and outline distance between the pad rows on the PCB is measured to 7.15mm.


Pads only:


Component "placed" on top of pads:

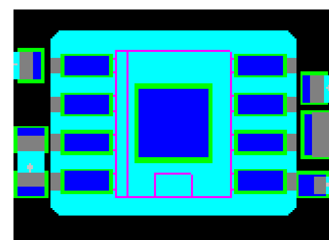

Pad layout seen "through" component:

Figure 26. VDFPN8 (MLP8) 8-lead Very thin Dual Flat Package No lead, 8 × 6 mm, package outline

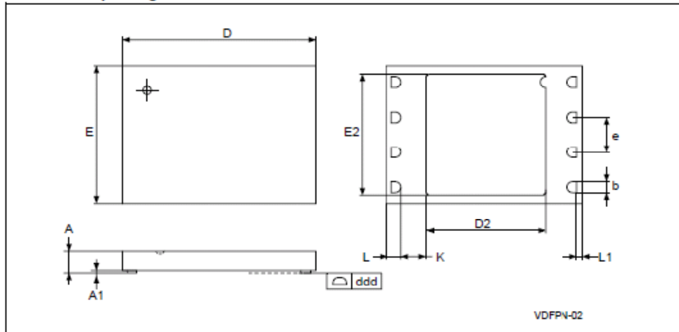


Table 18. VDFPN8 (MLP8) 8-lead Very thin Dual Flat Package No lead, 8 × 6 mm, package mechanical data

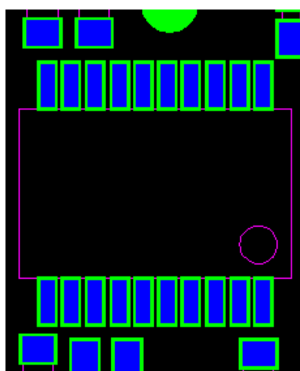
Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	0.85		1.00	0.0335		0.0394
A1		0.00	0.05		0.0000	0.0020
b	0.40	0.35	0.48	0.0157	0.0138	0.0189
D	8.00			0.3150		
D2	5.16		(1)	0.2031		
ddd			0.05			0.0020
E	6.00			0.2362		
E2	4.80			0.1890		
e	1.27	–	–	0.0500	–	–
K		0.82			0.0323	
L	0.50	0.45	0.60	0.0197	0.0177	0.0236
L1			0.15			0.0059
N		8			8	

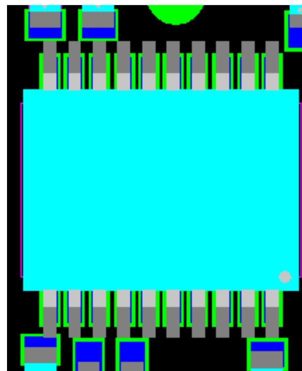
1. D2 Max must *not* exceed (D – K – 2 × L).

IC209:

3060200070	MAX3222EAP, SSOP20, SMD	1	PCS	IC209

This component is defined as SSOP20 in the BOM file but the CAD layout seems to be TSSOP20.

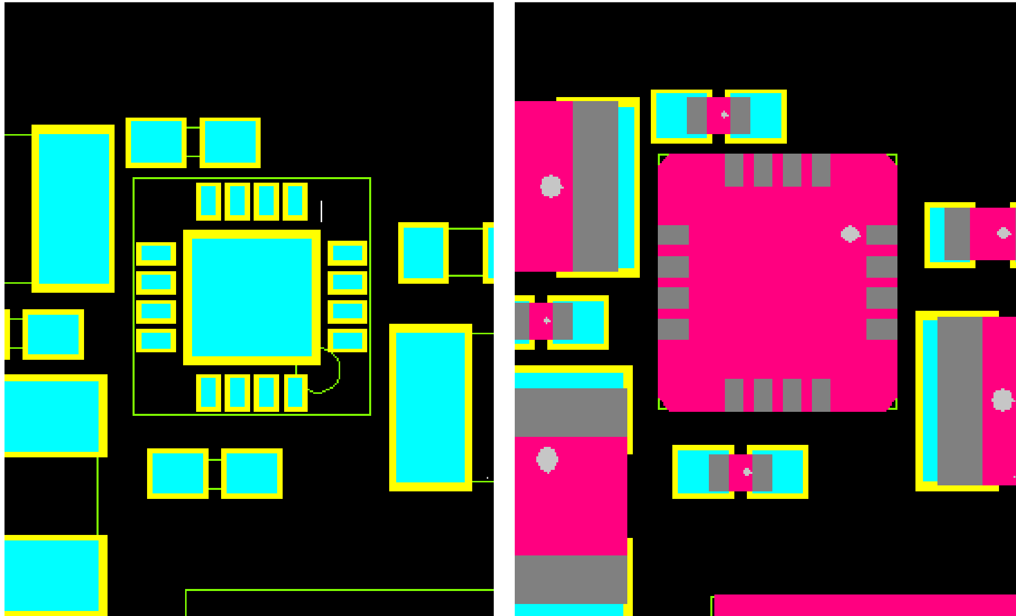




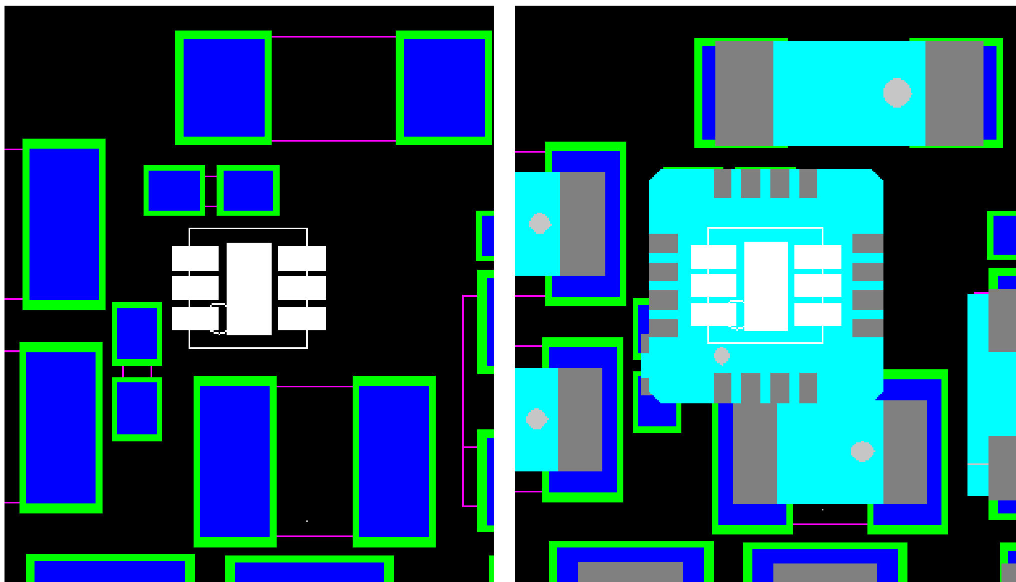
IC224:
IC223 and IC224 are both defined as LLP16 housing in the BOM file, but IC224 has another layout in the CAD data, seems to be SOT23-6 instead.

3032300250	Regulator DDR Termination LP2996 LLP16	2	PCS	IC223,IC224
LP2996LQ/NOPB	National			

IC223:



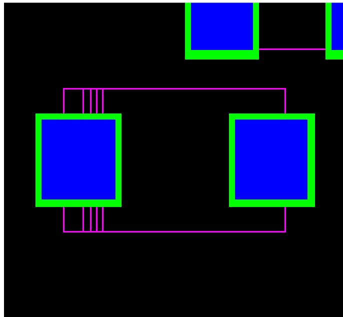
IC224:

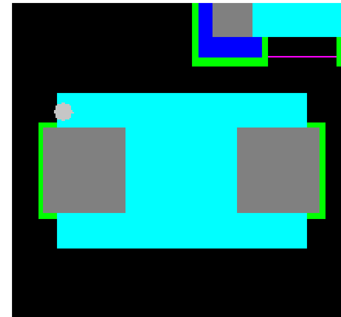


D6:

3101201180	D, 10MQ040N,40V 1,5A Schot,SMA	1	PCS	D6

The physical dimensions of this component do not fit the current CAD layout. The measured outline distance is 5.4mm and “International Rectifier” recommends 5.53mm as optimal distance.





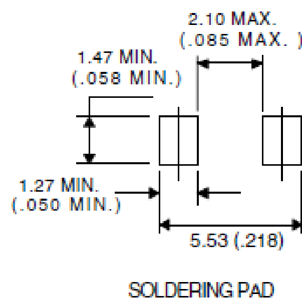
International
IOR Rectifier

PD-20518 rev. D 11/99

10MQ040N

SCHOTTKY RECTIFIER

2.1 Amp

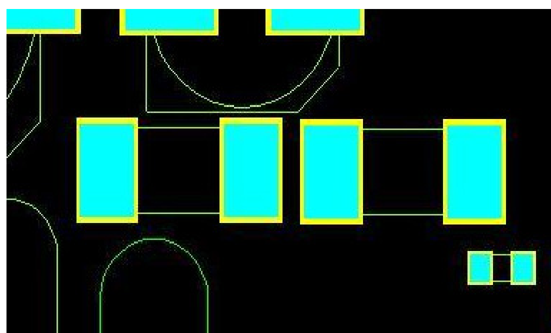


F1, F2:

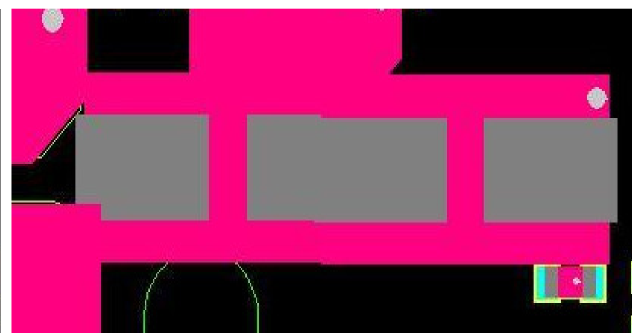
3203300290	Fuse 2,0A FF, SMD,w holder	2	PCS	F1,F2

The BOM file denotes the use of a fuse **with** a holder, but the CAD layout denotes the use of a fuse without a holder.

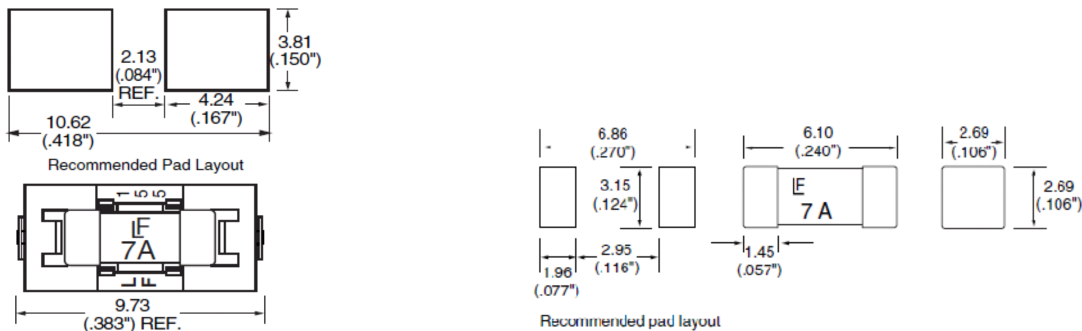
If you remove the holder, the fuse itself will actually fit the chosen CAD layout.



Recommended layout with holder:



Recommended layout without a holder:



The current layout has a measured outline pad to pad distance of 6.7mm which is smaller than the recommended 6.86mm, but the fuse without the holder will still fit the current layout.

6.10:
C730, C989, C991:

The BOM file denotes the use of SANYO CV-AX CAN capacitors for all three components. It seems that this particular type is obsolete or at least going to be in the nearby future and it is therefore recommended to use another type.
The SANYO OS-CON SVP series could be a recommendation assuming the right value and size can be found within this series.

7. Through hole components

No.	Issue	Result	[Position:] Comments
7.01	PTH design ok, paste volume, spacing between comp and PCB.	NA	Selective soldering recommended.
7.02	Annular rings comply with IPC-7251.	A	JTP1, JTP2 & J4, see comment below.

7.02:
JTP1 & JTP2:
The pin diameter for these components lies between 0.98 and 1.05mm.

Max Lead Dia	Finished Hole Dia	Mounted Land	Internal Layer Land Dia	Opposite Land	Solder Mask Top & Bottom	Assembly Top & Bottom	Plane Clearance "Anti-pad" Dia
0,90	1,05	1,55	1,55	1,55	1,55	1,55	1,55
0,95	1,10	1,60	1,60	1,60	1,60	1,60	1,60
1,00	1,15	1,65	1,65	1,65	1,65	1,65	1,65
1,05	1,20	1,70	1,70	1,70	1,70	1,70	1,70
1,10	1,25	1,75	1,75	1,75	1,75	1,75	1,75

IPC-7251 recommends a finished hole diameter of at least 1.20mm for a pin diameter of 1.05mm, so a finished hole diameter of 1.0998mm as recorded from gerber data is too small.

J4:
The pins for this component are square shaped. Hence the max lead diameter is the diagonal: 0.66mm x √2 = 0.93mm.

Max Lead Dia	Finished Hole Dia	Mounted Land	Internal Layer Land Dia	Opposite Land	Solder Mask Top & Bottom	Assembly Top & Bottom	Plane Clearance "Anti-pad" Dia
0,90	1,05	1,55	1,55	1,55	1,55	1,55	1,55
0,95	1,10	1,60	1,60	1,60	1,60	1,60	1,60
1,00	1,15	1,65	1,65	1,65	1,65	1,65	1,65
1,05	1,20	1,70	1,70	1,70	1,70	1,70	1,70
1,10	1,25	1,75	1,75	1,75	1,75	1,75	1,75

IPC-7251 recommends a finished hole diameter of at least 1.10mm for a pin diameter of 1.05mm, so a finished hole diameter of 1.0008mm as recorded from gerber data is too small.

8. Reflow soldering

No.	Issue	Result	[Position]: Comments
8.01	Reflow capability for each component	OK	
8.02	Thermal distribution for individual part, total. Thermal relief for through hole/SMD with ground connection.	OK	
8.03	Component population/ density. Even distribution, proper & consistent orientation for wave and/or reflow.	OK	
8.04	PTH can withstand temp if for PTH reflow.	OK	See below comments in 11.01.

9. Reflow/adhesive

No.	Issue	Result	[Position:] Comments
9.01	No high standoffs from PCB surface to component underside when using adhesive attachment. Max. 2mm	NA	

10. Wave soldering

No.	Issue	Result	[Position]: Comments
10.01	Pad geometry/ component orientation, solder thieves.	NA	
10.02	PTH header/connector perpendicular to wave	NA	
10.03	Component population/ density. Even distribution, proper & consistent orientation for wave and/or reflow.	NA	
10.04	Min of component spacing for wave soldering is height of tallest of two components.	NA	
10.05	Selective soldering with solder pallet – min 4mm free space from solder area, height 4-5mm, max height 8mm with special design.	NA	
10.06	No wave solder 4 sided SMD or fine pitch SMD, solder angle 45º	NA	

11. Selective soldering

No.	Issue	Result	[Position:] Comments
11.01	Dedicated selective soldering machine.	OK	JTP1, JTP2, J3, J4

12. Summary

It is recommended to do a re-layout of the board due to numerous occasions of critical design issues on both sides of the board. The conclusion is especially based on deviations in the paragraphs listed below:

5.09:
Numerous occasions where vias are placed under pads. IC206, IC221, IC222, IC223 & IC802 all have vias in ground pad.

5.15:
Numerous occasions where the recommendations listed in IPC-7351 has not been adhered to. Especially on the 0402 & 0603 chip layouts.

5.21:
Minimum etch distance from PCB edge 0.5mm. IC104: There is too little distance from one of the pads to the PCB edge. Such a small distance can be difficult for the PCB-manufacturer to manufacture; a potential risk exists, that the bare copper can be exposed during the milling process.

6.03:
Component to component body spacing. Minimum 0.3mm. C680, C684, C686 & C689. Insufficient distance between these 4 components has been detected.

6.09:
Component has right size for layout. IC206, IC209, IC224, D6.
IC224 is defined as LLP16 housing in the BOM file, but IC224 has another layout in the CAD data, seems to be SOT23-6 instead.

7.02
Annular rings comply with IPC-7251. JTP1, JTP2 & J4:
JTP1 & JTP2: The pin diameter for these components lies between 0.98 and 1.05mm.
IPC-7251 recommends a finished hole diameter of at least 1.20mm for a pin diameter of 1.05mm, so a finished hole diameter of 1.0998mm as recorded from gerber data is too small.
J4: The pins for this component are square shaped. Hence the max lead diameter is the diagonal: 0.66mm x √2 = 0.93mm.
IPC-7251 recommends a finished hole diameter of at least 1.10mm for a pin diameter of 1.05mm, so a finished hole diameter of 1.0008mm as recorded from gerber data is too small.