

Detectors for Particle Physics

Semiconductor Detectors

D. Bortoletto Purdue University

Tracking and Vertex Detector

- Solid state detectors especially silicon offer high segmentation
- Determine position of primary interaction vertex and secondary decays



Silicon Detectors in HEP (representative selection, approx. dates)

- Silicon detectors also continue to be improved
 - Size
 - Material
 - Radiation hardness



A brief history of solid state detectors

J. Kemmer 1979

NUCLEAR INSTRUMENTS AND METHODS 169 (1980) 499-502, © NORTH HOLLAND PUBLISHING CO

FABRICATION OF LOW NOISE SILICON RADIATION DETECTORS BY THE PLANAR PROCESS

J KEMMER

Fachbereich Physik der Technischen Universität Munchen, 8046 Garching, Germany

Received 30 July 1979 and in revised form 22 October 1979

Dedicated to Prof Dr H -J Born on the occasion of his 70th birthday

By applying the well known techniques of the planar process oxide passivation, photo engraving and ion implantation, Si pn-junction detectors were fabricated with leakage currents of less than $1 \text{ nA cm}^{-2}/100 \,\mu\text{m}$ at room temperature Best values for the energy resolution were 100 keV for the 5 486 MeV alphas of ²⁴¹Am at 22 °C using 5×5 mm² detector chips

NA11 at CERN

- First use of a position-sensitive silicon detector in HEP experiment
- Measurement of charm quark lifetimes
- 1200 diode strips on 24x 36 mm²
- 250-500 µm thick bulk material
- 4.5 µm resolution



LEP and SLAC SLC Experiments

LEP and SLC

- Readout ASICs at end of ladders
- Minimize mass inside tracking volume
- Minimize mass between interaction point and detectors
- Minimize the distance between interaction point and the detectors
- Enabled measurement of b-quark lifetimes and b-tagging



ALEPH

- 2 silicon layers, 40cm long, inner radius 6.3cm, outer radius 11cm
- 300 µm silicon wafers giving thickness of only 0.015X₀
- S/N(r-φ) = 28:1
- S/N(z)= 17:1
- r-φ= 12 μm; z = 14μm

CDF & D0 at the Tevatron

- CDF pioneered the silicon vertex detector in the hadron collider environment and pioneered the silicon vertex trigger separating *b*-hadrons
- Emphasis shifted to tracking and vertexing allowing precision measurements in very complex environment
- Cover large area with many silicon layers
- Detector modules including ASIC's and services INSIDE the tracking volume

CDF's first Silicon Vertex Detector at the Smithsonian Museum, Washington



The LHC silicon detectors

- ATLAS Strips: 61 m² of silicon, 4088 modules, 6x10⁶ channels Pixels: 1744 modules, 80 x 10⁶ channels
- CMS the world largest silicon tracker 200 m² of strip sensors (single sided) 11 x 10⁶ readout channels ~1m² of pixel sensors, 60x10⁶ channels
- ALICE Pixel sensors Drift detectors
 Double sided strip detectors





66 Million Pixels



D. Bortoletto Lecture 4

VELO: Si

Strips

LHCb

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The LHC detectors



From LEP to the LHC



Solid State Detector

- A solid state detector is an ionization chamber
 - Ionizing radiation creates electron/hole pairs
 - Charge carriers move in applied E field
 - Motion induces a current in an external circuit, which can be amplified and sensed.



However, free carriers must first be removed so the applied voltage doesn't simply result in a (large) DC current – this is usually accomplished with a reverse biased diode.

Comparison solid state versus gas

Ionization chamber medium could be gas, liquid, or solid

- Gas \Rightarrow electron and ion pairs; Semiconductor \Rightarrow electron and hole pairs

	Gas	Solid
Density	Low	High
Atomic number (Z)	Low	Moderate (Z=14)
lonization Energy (ε _ι)	Moderate (≈ 30 eV)	Low (≈3.6 eV)
Signal Speed	Moderate (10ns-10μs)	Fast (<20 ns)

Solid State Detectors

■ Energy (E) to create e-h pairs 10 times smaller than gas ionization ⇒ increase charge⇒ good E resolution

$$\frac{\Delta E}{E} \propto \frac{1}{\sqrt{N}} \propto \frac{1}{\sqrt{E/\varepsilon_I}} \propto \sqrt{\varepsilon_I}$$

- Greater density:
 - Reduced range of secondary electrons
 ⇒ excellent spatial resolution
 - Average E_{loss} ≈390eV/ μm ≈108 e-h/ μm (charge collected is a function of thickness d but no multiplication)
 - To minimize multiple scattering thickness d should be small
 - 300 μm ≈32,000 e-h pairs → good S/N

Why silicon ?

Leverages IC Technology Exponential improvements of silicon Ics WILL end someday... but when?



Semiconductor



Semiconductor: at room temperature electrons can already occupy the conduction band and may recombine with holes.

Thermal equilibrium is reached between excitation and recombination when the charge carrier concentration $n_e = n_h = n_i$ = intrinsic carrier concentration



Principle of operation





PN Junction

PN junction without external voltage

 Free charges move until the chemical potential is balanced by an electrical potential called the built-in potential



The space charge (depletion) region can be made bigger by applying a reverse bias voltage



Width of the depletion zone

- Solve Poisson eq. using conservation of charge N_Ad_p=N_Dd_n
- Effective doping concentration in typical silicon detector with p+-n junction
 - $N_A = 10^{15} \text{ cm}^{-3} \text{ in p+ region}$
 - $N_D = 10^{12} \text{ cm}^{-3} \text{ in n bulk.}$
- Without external voltage:

 $-W_p = 0.02 \ \mu m$ and $W_n = 23 \ \mu m$

- Applying a reverse bias voltage of 100 V:
 - $-W_{p} = 0.4 \ \mu m \text{ and } W_{n} = 363 \ \mu m$



 $N_{cl} \approx 10^{12} \text{ cm}^{-3}$

Width of depletion zone

$$W = \sqrt{\frac{2\varepsilon V}{e} \frac{1}{N_D}} \quad if \ N_A >> N_D$$

e=electron charge, ε=resistivity μ= majority carriers mobility N= dopant density

$$W \approx \sqrt{2\varepsilon\mu\rho V}$$
 with $\rho = \frac{1}{e\mu N}$

n

The voltage V needed to deplete a device of thickness d is called the depletion voltage V_d

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Depletion Zone & Capacitance

The depletion voltage can be determined by measuring the capacitance versus reverse bias voltage. The capacitance is simply the parallel plate capacity of the depletion zone.



Leakage current



Leakage current



Generation current

- From thermal generation in the depletion region
- Reduced by using pure and defect free material with high carrier lifetime
- Keep temperature low & controlled

$$j_{gen} \propto T^{3/2} \exp\left(\frac{1}{2kT}\right)$$

I_{leak} sensitive to process quality

Diffusion current

 charge generated in the undepleted zone adjacent to the depletion zone which diffuse into the depletion zone



Charge collection

 Electron and hole pairs created in the depletion region move under the E field

$$v_{e,h}(x) = \mu_{e,h} E(x)$$
$$\mu_e = 1500 cm^2 / Vs$$
$$\mu_h = 450 cm^2 / Vs$$

- 70 Charge Collection Time (Vd = 40 V) Electrons 60 50 <u>a</u> 40 2 III 30 2010 10 ns n 50 80 90 40 100 70 Bias Voltage
- The time required for a carrier to traverse the sensitive volume is the collection time.
- The collection time can be reduced by over-biasing the sensor

$$t(x) = \frac{D^2}{2\mu_p V_d} \ln \left(\frac{V_{bias} - V_{fd}}{V_{bias} - V_{fd} + 2V_{fd} \left(1 - \frac{x}{D}\right)} \right)$$

Silicon Strip Detectors (SSD)

- By segmenting the implant we can reconstruct the position of the traversing particle in one dimension
- DC-coupled strip detector simplest position sensitive Silicon detector
- Standard configuration:
 - Strips p implants
 - Substrate n doped (~2-10 kΩcm) and ~300µm thick
 - V dep < 200 V</p>
 - Backside Phosphorous implant to establish ohmic contact and to prevent early breakdown
- Highest field close to the collecting electrodes (junction side) where most of the signal is induced





Strip Detector

- AC coupling blocks DC leakage current
- Integration of coupling capacitances in standard planar process.
 - Deposition of SiO₂ with a thickness of 100–200 nm between p+ and aluminum strip
 - Increase quality of dielectric by a second layer of Si_3N_4 .
- Long poly silicon resistor with R>1MΩ to connect the bias voltage to the strips:







A typical strip module (CMS)



Double Sided Silicon Detectors

Advantages:

- More elegant way for measuring 2 coordinates than using stereo modules
- Saves material

Disadvantages:

- Needs special strip insulation of n-side (p-stop, p-spray techniques)
- Very complicated manufacturing and handling procedures
- Expensive
- Ghost hits possible





Scheme of a double sided strip detector (biasing structures not shown)



Positive oxide charges cause electron accumulation layer.

Pixel detector

- Advantages
 - Pixel detectors provides space-point information

solder

- Small pixel area
 - low detector capacitance (≈1 fF/ Pixel)
 - large signal-to-noise ratio (e.g.
 150:1).
 fine pitch (50 μm) bump placements
- Small pixel volume
 - low leakage curre
- Disadvantages:
 - Large number of
 - Large number of connections
 - Large bandwidth
 - Large power constant





indium

100

E 5 8 - 17



Signal

- The signal generated in a silicon detector depends essentially only on the thickness of the depletion zone and on the dE/dx of the particle.
 - The distribution is given by the Landau distribution
 - Since the mean energy loss per cm is 3.87 MeV/cm
 - For 300 µm silicon the most probable charge is ≈ 23400 e-/h pairs





Mean charge



Noise

- The noise depends on: geometry of the detector, the biasing scheme, the readout electronics..
- Noise is typically given as "equivalent noise charge" ENC. This is the noise at the input of the amplifier in elementary charges.
- The most important noise contributions are:
 - Leakage current
 - Detector capacitance
 - Detector parallel resistor
 - Detector series resistor
- The overall noise is the quadratic sum of all contributions:

$$ENC = \sqrt{ENC_{C}^{2} + ENC_{I}^{2} + ENC_{Rp}^{2} + ENC_{Rs}^{2}}$$





S/N optimization

- Silicon sensors have low occupancy ⇒ most channels have no signal. Good hits are select by requiring N_{ADC}> noise tail. If cut is too high ⇒ efficiency loss
- Typical Values for strip detectors is N/S> 10-15. Radiation damage severely degrades the S/N. Thus S/N determines lifetime of the detector in a harsh radiation environment
- To achieve a high signal to noise ratio:
 - Low detector capacitance (i.e. small pixel size or short strips)
 - Low leakage current
 - Large bias resistor
 - Short and low resistance connection to the amplifier
 - Long integration time
- The optimal design depends on the application
- For pixel detectors the important parameter is the S/Threshold. The threshold in current detectors is of the order of 2500 e⁻.

Diffusion

Diffusion is caused by random thermal motionWidth of charge cloud after a time t given by

$$\sigma_D = \sqrt{2Dt}$$
 with $D = \frac{kT}{e}\mu$

Drift time for: d=300 μm, E=2.5KV/cm: t_d(e) = 9 ns, t_d(h)=27 ns

Diffusion: Typical value: 8 μm for 300 μm drift.



 σ_D =width "root-mean-square" of the charge carrier distribution t=drift time K=Boltzman constant e=electron charge D=diffusion coefficient T=temperature μ =mobility μ_e = 1350 cm² / V·s, μ_h = 450 cm² / V·s





Charge density distribution for 5 equidistant time intervalls:



r (a.u.)

Position resolution

Resolution is the spread of the reconstructed position minus the true position



Position resolution

- Position resolution is degraded by many factors
- Relationship of strip pitch and diffusion width (typically 25-150 μm and 5-10 μm)
- Statistical fluctuations on the energy deposition
- Typical position resolution s for a 300μm thick sensor with S/N=20



Radiation damage

- Damage due to non ionizing energy loss (NIEL)
 - Atomic displacement caused by massive particles (p,n,π)



Affects mainly the sensors

- Damage due to ionizing energy loss
 - Proportional to absorbed radiation dose
 - 1 Gy = 1 J/kg = 100 rad = 10⁴ erg/ g (energy loss per unit mass)
 - Trap of ionization induced holes by "dangling bond" at Si-SiO2 interface



Affects both detector and electronics

- Atomic displacement caused by massive particles (p,n,π)
 - Charged defects create donors and acceptors
 - Increase Neff (= $N_D N_A$) and depletion voltage ($V_{dep} \propto |N_{eff}|$)
 - Type Inversion
- Shallow defects trap and detrap electrons and holes
 - Degrade charge collection efficiency
- Midgap defects effectively reduces Eg
 - Increase dark current





INCREASE IN DARK CURRENT

- It can saturate a charge integrating amplifier
- It can lead to thermal runaway

- TYPE INVERSION
 - Increase of depletion voltage
 - Attention must be taken to avoid breakdown



Even after heavy irradiation **both** p and n sides work at low voltage (under depleted) and sensors act as if there were 2 diode junctions!

- Deterioration of Charge Collection Efficiency (CCE) by trapping
- Trapping is characterized by an effective trapping time τ_{eff} for electrons and holes:



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- The conjecture that bulk damage is proportional to the total KE imparted to displaced silicon atoms is called "the NIEL hypothesis."
- It is conventional to use 1 MeV neutrons as the benchmark

KERMA = Kinetic Energy Released in Matter

$$KERMA(MeV) = D(MeVmb) \times \phi(\frac{\#}{cm^2}) \times (\#Si) \times (\frac{10^{-27} \text{ cm}^2}{\text{mb}})$$



Challenges for the future

High Luminosity LHC

- Radiation tolerance (~10¹⁶/cm² for pixels, 10¹⁵/cm² for strips; ~20 x current)
- High hit rate (up to 1.5 GHz/cm² in pixels)
- High track density (200 or more spectator events)
- e⁺e⁻ colliders
 - Extremely low material (minimize multiple scattering)
 - Requires very low average power
 - Extremely good position resolution (ILC goal is ~3 microns)

Ultra radiation hard detectors: 3D

- P-N junction in the bulk by "drilling" electrodes using Deep Reactive Ion Etching (DRIE)
 - Maximum drift and depletion distance governed by electrode spacing
 - Lower depletion voltages
 - Radiation hardness
 - Fast response







Industrialization has been successful and 3D technology is used ATLAS IBL

Monolithic Pixels

- Sensors and ROC in the same wafer
- Signal is created in epitaxial layer (10-15 µm e.g. AMS 0.35 µm)
 - Q~ 80 e-h / µm → signal <1000 e-
- Q collection (thermally) to diode with help of reflection on boundaries with pwell and substrate (high doping)
- Advantages of CMOS sensors:



- Sensitive volume (epitaxial layer) is 10–15 µm thick
- Standard production, fabrication technology \rightarrow cheap, fast turn-around
- small pixel sizes(pitch 20 –30 µm)→few µm resolution!
- BUT :
 - Very thin sensitive volume impact on signal magnitude
 - Sensitive volume almost un-depleted impact on radiation tolerance & speed



Silicon-on-Insulator

Chemical bonding of low resistivity wafer electronics with high resistivity sensor wafer

- Full CMOS capability
 - In-pixel processing, low power, high speed
- Fully depleted sensor wafer
- Back gating effect

V_{bias} affects analog transistor functionality



Different pixel technologies



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BACKUP

Simulation



Silicon Properties

Excellent detector material

- Low ionization energy (good signal). The band gap is 1.12 eV, but it takes 3.6 eV to ionize an atom. The remaining energy goes to phonon excitations (heat).
- Long mean free path (good charge collection efficiency)
- High mobility (fast charge collection)
- Low Z (Z=14 low multiple scattering)
- Oxide (SiO₂) has excellent electrical properties
- Good mechanical properties
 - Easily patterned to small dimensions
 - Can be operated in air and at room temperature (many SSD require cooling)
- Industrial experience and commercial applications
- Crystalline \Rightarrow radiation damage



Hybrid Pixel Module for CMS

Sensor:

- Pixel Size: 150mm x 100mm
 - Resolution $\sigma_{r-\phi} \sim 15 \mu m$
 - Resolution $\sigma_z \sim 20 \mu m$
- n+-pixel on n-silicon design
 - Moderated p-spray → HV robustness

Readout Chip:

- Thinned to 175µm
- 250nm CMOS IBM Process
- 8" Wafer

Kapton signal cable 21 traces, 300µ pitch Alu-power cable 6 x 250µ ribbon

High Density Print 3 Layers, 48µ thick

Silicon Sensor t=285μ > 100μ x 150μ pixels

>µ-bump bonding

16 x Readout Chips (CMOS) 175μ thick

SiN base strips 250m thick, screw holes

screw holes

R. Horisberger

CMS Pixel Sensors

 Baseline CMS design: n⁺-n pixels for partial depletion operation and increased Lorentz angle in high B field.

- 78 μm n⁺-implants.
- P-spay or open p-stops rings provide isolation



Ultra-radiation hard: Diamond

- Poly crystalline and single crystal
- Competitive (to Si), used in several radiation monitor detectors
- Large band gap (x5 Si)
 - no leakage current
 - no shot noise
- Smaller $\varepsilon_r (x \ 0.5 \ Si)$
 - lower input capacitance
 - lower thermal and 1/f noise
- Small Z=6 →large radiation length (x2 in g/cm²)
- Narrower Landau distribution (by 10%)
- Excellent thermal conductivity (x15)
- Large w_i (x 3.6) →smaller signal charge

- poly-CVD diamond wafers can be grown
 >12 cm diameter, >2 mm thickness.
- Wafer collection distance now typically 250µm (edge) to 310µm (center).
- 16 chip diamond ATLAS modules



- sc-CVD sensors of few cm² size used as pixel detectors
- High quality scCVD diamond can collect full charge for thickness 880µm



Summary of material properties

Drift velocity for electrons: $\vec{v}_n = -\mu_n \cdot \vec{E}$ for holes: $\vec{v}_p = -\mu_p \cdot \vec{E}$

Mobility for electrons:

for holes:

S:

$$\mu_n = \frac{e\tau_n}{m_n}$$

$$\mu_p = \frac{e\tau_p}{m_p}$$

μ_p(Si, 300K)≈450 cm²/Vs μ_n(Si, 300K)≈1450 cm²/Vs

Resistivity:

$$\rho = \frac{1}{e\left(\mu_n n_e + \mu_p n_h\right)}$$



- e= electric charge
- E= external field
- m_n and m_p = effective mass of electrons and holes
- τ_n and τ_p = mean free path of electrons and holes
- n_n and n_p = density of electrons and holes

Wafer Fabrication

 Start with very pure quartzite sand. Clean it and further purify by chemical processes. Melt it and add the tiny concentration of phosphorus (boron) dopant to make n(p) type silicon. Pour it in a mold to make a polycrystalline silicon cylinder



 Using a single silicon crystal seed, melt the vertically oriented polysilicon cylinder onto the seed using RF power to obtain single crystal 'ingot'.







3) Slice ingot into wafers of thickness 300- $500\mu m$ with diamond encrusted wire or disc saws.

Diode Processing

animation



Start with n-doped silicon wafer, $\rho \approx 1-10 \text{ k}\Omega \text{ cm}$. Silicon can be turned into n-type by neutron doping (³⁰Si+n \rightarrow ³¹Si, ³¹Si \rightarrow ³¹P+ β + ν)

Oxidation at 800 - 1200°C

3) Photolithography (= mask align + photo-resist layer + developing) followed by etching to make windows in oxide



Diode Processing



Doping by ion implantation (or by diffusion)

Annealing (healing of crystal lattice) at 600 °C



Photolithography followed by AI metallization over implanted strips and over backplane usually by evaporation.

⇒Simple DC-coupled silicon strip detector

Oxide Charge

- Many defects can appear at the interface between Si and SiO₂.
 - Some of the interface atoms will miss oxygen atoms and create Si-O bonds
 - Impurities (H, OH,N)
- These will create levels that can trap mobile electrons and holes (Interface traps)
- The charge due to the trapped electrons and holes onto the oxide defects is the "oxide charge"
- The oxide charge is usually positive ⇒ electron accumulation layer
- It can affect device characteristics: breakdown voltage, strip isolation, interstrip capacitance
 D. Borto



Figure 2.14 Illustration of the oxide–silicon interface and the associated defects: (a) a two-dimensional chemical-bond model and (b) the energy-band model.

Dimitrijev

Radiation Damage in Silicon

- Two general types of radiation damage
 - "Bulk" damage due to physical impact within the crystal
 - "Surface" damage in the oxide or Si/SiO₂ interface
- Cumulative effects
 - Increased leakage current (increased shot noise)
 - Silicon bulk type inversion (n-type to p-type)
 - Increased depletion voltage
 - Increased capacitance
- Sensors can fail from radiation damage
 - Noise too high to effectively operate
 - Depletion voltage too high to deplete
 - Loss of inter-strip isolation (charge spreading)
- Signal/noise ratio is the quantity to watch

Surface Damage

- Surface damage generation:
 - Ionizing radiation creates electron-hole pairs in the SiO₂
 - Many recombine, electrons migrate quickly
 - Holes slowly migrate to Si/SiO₂ interface since hole mobility is much lower than for electrons (20 cm²/Vs vs. 2x10⁵ cm²/Vs)
 - Some holes 'stick' in the boundary layer
- Surface damage results in
 - Increased interface trapped charge
 - Increased fixed oxide charges
 - Surface generation centers
- MOS devices are sensitive to surface damage
 - Electron accumulation under the oxide interface can alter the depletion voltage (depends on oxide quality and sensor geometry)
 - In silicon strip sensors, surface damage effects (oxide charge) saturate at a few hundred kRad





After electron transport:



After transport of the holes



Surface Damage Effects



Figure 4-14 Silicon/silicon dioxide structure with mobile, fixed charge, and interface states (©1980.





- Charges in the oxide layer can cause:
 - Risk to readout electronics
 threshold shifts
 - noise and gain deterioration
 - Increase in the sensors capacitances
 - Single event upset in small feature size devices
- Problems can be minimized by:
 - Silicon crystal orientation (<100> rather than <111>) can minimize interface traps at boundary
 - Reducing oxide thickness
 - Voltage shifts are proportional to the square of the thickness (0.25 µm CMOS more rad hard)
 - Processing

Surface Damage

- Oxide charges in the silicon strip sensors depend on vendor
 - Oxide charge starts out high before irradiation
 - Adversely influences operation in certain biasing configurations
 - Could set a limit to max bias voltage

CDF





D. Bortoletto Lecture 4

Bulk Damage

- Bulk damage is mainly from hadrons displacing primary lattice atoms (for E > 25 eV)
 - Results in silicon interstitial, vacancy, and large disordered region
 - 1 MeV neutron transfers 60-70 keV to recoiling silicon atom, which in turn displaces ~1000 additional atoms
- Defects can recombine or migrate through the lattice to form more complex and stable defects
 - Annealing can be beneficial
 - Defects can be stable or unstable
 - Displacement damage is directly related to the non-ionizing energy loss (NIEL) of the interaction
 - Varies by incident particle type and energy



Bulk Damage

- Displacement damage occurs for all particles
 - Pions and neutrons are typically the most numerous
- Particle flux in a collider environment
 - Experience from CDF Run I suggests $\Phi = \Phi_0/r^{1.7}$
 - Neutron flux falls less rapidly; it eventually becomes significant
- NIEL Radiation damage studies typically normalized to 1 MeV neutron damage equivalent



Bulk Damage Effects

• Leakage Current: $\Delta I = \alpha(t) \Phi V$

- α (t) (damage constant), V (volume), and Φ (fluence).
- Annealing reduces the current
- Independent of particle type

Depletion Voltage:

- $V_{dep} = q |N_{eff}| d^2 / 2\epsilon\epsilon_0$
- Effective dopant concentration $(N_{eff} = N_{donors} - N_{acceptors})$, sensor thickness (d), permitivity ($\epsilon\epsilon_0$).
- Depletion voltage is parameterized in three parts:
 - Short term annealing (N_a)
 - A stable component (N_c)
 - Long term reverse annealing (Non)e 4



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Leakage Current

- Defects create intermediate states within the band gap
 - intermediate states act as 'stepping stones' of thermal generation of electron/hole pairs
 - Some of these states anneal away; the bulk current reduces with time (and temperature after irradiation
- Annealing function $\alpha(t)$
 - Parameterized by the sum of several exponentials α_iexp(-t/τ_i)
 - Full annealing (for the example below) reached after ~1 year at 20°C
 - At low temperatures, annealing effectively stops
 - Dependant on incident particle type (?)



Fig. 3.24 Classification of levels in the forbidden gap.

A: shallow acceptor, e.g. B, B: deep donor, e.g. C₁O₁ C: deep acceptor, e.g. V O₁ D: shallow donor, e.g. P, E: amphoteric level, e.g. V V





Leakage Current

• Measured values of $\alpha(t)$

- One quotes measured values of α(t) after complete annealing at T=20°C: α_∞ = α(t=∞)
 - 'World averages' for α_∞ are :
 2.2 x 10⁻¹⁷ A/cm³ for protons, pions

■ 2.9 x 10⁻¹⁷ A/cm³ for neutrons

- Recent results show α (t=80min,T=60°C)= 4.0 x 10⁻¹⁷ A/cm³ for all types of silicon, levels of impurities, and incident particle types (NIM A426 (1999)86).



Depletion Voltage





Depletion voltage is often parameterized in three parts (Hamburg model): $\Delta N_{eff}(T,t,\Phi) = N_A + N_C + N_Y$ Short term annealing (N_A)

- $N_A = \Phi_{eq} \sum_i g_{a,i} exp(-k_{a,i}(T)t)$
 - Reduces N_Y (beneficial)
 - Time constant is a few days at 20 C
- Stable component (N_c)

$$N_c = N_{c0}(1 - exp(-c\Phi_{eq})) + g_c\Phi_{eq}$$

- Does not anneal
- Partial donor removal (exponential)
- Creation of acceptor sites (linear)
- Long term reverse annealing (N_Y)

 $N_{Y} = N_{Y,\infty}[1-1/(1+N_{Y,\infty}k_{Y}(T)t)], N_{Y,\infty} = g_{Y}\Phi_{eq}$

- Strong temperature dependence
- 1 year at T=20 C or ~100 years at T= -7 C (LHC)
- Must cool Si at the LHC

Most common semiconductors

Germanium:

- Used in nuclear physics
- Needs cooling due to small band gap of 0.66 eV (usually done with liquid nitrogen at 77 K)

Silicon:

- Can be operated at room temperature (but electronics requires cooling)
- Synergies with micro electronics industry
- Standard material for vertex and tracking detectors in high energy physics
- Diamond (CVD or single crystal):
 - Large band gap (requires no depletion zone)
 - very radiation hard
 - Disadvantages: low signal and high cost

Compound semiconductors

Compound semiconductors consist of

- two (binary semiconductors) or
- more than two atomic elements of the periodic table.
 - IV-IV- (e.g. SiGe, SiC),
 - II-V- (e.g. GaAs)
 - II-VI compounds (CdTe, ZnSe)
- Important III-V compounds:
 - GaAs: Faster and probably more radiation resistant than Si. Drawback is less experience in industry and higher costs.
 - GaP, GaSb, InP, InAs, InSb, InAlP
- important II-VI compounds:
 - *CdTe*: High atomic numbers (48+52) hence very efficient to detect photons.
 - ZnS, ZnSe, ZnTe, CdS, CdSe, Cd1xZnxTe, Cd1-xZnxSe

	Ι	II	111	IV	v	VI	VII	VIII
1	1 H							2 He
2	3	4	5	6	7	<mark>8</mark>	9	10
	Li	Be	B	C	N	0	F	Ne
3	11	12	13	14	15	16	17	18
	Na	Mg	Al	Si	P	S	Cl	Ar
4	19	20	31	32	33	34	35	36
	K	Ca	Ga	Ge	As	Se	Br	Kr
5	37	38	49	50	51	52	53	54
	Rb	Sr	In	Sn	Sb	Te	1	Xe
6	55	56	81	82	83	84	85	86
	Cs	Ba	Tl	Pb	Bi	Po	At	Rn
7	87	88	113	114	114	115	117	118
	Fr	Ra	Uut	Uuq	Uup	Uuh	Uus	Uuo