SRS + Timepix

A readout system for the Timepix chip

Michael Lupberger

University of Bonn

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Outline

- Timepix chip
- First system on Xilinx Evaluation Board
- SRS based readout system
  - First steps
  - Common code used
  - Status
- Test beam

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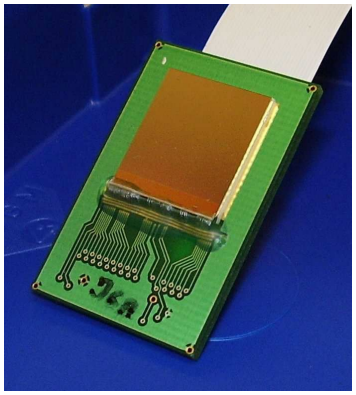
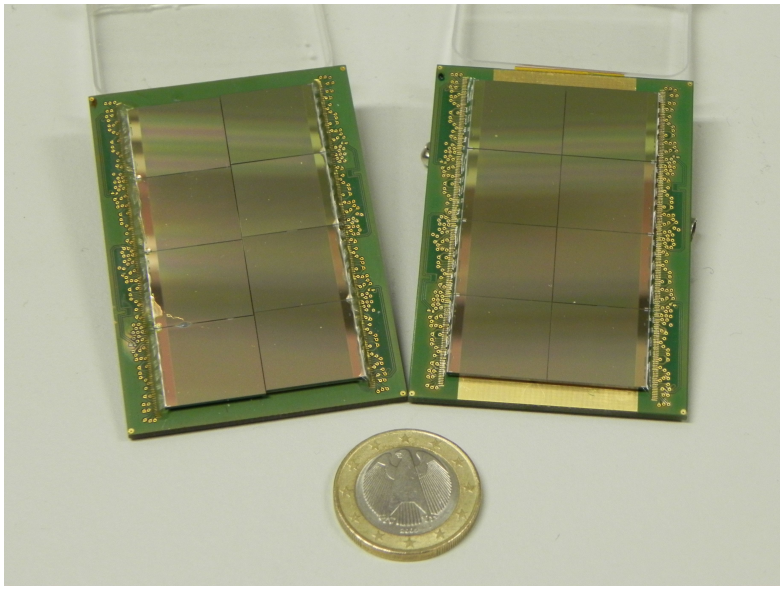
Timepix chip

- Digital readout chip: The Timepix ASIC



- Properties
  - 1.4 x 1.4 cm² active surface
  - 256 x 256 pixel matrix
  - CMOS 250 nm technology, IBM
  - 55 x 55 µm² per pixel
  - amplifier/shaper (t_{rise} ~150 ns)
  - 14 bits count clock cycles
    → Pixel pit when/how long
  - clock up to 100 MHz in every pixel
  - lower threshold
  - threshold level ~ 500 e^- (90 e^- ENC)



- Used as readout anode plane in gaseous detectors

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New readout system

Goals:

- ultimately read out ~100 chips
  → large area detector (full TPC endplate module)
- modular system, Virtex FPGA → use SRS
- ethernet based
- open source firmware and software code
- highest data rate possible (Timepix is slow)
- triggerable, integrate slow control & calibration

- demonstrator for a pixelated TPCs

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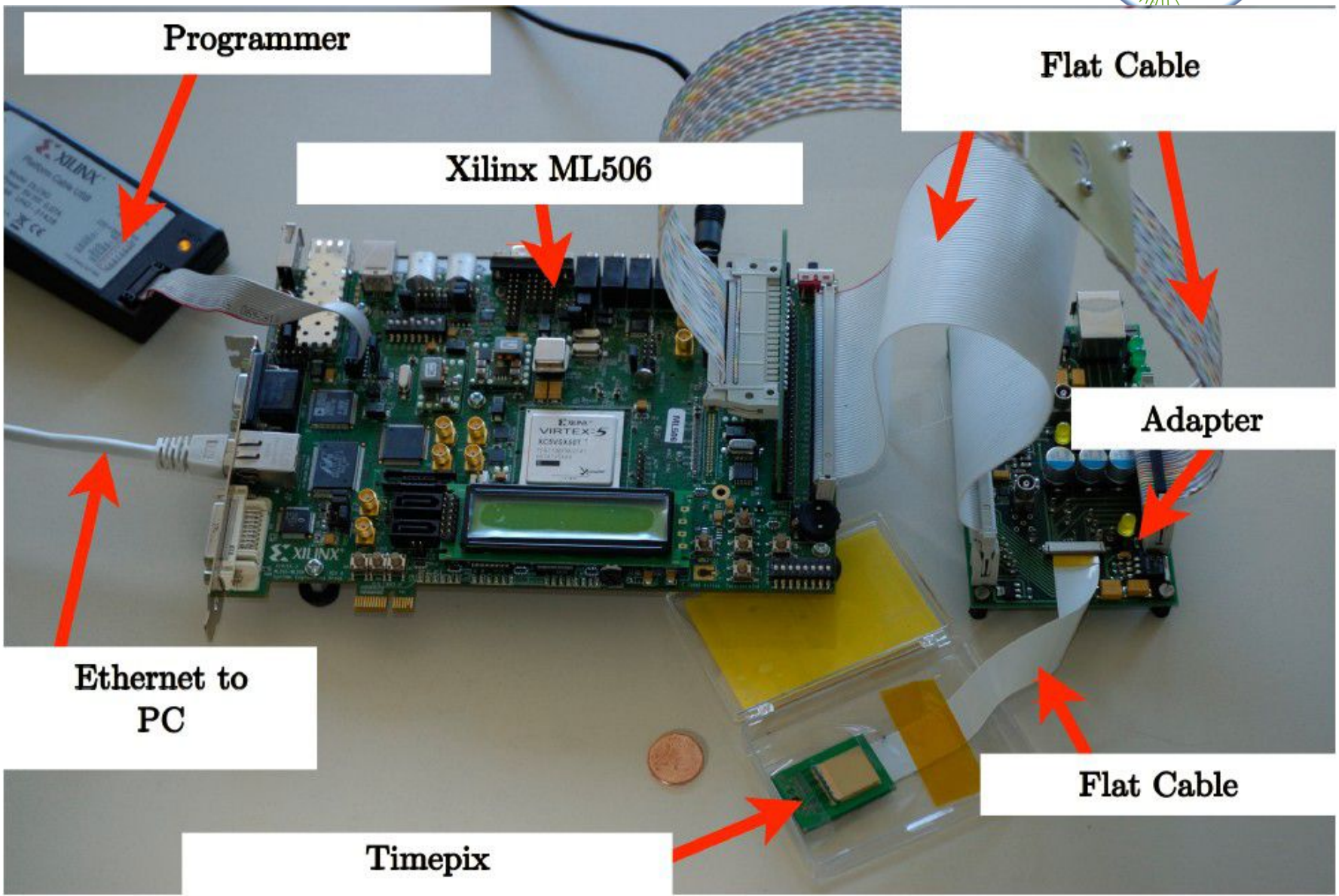
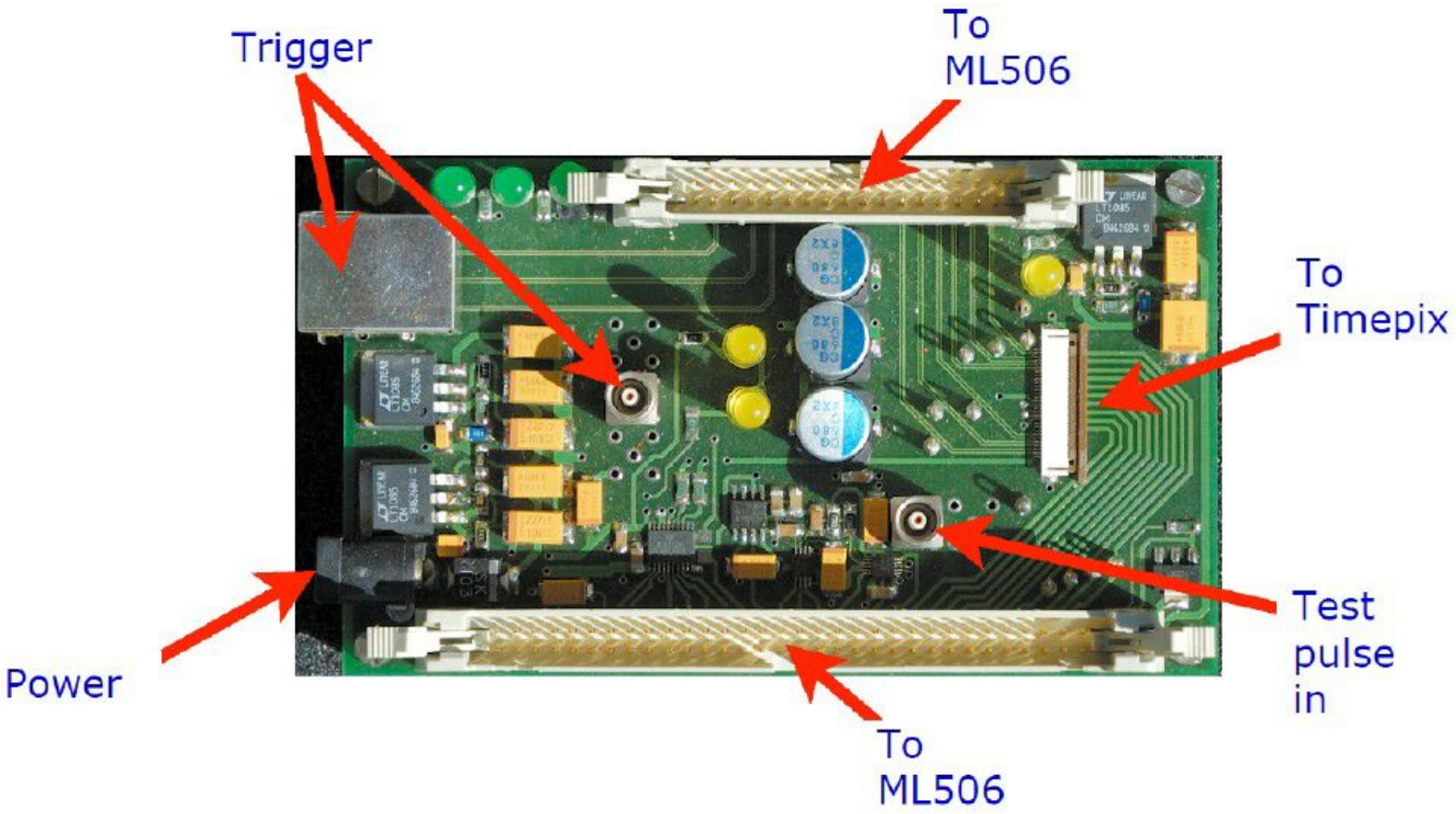
Mainz readout system



Adapter board for Xilinx kit



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Activities on Xilinx Boards

- Setup of second Mainz system in Bonn
  - Xilinx ML506 board with Virtex5 FPGA + adapter board
  - single Timepix readout
- Re-target to Virtex6
  - Xilinx ML605 board with Virtex6 FPGA, new adapter board
- Extension of firmware: zero suppressed, multi threaded readout (maximum readout speed), can handle octoboards

  Development still ongoing (updates from modified SRS firmware)
- Lately: new adapter board with I2C: ADC for analog DAC_out

  DACs + multiplexer for calibration, LVDS drivers, CMOS level shifter

  → small readout system for Uni Siegen and a new detector at CAST

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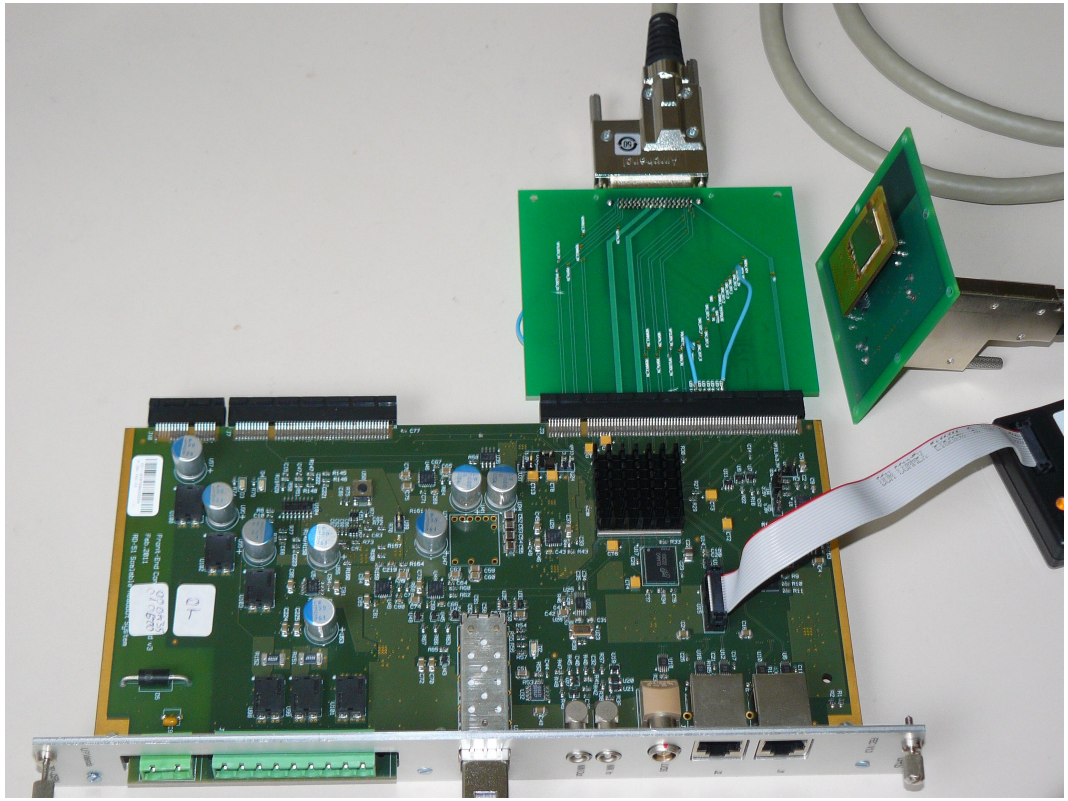
SRS based readout

Activities started in November 2011

- Transformation of firmware from Xilinx evaluation board to SRS
- Difficulties:
  - SFP ethernet
  - use SRS gigabit ethernet modules (gbt_top + submodules)
  - design new adapter board



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SRS: common code used

- gbt_top: handling of ethernet frames in SRS,
  - dataout bit wise
- Evaluation board used sgmii ethernet
  - dataout byte wise

→ Merge timepix control modules with SRS gbt

- Future: Want to use DDR2 RAM in SRS
  - use memory interface generator (mig)
  - need a data handler: Timepix control ↔ DDR2 DAM

  Any experience ??? Hints and code is welcome!

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Status of SRS + Timepix

System fully operational for 1-8 chips

- Data readout rate at theoretical maximum (up to 3 chips)

- Software extended to do
  - threshold equalisation
  - calibration with external test pulses
  - fast data taking: triggered, untriggered

- Missing:
  - DAC for test pulses generated by multiplexer,
    ADC for Timepix analog DAC_out scan (hardware not implemented)
  - DDR2 RAM on SRS (FPGA code not written)

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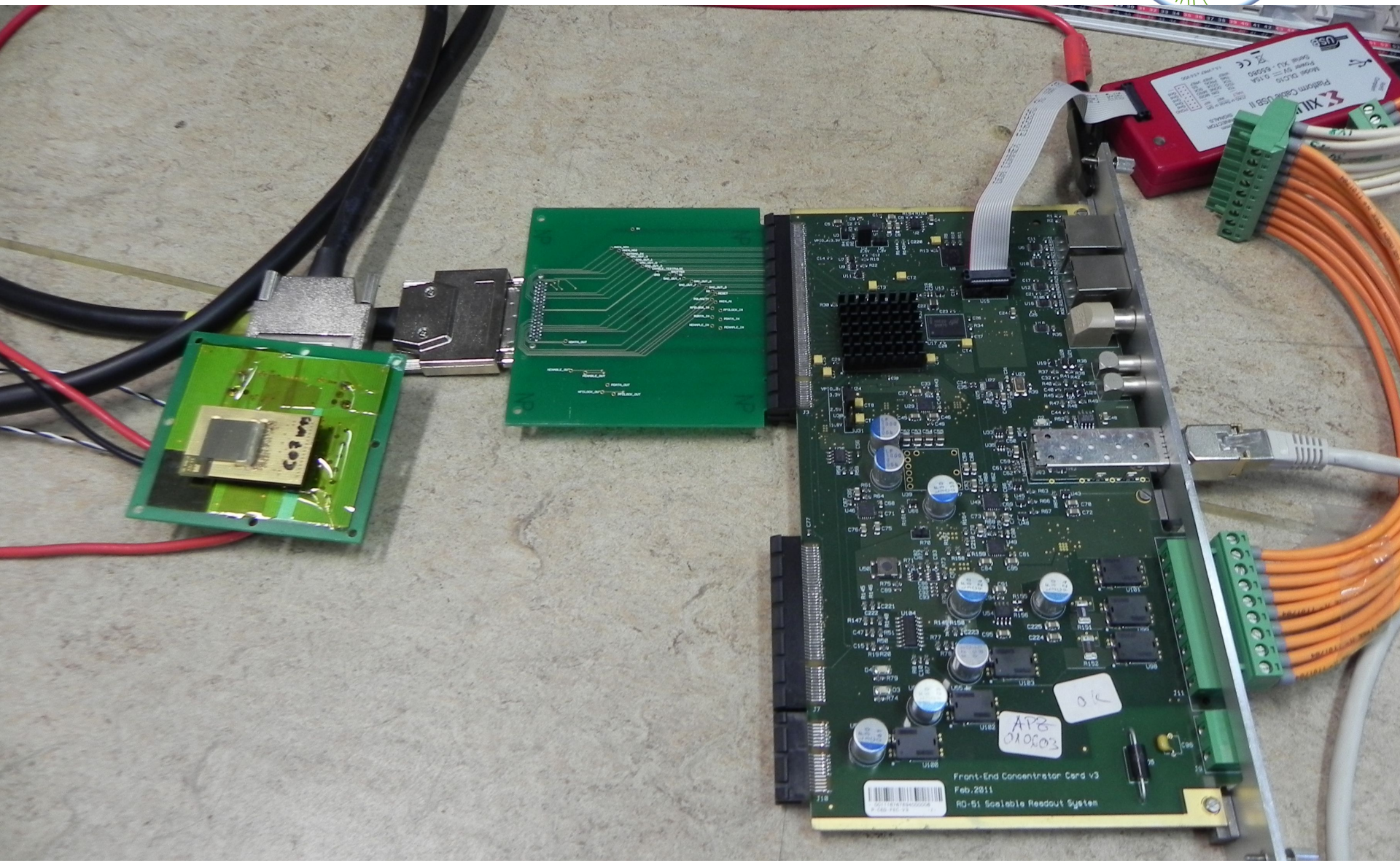
Status of SRS + Timepix



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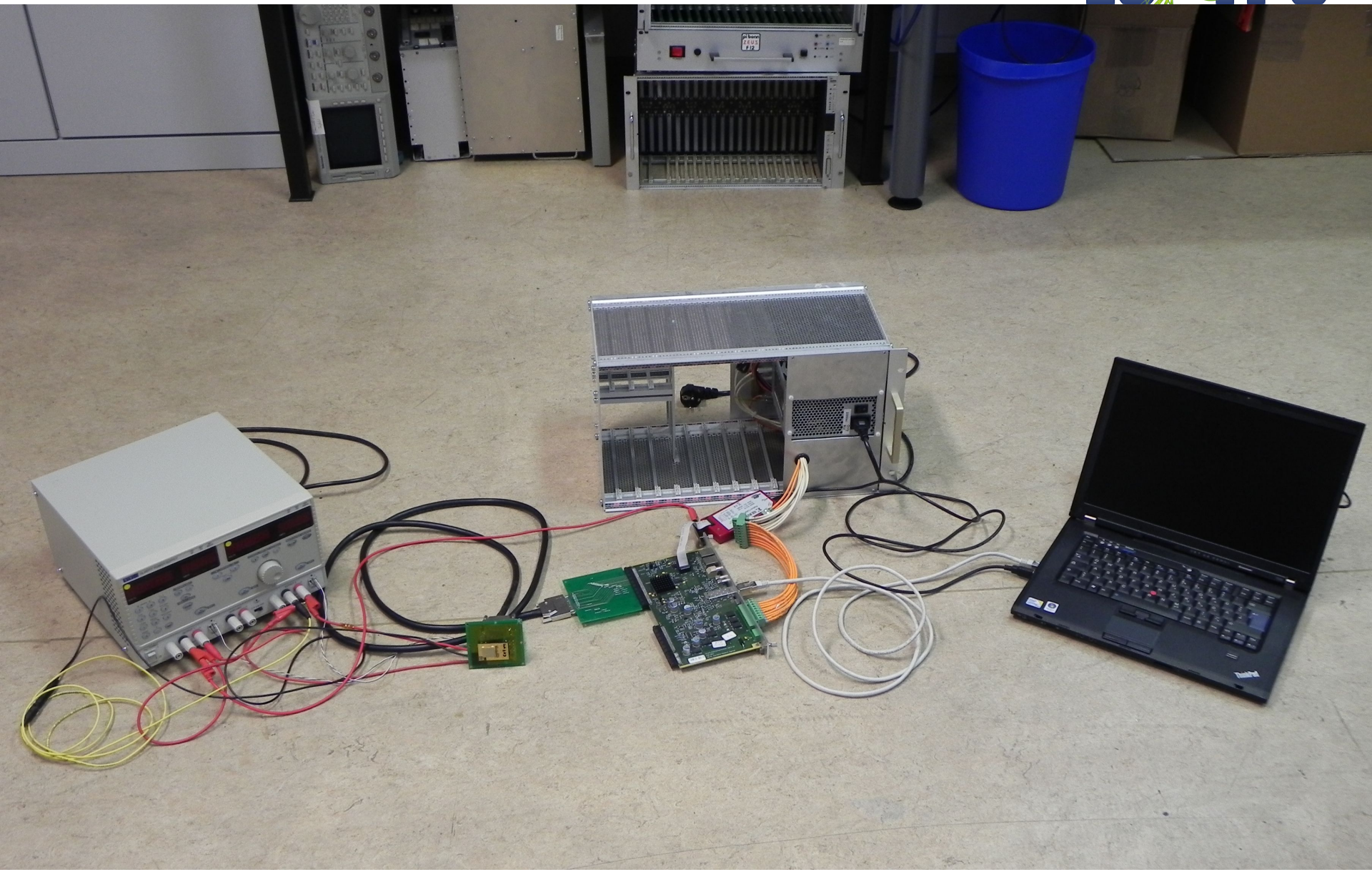

Status of SRS + Timepix

System was used in a two weeks testbeam at DESY in March/April

→ excellent performance, expectations were more than met!

- Data recorded with 2,5 Hz, not zero suppressed
- Two LCTPC modules (GEM and InGrid)
- Few runs interrupted by failure of SRS system
  (bugs in Code?, UDP, receiver time out)

- ATX power supply could not stand stray field of 1T magnet
  - crate was placed at position with ~ 0,1 – 0,3 T
  - ATX died during magnet ramp up

  → ATX + crate placed further away → longer power cables (~3m)
  - FEC stayed next to magnet

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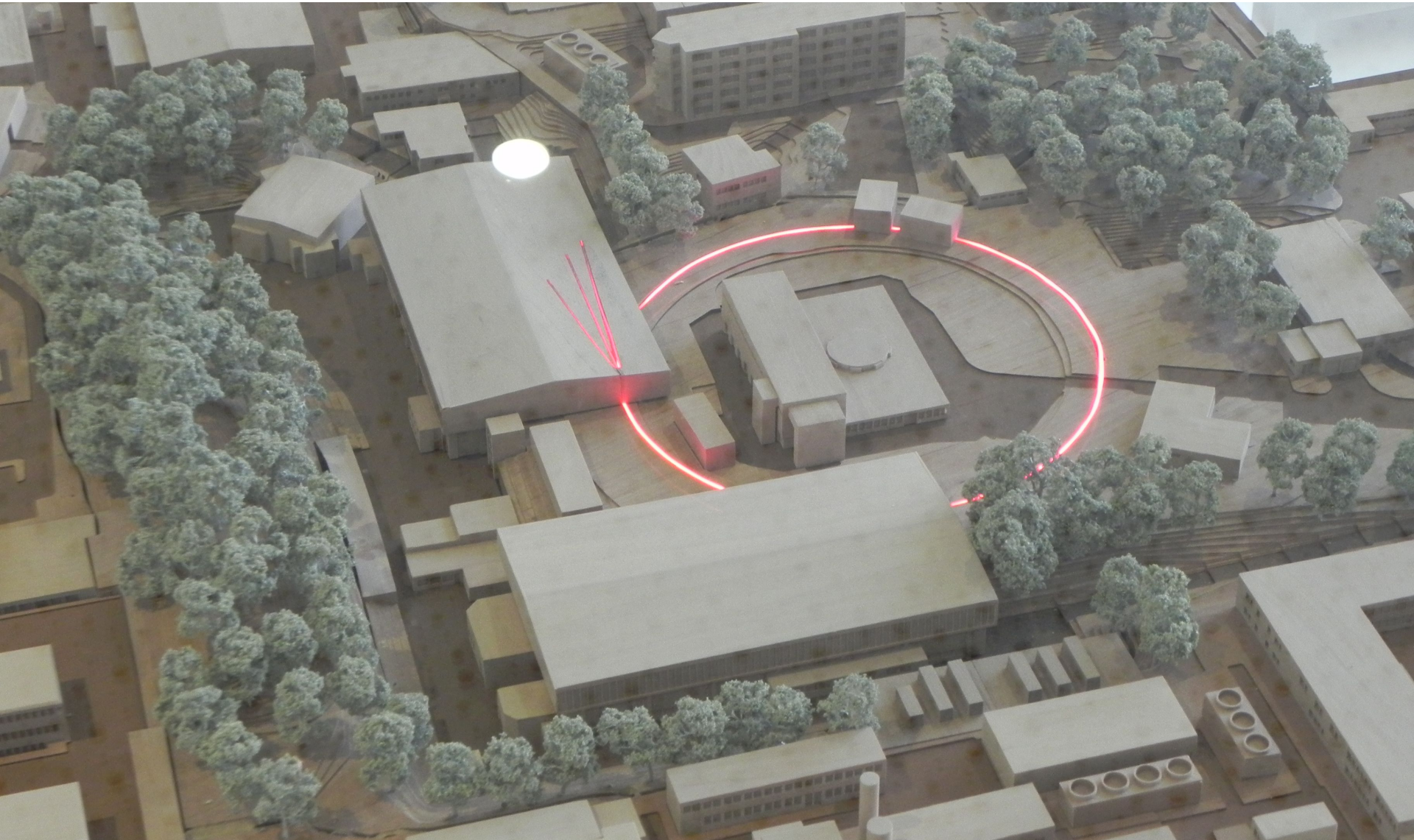
SRS + Timepix @ test beam



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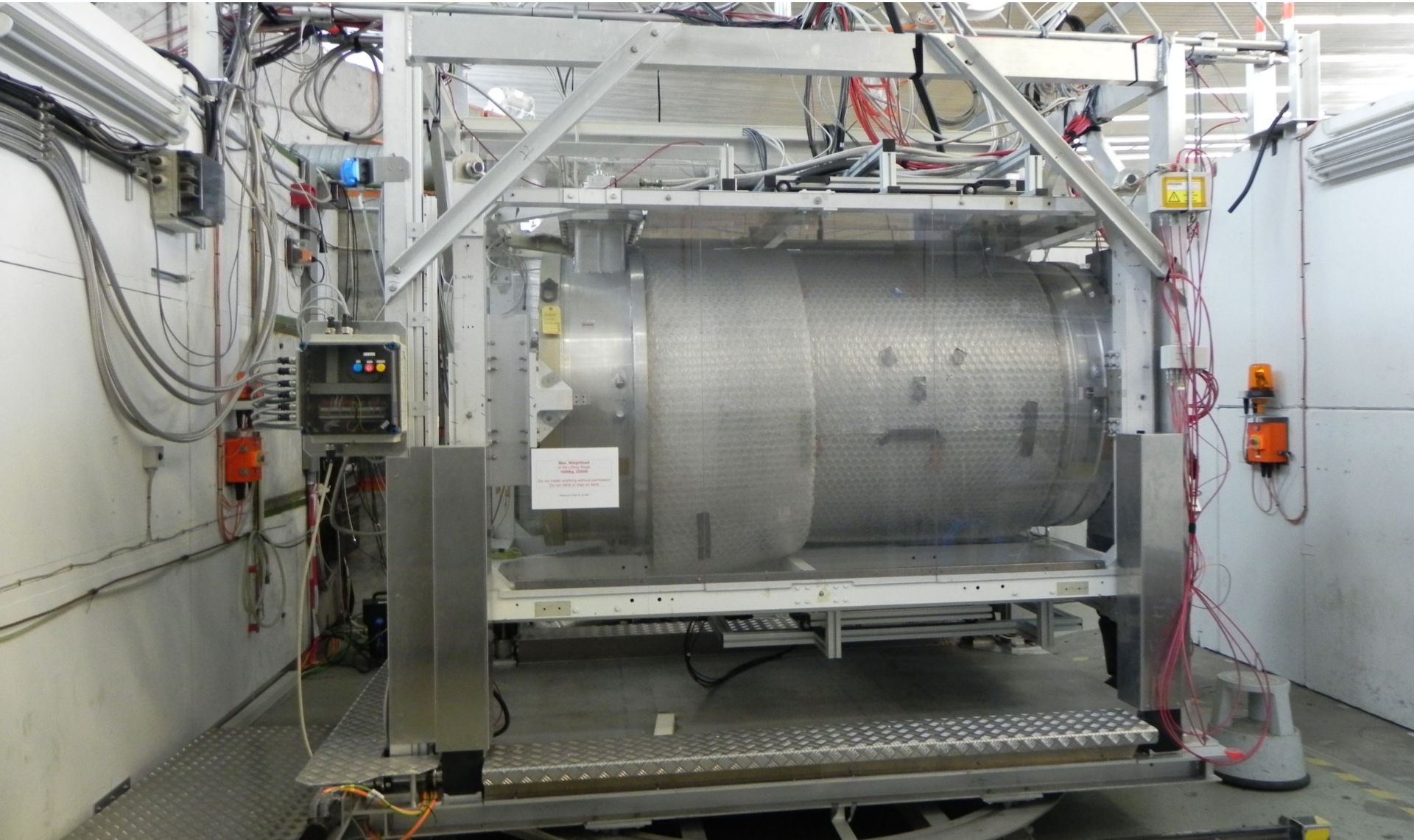

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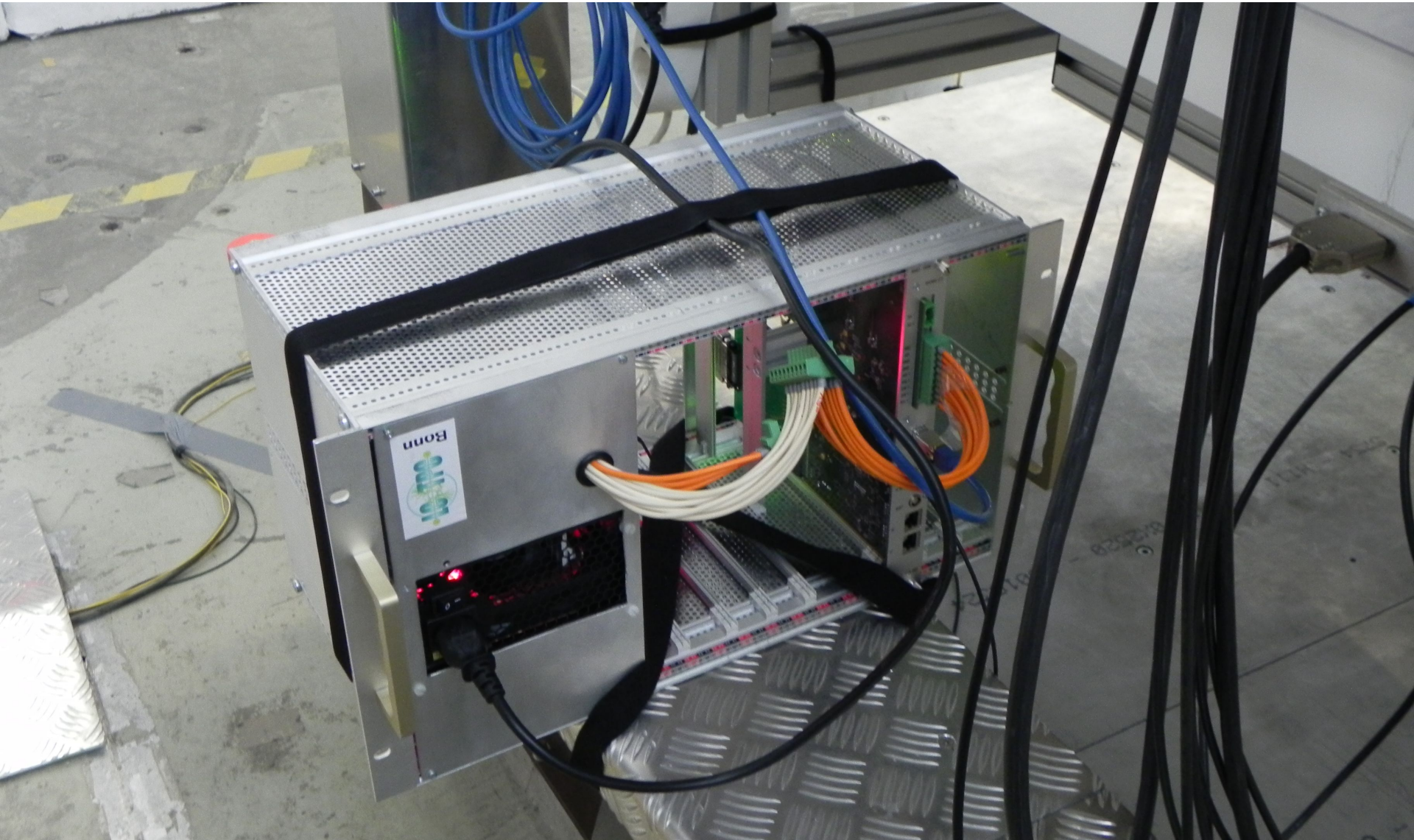

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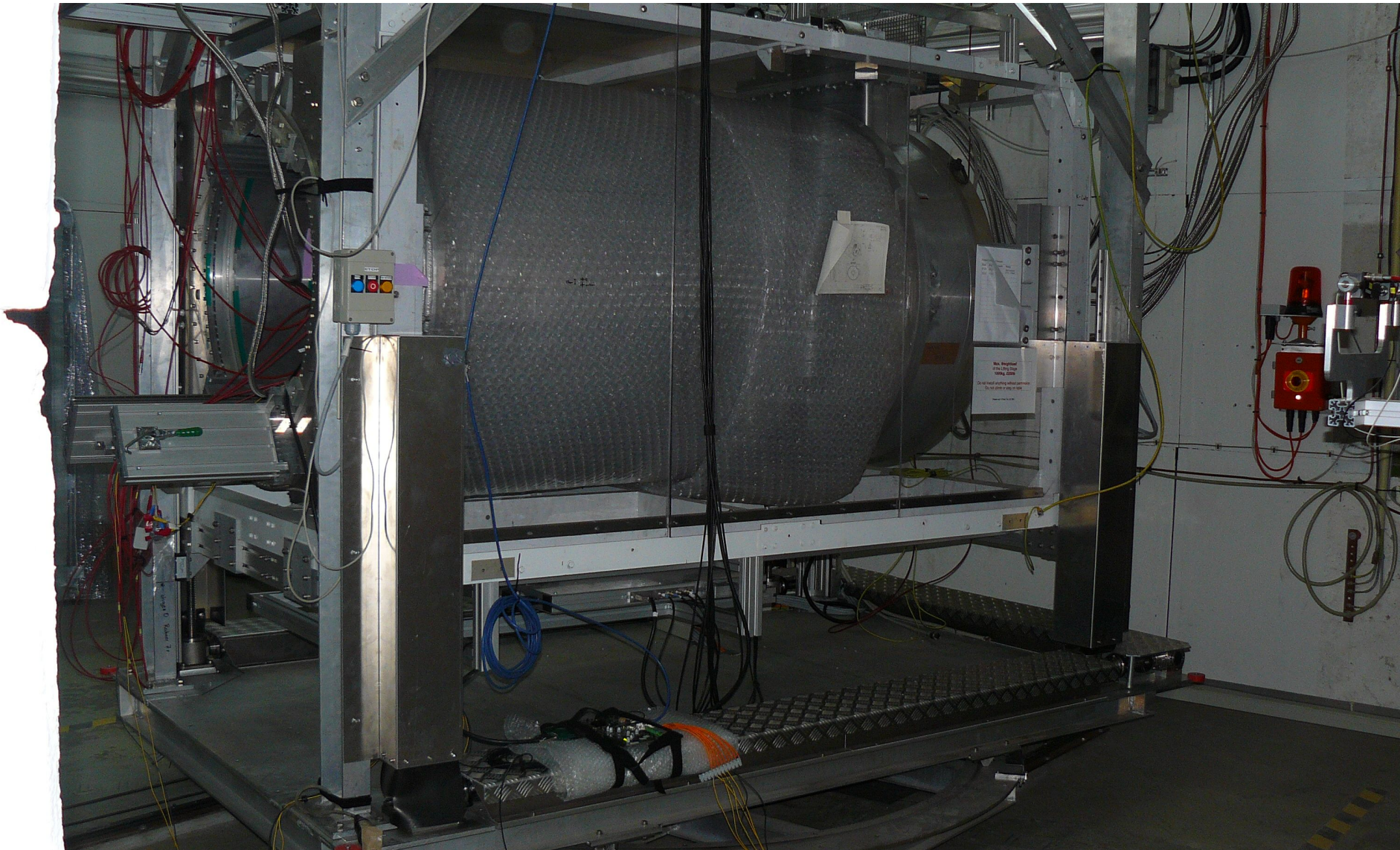

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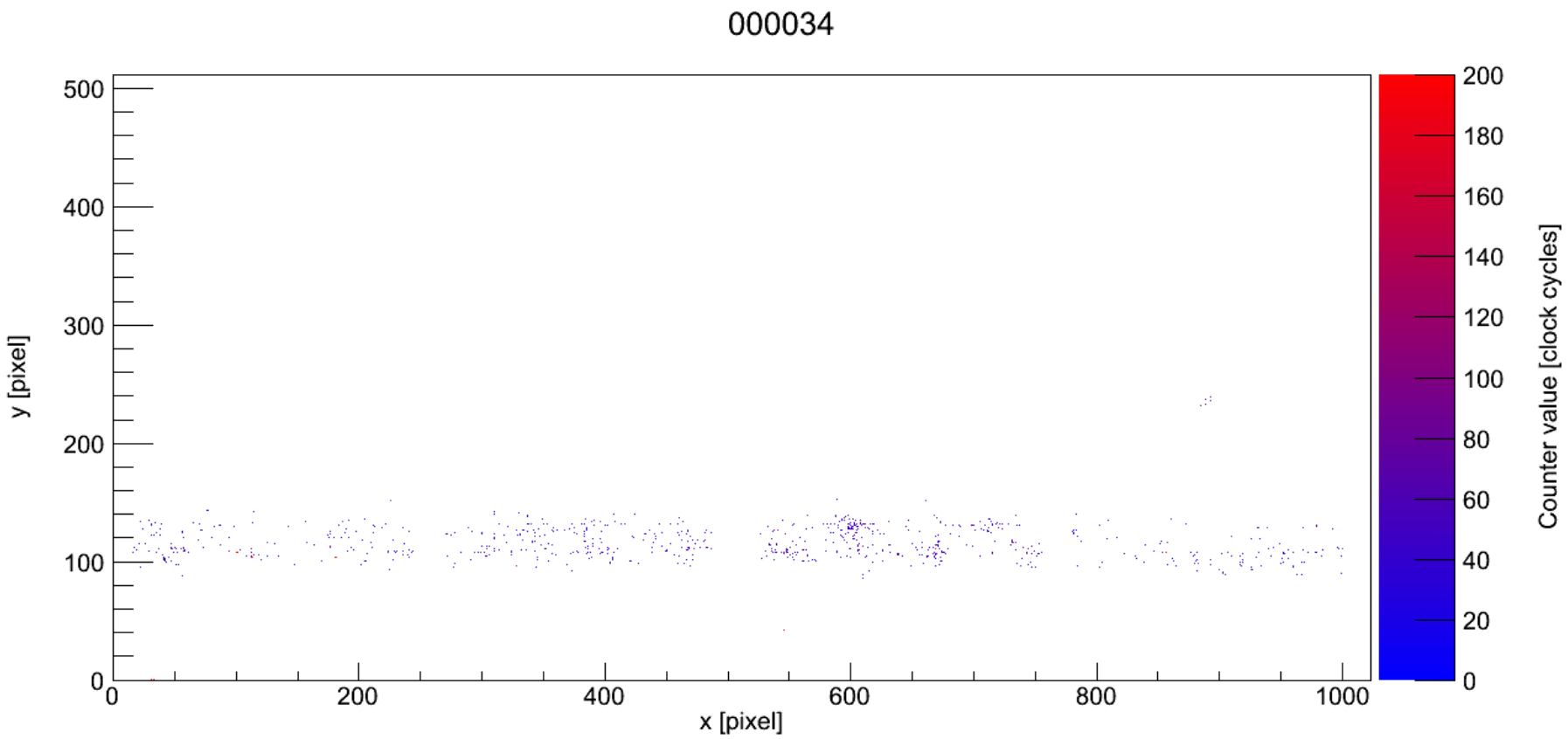

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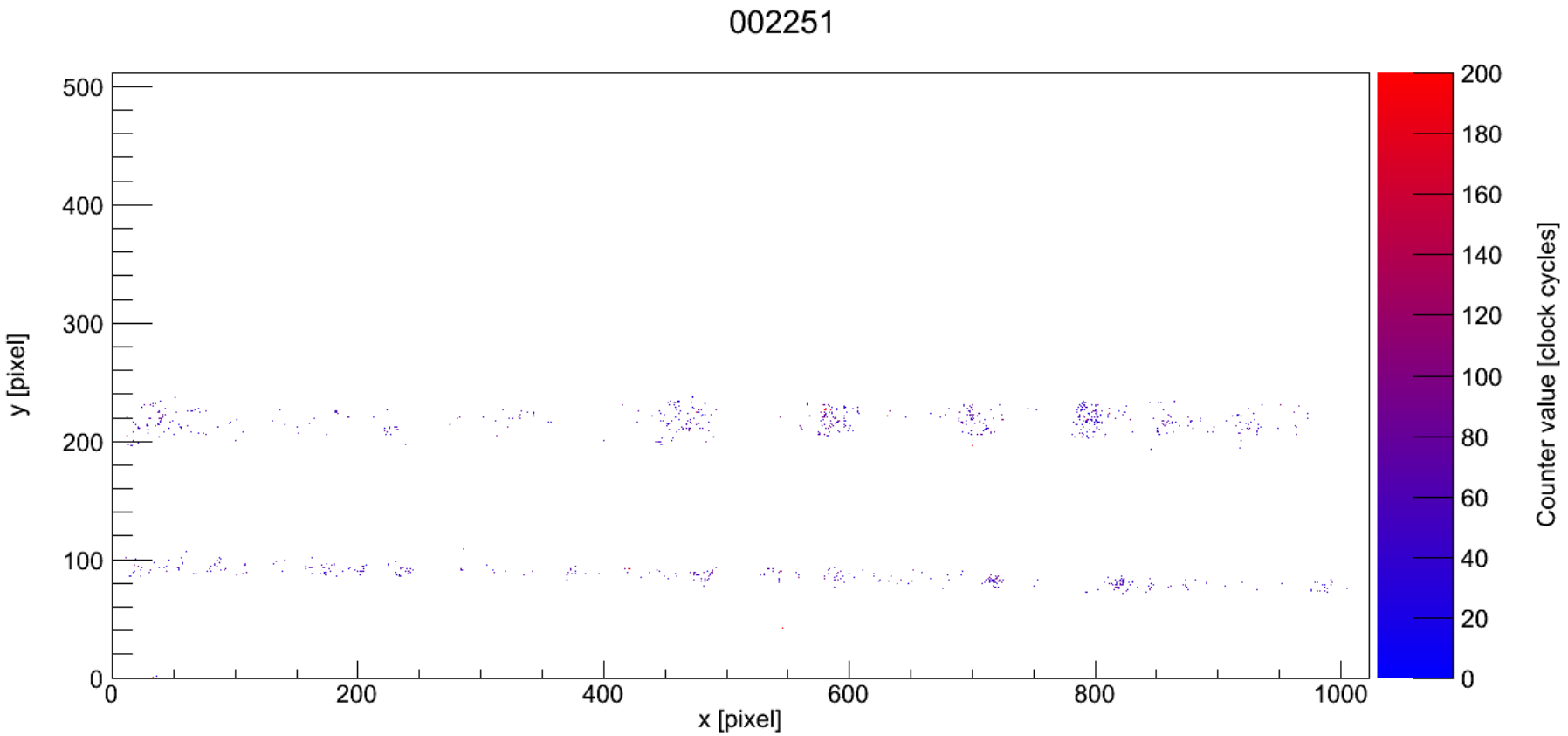

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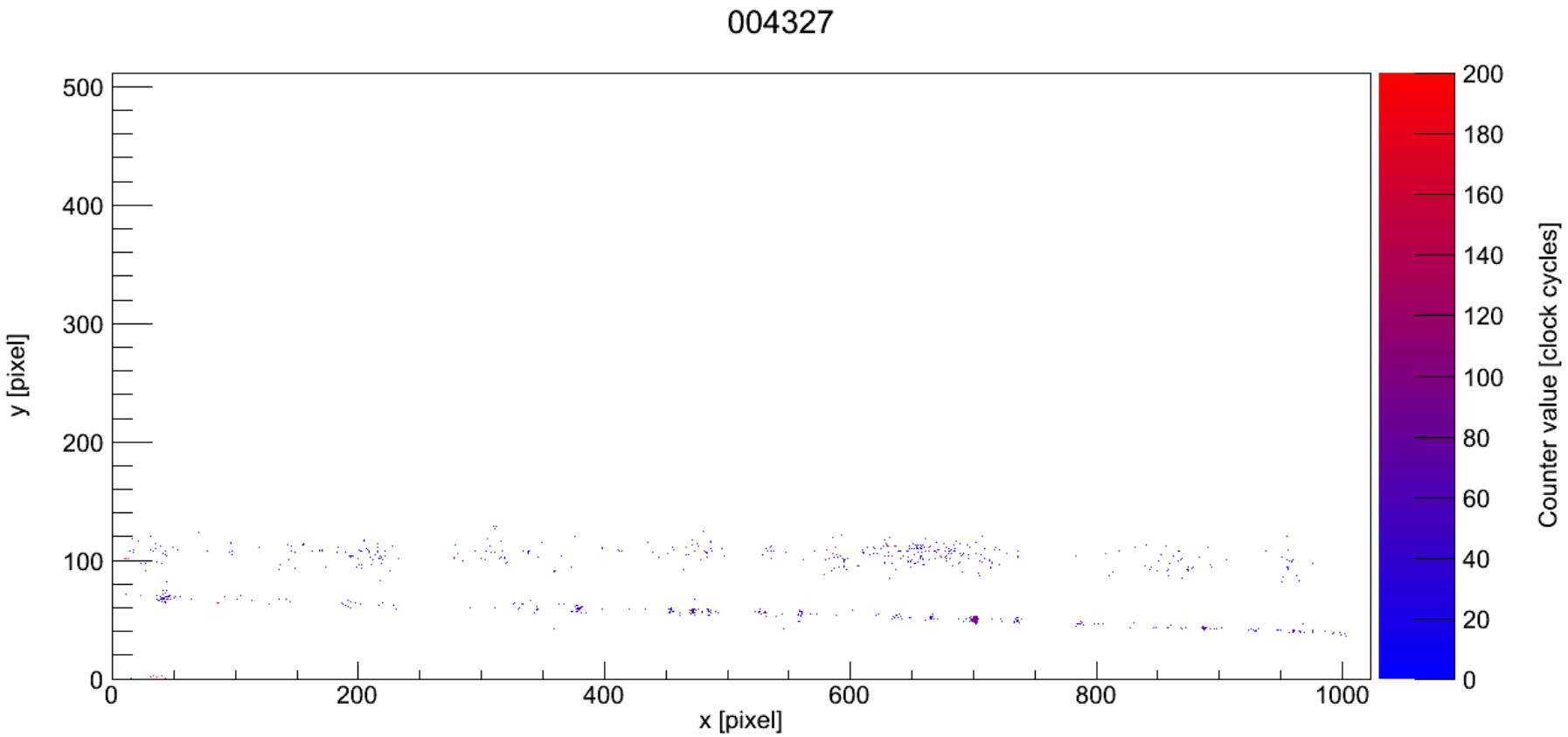

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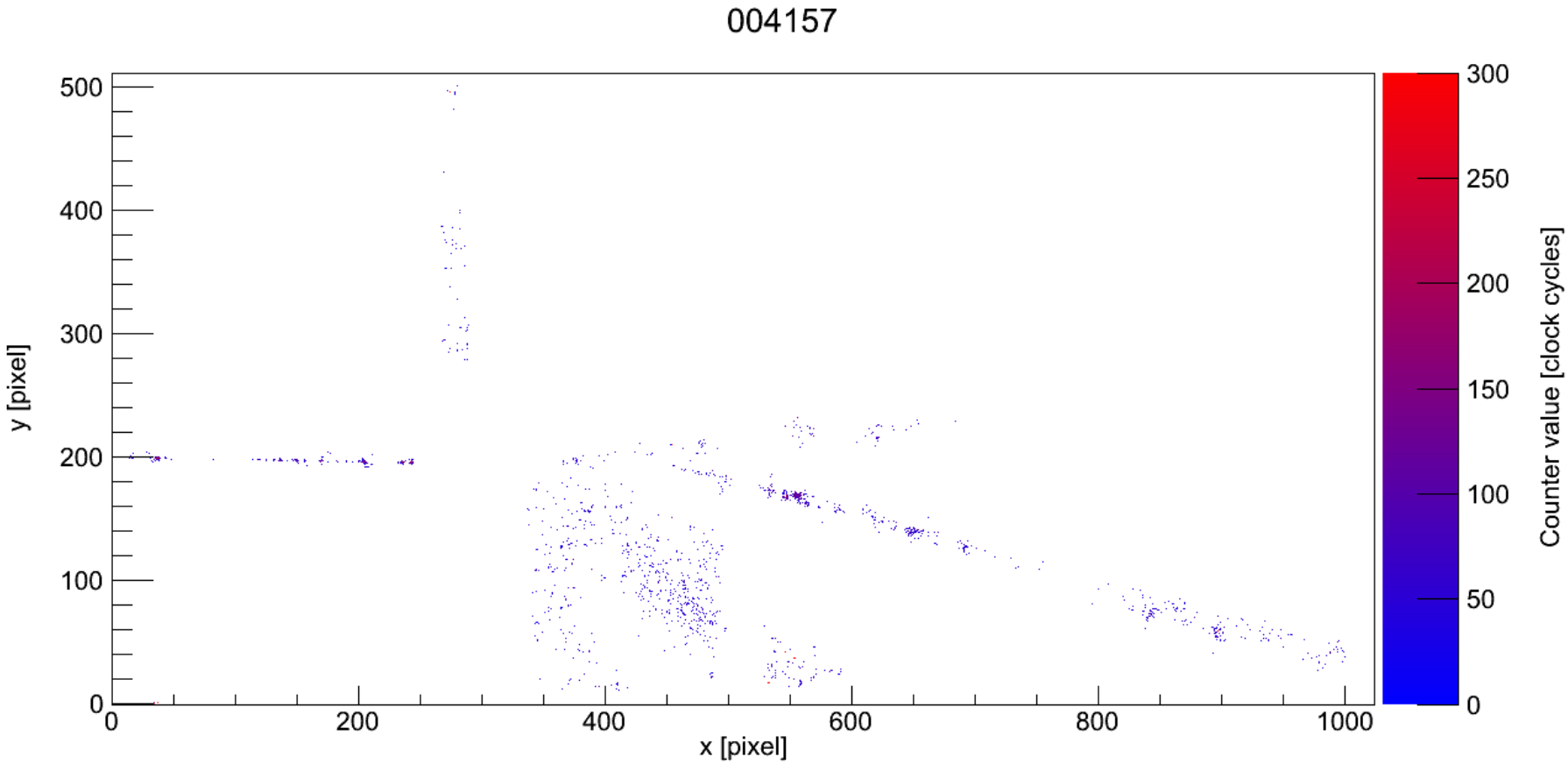

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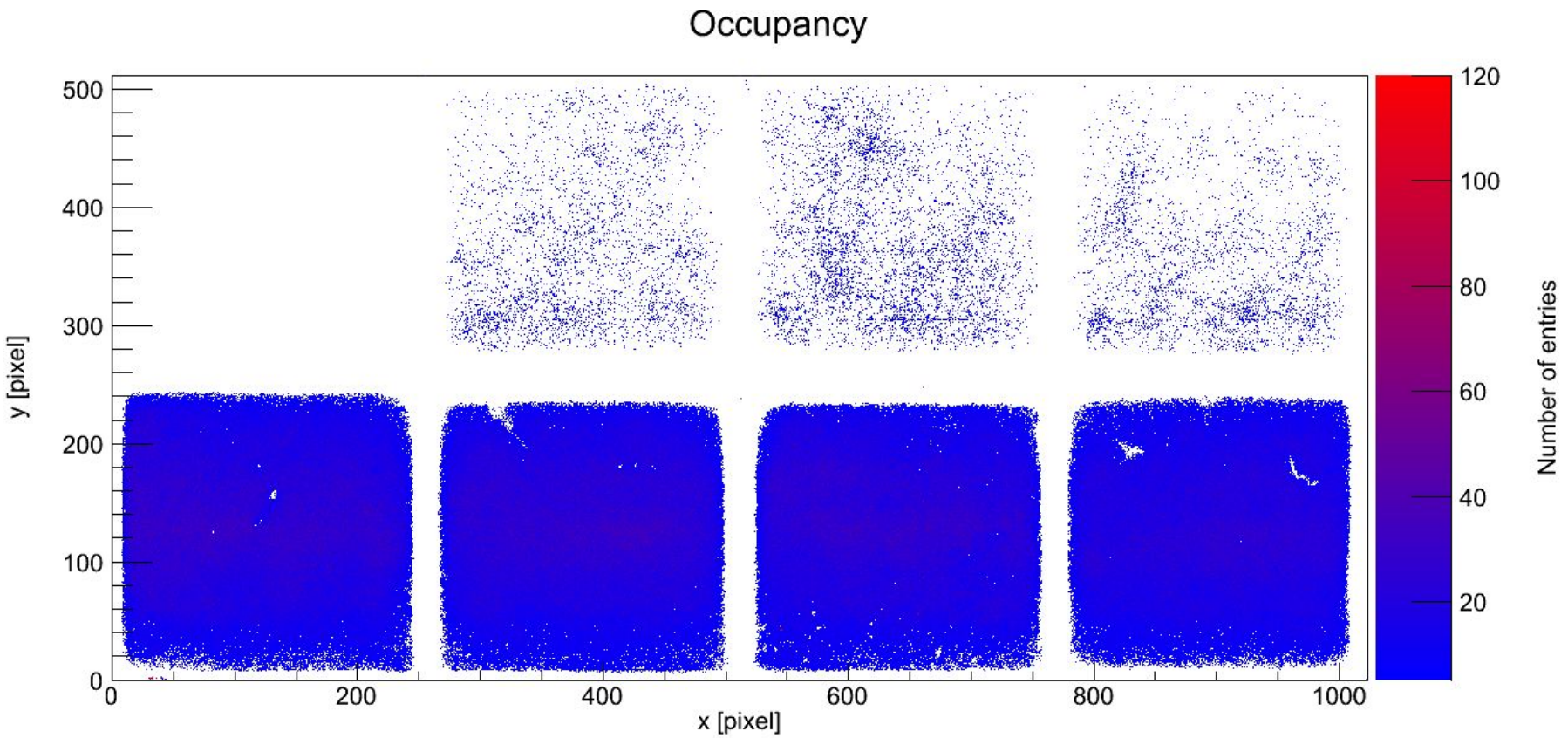

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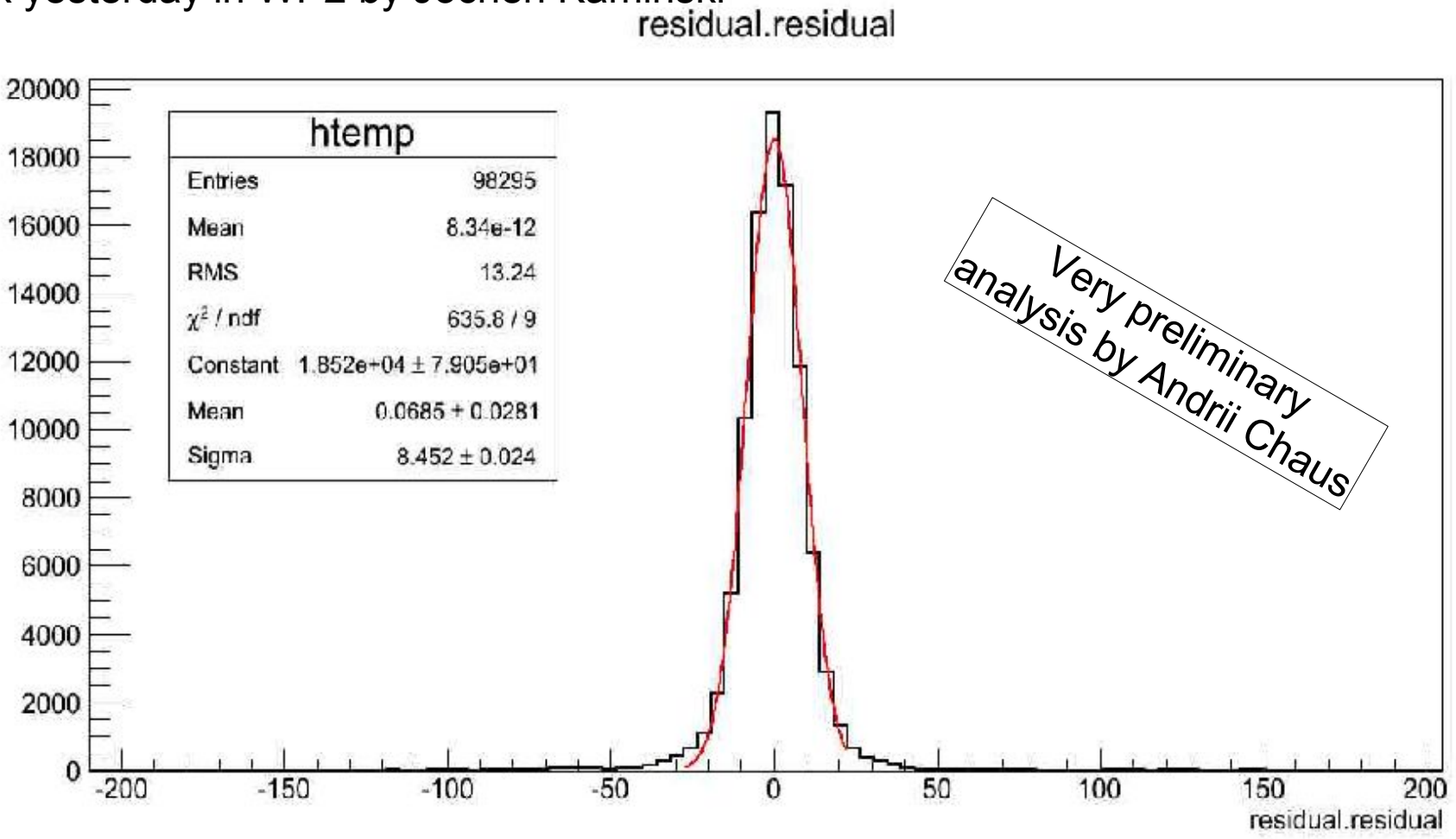
SRS + Timepix @ test beam

Some physics results and detector development:
talk yesterday in WP2 by Jochen Kaminski



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Summary

Status of SRS + Timepix:

- System is ready for use
  - read out boards with 1-8 Timepix chips
  - threshold equalisation and calibration with external pulses possible
  - data taking was confirmed in a test beam (~ 2 mio. frames recorded)

- Modified FPGA code used for small scale systems on Xilinx Boards
  - Uni Siegen (Timepix + GEM): R&D
  - CAST (InGrid): Dark matter search

- Development on FPGA code and hardware (FEC adapter + chip carrier)
  - HDMI cables
  - DACs and ADC on FEC adapter, I2C communication
  - support would be appreciated for DDR2 implementation

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Motivation

Advanced European Infrastructures for Detectors at Accelerators
- 4 year EU FP 7 Research Infrastructures program project
- Started February 2011
- > 80 institutes from 23 European countries
- Budget: 27 million € (8 million € from the EU)
- Coordinated by CERN

Subtask 9.2.3 (Bonn, CEA, Mainz, NIKHEF):
Common readout systems for gaseous detectors. Auxiliary electronics for the read-out of pixellated front-end chips, aimed at highly granular pixel read-out of gas detectors, are to be developed.

→ New readout system for pixellated chip (Timepix chip)
→ Cover large area for TPC/inner tracker application

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