

SRS DIGITAL C-CARD. TEST AND APPLICATIONS

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Outline

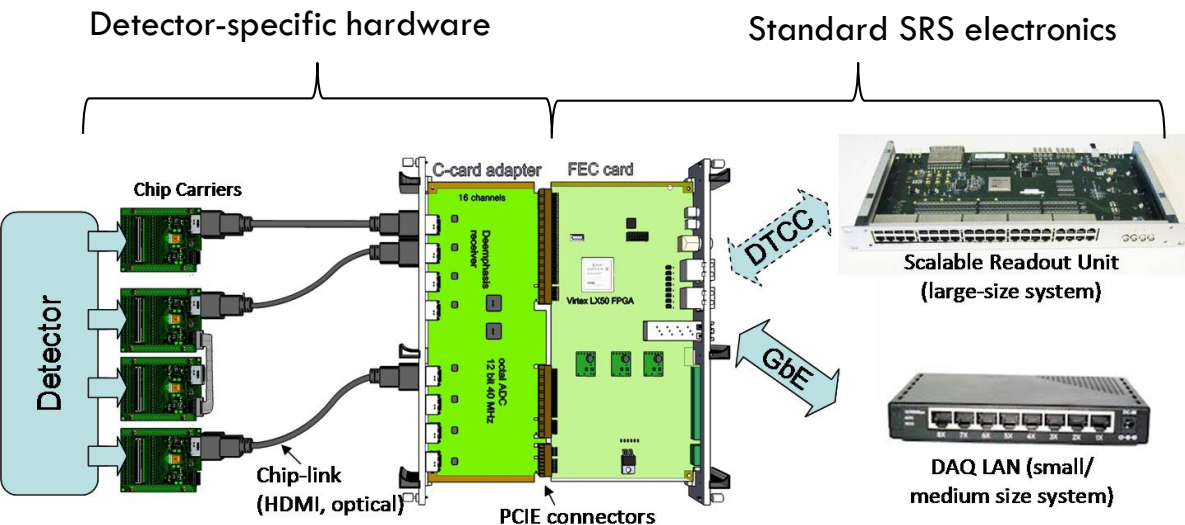
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- Introduction
- Assembly
- Tests

Introduction

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- Digital adapter card would allow easy connection to the VFAT2 and Beetle chips
- It plugs into the Front-End Card
- Can be used as generic digital acquisition card, with up to 40Gbps total bw (32 ports x 1.25 Gbps)
- Can be used as a FPGA-based TDC (up to 32 ports)

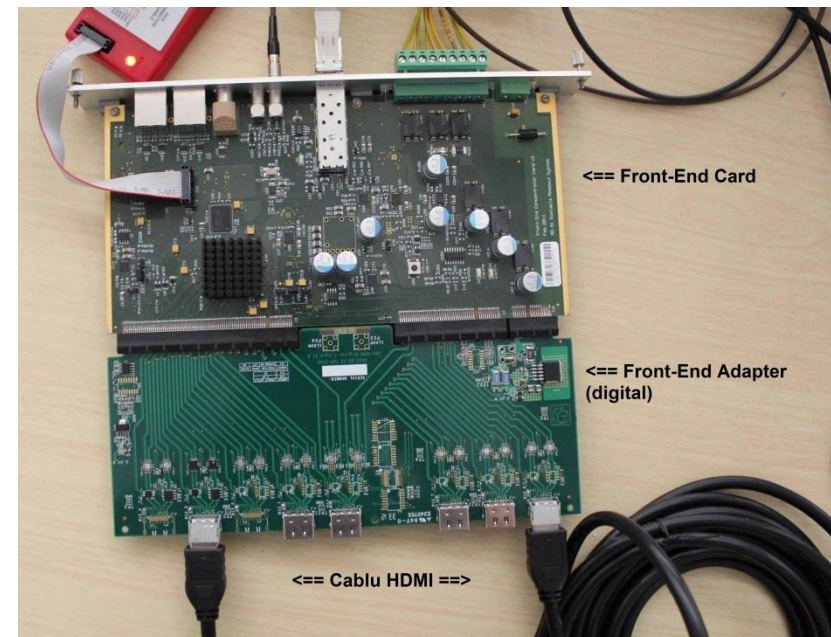


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Assembly

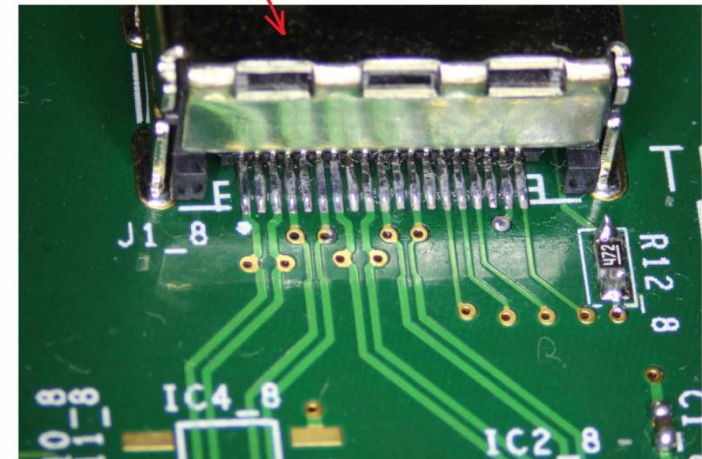
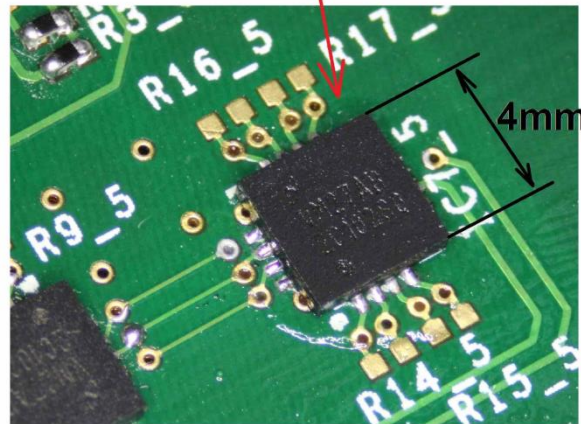
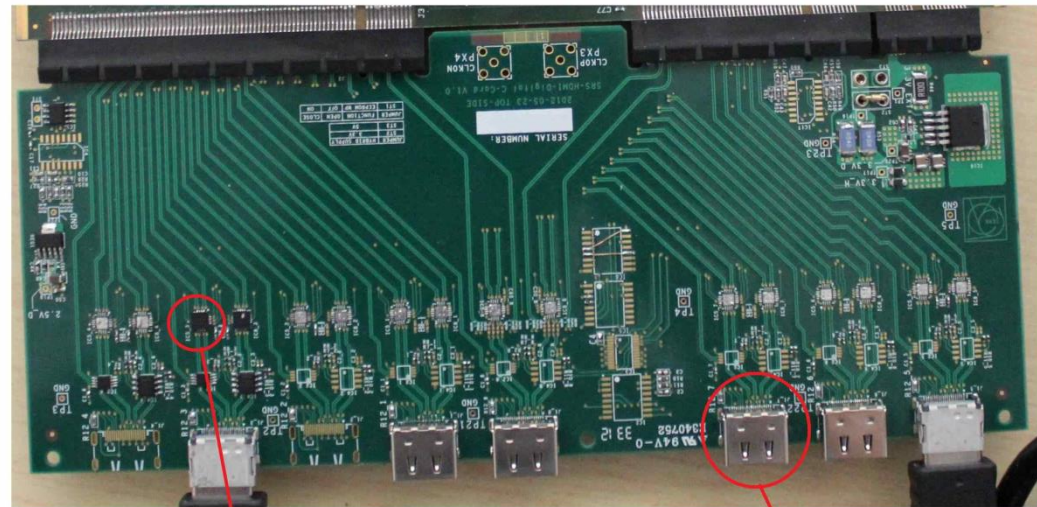
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- Digital card was ready but unassembled
 - ▣ Now partly assembled (such that a couple of links can be tested)
- Designed to be used with 40MHz chips
 - ▣ Used LVDS interface chips having data rates of the order of $\sim 1\text{Gbps}$
 - ▣ Can be used for much higher data rates
- Wrote some simple test firmware to check the data links



Assembly

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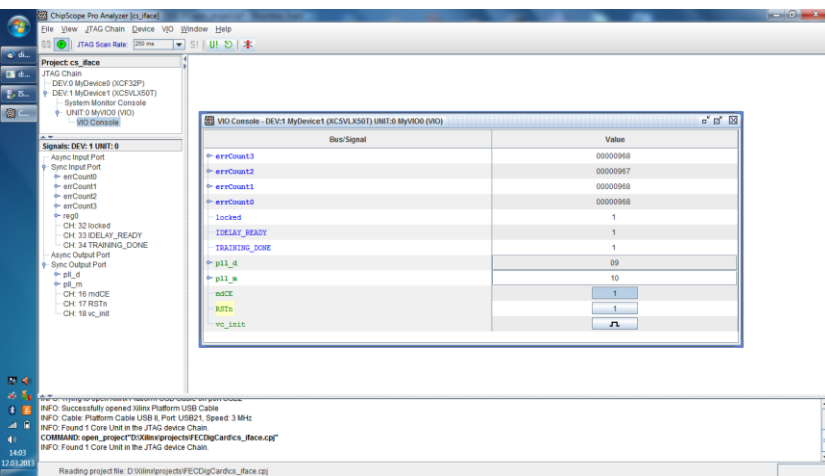
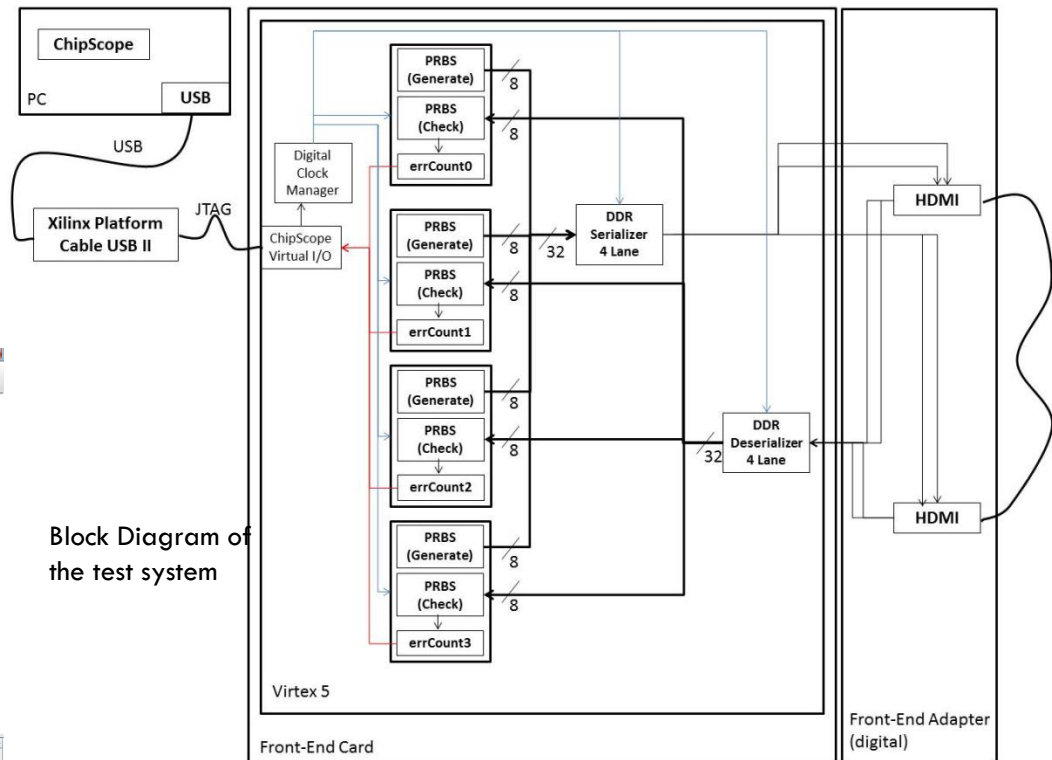


Package dimensions
made for some tricky
soldering

Testing

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- Stand-alone firmware for testing
 - Used ChipScope as an interface to the system
 - Looped the output of a PRBS generator through the cable to check the signal integrity
 - Used SERDESes to allow for high (DDR) transfer rates

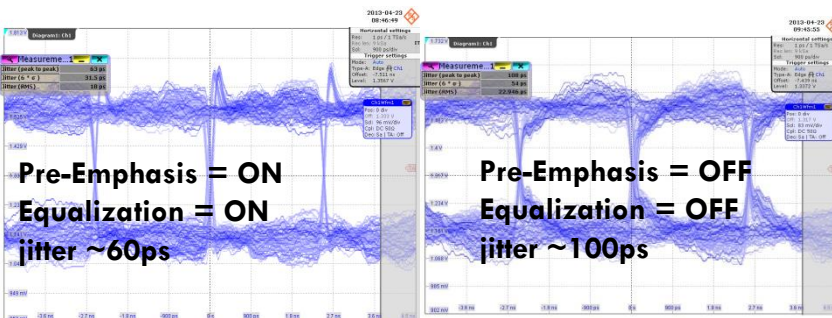
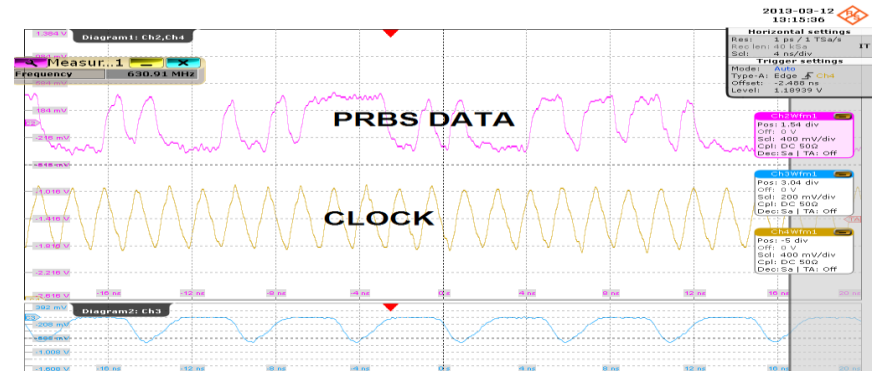
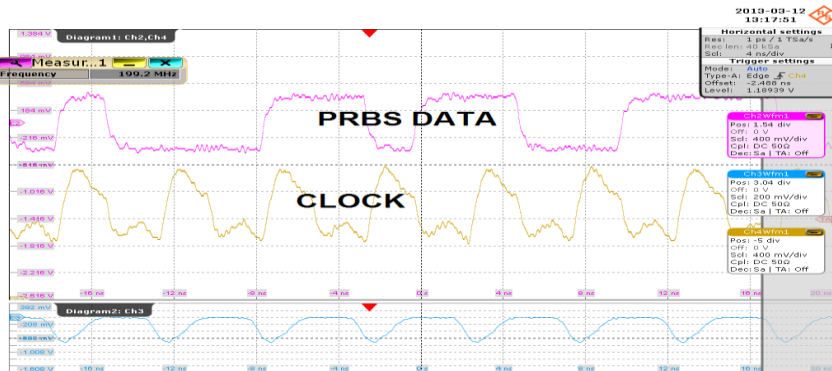


ChipScope UI

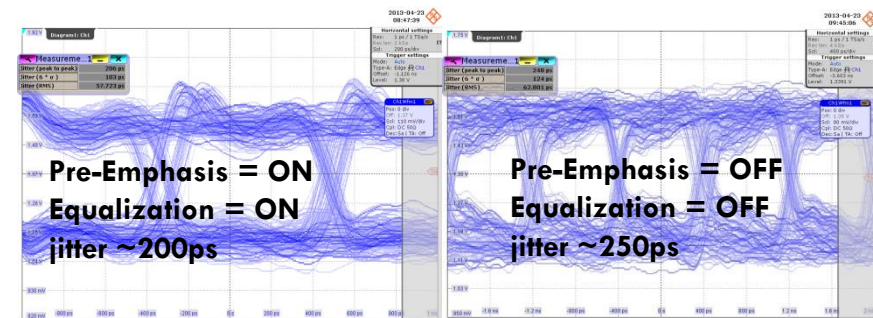
Testing

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- Using pseudorandom bit streams we've checked data integrity across the link. Plots below show the signal across one of the HDMI differential pairs. While the signal does get degraded at higher frequencies, it still can be heard.



Data transfer at 200MHz

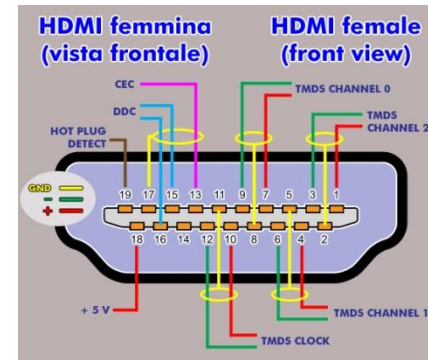
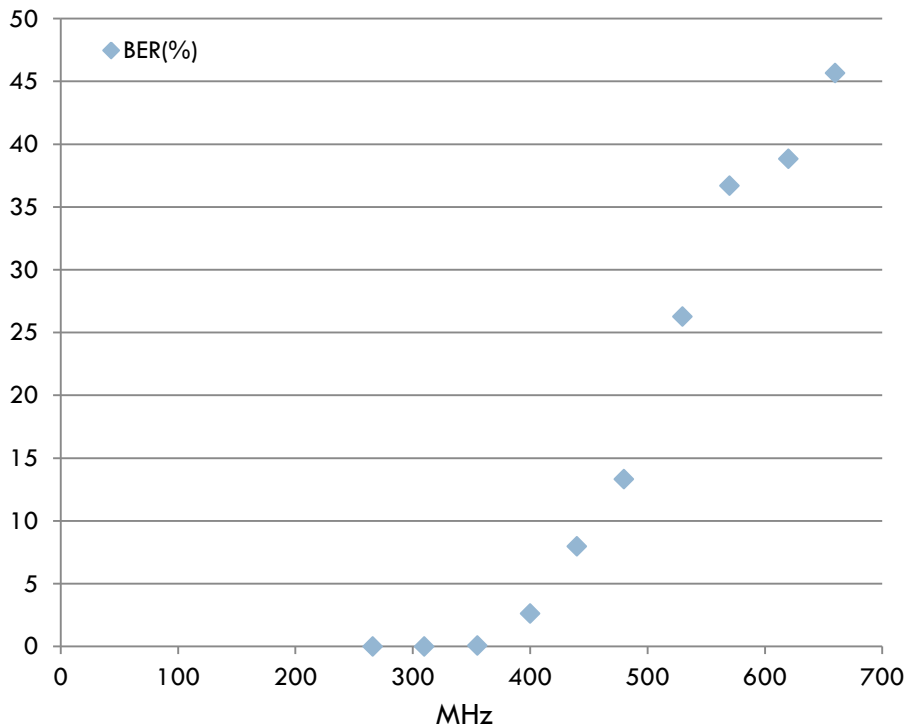


Data transfer at 630MHz

Testing

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- The 4 main links in the HDMI cable hold up nicely up to at least 700MHz (1.4Gbps DDR) providing a nearly error-free transmissions
- Using the additional channel (pins 14, 19, which in HDMI 1.4+ is used for the HDMI Ethernet Channel) in the cable transmission is possible up to ~350MHz (0.7Gbps DDR) due to the poor implementation of the pair in the HDMI 1.3 cable we're using.



Pin 14	Reserved (HDMI 1.0–1.3c), HEC Data– (Optional, HDMI 1.4+ with Ethernet)
Pin 15	SCL (I ² C Serial Clock for DDC)
Pin 16	SDA (I ² C Serial Data Line for DDC)
Pin 17	DDC/CEC/HEC Ground
Pin 18	+5 V (max 50 mA)
Pin 19	Hot Plug detect (all versions) and HEC Data+ (optional, HDMI 1.4+ with Ethernet)

Summary

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- A Front-End Adapter Card with digital interfaces has been partially populated such that functionality can be tested
- Wrote testing firmware for this card
- Made preliminary checks on possible transmission rates using a 5m HDMI cable
 - ▣ 1.4 Gbps per (proper) link
 - ▣ 700Mbps on the additional channel, need to retest this with an HDMI 1.4 cable

To do

- Integrate the tests (in a more configurable manner) into the SRS firmware architecture
- Continue measurements for different link pairs / transfer rates / cable lengths