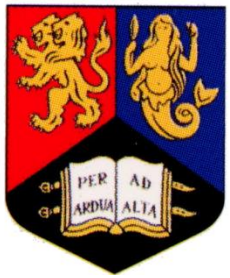


Alice CTP upgrade

Marián Krivda on behalf of the ALICE trigger group

The University of Birmingham

Triggering Discoveries in High Energy Physics

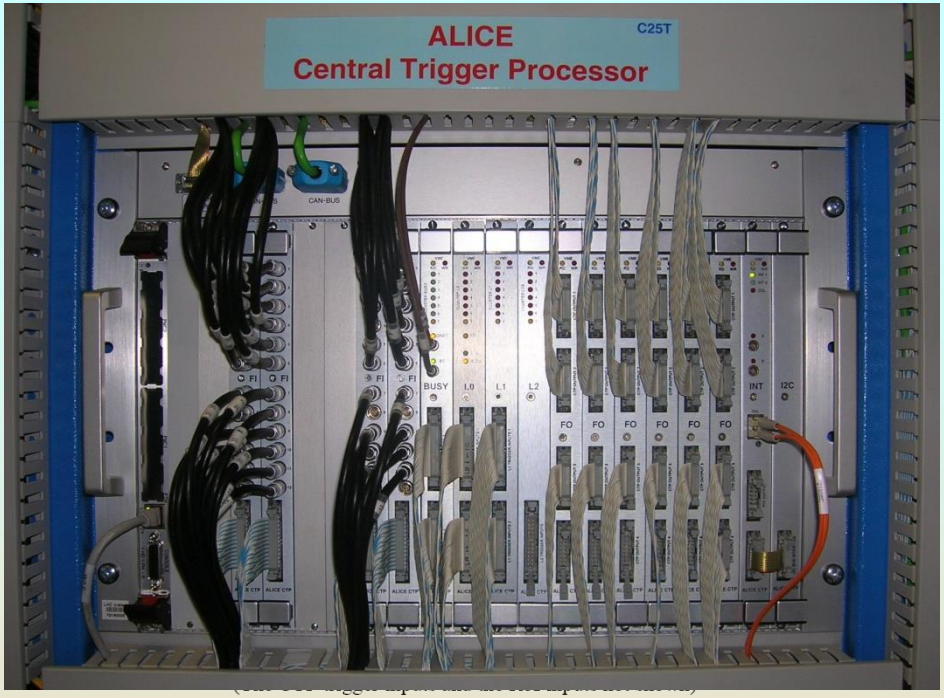
9-14 September 2013 , Jammu, India

Plan of talk

- Short overview of current CTP
- Upgrade requirements for Run 2 (2015-2017)
  - LM level
  - Extension of classes
  - Extension of clusters
  - Second link to DAQ
  - New L0 board
- Ideas for upgrade for Run3 (2019-2021)

Current Alice trigger system

- Central Trigger Processor (CTP):
  receives trigger detector inputs, makes decision
- Local Trigger Unit (LTU):
  interface between CTP and readout detectors
- Trigger and Time Control (TTC):
  transmits LHC clock and delivers trigger signals to detectors

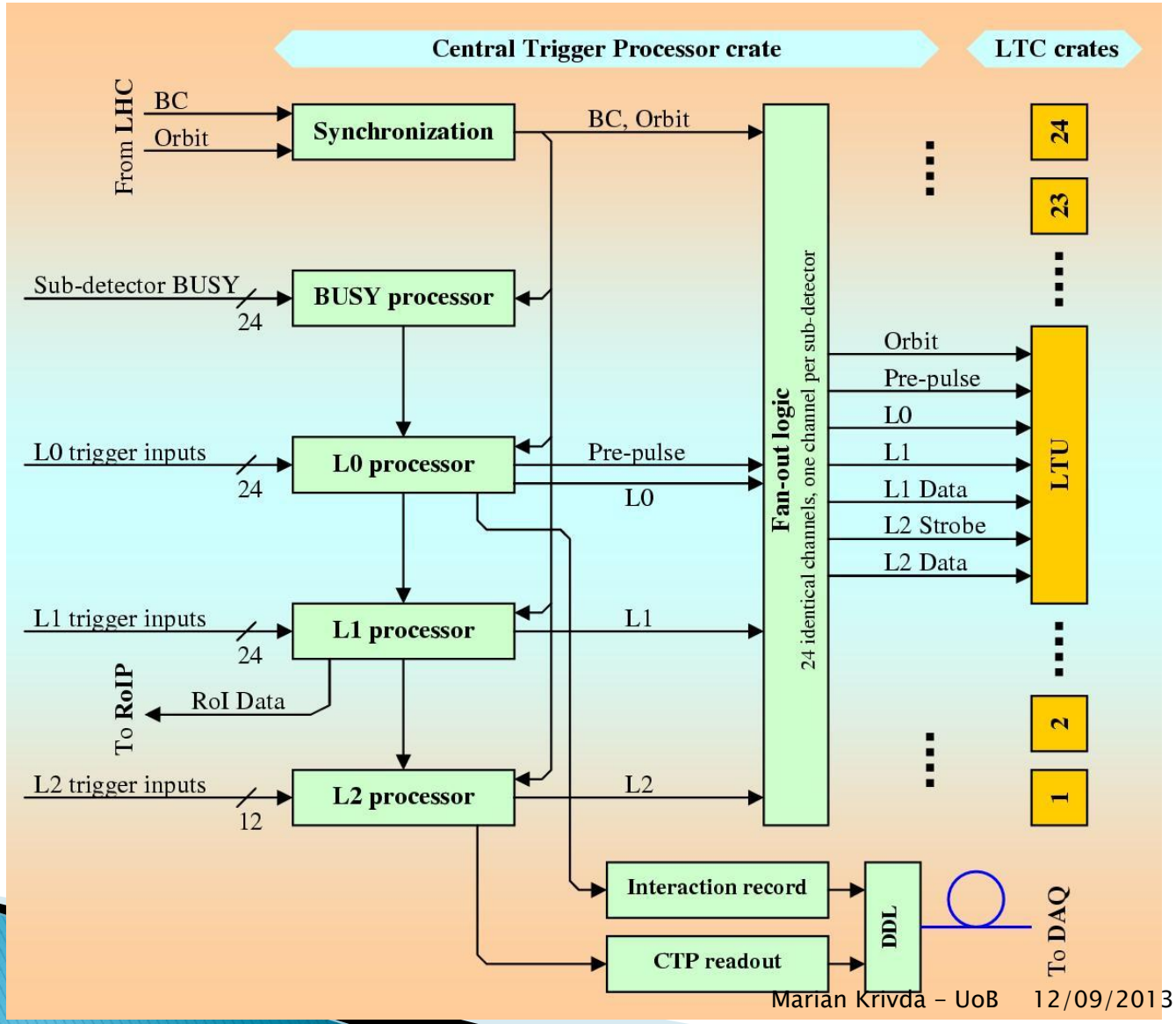


- Due to short time for L0 latency the CTP is in the experimental cavern
- 6U VME boards
  - L0, L1, L2 boards
  - BUSY board
  - FO boards
  - INT board
  - I2C board
- LVDS Trigger inputs
- Outputs are sent to Local Trigger Units (LTUs) where conversion to TTC format occurs

Current CTP

- 3 HW trigger levels:
  - **L0** inputs to CTP up to 800 ns, time for making decision 100 ns, time for delivery to detectors up to 300 ns, together is max. **1.2 μs** from interaction;
  - **L1** inputs to CTP up to 6.1 μs; time for making decision 100 ns, together is max. **6.5 μs** from interaction;
  - **L2** delivered to detectors **105 μs** from interaction.
- 60 trigger inputs
  - **L0** 24; **L1** 24; **L2** 12.
- Up to 24 detectors
- 6 independent partitions (*clusters*)
- 50 classes
- 4 past/future protection circuits
- Interaction record - a list of all the bunch-crossings in which the Interaction signal has been detected; also for past-future protection check and pattern recognition
- Rare event handling

CTP data flow



Requirements for Run 2

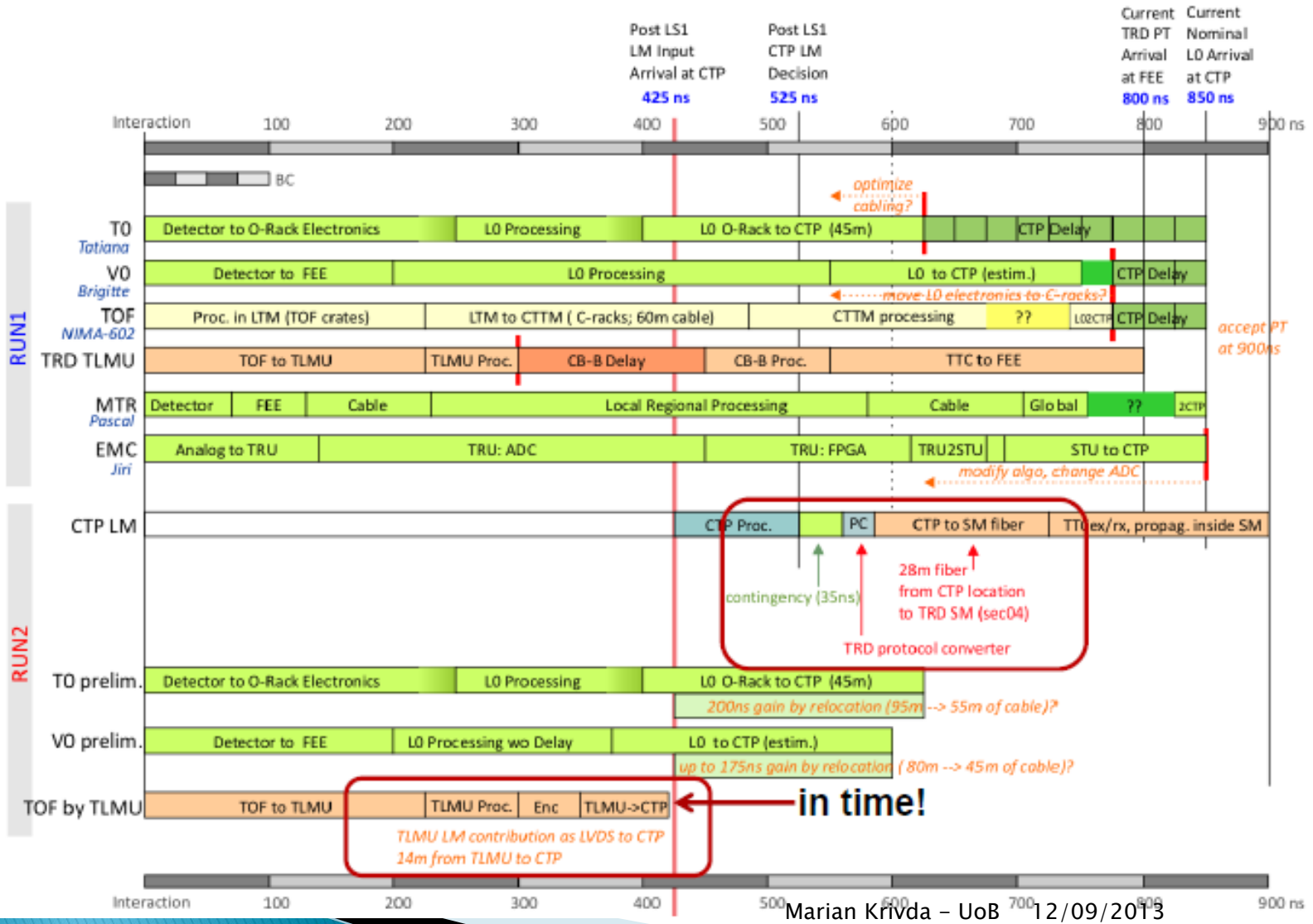
- New CTP level -> LM (instead of TRD pretrigger)
- 100 classes (instead 50)
- 8 physics clusters (instead 6)

LM trigger for TRD

New trigger level -> LM

- Currently TRD pre-trigger is generated even if CTP is busy i.e. TRD pre-trigger electronics doesn`t see CTP busy signal
- In order to reduce the level of "wasted" pre-triggers currently generated by TRD pre-trigger, the pre-trigger electronics will be replaced by a new level (LM) of trigger logic, run at the CTP, which will be used to generate a wake-up signal to the TRD
  - Needs new faster inputs from T0, and VZERO
  - Needs relocation of T0 and VZERO electronics closer to CTP -> in progress
  - Needs re-cabling of T0, VZERO and TRD trigger cables -> in progress
  - Needs new L0 board

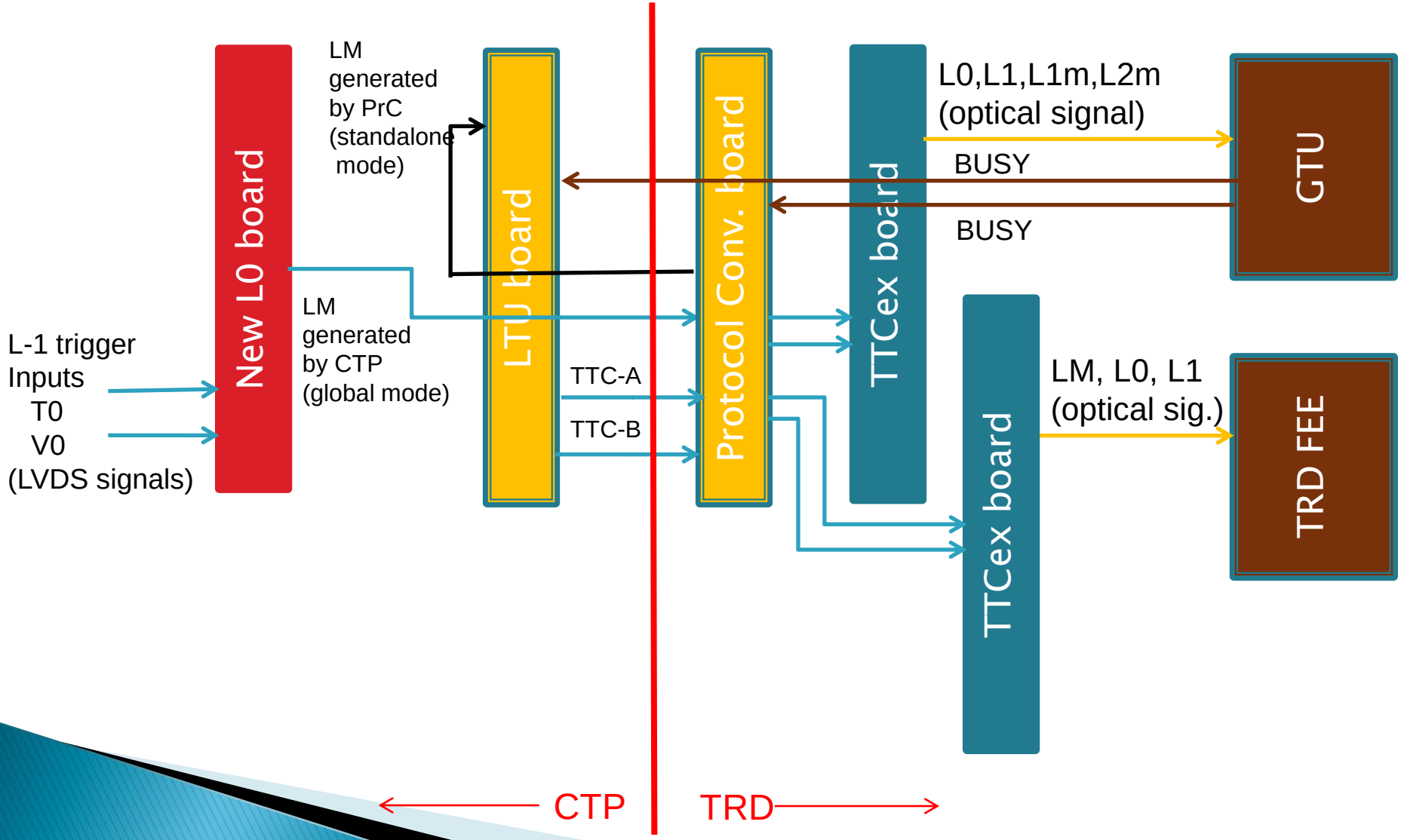
Preliminary timing for T0, V0 and TOF trigger inputs



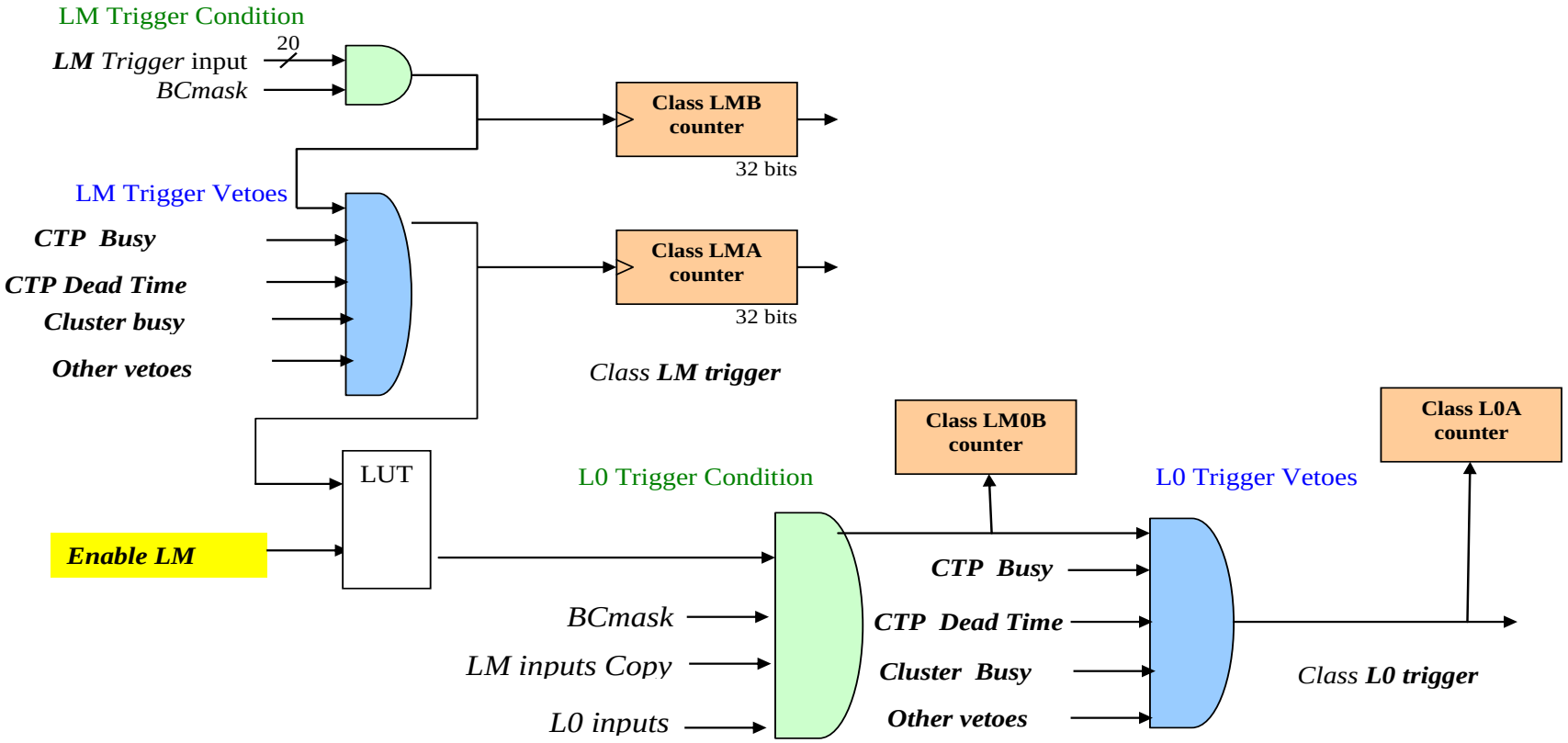
LM trigger for TRD

- Two trigger sequences for TRD
  - GTU receives standard TTC sequence (L0 – L1 – L2) from LTU -> TTCex
  - FEE receives custom trigger sequence (LM – L0 – L1) from CTP -> Protocol Converter -> TTCex
- Global\Standalone mode
  - In global mode CTP generates LM trigger which is sent to Protocol Converter (PC) board
  - In standalone mode PC board generates LM trigger which is sent to PULSER input on LTU board

LM trigger for TRD



LM trigger for TRD – FPGA logic



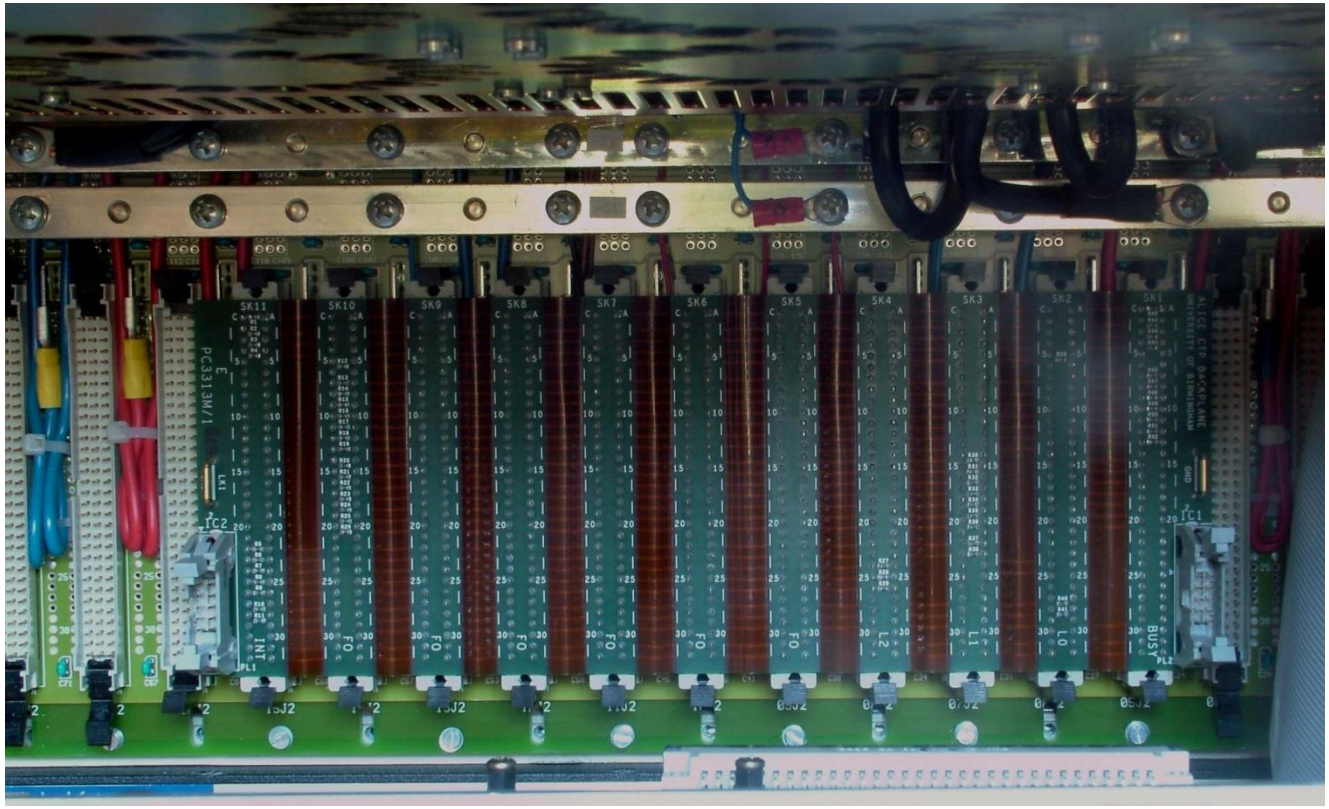
- Delayed copy of LM trigger input will be provided at L0 time

Extension of Classes

100 classes

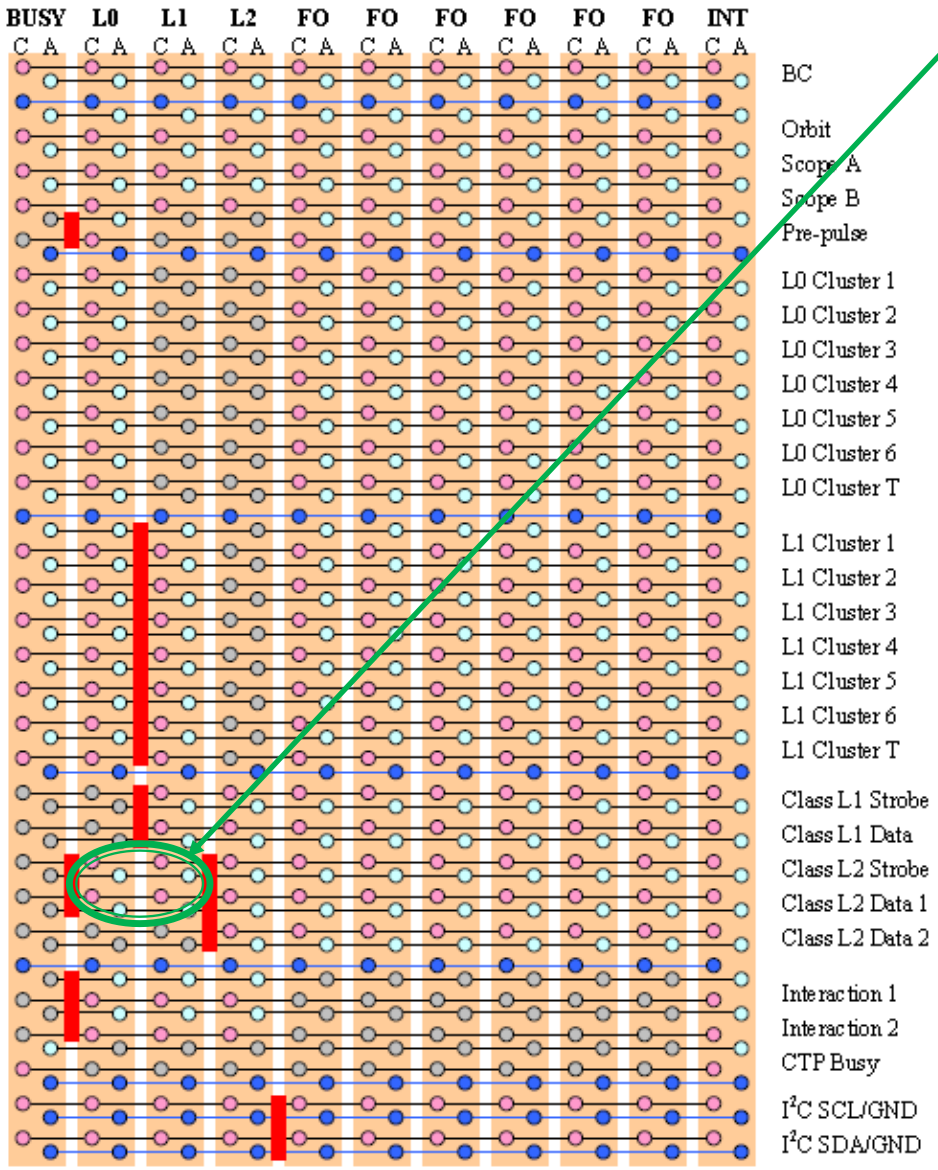
- Extension of the number of classes, each defined in the same way as at present
  - Simple to implement at CTP (just scaling)
  - Need to check space on L1, L2, FO boards (their FPGAs)
  - Simple to implement in offline
  - no restrictions on attributes e.g. bc masks
- Consequences:
  - Change of L2A message (50 bits longer)
  - Change of Common Data Header (CDH)

All connections between CTP boards are on CTP backplane



- Flex PCB with VME connectors
- User Defined (UD) pins on VME are used for connections

100 classes



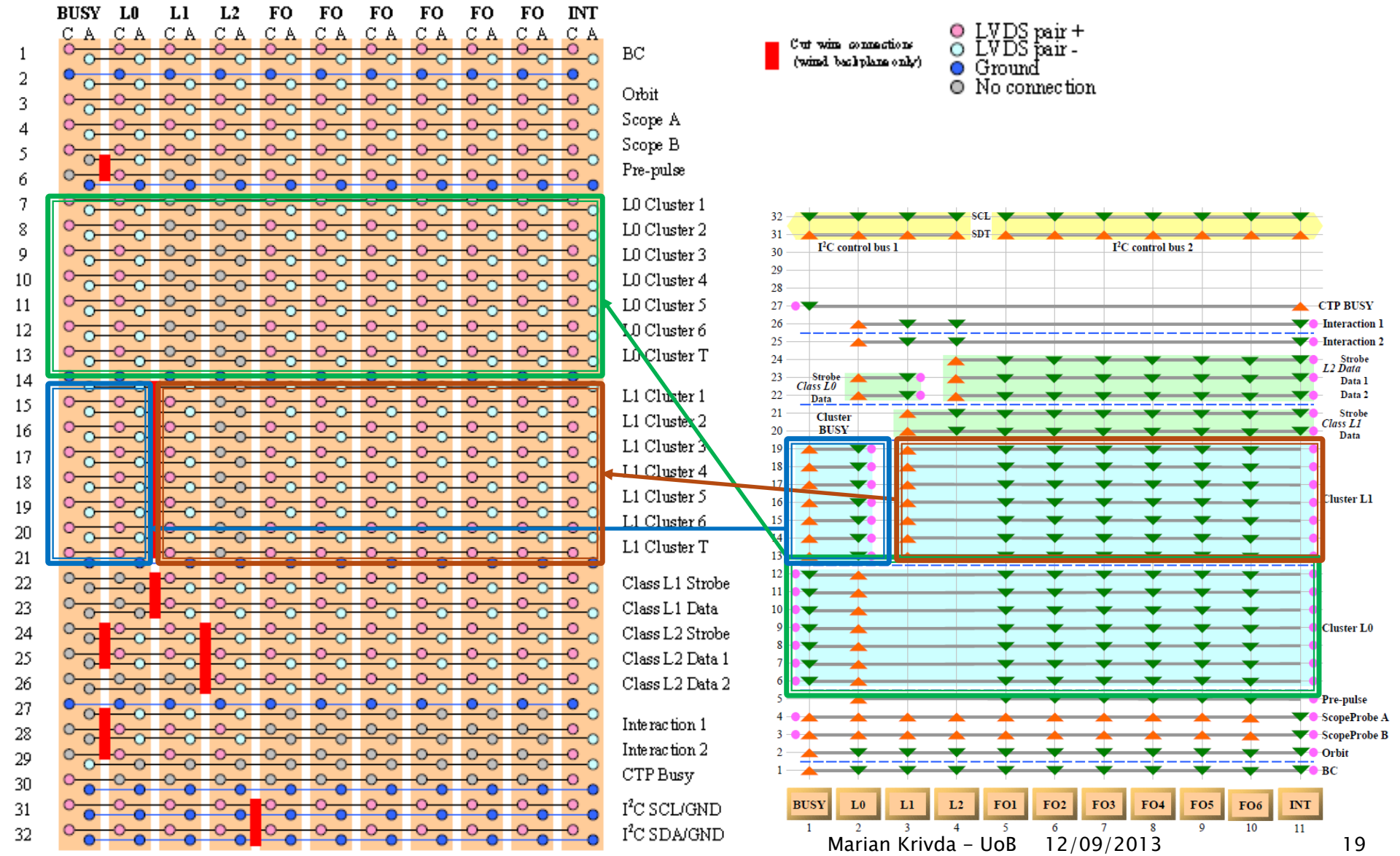
- 2 links:
  - **L0 Class data**
  - **L0 Class strobe**
- **L0 Class data** used on current CTP to transmit 50 class bits
- **L0 Class strobe** used on current CTP to transmit "L0 inputs" (sent from INT board to DAQ after each L2a trigger)
- New L0 board => "L0 inputs" sent to DAQ directly (after each L0 trigger)
- **L0 Class strobe** can be used to transmit another 50 class bits

Extension of Clusters

Clusters

- 6 physics + 1 software cluster available now
- Limited by number of links on backplane connections between L0/L1/2 and FO boards
- Increasing number of clusters to 8 requires multiplexing on backplane
- Consequences:
  - Increased latency of CTP for L0 trigger by at least one BC
  - Change in L2a trigger message

CTP backplane limitations for clusters



Cluster data on CTP backplane

- Cluster strobe can start at even or odd slice of transmission
- 2 consecutive BCs x 7 links = 14 bits available
- STROBE + 9 data bits + 4 Hamming bits
- 8 clusters + 1 test cluster (sw triggers) + 4 Hamming bits

CLST_1	CLST_7
CLST_2	CLST_8
CLST_3	CLST_9 (T)
CLST_4	Hamming_1
CLST_5	Hamming_2
CLST_6	Hamming_3
STROBE	Hamming_4

Cluster BUSY on CTP backplane

- 2 consecutive BCs x 7 links = 14 bits available
- STROBE + 9 data bits + 4 Hamming bits
- Consequences -> 1 BC delay for BUSY

CLST_1_B	CLST_7_B
CLST_2_B	CLST_8_B
CLST_3_B	CLST_9_B (T)
CLST_4_B	Hamming_1
CLST_5_B	Hamming_2
CLST_6_B	Hamming_3
STROBE	Hamming_4

Current solution for Cluster BUSY

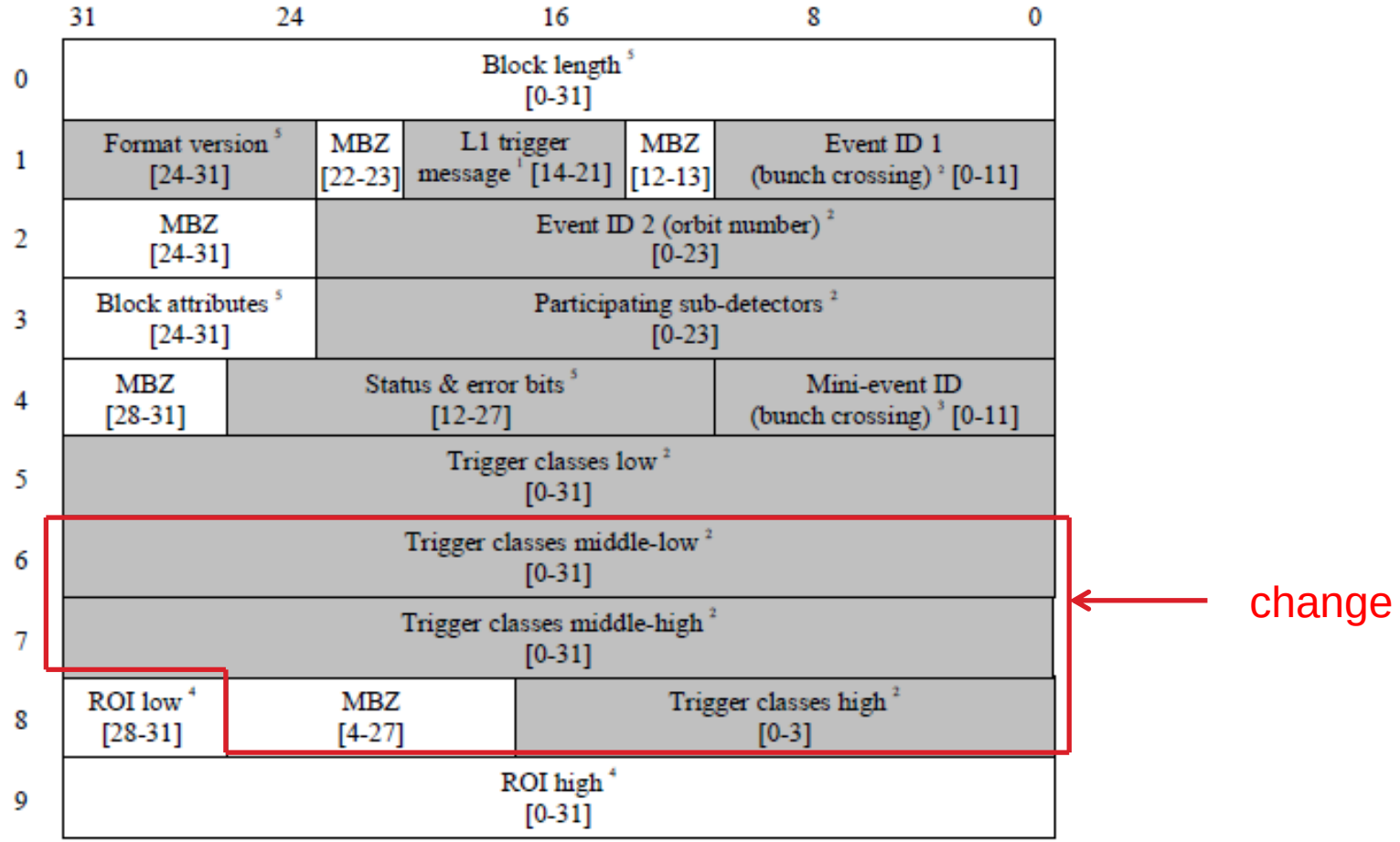
- If no cluster BUSY => no cluster BUSY strobe active
- Cluster BUSY strobe can start at even or odd slice of transmission
- Always make OR from 2 consecutive BUSY signals in order not to miss BUSY during transmission (50 ns)
- 8 clusters BUSYs + 1 test cluster BUSY (sw triggers) + Hamming bits

New format for L1 and L2 trigger data

L1 Data serial format					
Serial bit	*Data*	*Sequence List*		*L1 Message*	
		Word	*Bit*	*Word*	*Bit*
1	Spare	0	15	1	11
2	**ClT**	0	14	1	10
3..6	**RoC[4..1]**	0	13..10	1	9..6
7	**ESR**	0	9	1	5
8	**L1SwC**	0	8	1	4
9..10	**L1Class[50..1]**	0	7..6	1	3..2
11..12		1	15..14	1	1..0
13..24		1	13..2	2	11..0
25..26		1	1..0	3	11..10
27..36		2	15..6	3	9..0
37..42		2	5..0	4	11..6
43..48		3	15..10	4	5..0
49..58		3	9..0	5	11..2
59..70	**L1Class[100..51]**	8	11..0	6	11..0
71..74		8	15..12	7	3..0
75..82		9	7..0	7	11..4
83..90		9	15..8	8	7..0
91..94		10	3..0	8	11..8
95..106		10	15..4	9	11..0
107..108		11	1..0	10	1.0
	Spare			10	11..2

L2 Data serial format					
Serial bit	*Data*	*Sequence List*		*L2a Message*	
		Word	*Bit*	*Word*	*Bit*
1	**L2arF**				
2..13	**BCID[12..1]**			1	11..0
14..25	**OrbitID[24..13]**			2	11..0
26..37	**OrbitID[12..1]**			3	11..0
38	Spare	4	14	4	11
39	**ESR**	4	13	4	10
40	**ClT**	4	12	4	9
41	**L2SwC**	4	11	4	8
42..47	**L2Cluster[6..1]**	4	10..5	4	7..2
48..49	**L2Class[50..49]**	4	4..3	4	1..0
50..52	**L2Class[48..25]** or **Detector[24..1]**	4	2..0	5	11..9
53..61		5	15..7	5	8..0
62..68		5	6..0	6	11..5
69..73		6	15..11	6	4..0
74..84	**L2Class[24..1]**	6	10..0	7	11..1
85		7	15	7	0
86..97		7	14..3	8	11..0
98..109	**L2Class[100..51]**	12	11..0	9	11..0
110..113		12	15..12	10	3..0
114..121		13	7..0	10	11..4
122..129		13	15..8	11	7..0
130..133		14	3..0	11	11..8
134..145		14	15..4	12	11..0
146..148		11	3..2	13	1..0
149.150	**L2Cluster[8..7]**	11	5..4	13	3..2
	Spare	11	15..6	13	11..4

New Common Data Header format



Second link to DAQ

Second (new) link to DAQ

- 10G Ethernet
- New interaction (INT) record -> send 24 (48) inputs with each BC when interaction occurred instead of many INT definitions
- DAQ pick-up L0 trigger inputs from interaction stream (discussion with Alice DAQ group ongoing)

New format of CTP readout (via first link to DAQ)

Word	[31..16]	[15]	[14..12]	[11..0]
1	*Don't care* (0)	**BlockID** = 0	*Don't care* (0)	**BCID**[11..0]
2				**OrbitID**[23..12]
3				**OrbitID**[11..0]

Physics trigger

	Bit	*Data*
Word **4**	[31..16]	*Don't care* (0)
	[15]	**BlockID** = 0
	[14..11]	*Don't care* (0)
	[10]	**ESR**
	[9]	*Don't care* (0)
	[8]	**L2SwC** = 0
	[7..6]	**L2Cluster** [6..5]
	[5..2]	**L2Cluster** [4..1]
	[1..0]	**L2Class** [50..49]

Software trigger

	Bit	*Data*
Word **4**	[31..16]	*Don't care* (0)
	[15]	**BlockID** = 0
	[14..11]	*Don't care* (0)
	[10]	*Don't care* (0)
	[9]	**CIT**
	[8]	**L2SwC** = 1
	[7..6]	*Don't care* (0)
	[5..2]	**RoC**[4..1]
	[1..0]	*Don't care* (0)

Word	[31..16]	[15]	[14..12]	[11..0]
5	*Don't care* (0)	**BlockID** = 0	*Don't care* (0)	**L2Class** [48..37]
6				**L2Class** [36..25]
7				**L2Class** [24..13]
8				**L2Class** [12..1]

Word	[31..16]	[15]	[14..12]	[11..0]
5	*Don't care* (0)	**BlockID** = 0	*Don't care* (0)	**L2Detector** [24..13]
6				**L2Detector** [12..1]
7				*Don't care* (0)
8				*Don't care* (0)

Word	[31..16]	[15]	[14..12]	[11..0]
9	*Don't care* (0)	**BlockID** = 0	*Don't care* (0)	~~**L0TrgIn**[24..13]~~
10				~~**L0TrgIn**[12..1]~~
11				**L1TrgIn**[24..13]
12				**L1TrgIn**[12..1]
13				**L2TrgIn**[12..1]

New Interaction record format (proposal)

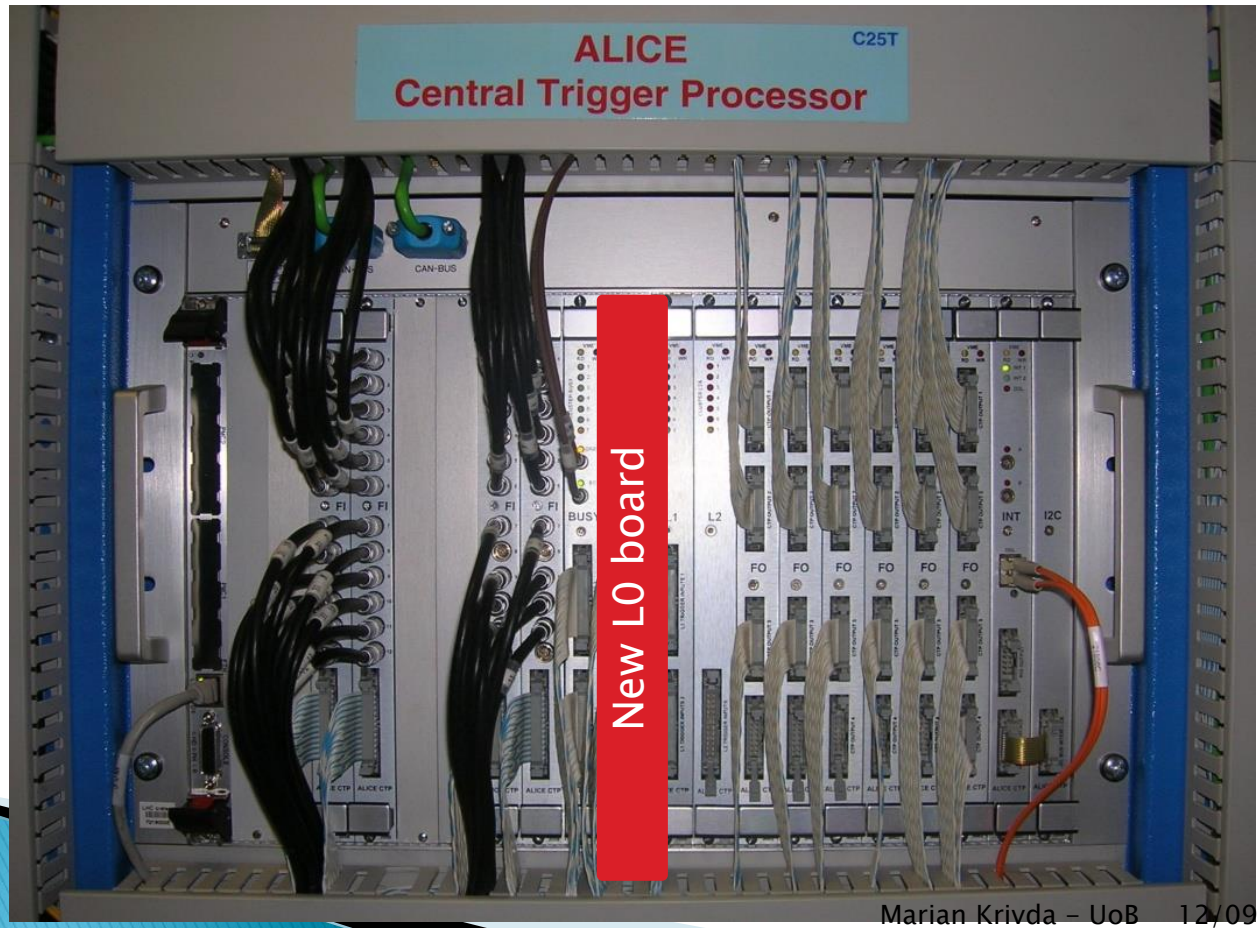
Word	[31]	[30]	[29]	[28..12]	[11..0]
1	**1 (Orbit)**	**1 (first word)**	**Err**	Don`t care	**Orbit** number [23..12]
2	**1**	**0 (second w.)**	**Err**	Don't care	**Orbit** number [11..0]
3	0 (BC)	1 (first word)	**L0ti[18..1]**		**BC** number [11..0]
4	0	**0 (second w.)**	**L0ti[48..19]**		
⋮			⋮		⋮
n	0	1	**L0ti[18..1]**		**BC** number [11..0]
n+1	0	**0**	**L0ti[48..19]**		
⋮			⋮		⋮
251	0	1	**L0ti[18..1]**		**BC** number [11..0]
252	0	**0**	**L0ti[48..19]**		
253	0	0	0	*Don`t care*	*Incomplete record* (hFFF)

- Discussion with Alice DAQ group ongoing

New L0 board

Alice trigger system for Run 2

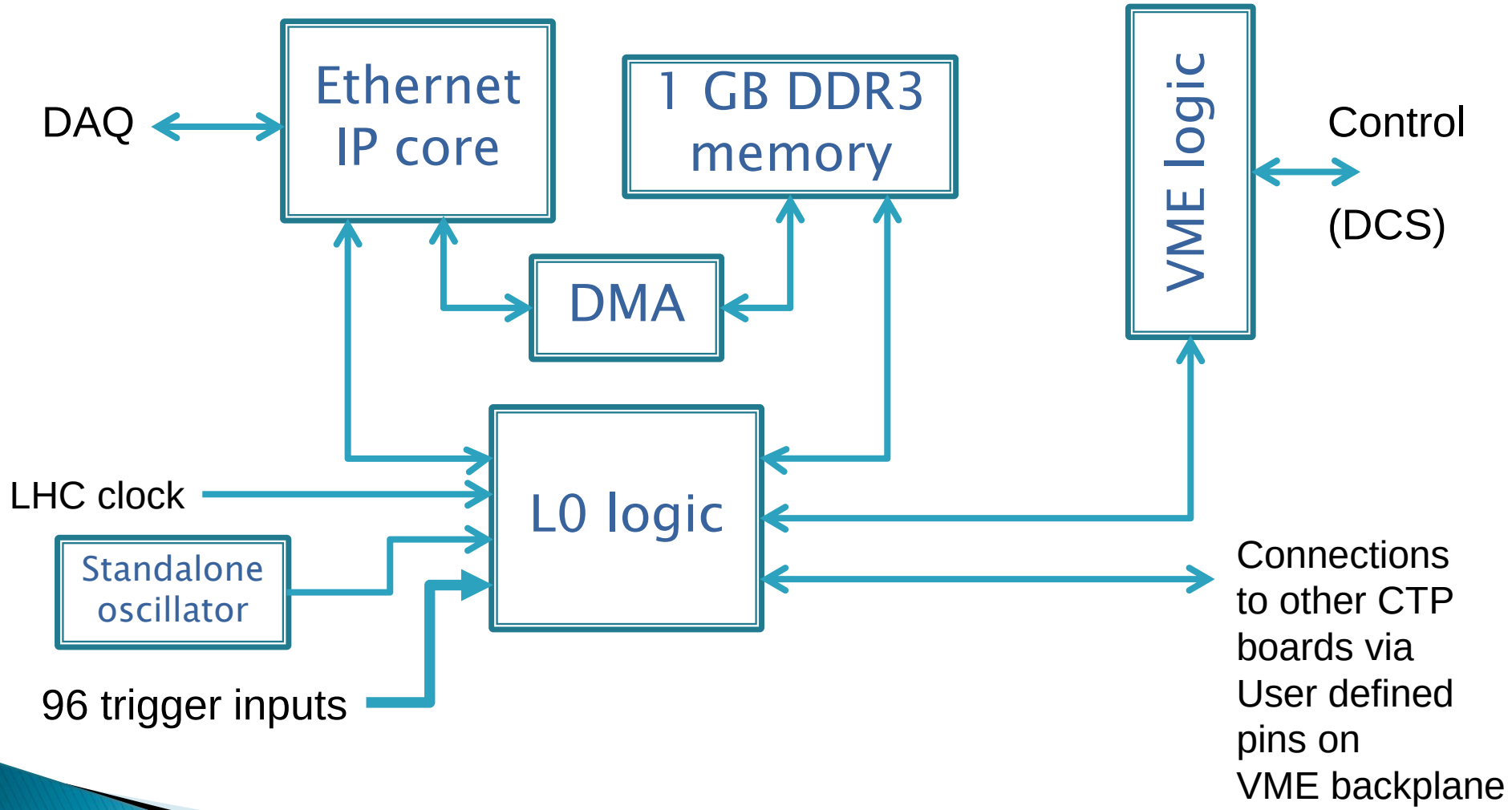
- Faster inputs from T0 and V0
- Upgrade of firmware for L1 ,L2 ,FO, BUSY and INT boards
- Completely new L0 board



New L0 board

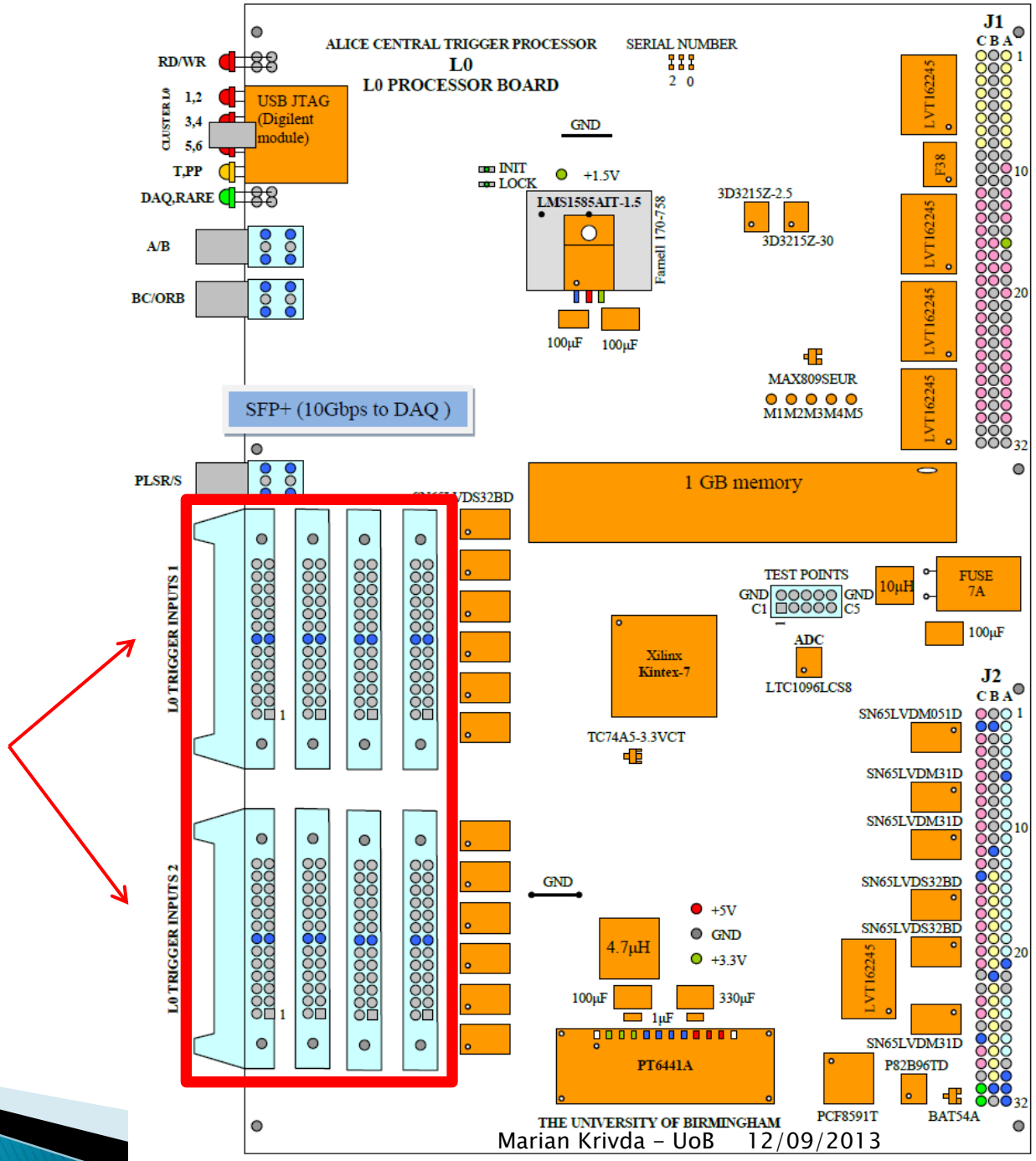
- 96 trigger inputs -> new type of connector for front panel (48 inputs for L0 + other possible trigger inputs)
- New FPGA – Xilinx Kintex7
- Bigger memory (DDR3 – 1GB)
- Synchronized downscaling
- CTP switch for L0 trigger inputs (48->24) inside FPGA
- More counters i.e. for classes and clusters
- New 10G link to DAQ from L0 board
- New interaction record -> send 24/48 inputs with each interaction
- Control of L0 board via 10G Ethernet (or other protocol) in future

New L0 board – block diagram

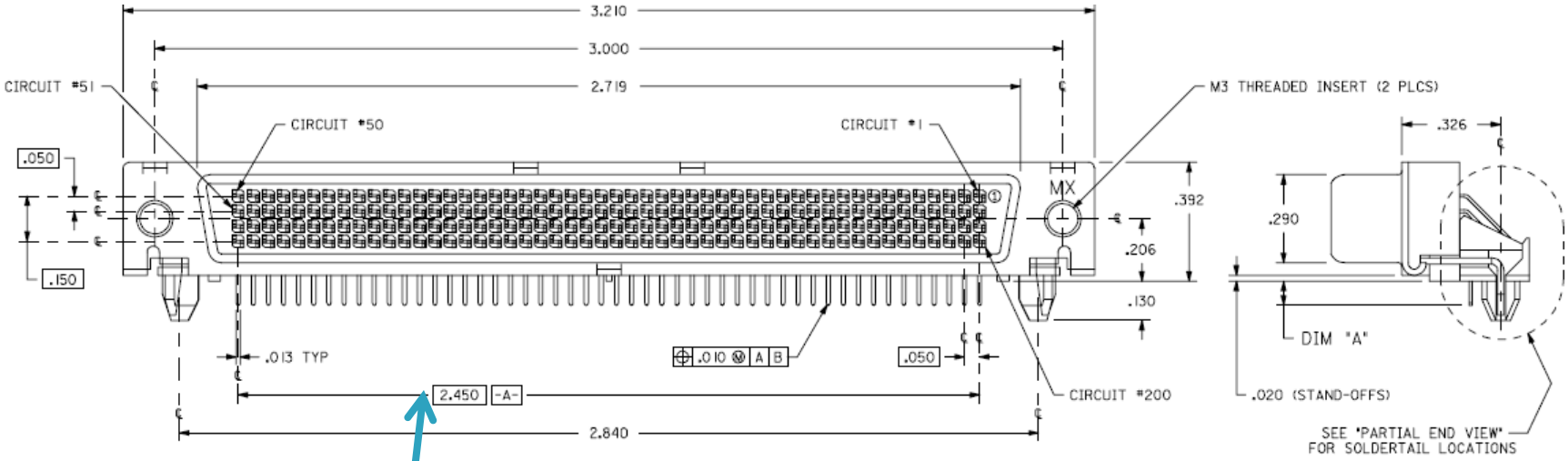


New L0 board

Very limited space for 4 flat cables



Front panel connector for 96 LVDS trigger inputs (200 pins – 96 diff. pairs + 8 GND pins)



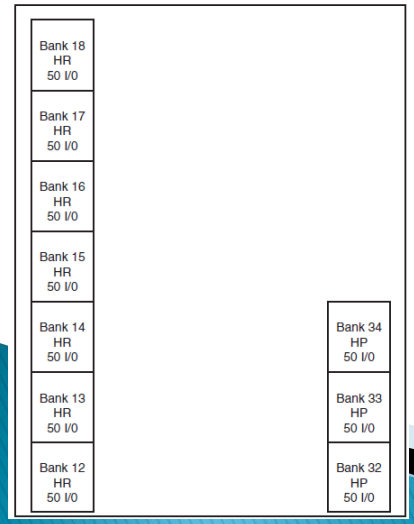
Right angle connector for 6U VME board (81.534 mm x 9.957 mm)

FPGA – Xilinx XC7K325TFFG900

Kintex-7 FPGA Feature Summary

Table 5: **Kintex-7 FPGA Feature Summary by Device**

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP Slices[2]	Block RAM Blocks[3]			CMTs[4]	PCIe[5]	GTXs	XADC Blocks	Total I/O Banks[6]	Max User I/O[7]
		Slices[1]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)						
XC7K70T	65,600	10,250	838	240	270	135	4,860	6	1	8	1	6	300
XC7K160T	162,240	25,350	2,188	600	650	325	11,700	8	1	8	1	8	400
XC7K325T	326,080	50,950	4,000	840	890	445	16,020	10	1	16	1	10	500
XC7K355T	356,160	55,650	5,088	1,440	1,430	715	25,740	6	1	24	1	6	300
XC7K410T	406,720	63,550	5,663	1,540	1,590	795	28,620	10	1	16	1	10	500
XC7K420T	416,960	65,150	5,938	1,680	1,670	835	30,060	8	1	32	1	8	400
XC7K480T	477,760	74,650	6,788	1,920	1,910	955	34,380	8	1	32	1	8	400



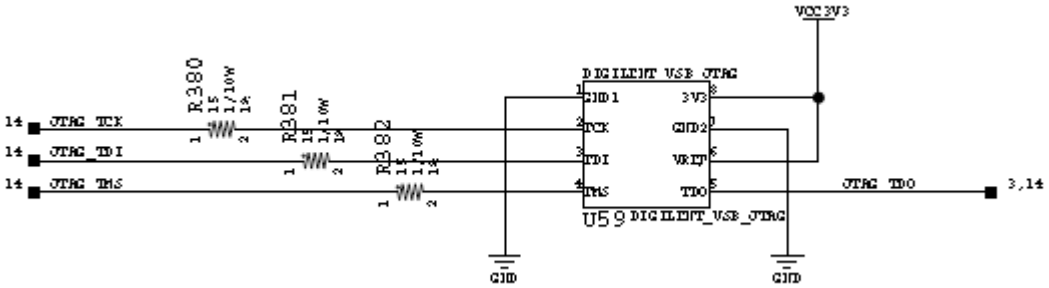
- 10 usable I/O banks
  - 7 High Range (HR) banks -> support 1.35 – 3.3V standards
  - 3 High Performance (HP) banks -> support 1.35 – 1.8 V standards

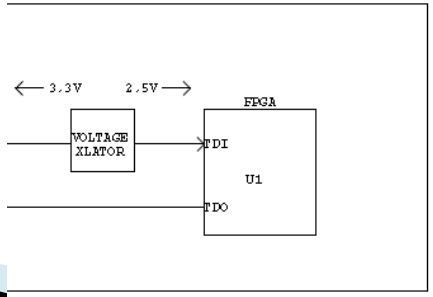
Configuration of Xilinx XC7K325T FPGA from memory

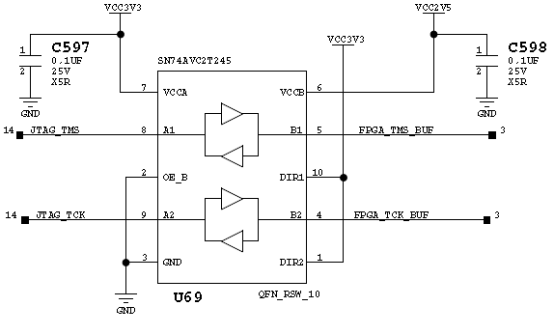
- The Master SPI configuration mode supports reading from an SPI flash using a data bus up to four bits wide
- Config. CLK generated by FPGA
- Configuration bitstream length -> 91,548,896
- MICRON – **N25Q128** (128-Mbit 3 V, 4-data pins, serial flash memory with 108 MHz SPI bus interface

Configuration of FPGA via JTAG serial interface

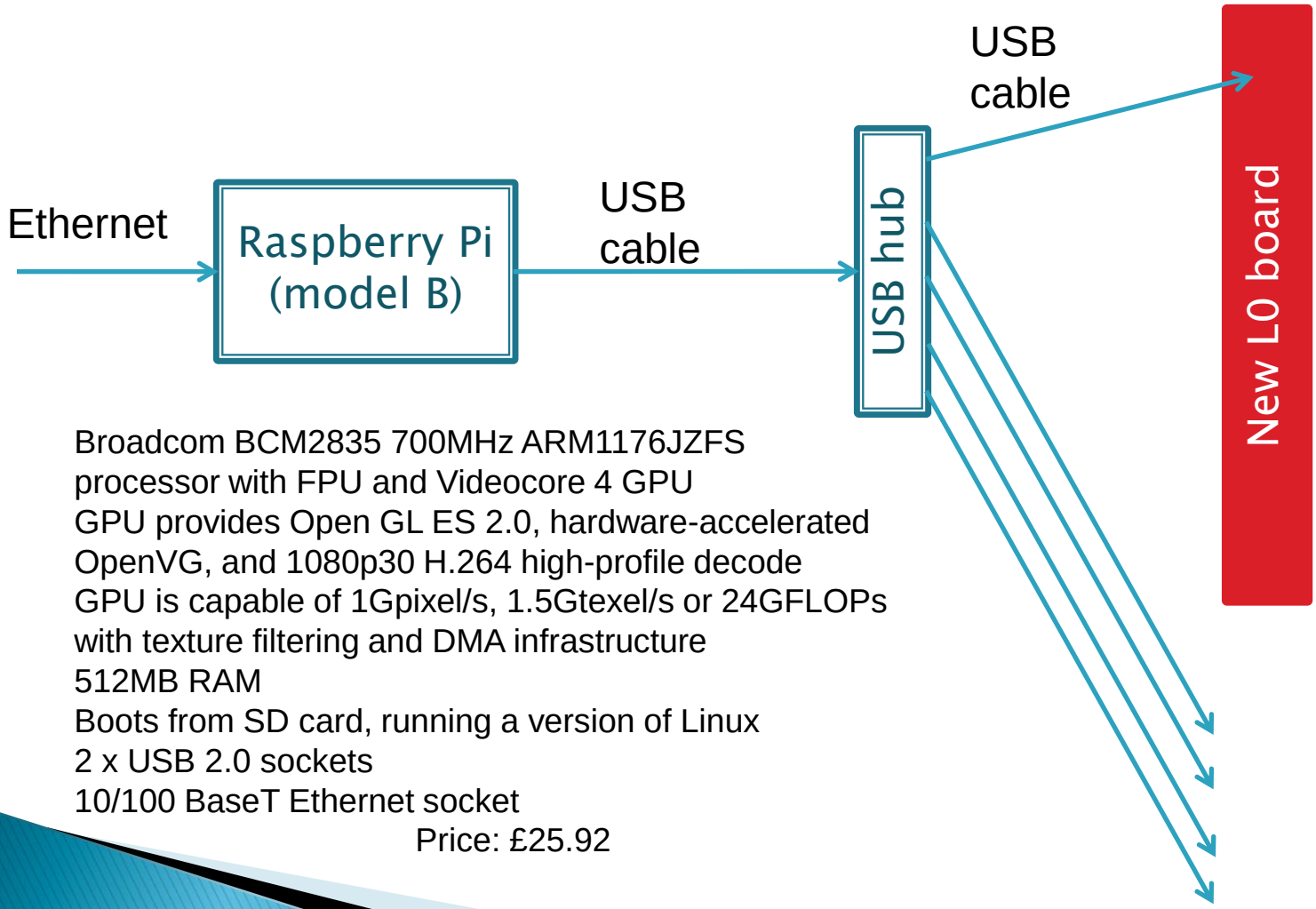
- JTAG interface for prototyping and debugging
- On-board JTAG configuration circuitry to enable configuration over USB
- USB JTAG module (DIGILENT, price 40 USD)







Remote configuration of FPGA

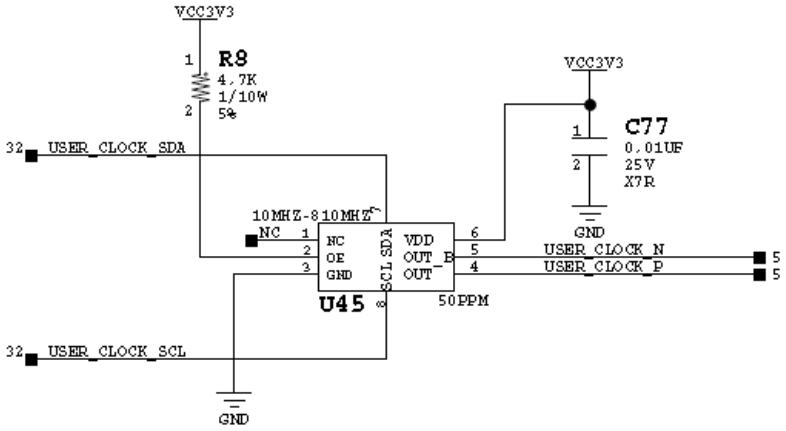


Broadcom BCM2835 700MHz ARM1176JZFS processor with FPU and Videocore 4 GPU
GPU provides Open GL ES 2.0, hardware-accelerated OpenVG, and 1080p30 H.264 high-profile decode
GPU is capable of 1Gpixel/s, 1.5Gtexel/s or 24GFLOPs with texture filtering and DMA infrastructure
512MB RAM
Boots from SD card, running a version of Linux
2 x USB 2.0 sockets
10/100 BaseT Ethernet socket

Price: £25.92

Clock

- LHC clock as default
- In case LHC clock missing -> “switch over” functionality inside Xilinx Kintex-7 used for on-board oscillator (SILABS 570BAB000544DG)
  - Programmable (via I2C) oscillator 10-810 MHz



Ideas for CTP upgrade for Run 3

3 Trigger levels

- LM: latency 0.8 μs, contribution from interaction trigger (upgraded V0/T0)
- L0: latency 1.2us, possible contribution from EMCAL, PHOS, TOF, ACORDE
- L1: latency 1.2-6 μs (fixed latency, but programmable in the given range), possible contribution from ZDC, EMCAL
- LM would still just be used as TRD pretrigger and would NOT be distributed to the other detectors.

Continuous and Triggered mode

- ITS, TPC and Muon Chambers can work in continuous AND triggered mode
- ITS is read out upon L0, all other detectors are read out upon L1
- If we do not introduce any selectivity at L1, then L1 can be made equal to L0.

Each detector as separate cluster

- The default operation for PbPb, pPb and pp reference running would be a readout of all detectors, that are not busy, upon an Minimum Bias (MB) interaction trigger, with ITS, TPC and MCH in continuous readout mode.

Cluster with more detectors still possible

- Operating at rates beyond the EMCAL readout rate it might then happen that there are a fraction of events with EMCAL data only and another fraction with TRD data only, and very few with both of them. Triggering an additional cluster containing EMCAL and TRD and triggering this cluster with a controlled rate will guarantee a given number of events with both detectors.
- For calibration purposes one might also want to have a fraction of events with ALL detectors present, so there would be an additional cluster with ALL detectors.

Elimination of CTP dead time

- At 100kHz interaction rate the present CTP deadtime of 1.5 μs would lead to 15% inefficiency, which is of course too much.
- The deadtime must therefore be reduced below 100ns and additional “input FIFO” can eliminate the CTP deadtime (de-randomizing in addition the CTP must be able to accept more than one L0 before arrival of L1).
- In this way the CTP is not responsible for any rejection of data, it will only depend on the detector capabilities what fraction triggers is rejected by their own Busy i.e. by their deadtime and buffering capabilities.

Heartbeat trigger

- Specific trigger issued by CTP at appropriate ORBIT/BC
- Reduces trigger data bandwidth
- Carrying commands and specific synchronization information
- Used by detectors – create “heartbeat events” sent via output links
- Used by processing nodes – data segmentation, fault finding, recovery procedures, …

Trigger distribution -> GBT/TTC

- Proposal is to use GBT
- Some detectors will keep TTC

- CTP needs to serve both systems

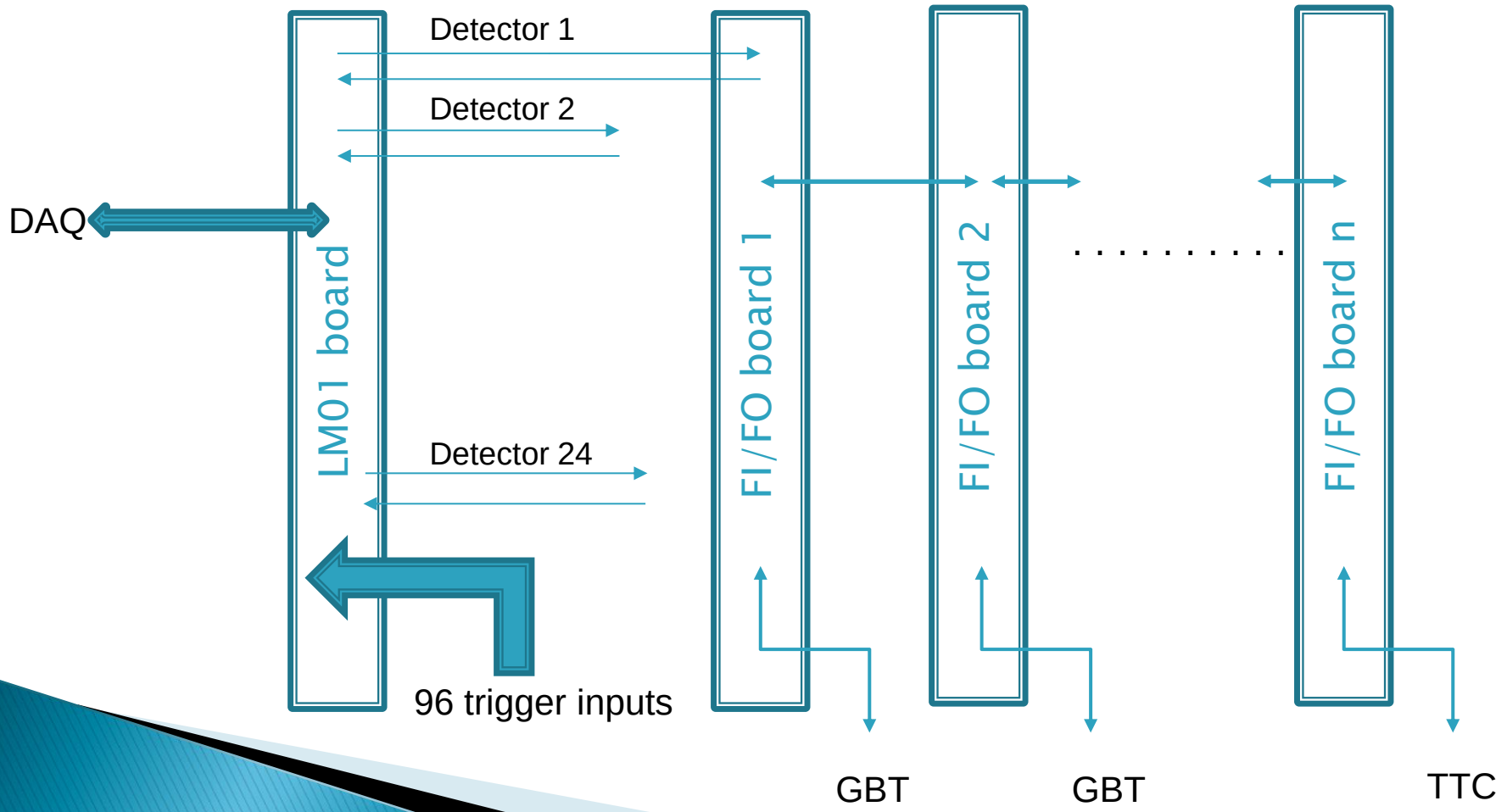
Detector`s behaviour

- ITS Cont / L0
- TPC Cont / L1
- TRD LM/LM+L1
- TOF L1
- EMC/PHOS L0+L1
- HMPID L0+L1
- MuID L1
- MCH Cont / L1
- V0/T0 L1
- ZDC L1

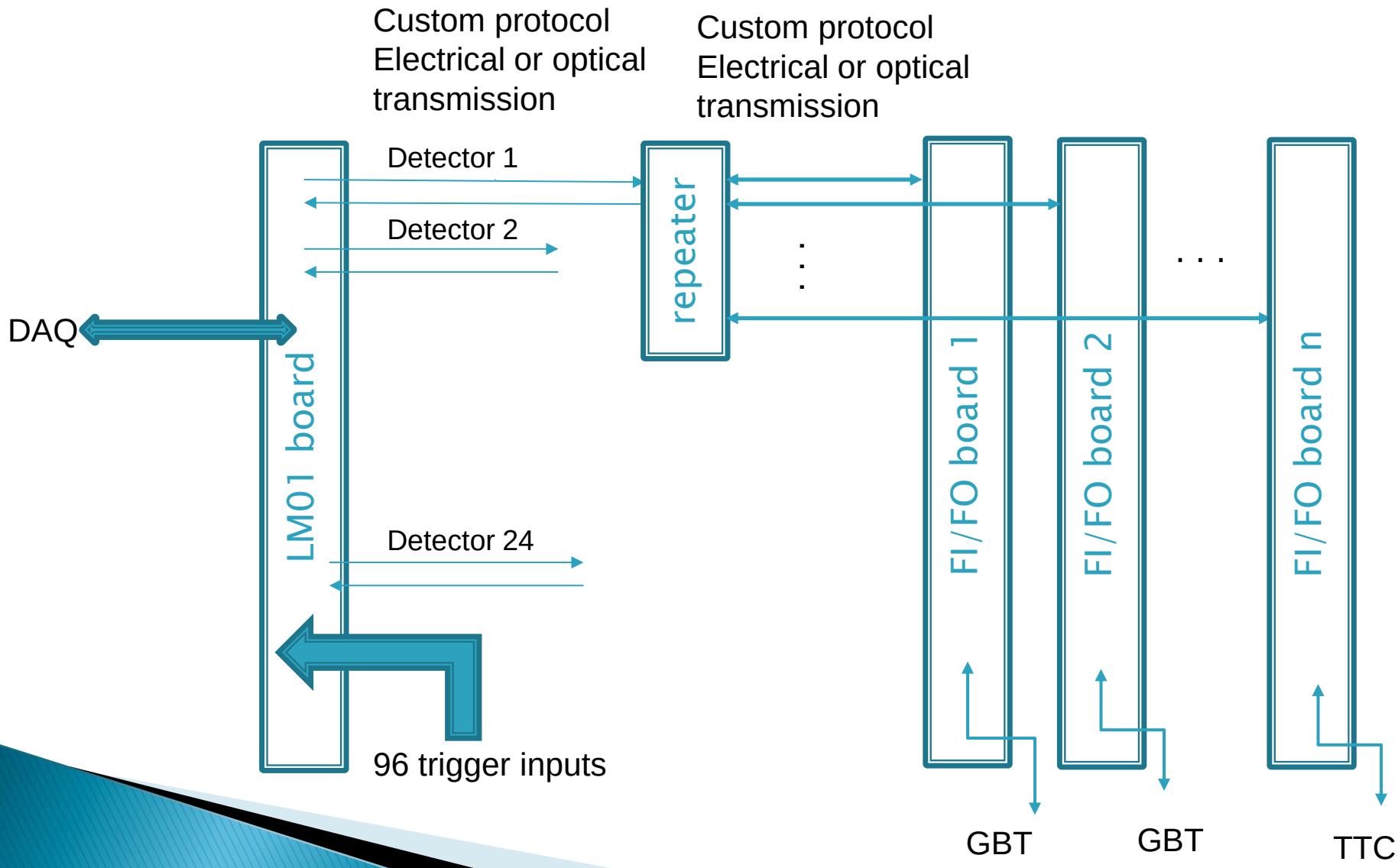
Distribution of trigger signals

Custom protocol
Electrical or optical transmission

Daisy – chain of FI/FO boards in case that more than one FI/FO board is necessary



Distribution of trigger signals



Summary

- Activities for relocation and recabling of T0, V0 and TRD are ongoing.
- A new L0 board is in progress, production expected in Autumn 2013
- Firmware development and testing in 2014
- CTP proposal for run 3 is in preparation

- The upgraded CTP for Run 3 will be able to provide enough flexibility for all foreseen running scenario

Back up slides

Summary table (Run 3)

Detector	type	MEB	t_{RO} PbPb	Max. PbPb readout rate	Max. pp and pPb readout rate
ITS	Cont. / L0	n.a. / ?	n.a. / ?	100 kHz	400kHz
TPC	Cont. / L1	n.a.	n.a.	n.a.	n.a.
TRD	LM/LM+L1	no	7-8 μs	100 kHz	100kHz
TOF	L1	yes	5 μs	200 kHz	400kHz
EMC/PHOS	L0+L1	yes at L1	20 μs	50 kHz	50kHz
HMPID	L0+L1	?	?	10 kHz	10kHz
MuID	L1	yes	<200 ns	100 kHz	400kHz
MCH	Cont. / L1	n.a.	n.a.	100 kHz	400kHz
V0/T0	L1	yes	5us	200 kHz	400kHz
ZDC	L1	yes	5 μs	100kHz	400kHz

Current L0 trigger input switch

- In order to handle more L0 trigger inputs the L0 trigger input multiplexer 50:24 has been made from available Faninout boards