# Test Automation of 3D Integrated Systems

Stephen Pateras

Mentor Graphics Corporation

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# Agenda

- Basic semiconductor test concepts
  - Scan test
  - Design-for-Test (DFT)
  - Built-In Self-Test (BIST)
- 3D-IC Testing
  - New challenges
  - Known-Good-Die (KGD)
  - Test access for stacked die
  - Testing die within 3D stack
  - Testing TSV connections between stacked die


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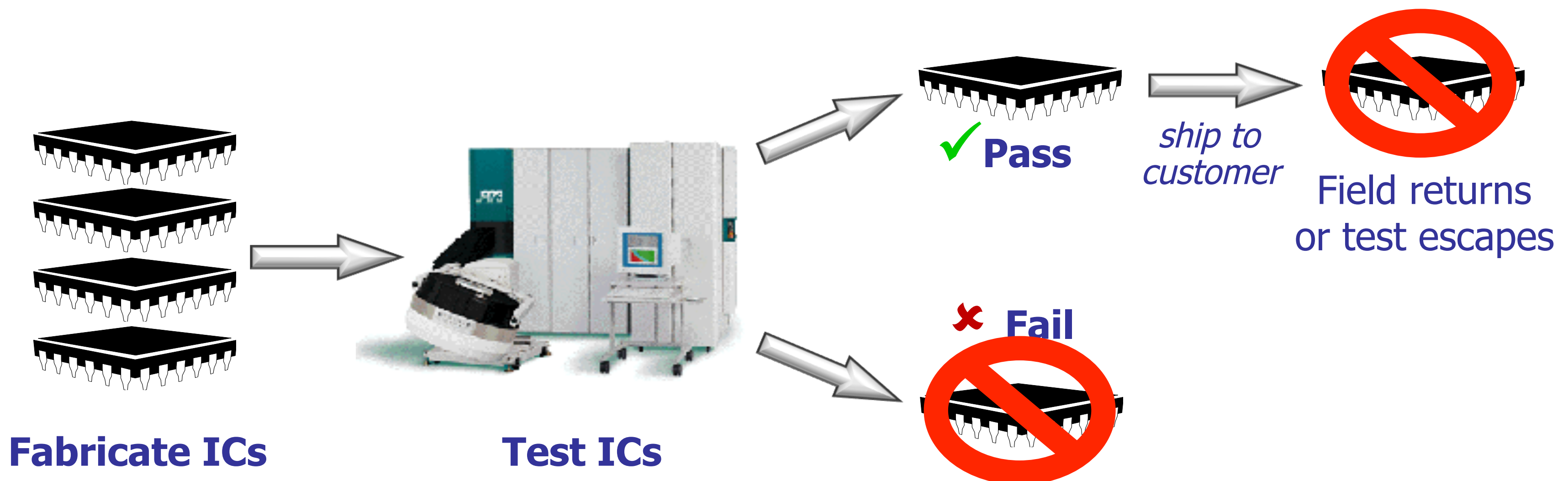
# Semiconductor Test – In a Nutshell

- Process to ensure fabricated IC works correctly
  - Tester applies stimulus to input and examines output data
- Test automation: input patterns and expected output data generated automatically
  - Need to maximize defect detection and minimize patterns





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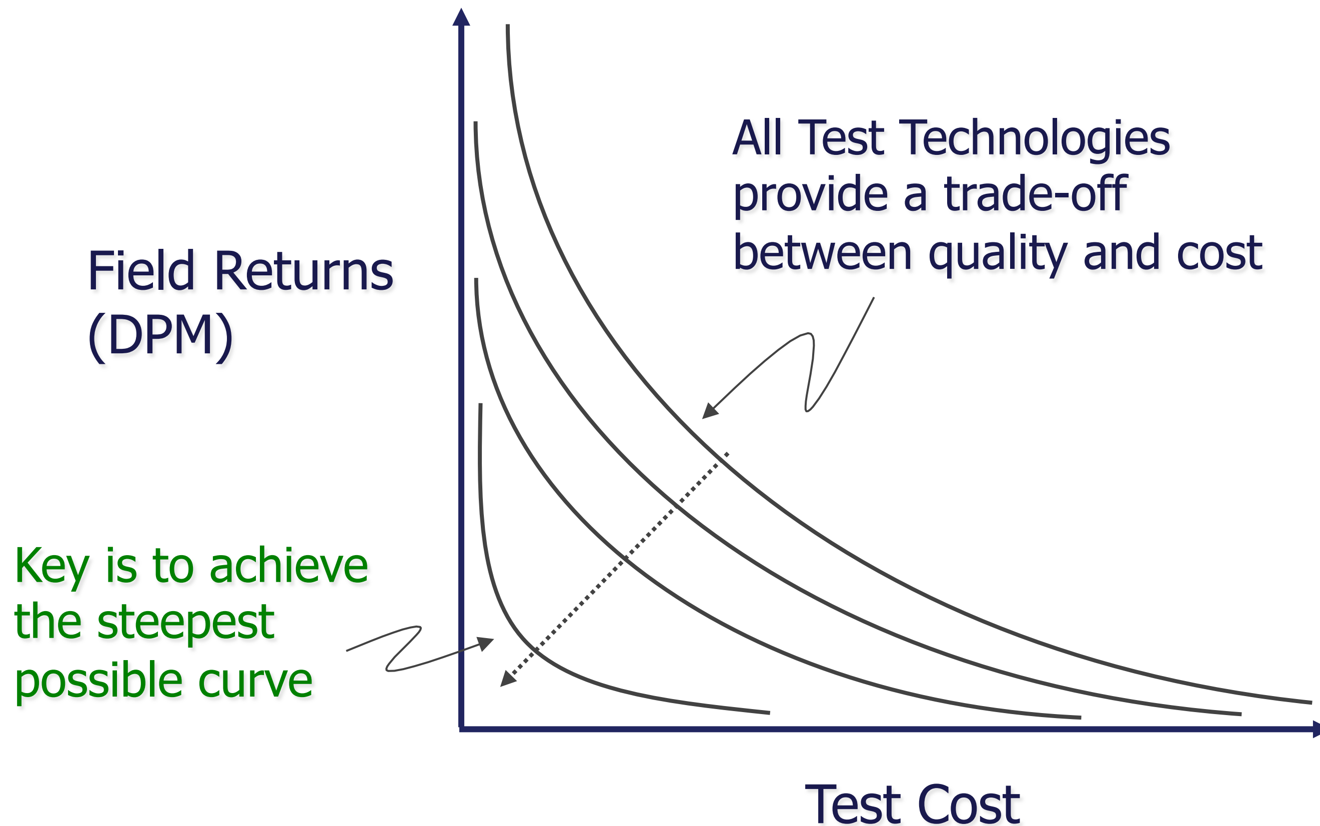
# Field Returns vs Test Cost Correlation

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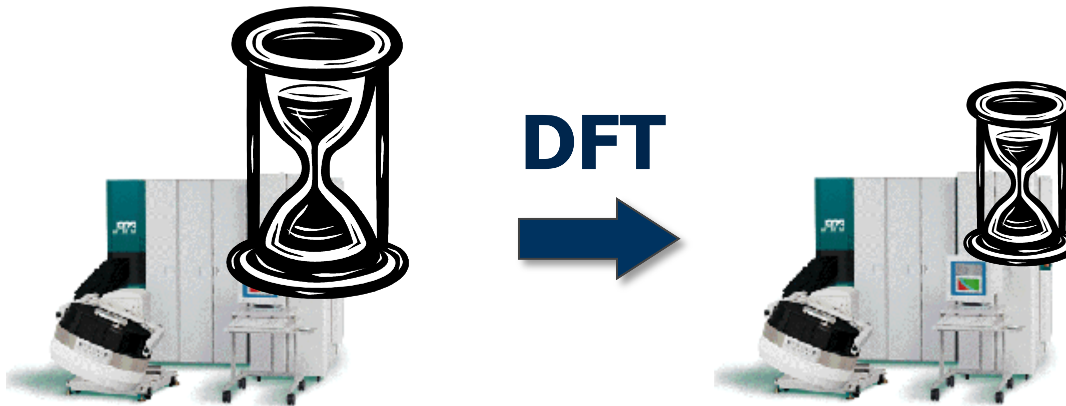
# Design-For-Test (DFT)

- Circuit modification and/or additions to make IC easier to test
  - Scan for ATPG
  - Built-In Self-Test (BIST): all testing done on chip




**Reduced test time and hence cost**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# Scan Design

- Internal scan is a structured DFT technique that
  - Replaces sequential storage elements with scan cells
  - Stitches scan cells into a serial scan register (scan chain)
  - Makes sequential circuitry appear combinational
- Structural test technique
  - Directly tests circuit structure rather than higher-level function
  - Easier to automate
  - Enables standardized defect coverage metrics


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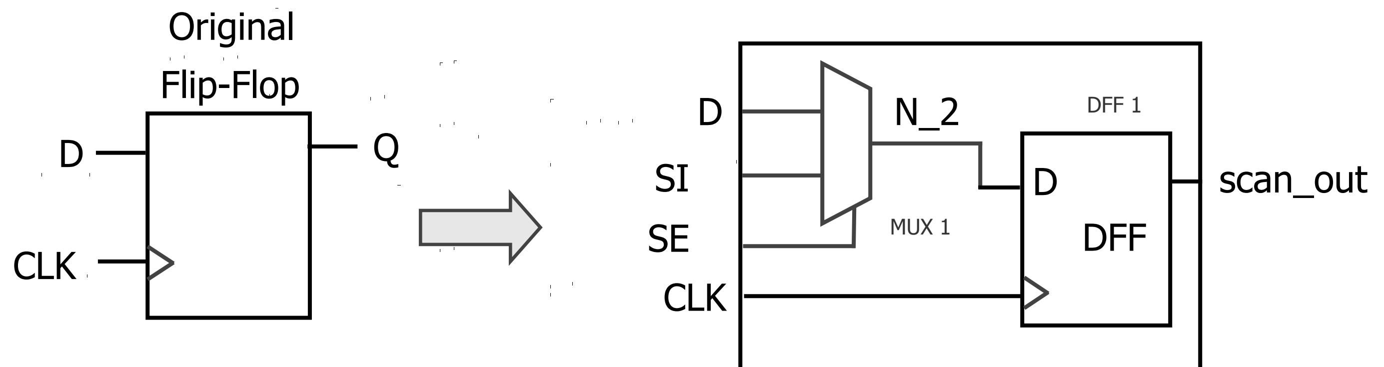
# Mux DFF Scan Cell

- Multiplexer selects data input:
  - D in normal mode
  - Scan_in (SI) scan mode
- Scan_enable (SE) selects mode of operation
- Increased propagation delay
- Adds 5-15% area overhead
- Standard approach today





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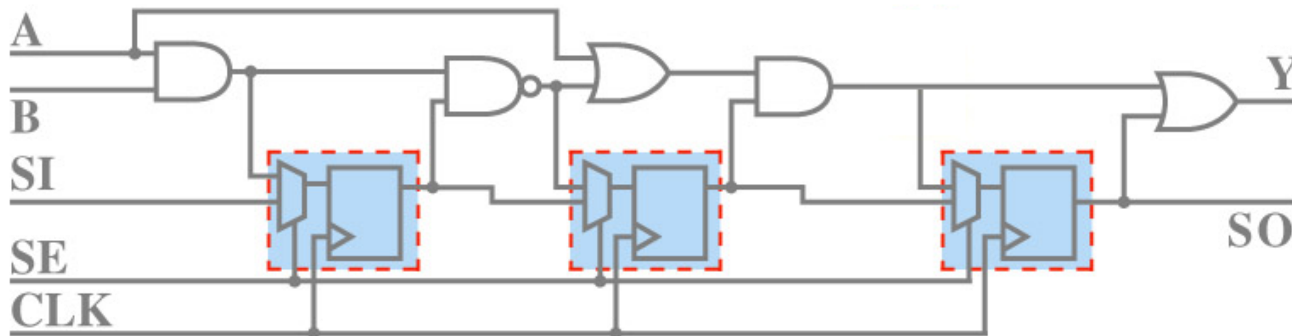
# Scan Chains

- Scan_Enable (SE):
  - When active allows scan data to enter the registers.
- Scan input port (SI):
  - Data is loaded into scan cells.
- Scan output port (SO):
  - Data is read by shifting data out.

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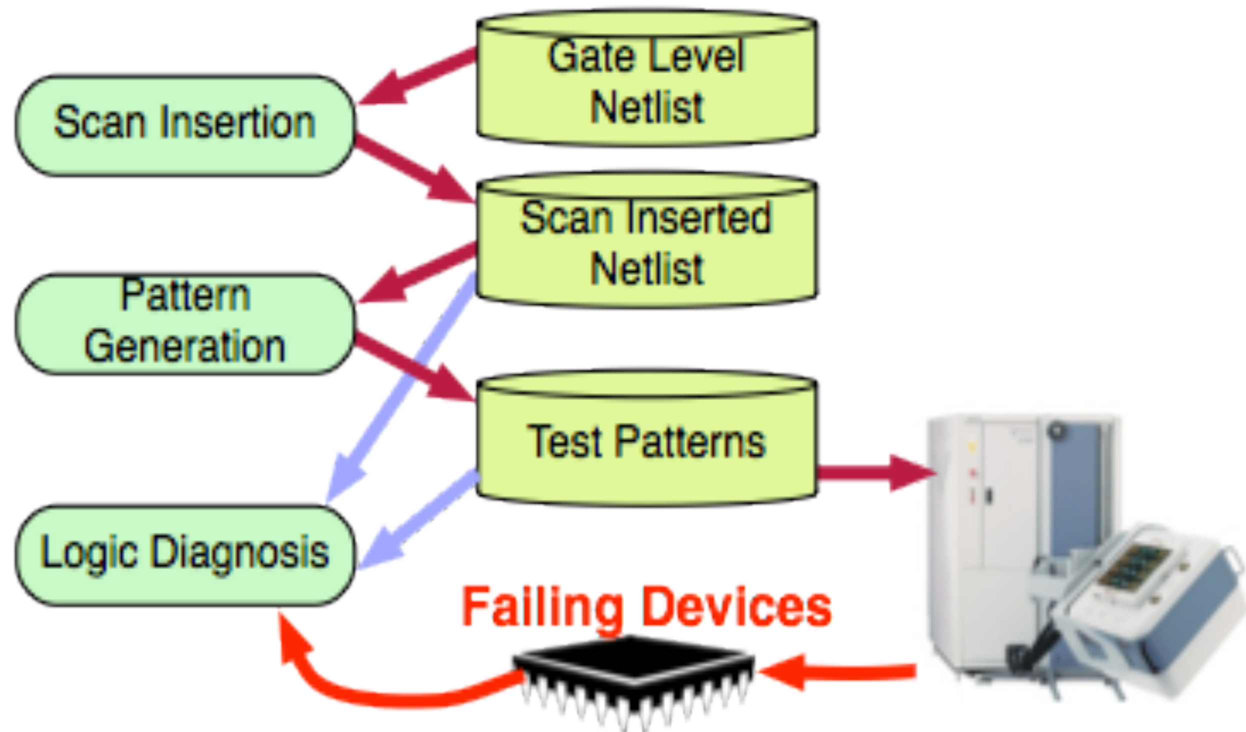
# Typical ATPG Flow

ATPG: Automatic Test Pattern Generation

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# Stuck-At Fault Model

- Fault models are logic targets for defects.
- A fault is detected:
  - When a difference is observed between a "good" and "faulty" circuit.
- Most common fault model:
  - Most defects are detected with the stuck-at fault model.
  - A terminal of a gate is permanently stuck-at 0 or 1.
  - Also detects other defects:
    - Opens
    - Shorts
    - Bridging faults
    - Others…

| A | B | Y | | |
|---|---|---|---|---|
| | | Good | A s.a.0 | A s.a.1 |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 |

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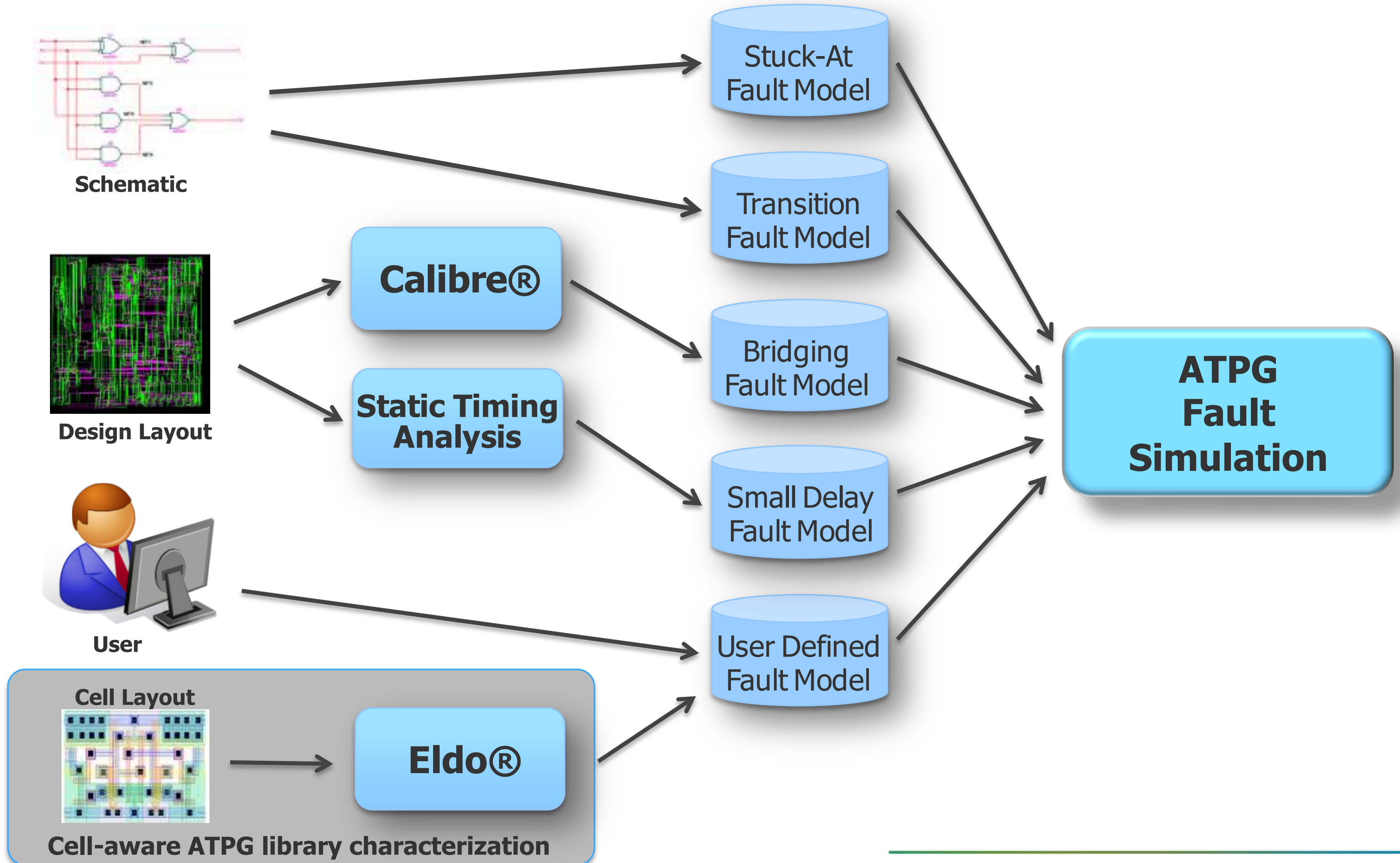
# Fault Model Progression



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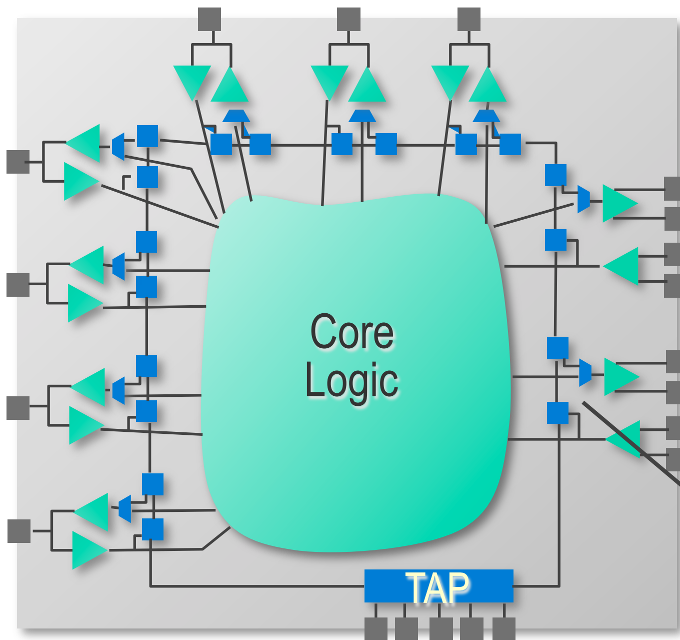
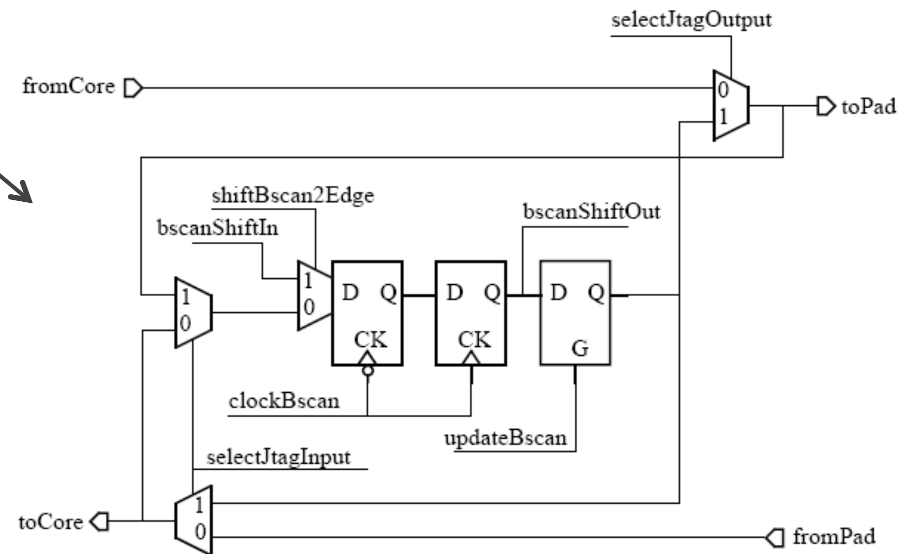
# Boundary Scan – IEEE 1149.1 Standard




Scan cells placed on I/O support both external test of interconnect as well as internal test of die

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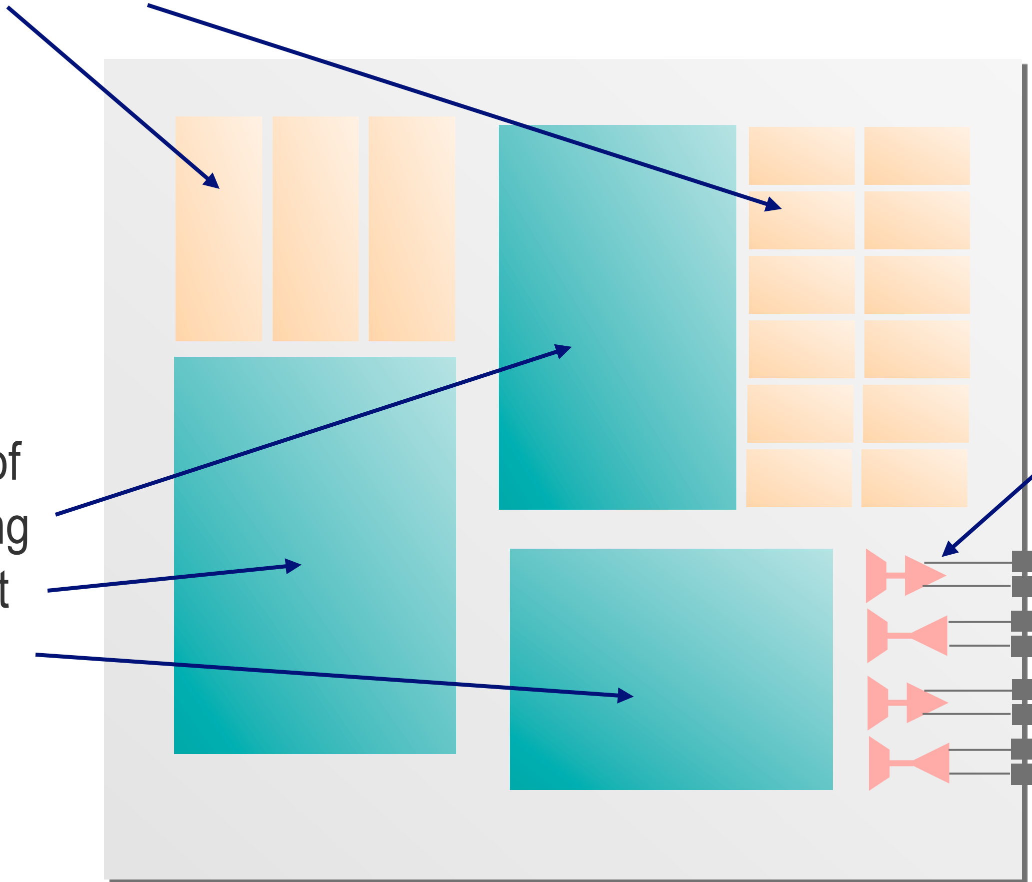
# Embedded Test IP - BIST

Megabits worth of high performance memories



Tens of millions of logic gates running at many different asynchronous frequencies

Dozens of multi-gigahertz Serdes I/O



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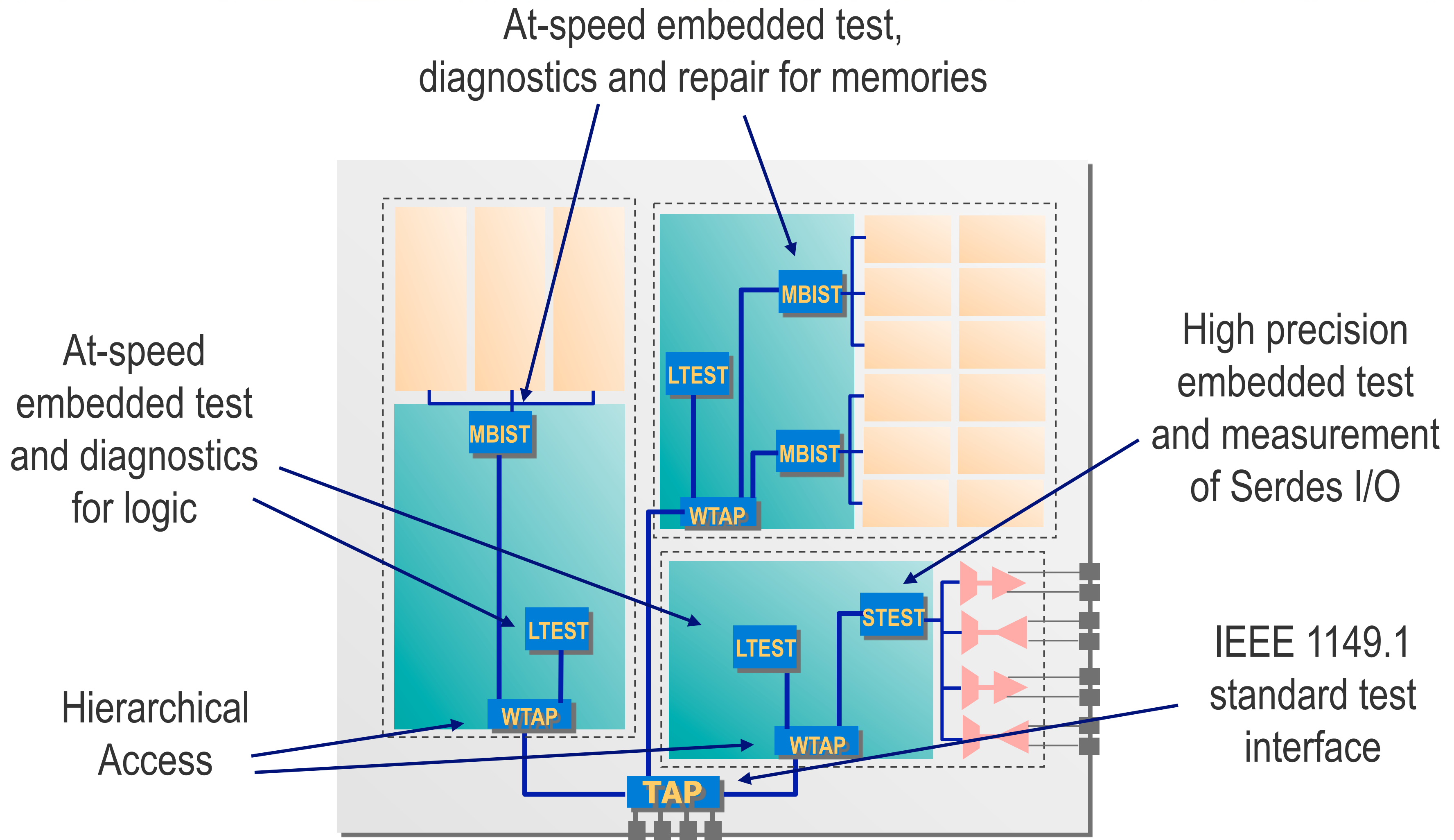
# Embedded IP Architecture

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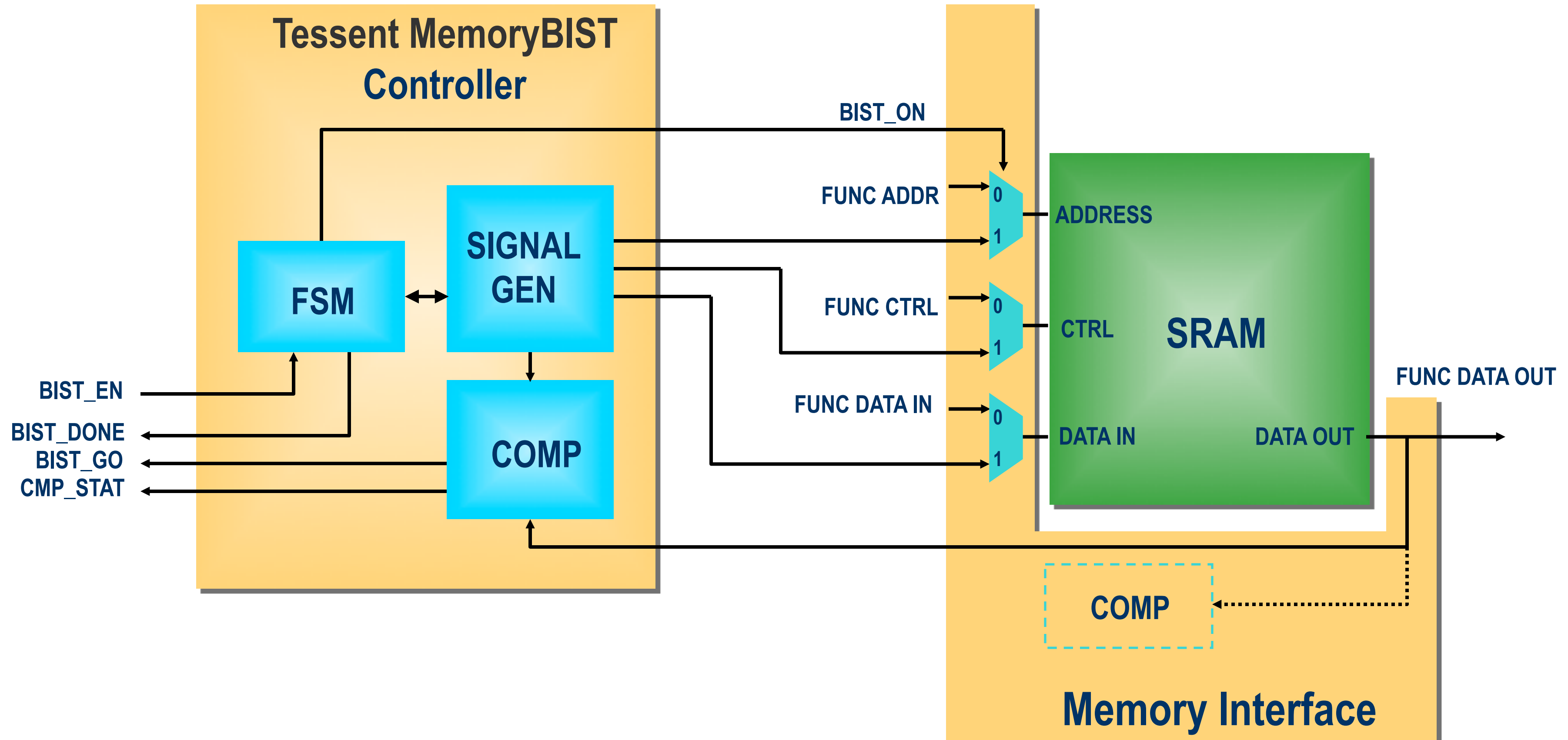
# Memory BIST – Basic Architecture



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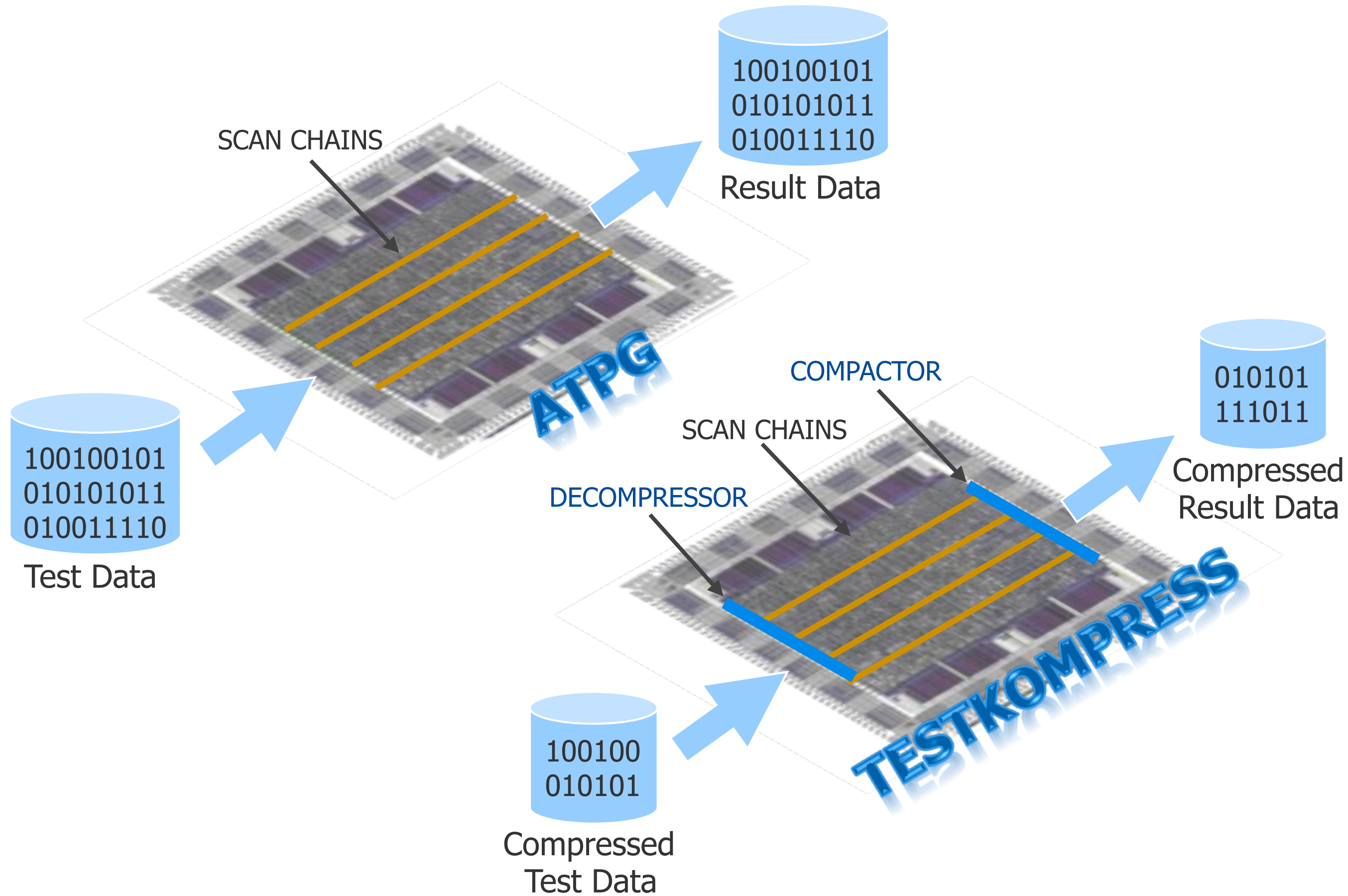
# Logic Test Solutions



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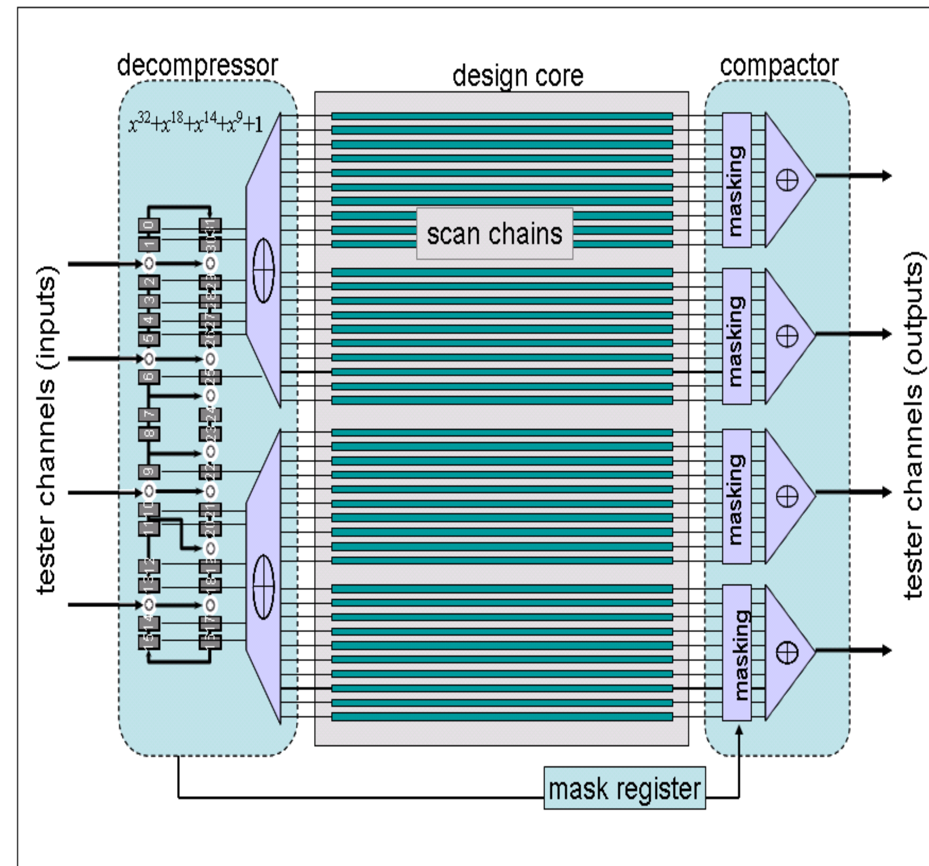
# ATPG Compression Technology

- Use logic to convert compressed tester stimulus to many short internal chains
- Cycles/time to load each pattern dramatically reduced
- 100X time & data compression enables higher test quality
- Patented X-masking ensures no loss in test coverage





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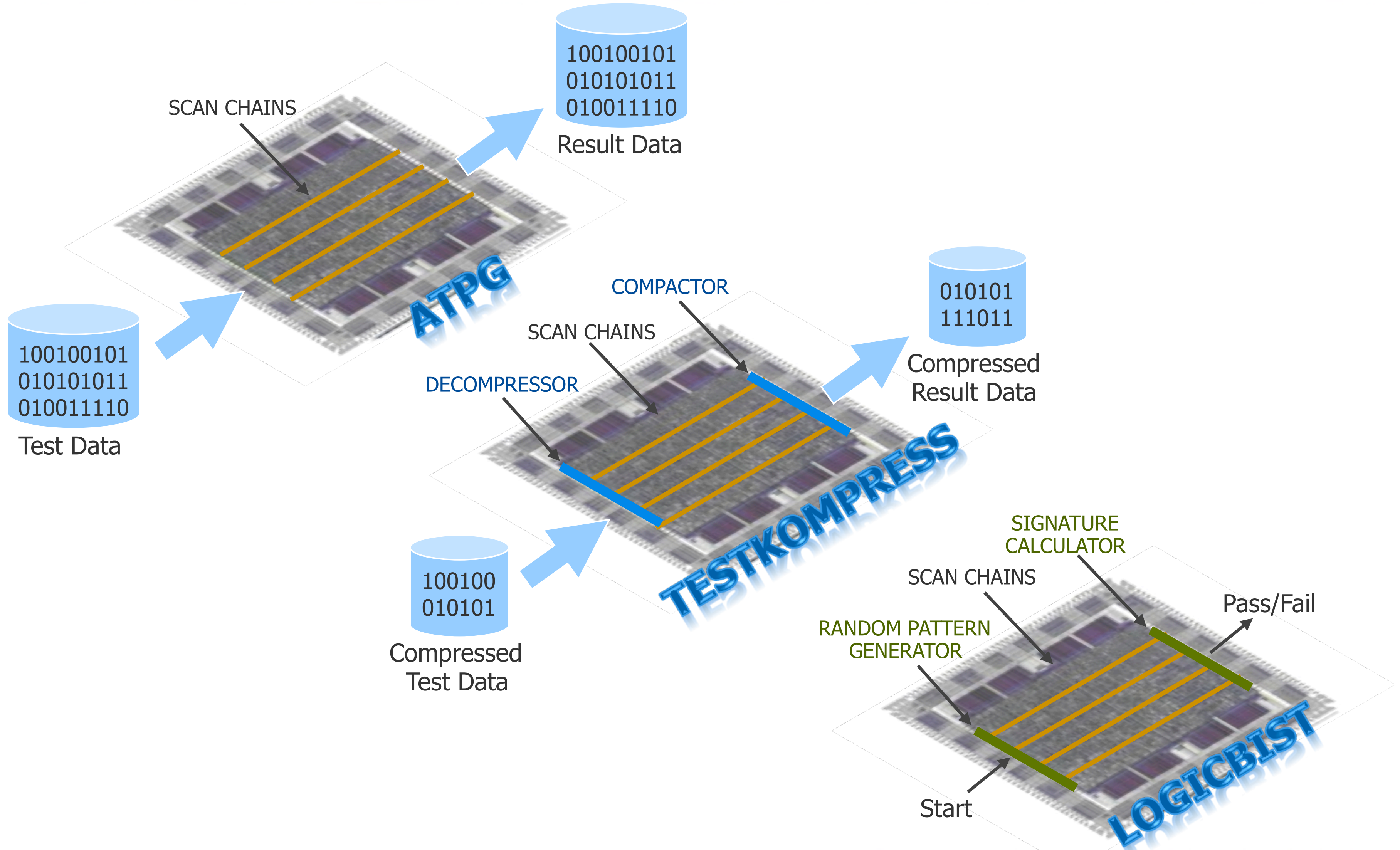
# Logic Test Solutions

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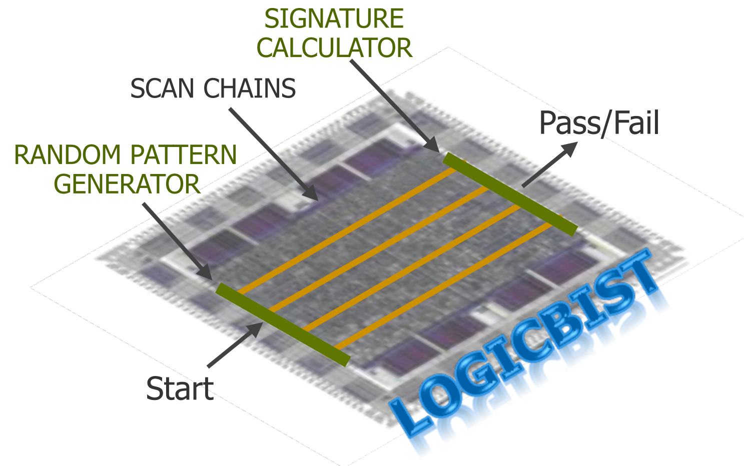
# Logic BIST Overview




- On-chip random pattern generator (PRPG) creates test patterns on the fly
- On-chip signature calculator (MISR) accumulates all response data into single pass/fail signature
- Uses same scan architecture as ATPG
- Eliminates the need for stored patterns
  - Not limited by tester memory or clock speed
- Perfect for test reuse and in-system test applications
  - Addresses mil-aero, medical and automotive POR test requirements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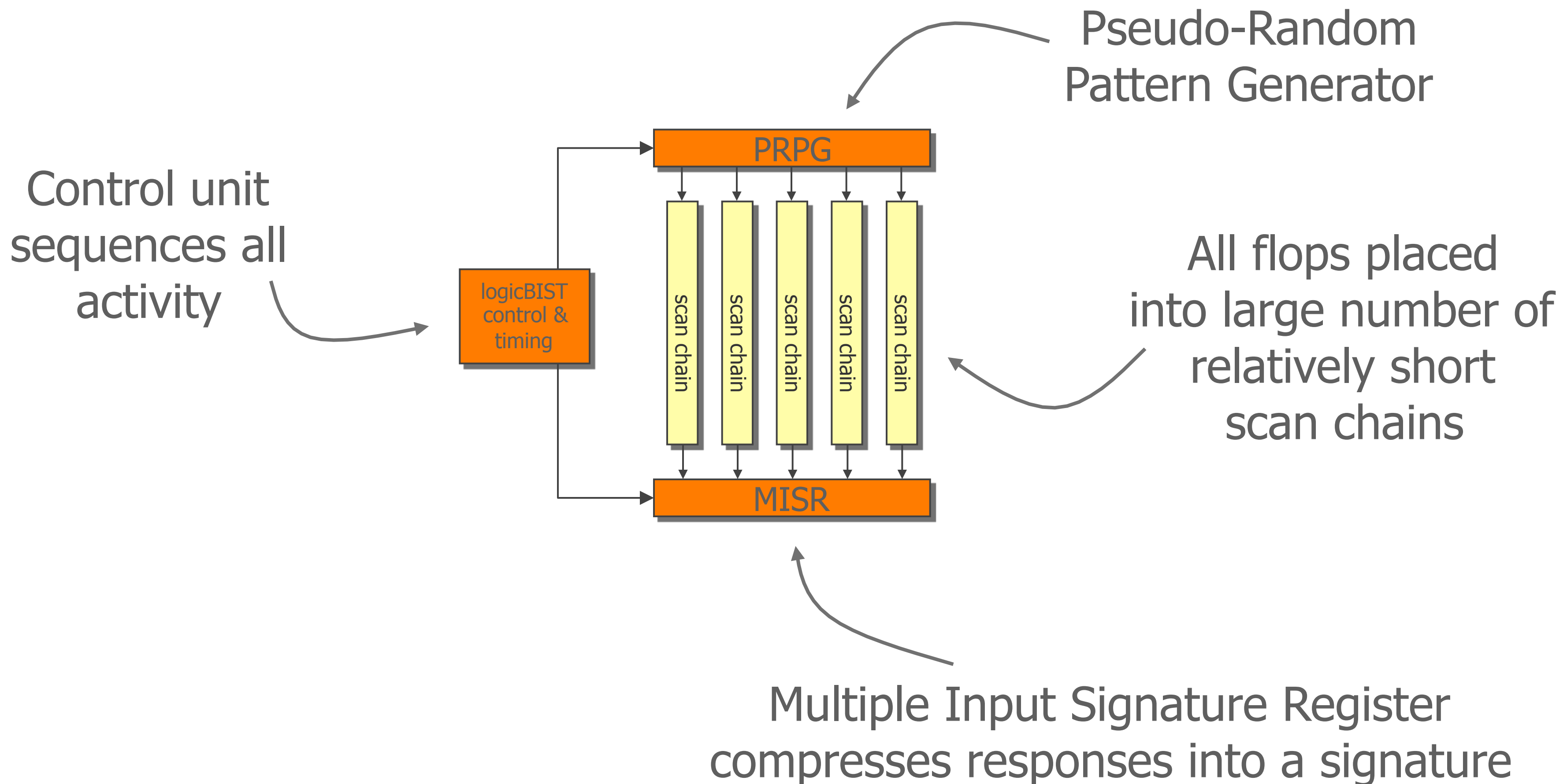
# Logic BIST –
# Basic Architecture

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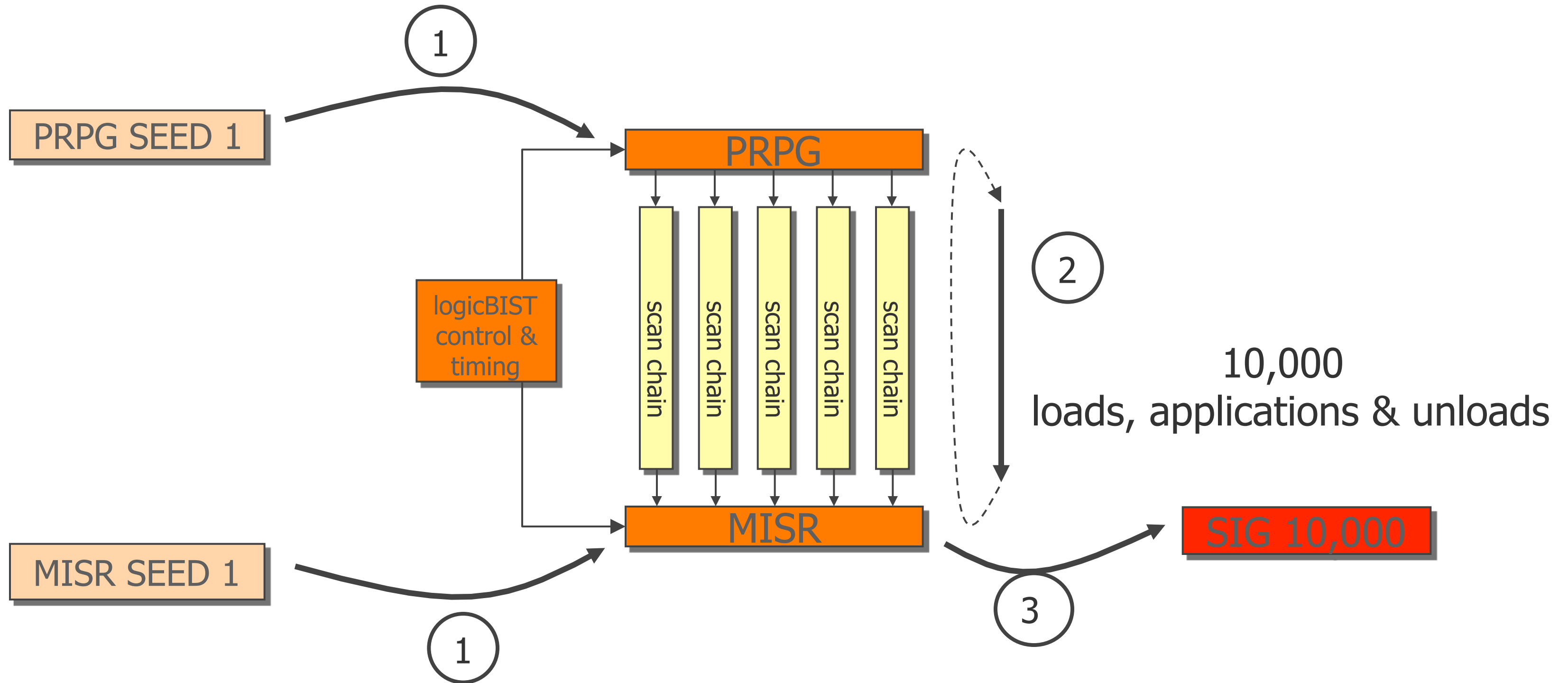
# Logic BIST –
# Test Sequence





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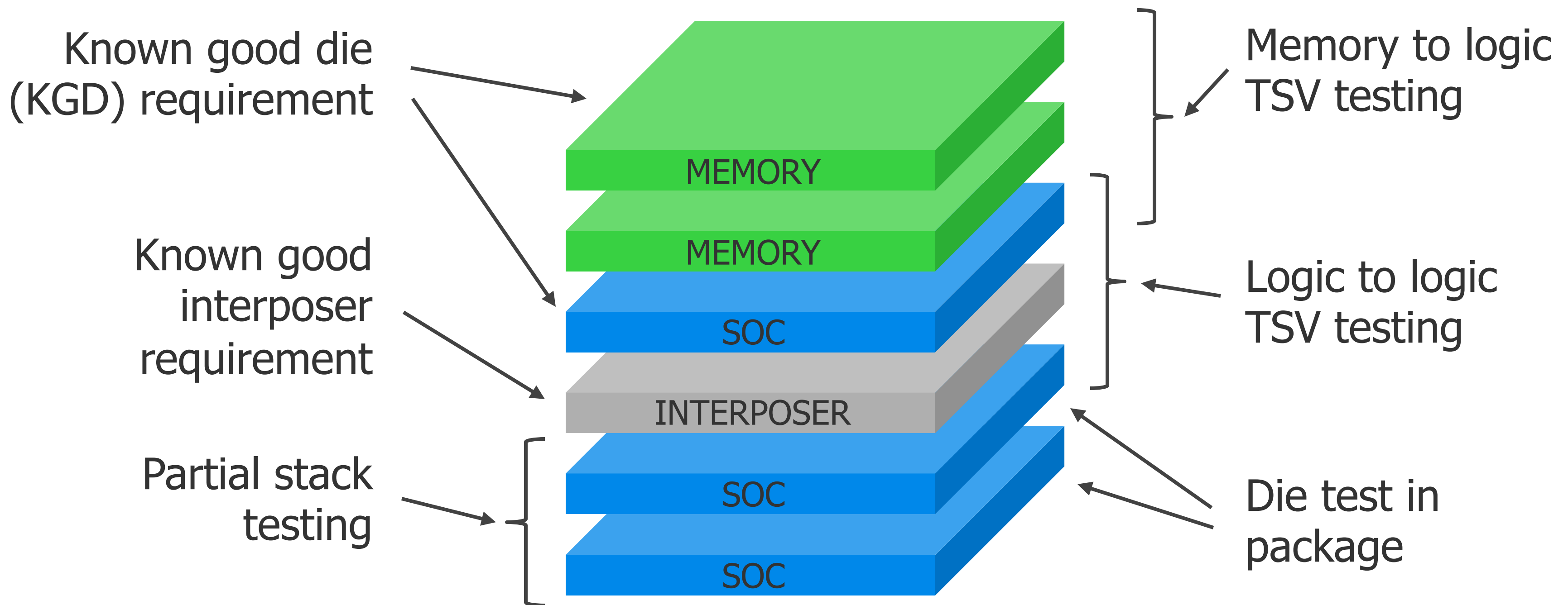
# 3D-IC TEST

# 3D IC Test Challenges

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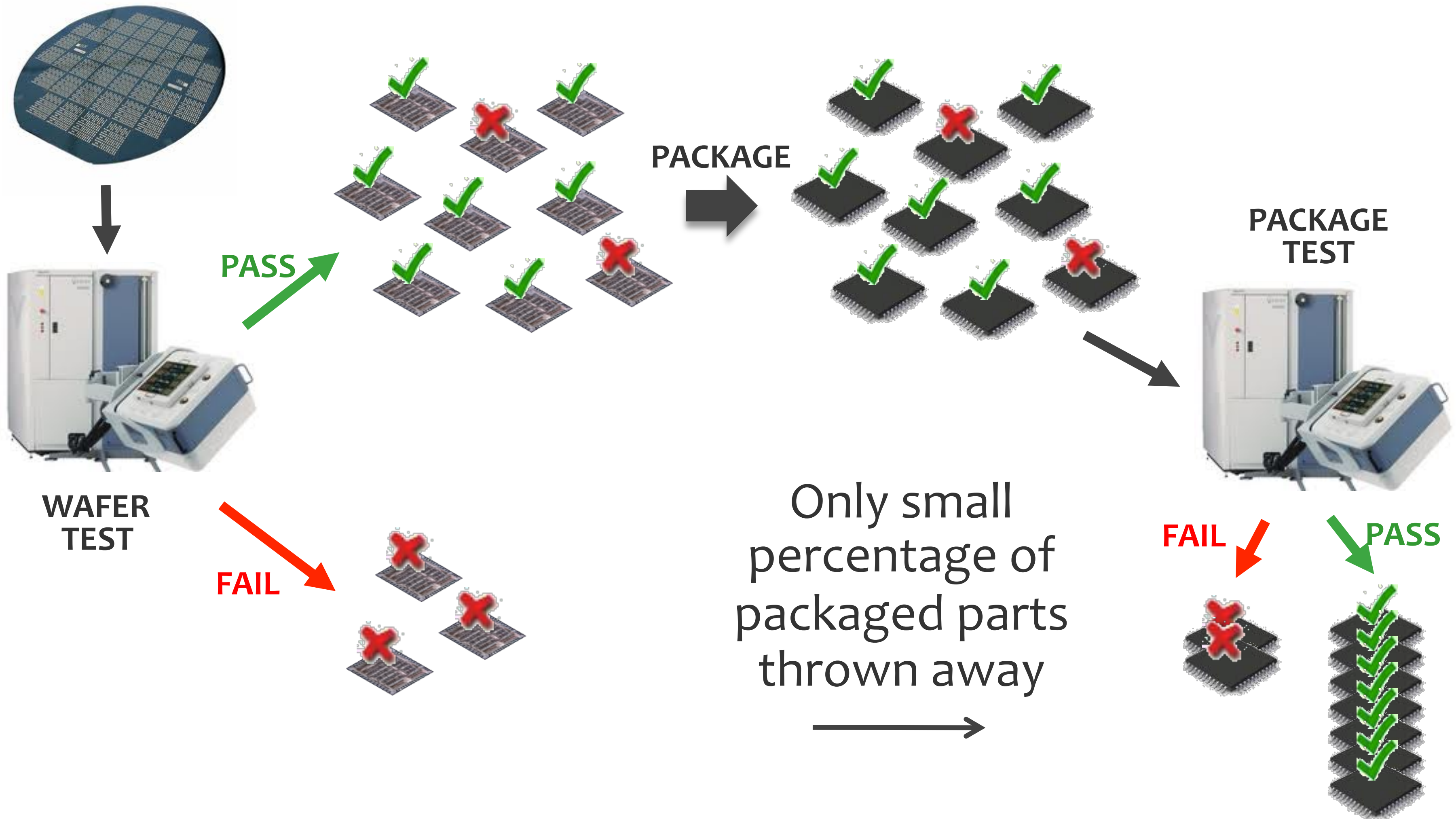
ENSURING
KNOWN GOOD DIE

# Wafer vs Package Test – Before 3D





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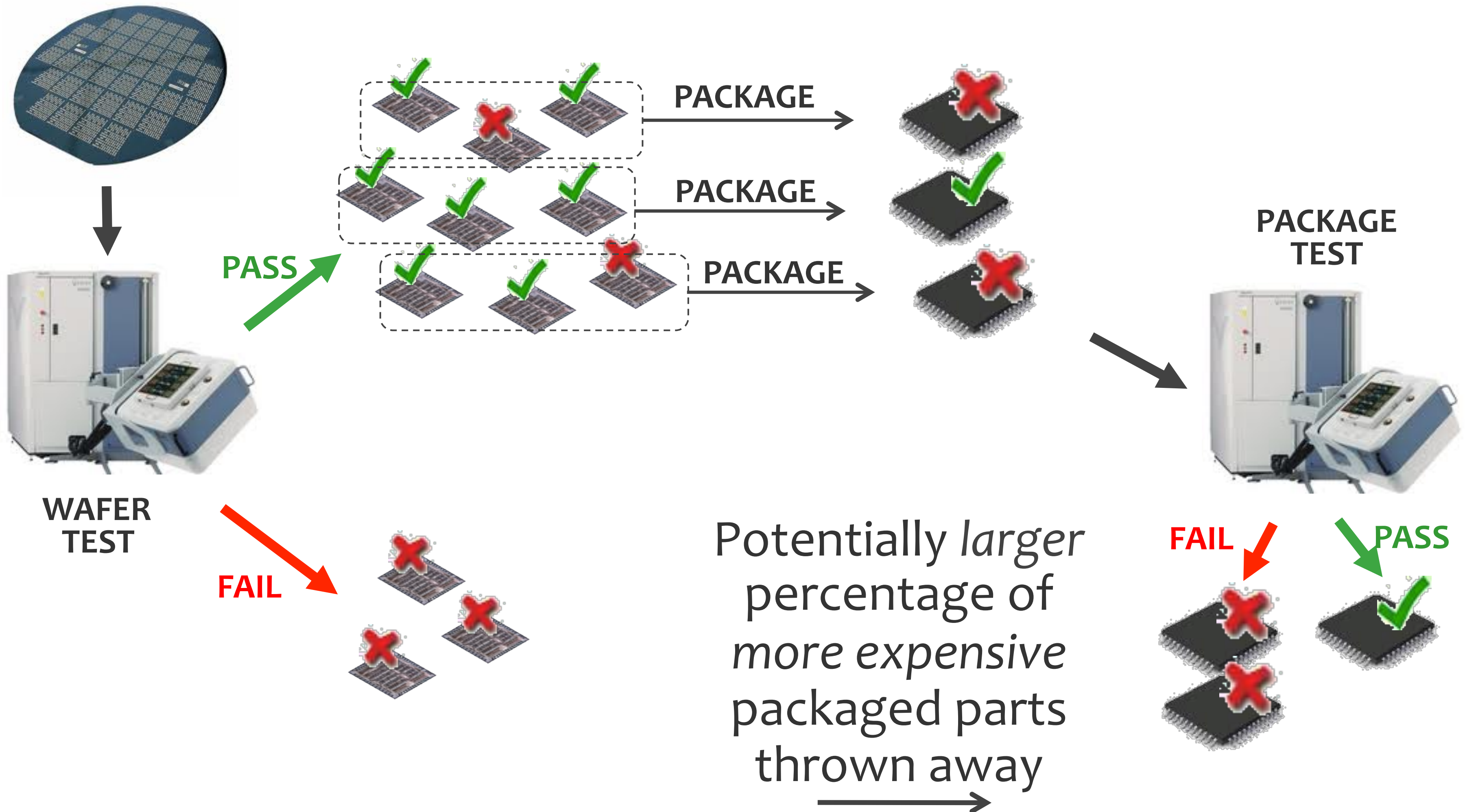
# Wafer vs Package Test – With 3D

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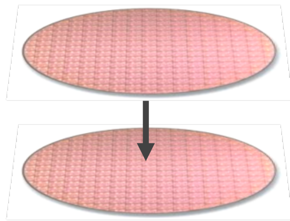
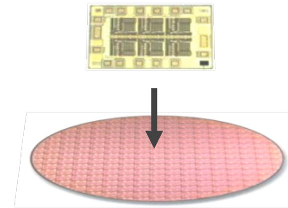
# Stacking Approaches

| Wafer-to-wafer (W2W) Bonding | Die-to-wafer (D2W) Bonding |
| --- | --- |
|  |  |
| Works only with homogeneous die | Necessary for heterogeneous stacked die |
| Very difficult to control individual stack yield | Stack yield controlled with KGD and partial stack testing |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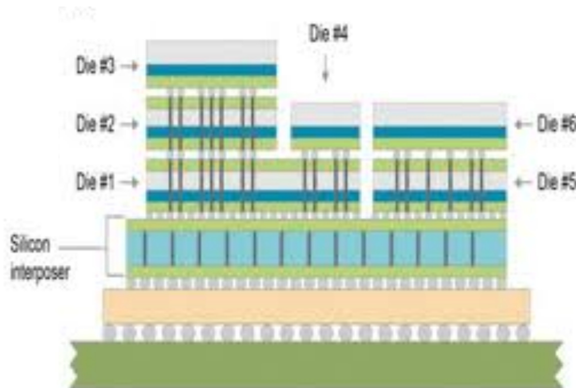
# Known Good Die Requirement

Die Defect Coverage
=
$DC_D$

Final Package Yield
=
$\Pi\ DC_{Di}$

Bare die
Low Cost




3D Stack
High Cost

… For 10 Die Stack:

| $DC_D$ | $\Pi\ DC_{Di}$ |
|---|---|
| 90% | 35% |
| 95% | 60% |
| 99% | 90% |
| 99.9% | 99% |

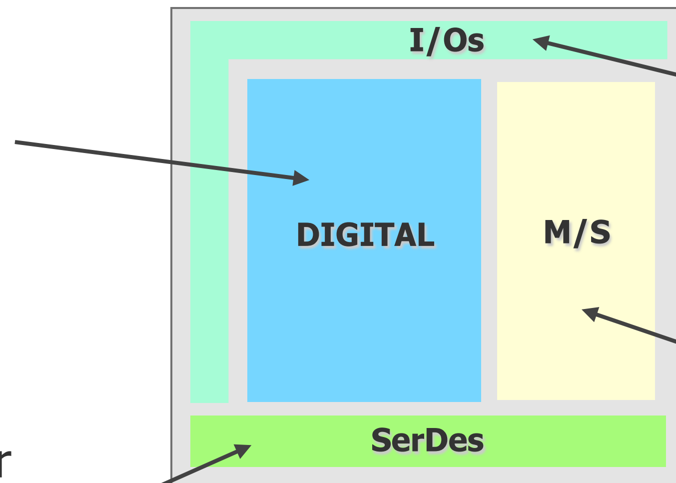
Still 10 times more wasted packages and test time

# Known Good Die Requirement

Need comprehensive wafer test coverage

High coverage of multiple fault models
Stuck-at, TDF, N-Detect, Cell-Aware, …

Contactless performance test
Leakage, delay testing, …




At least basic coverage of common functions
PLLs, ADC/DAC, filters, …

Contactless parameter measurement
Jitter, sampling instant, BER, …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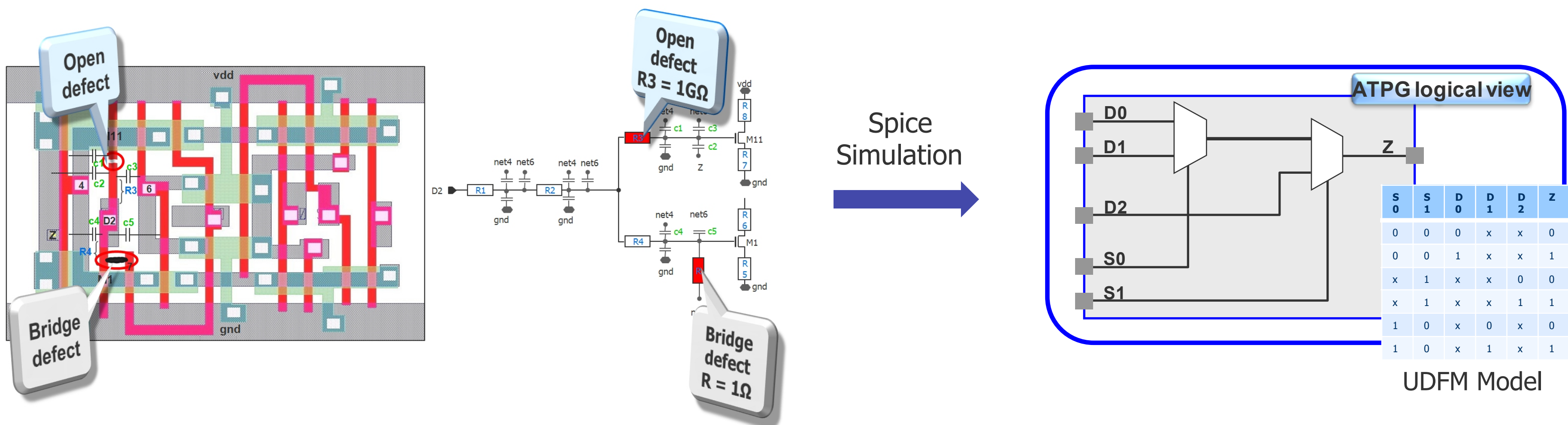
# High Logic Defect Coverage
## Transistor Level (Cell-Aware) ATPG

Methodology for improving detection of defects internal to standard cells

- Layout defects mapped to transistor faults
- Spice simulation maps fault effects to UDFM model
  - UDFM is generalized truth-table based fault representation
- ATPG engine enhanced to target UDFM-based faults




| S0 | S1 | D0 | D1 | D2 | Z |
|---|---|---|---|---|---|
| 0 | 0 | 0 | x | x | 0 |
| 0 | 0 | 1 | x | x | 1 |
| x | 1 | x | x | 0 | 0 |
| x | 1 | x | x | 1 | 1 |
| 1 | 0 | x | 0 | x | 0 |
| 1 | 0 | x | 1 | x | 1 |

UDFM Model

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# Cell-Aware ATPG
## *Silicon Results - 32nm experiment*

The methodology has demonstrated an ability to target otherwise uncovered and hard-to-get-to defect sites

| Pattern Type | #fails | DPM |
|---|---|---|
| Cell-aware slow speed | 98 | 218 |
| Cell-aware at-speed | 268 | 597 |

Results from 400k tested ICs

*Data source: AMD presentation at Mentor's ITC Theater 2011*

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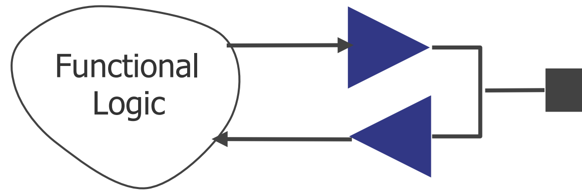
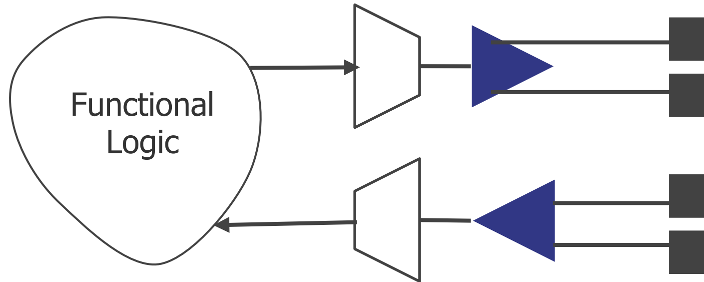
# KGD IO Test Requirements

Regular IO



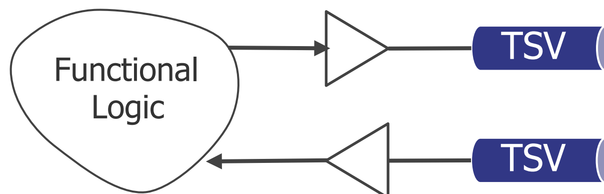

Structural, performance and leakage test of drivers and receivers

SerDes IO




Accurate measurement of performance parameters (Jitter, duty cycle, slew rate, etc)

Pre-Bond TSV




Structural and performance test of partial logic

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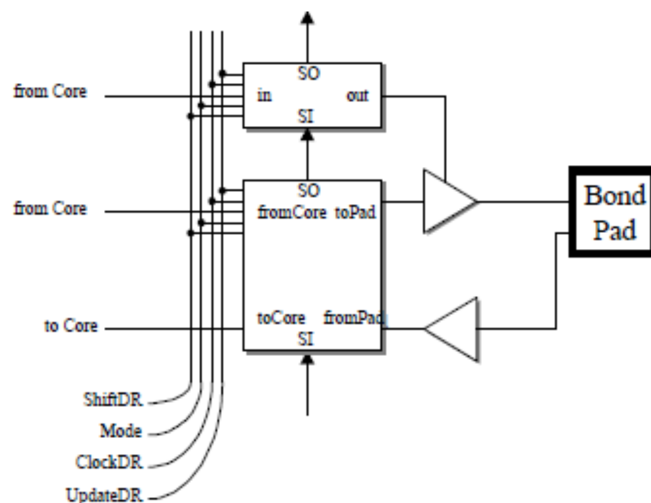
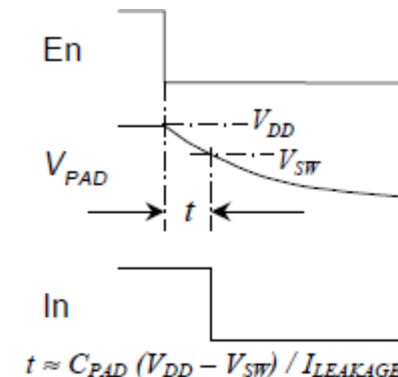
# Contactless Test of Regular IO
## Boundary Scan Based Solutions

- Test for structural I/O defects using wrap test approach
  - Standard Bidi Bscan cell used to drive and capture data
- Measure/test IIL, IIH, and inter-pin leakage without contacting bond pads on any tester
  - IIH test procedure
    - Drive pads to logic 1
    - Disable drivers – leakage current affects $V_{PAD}$
    - Capture pad logic values precise time later

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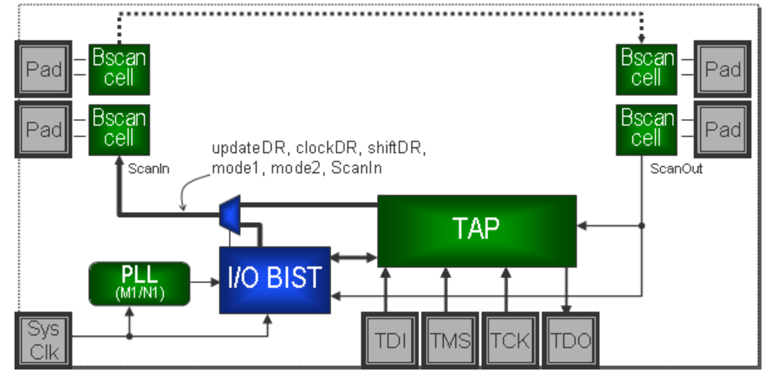
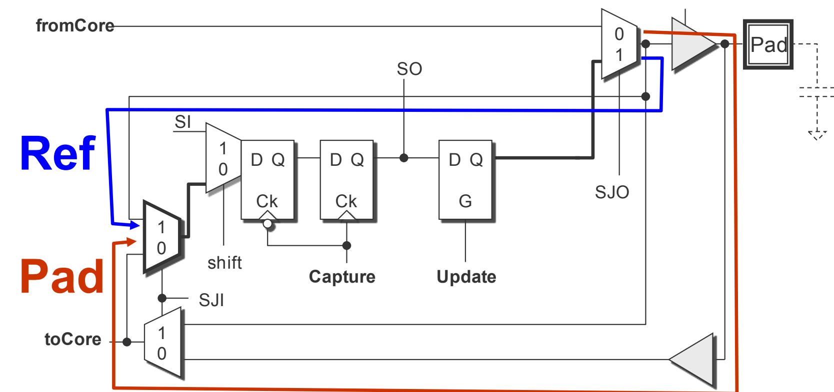
# Contactless Test of Regular IO
## IO BIST

- Propagation delay measurement using Bscan
- BIST provides high-speed Bscan control signals
- Delay-difference measurement eliminates signal propagation variations and noise
- Rise and fall delay measurement with resolution adjustable from nanoseconds to picoseconds

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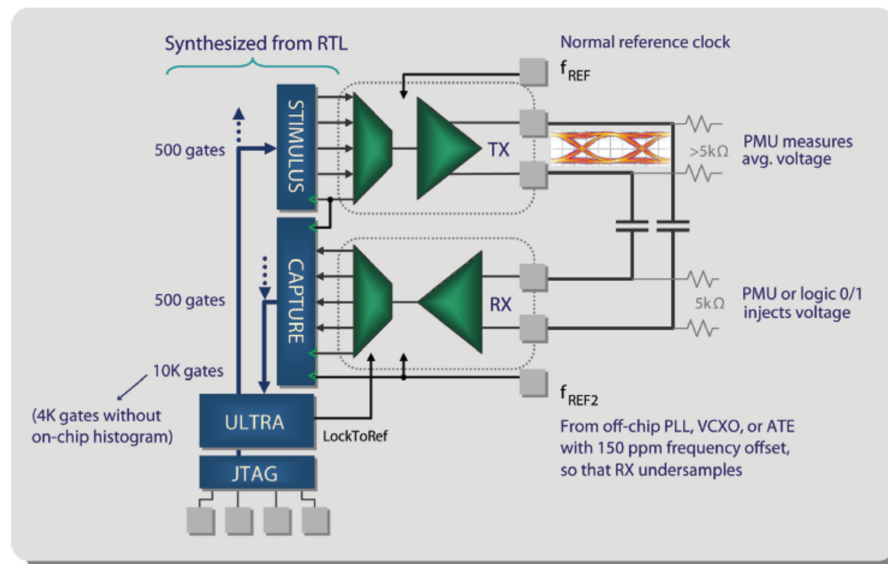
# Contactless Test of SerDes IO
## SerDes BIST

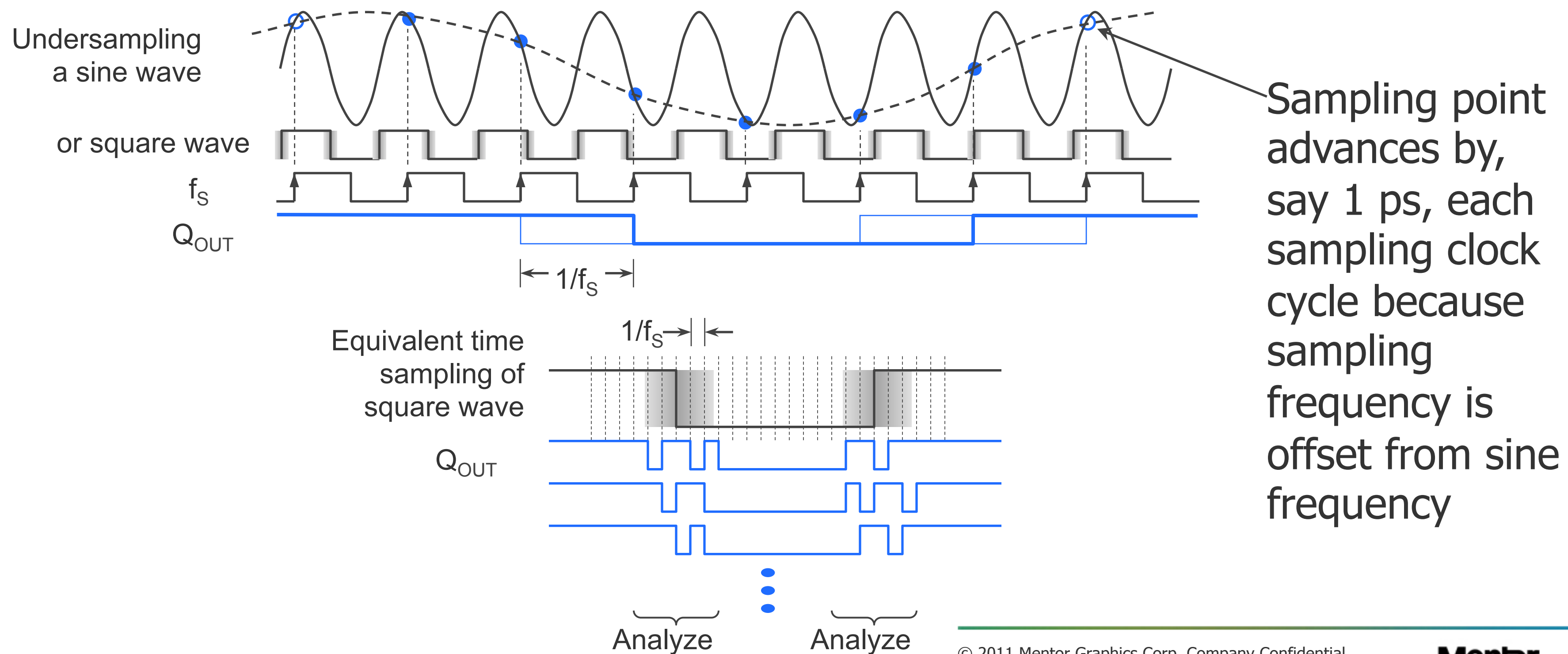
- Accurate picosecond measurements of critical parameters
  - Jitter (Random, Total)
  - Jitter Tolerance
  - Rise/fall time, Slew rate
- RTL-based, vendor independent BIST
- No changes to physical IP under test



# Contactless Test of SerDes IO
## SerDes BIST

### Undersampling-Based Approach

- Samples continuously, but only analyzes transitions
- Measures jitter and phase delays relative to median edge positions
- On-chip capture of histogram or RMS value of HF or LF jitter





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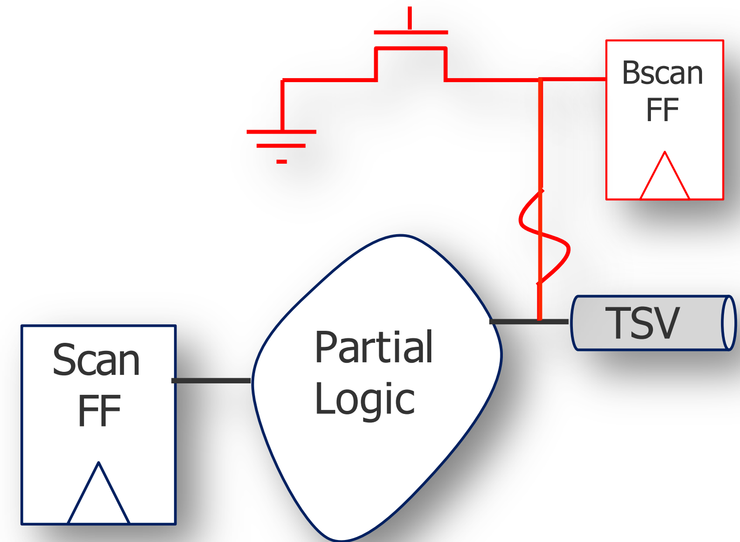
# Contactless Test of Pre-Bond TSVs

- All techniques described for regular IOs can be applied to pre-bond TSVs
  - Boundary Scan based solutions
  - IO BIST
- Extra load may be problematic due to lack of IO driver
  - Fuse can be used to eliminate load after test

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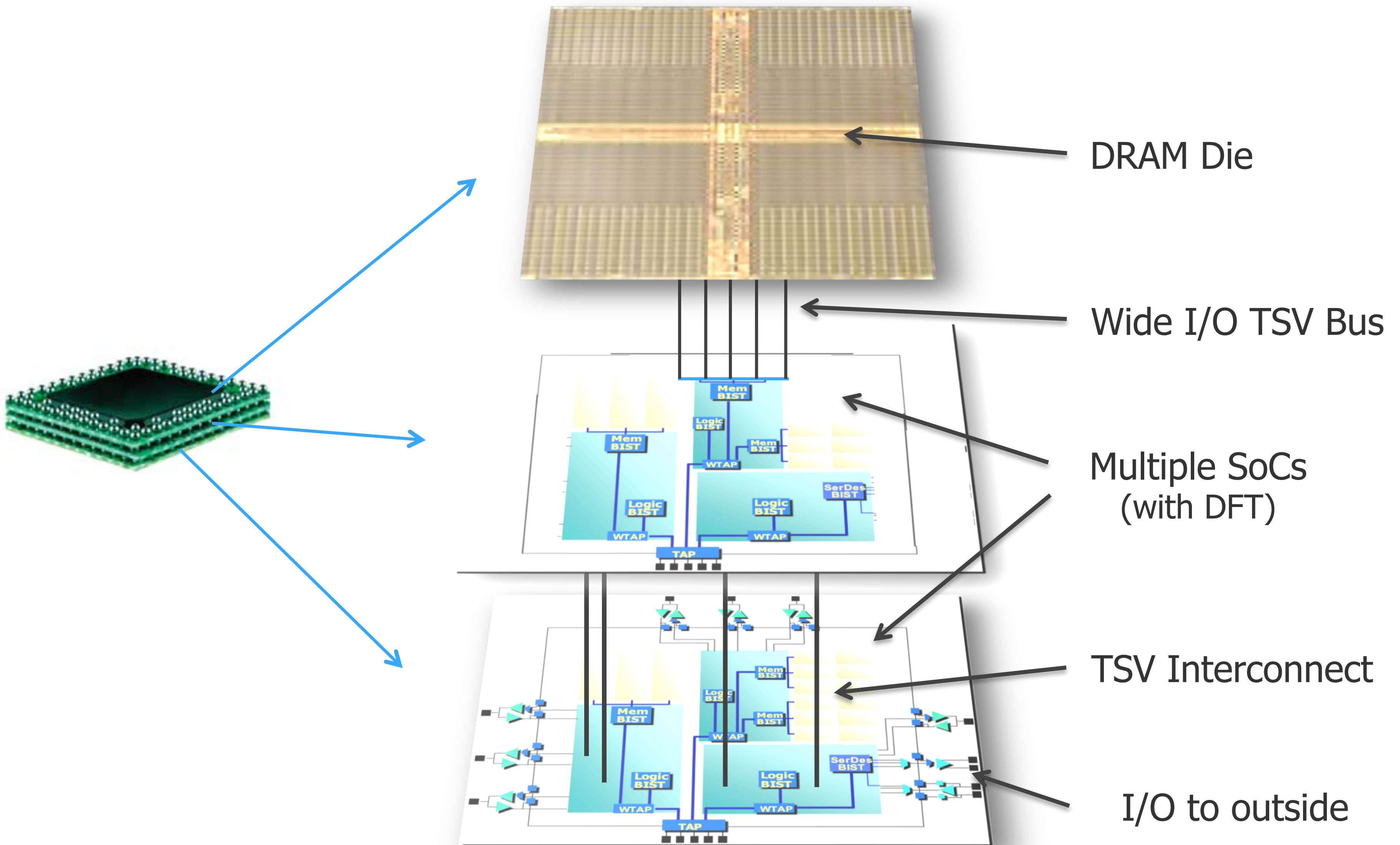
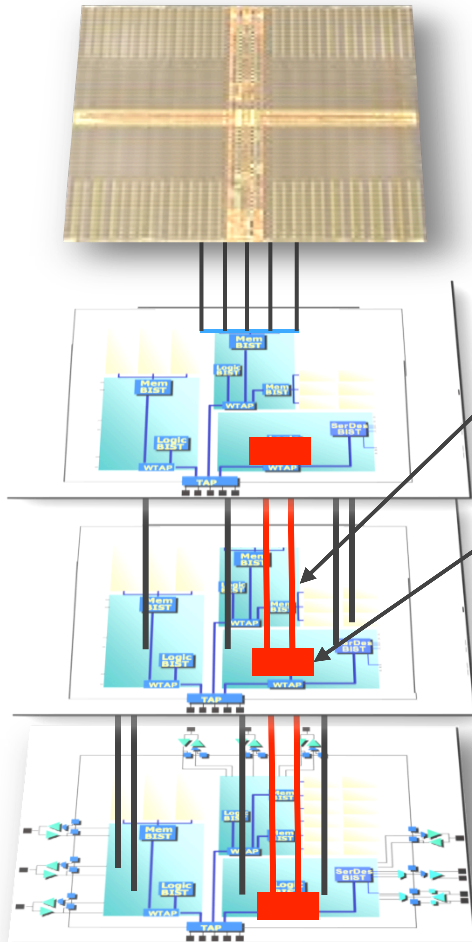
# TEST ACCESS FOR STACKED DIE

# Generic 3D Package Components



# Test Access Within Stack




- Dedicated TSVs used for test signals between die
- Control hardware needed to route test data up and down stack
- Standard architecture necessary to support heterogeneous die from multiple vendors.
  - IEEE P1838 under development



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# Mentor 3D Test Access

- Uses cascaded TAPs
  - Each TAP can be instructed to enable the next higher TAP
- Default is bottom TAP only in path
- Standard structure for die independent of position
- Die can work directly if packaged as a stand-alone device


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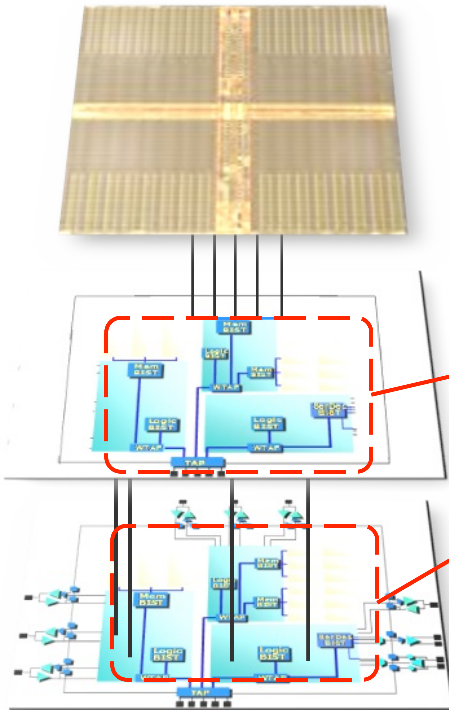
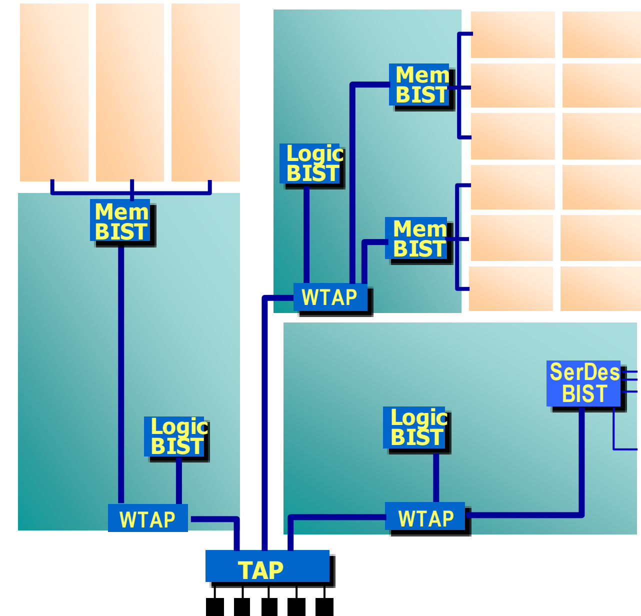
# TESTING DIE WITHIN 3D STACK

# Die Test In-Package






- BIST best suited for re-test of die within stack
  - ATPG patterns can also be used
- Dies can be tested in parallel to minimize test time
- Screens for any new defects due to the packaging process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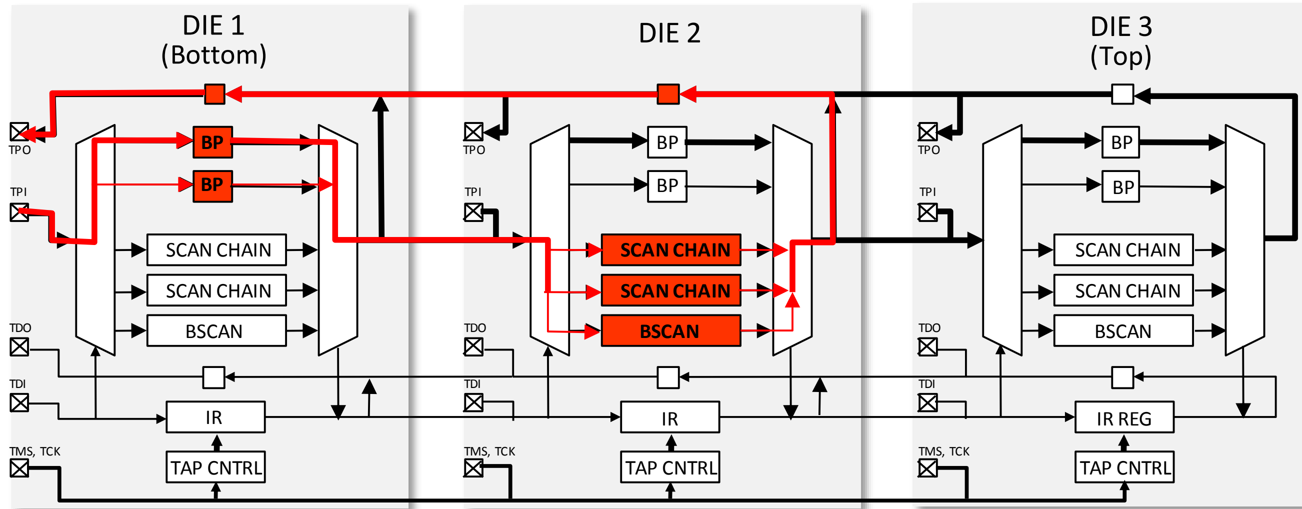
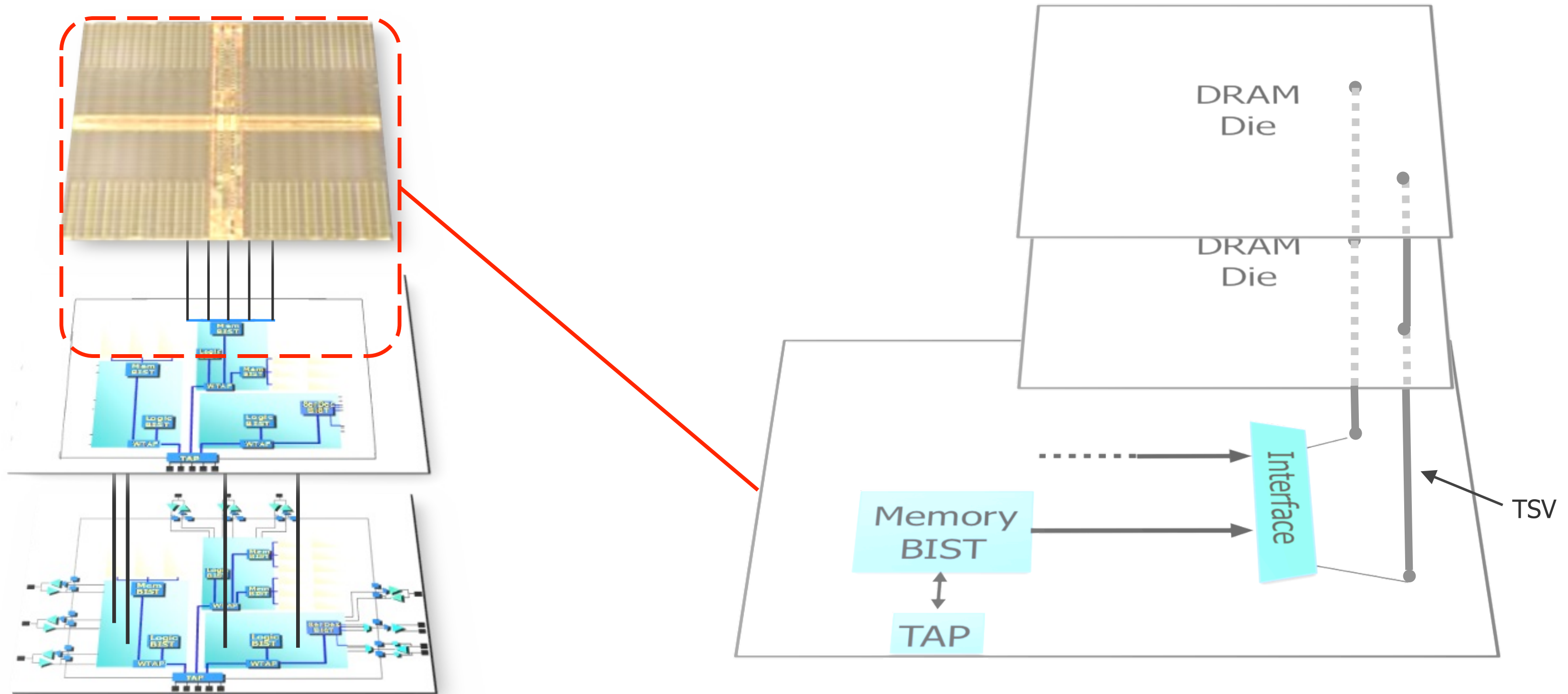
# In-Package ATPG Application




- Options
  - Die-level ATPG patterns generated at package level
    - Full package netlist is used
    - Non-targeted die are grayboxed
  - Die-level ATPG patterns retargeted from wafer level
    - Patterns resequenced in accordance to active bypass stages

# STACKED MEMORY TEST

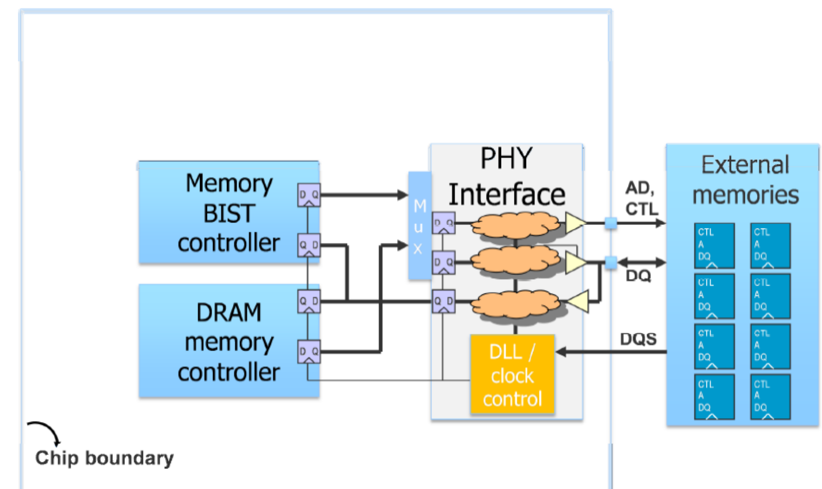
# Stacked Memory Test
## BIST Approach



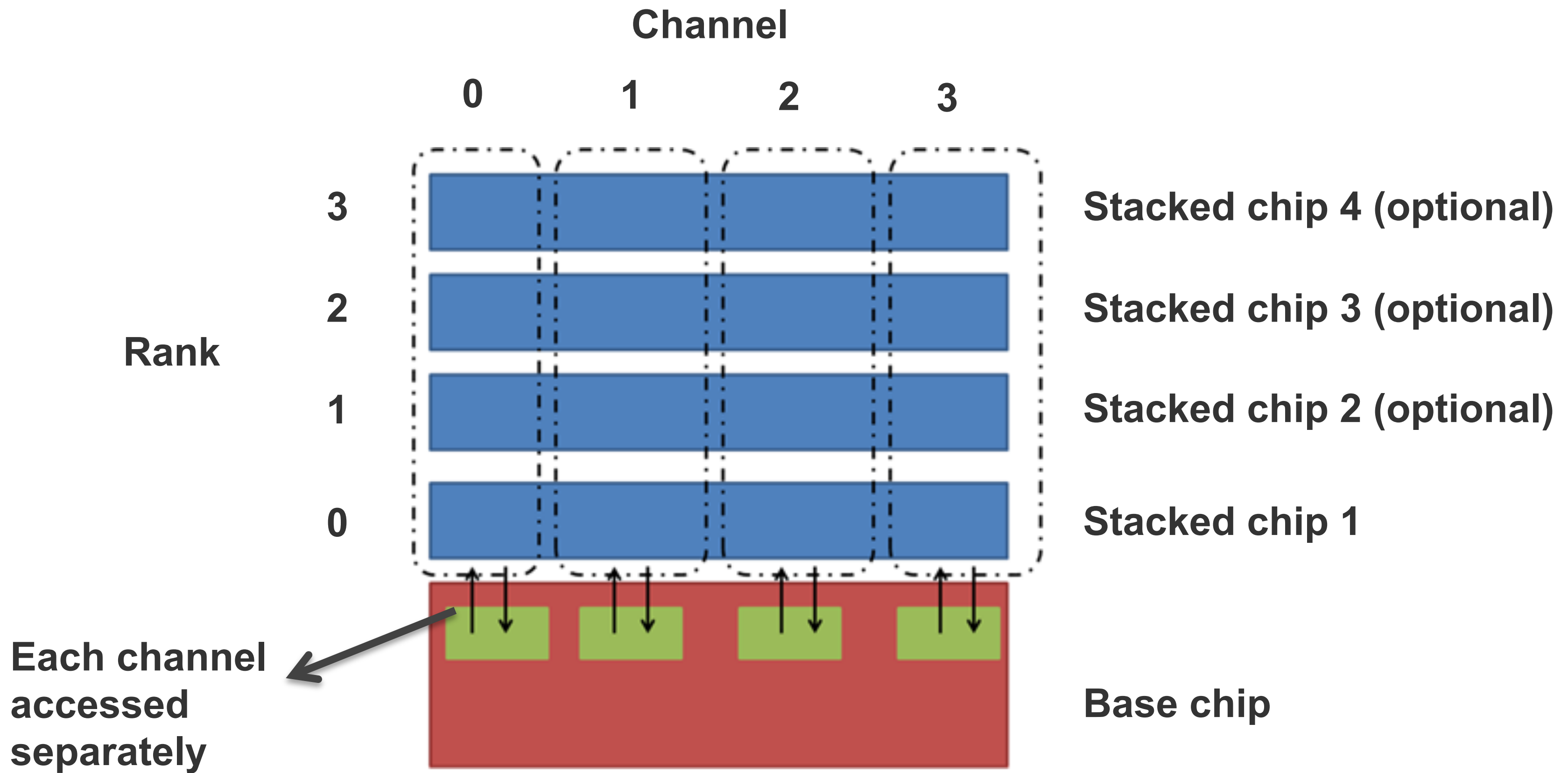

- External Memory BIST added to logic die
  - — Provides full-speed testing of memory die and bus
  - — Bus-only test algorithms can optionally be used
- Post-silicon programmability supports changes in memory die

# Stacked Memory Test
## BIST Approach

- All BIST transactions performed through functional PHY interface
  - Interface handles all signal synchronization
  - Interface also handles mux/demuxing for DDRs
- BIST supports all forms of DRAM access
  - Bursting, Refresh, etc
- BIST highly programmable
  - Address range and read/write operations for supporting different memories
  - Algorithms for different quality and test cost needs
    E.g. Interconnect only coverage
- Supports bussed memories



# Wide IO DRAM Example

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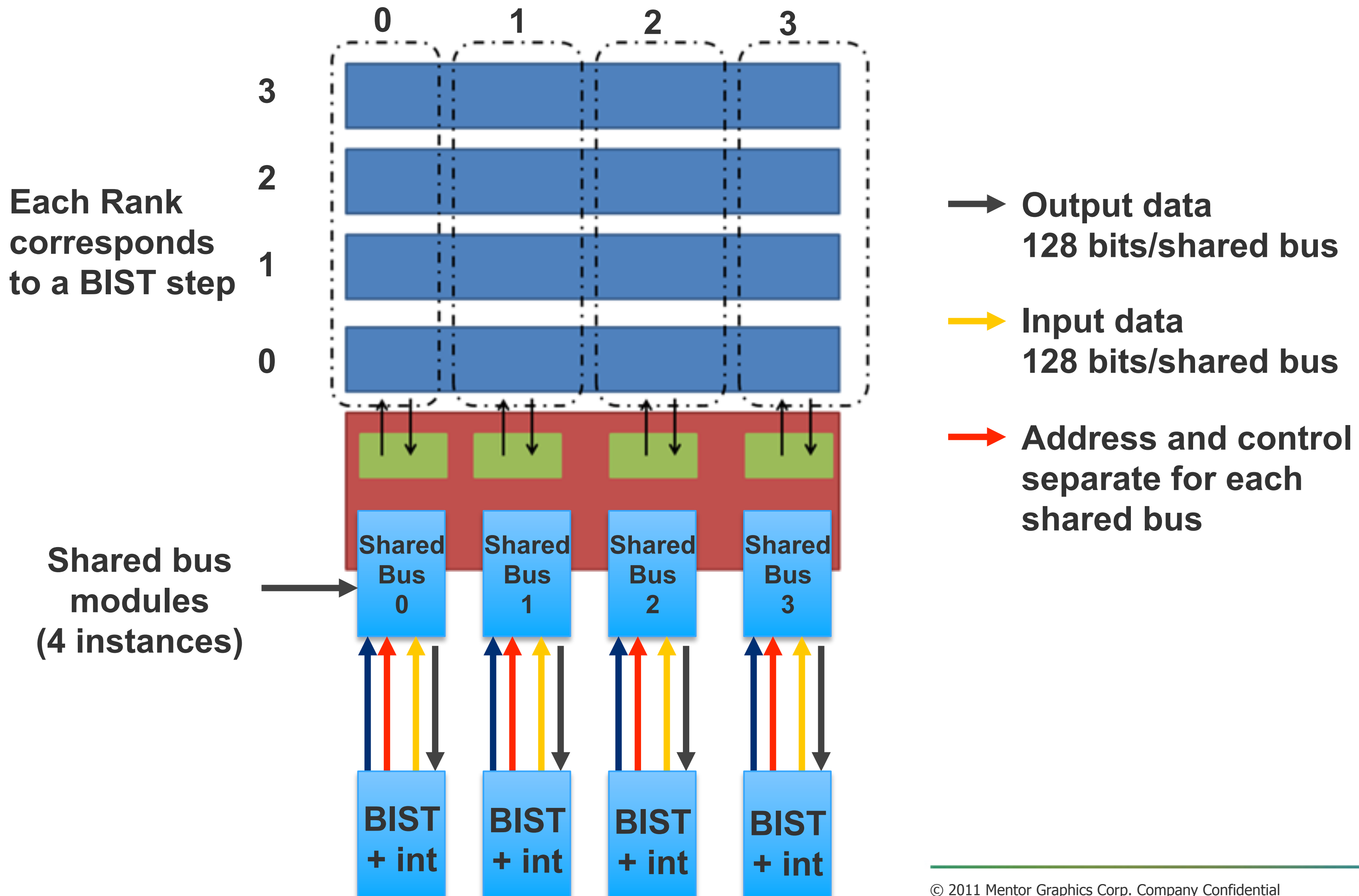
# Wide IO DRAM Example Implementation

## 4 shared buses, 4 DRAMs behind each shared bus, 128-bit bus




Output data
128 bits/shared bus

Input data
128 bits/shared bus

Address and control separate for each shared bus

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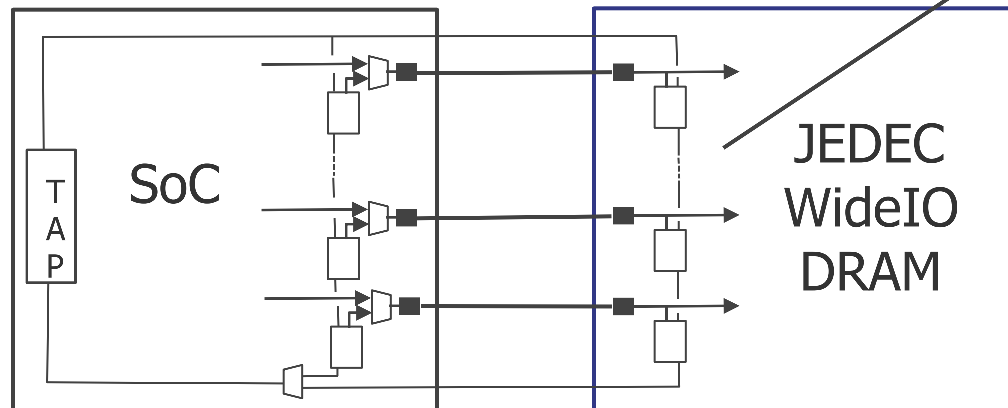
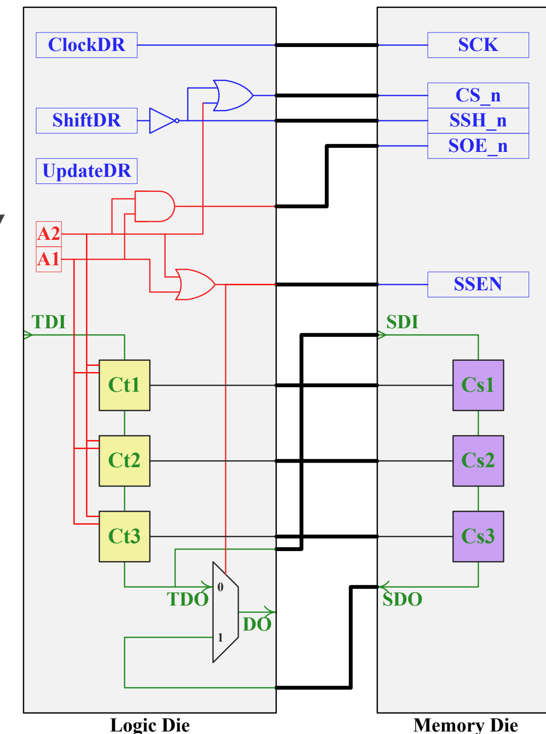
# Stacked Memory Test
## Boundary Scan Approach

- Interconnect test performed using boundary scan
- JEDEC WideIO standard defines bscan chain for DRAM
- Advantages
  - Does not require functional DRAM core for test and diagnosis
- Disadvantages
  - Low speed test might not be sufficient to detect/diagnose parasitic effects
  - Does not support memory re-test

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# STACKED LOGIC TEST

# Logic Die to Logic Die Interconnect Test
## Various Approaches

- Traditional Boundary scan
  - Boundary scan cell placed at each die TSV and IO
  - Interconnect test patterns produced to find shorts or opens
  - Test operation based on standard boundary scan board test approach
  - Limitation: does not support at-speed test of TSV connections
- Pulse-Vanishing
- Hierarchical ATPG Approach


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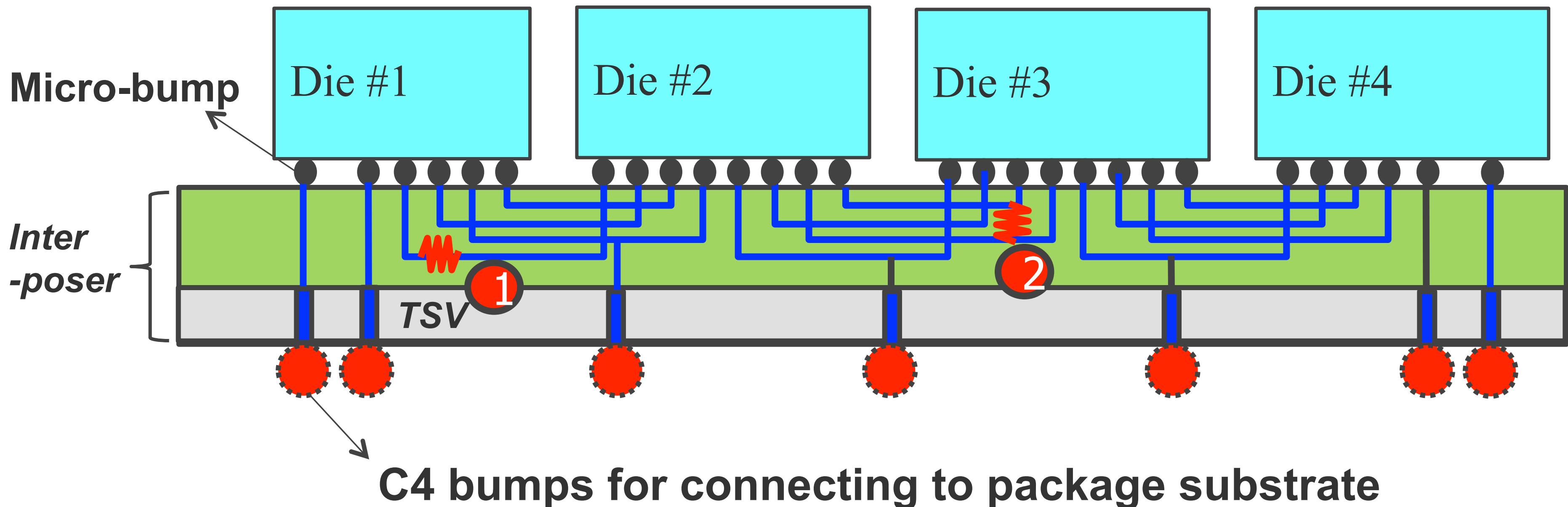
# Pulse-Vanishing Approach
## Targeted Faults in an Interposer

(1) **Parametric Open Fault** in an interposer wire 1
(2) **Parametric Bridging Fault** between two interposer wires 2





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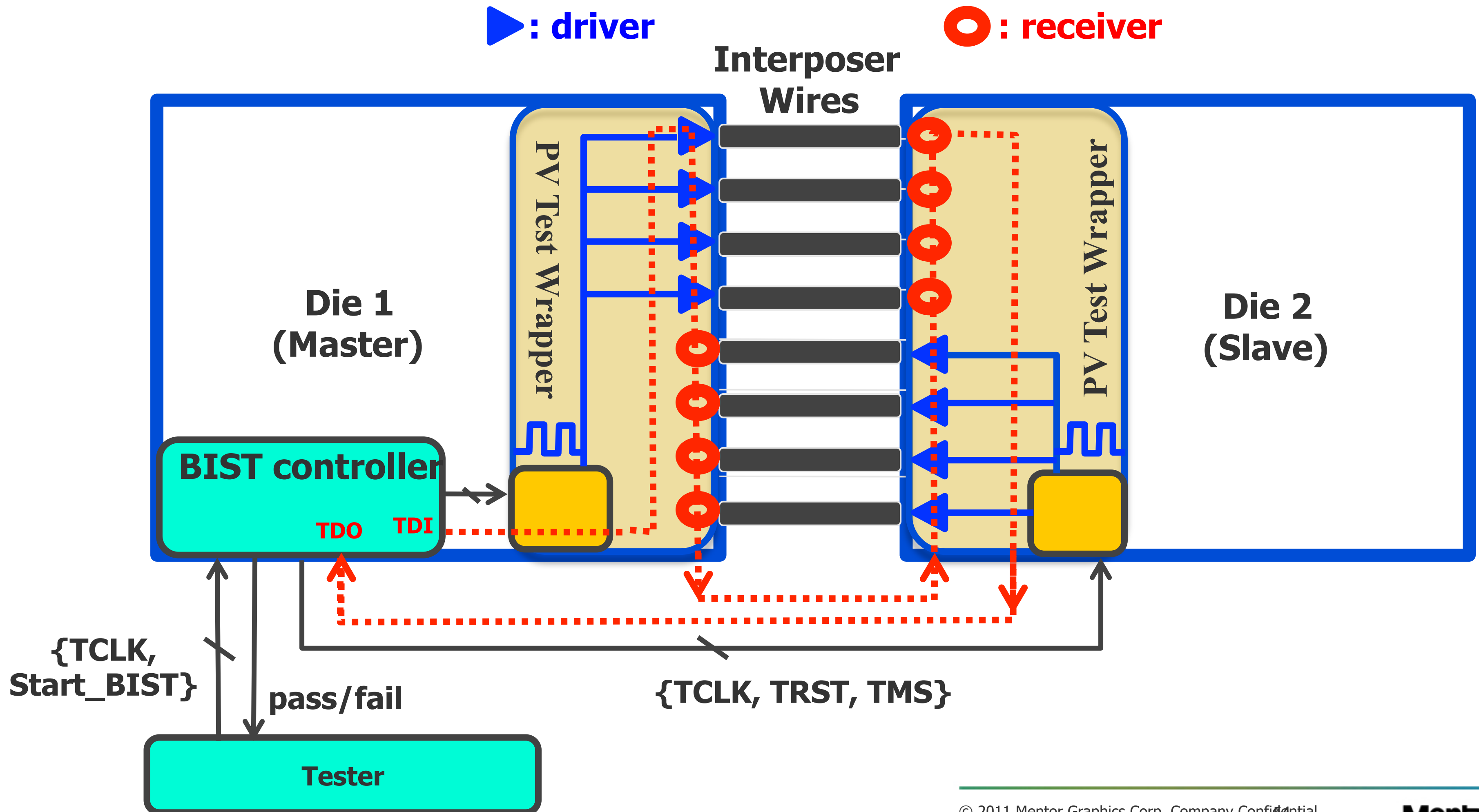
# Boundary-Scan Based Architecture

## The proposed test methods can be built on top of the IEEE-1149.1

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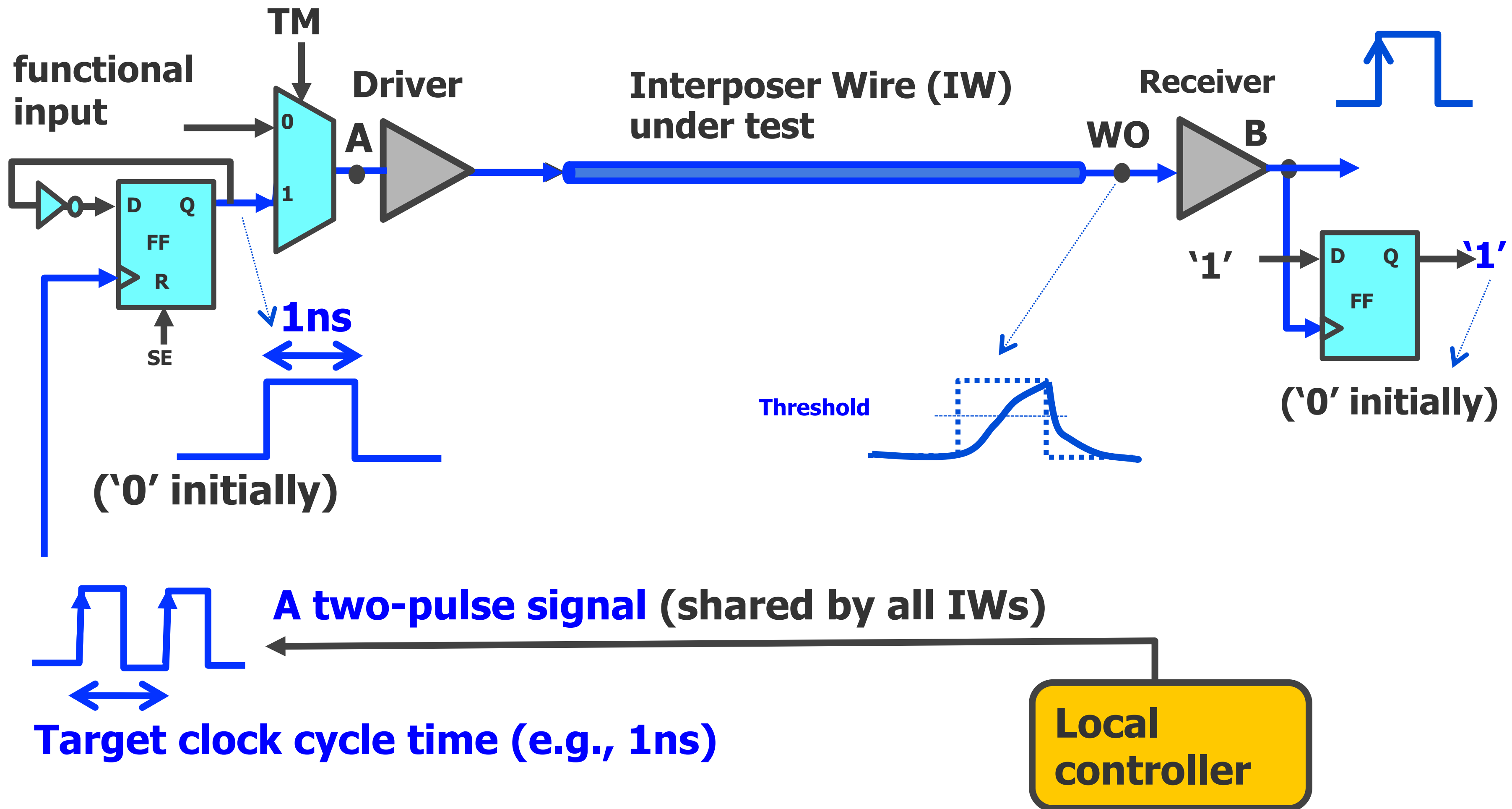
# Concept of Pulse-Vanishing Test





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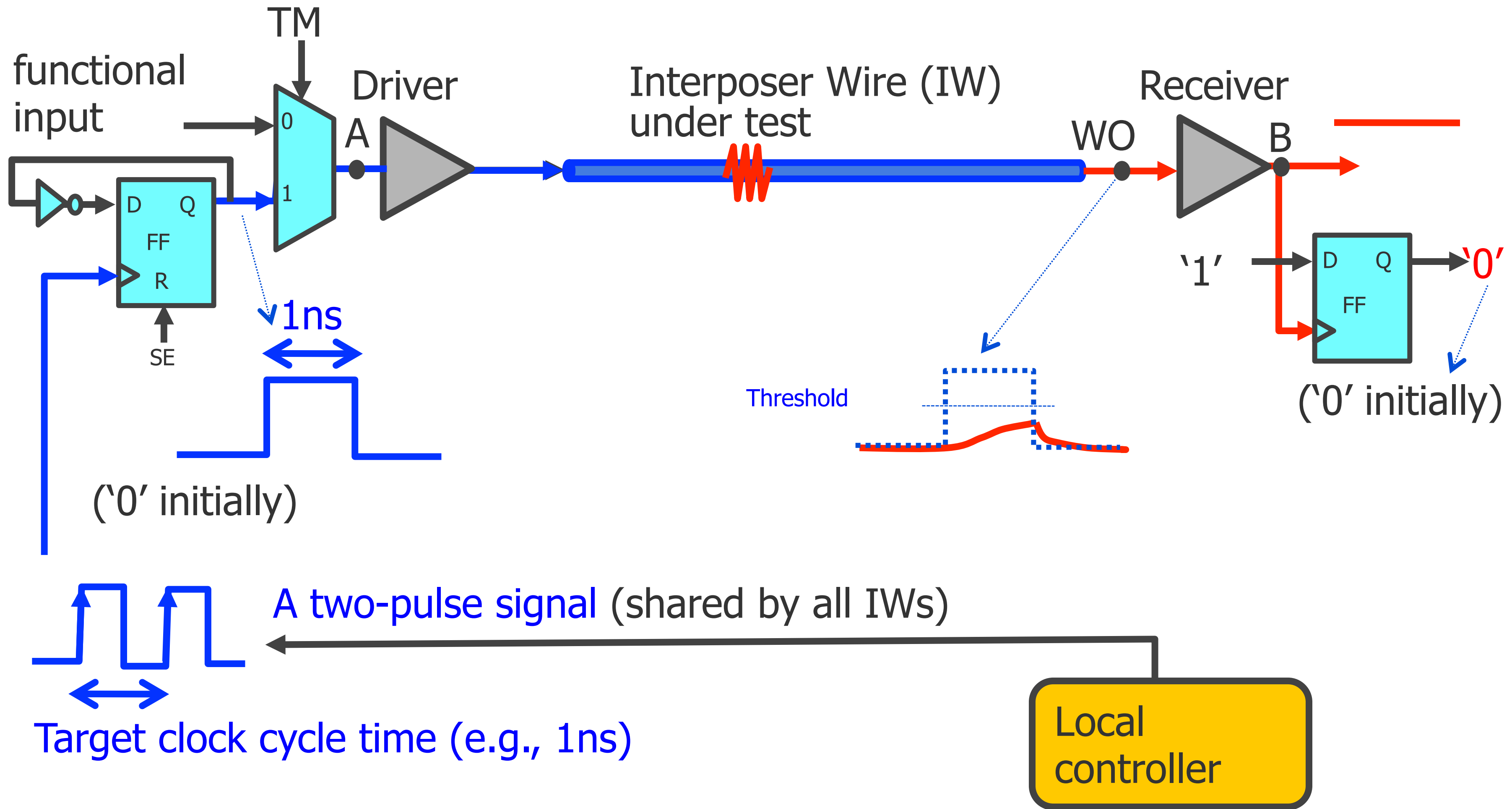
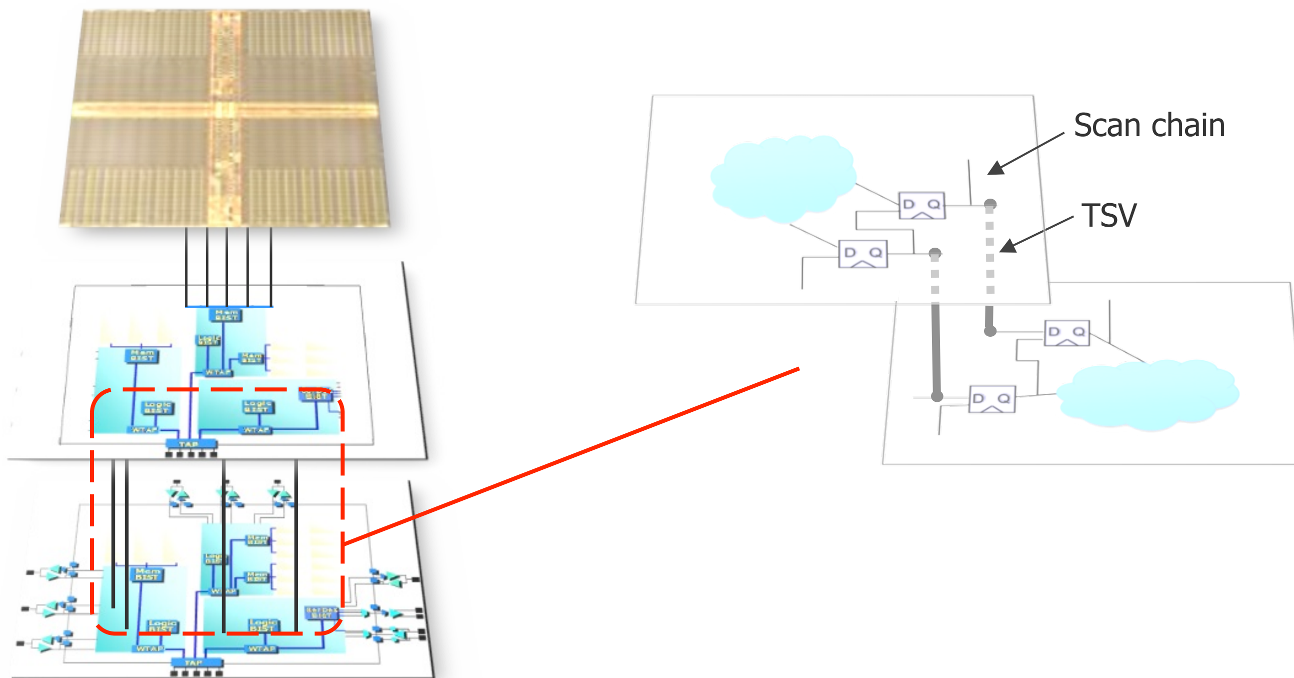
# When There is a Delay Fault…



# Logic-to-Logic TSV Interconnect Test
# Hierarchical ATPG Approach




- Approach based on TSVs between scan-isolated cores
- Hierarchical ATPG tests signals between cores
- Cores on neighboring die conceptually the same

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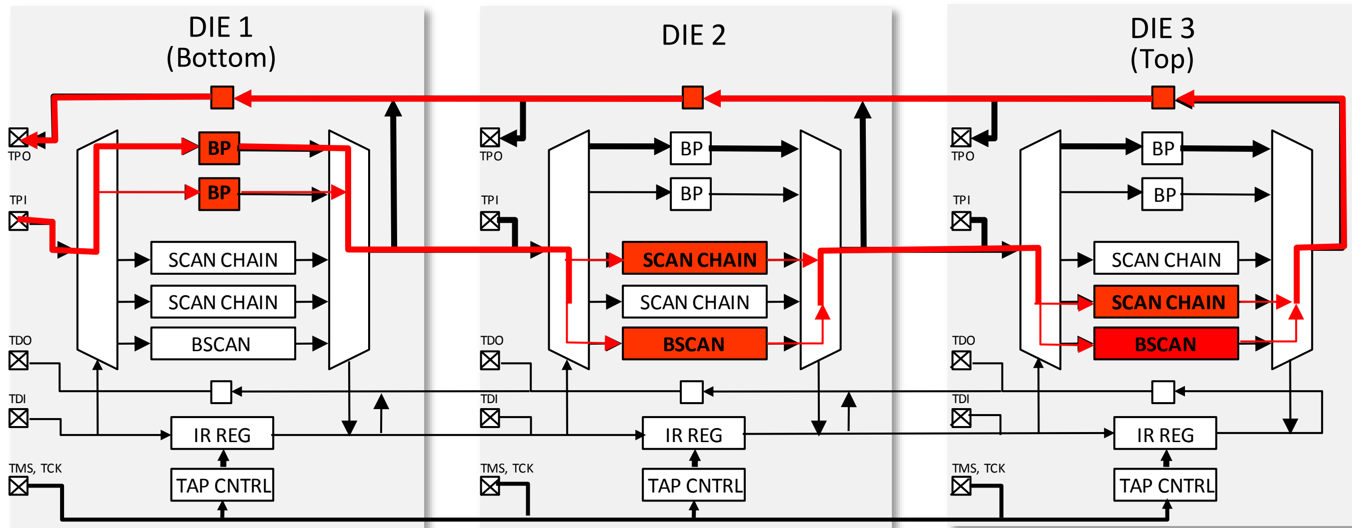
# Logic TSV Test Pattern Generation




- TSV test patterns applied using scan chains in two or more die
- ATPG engine generates patterns using full package netlist
  - Non-targeted die and/or cores are grayboxed
- Only ATPG is supported
  - BIST and Compression can not easily be extended across multiple die
  - Less critical as TSV test set should be relatively small

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# Summary

- 3D-ICs introduce new test challenges and requirements
- Critical test solution components include
  - Known-Good-die test
  - Standardized TSV-based test access to die in stack
  - Programmable BIST for stacked memory die
  - Scan based testing of logic-to-logic TSV connections


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