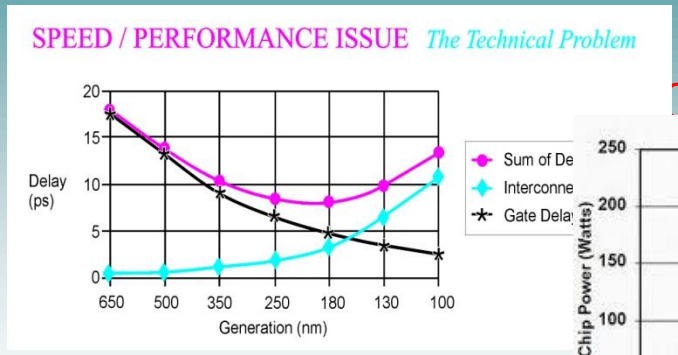
3D Integration:

New Opportunities for Speed, Power and Performance

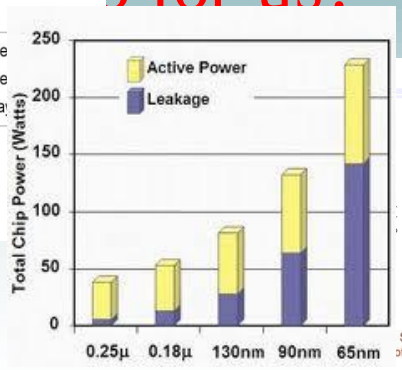
Robert Patti, CTO

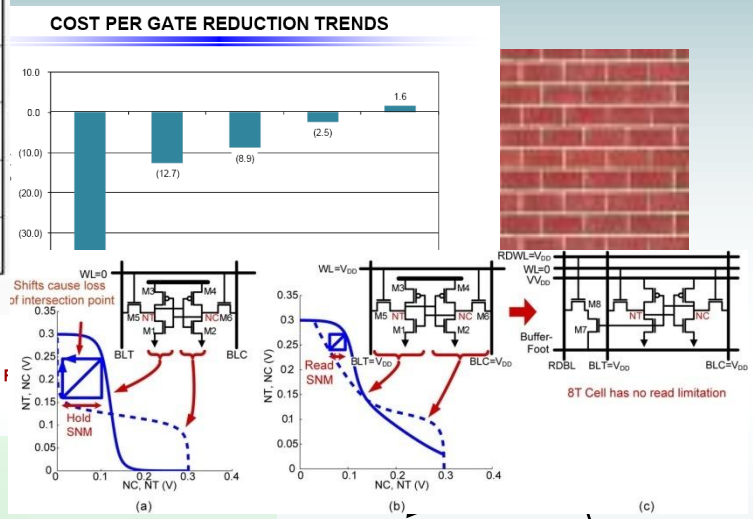
rpatti@tezzaron.com

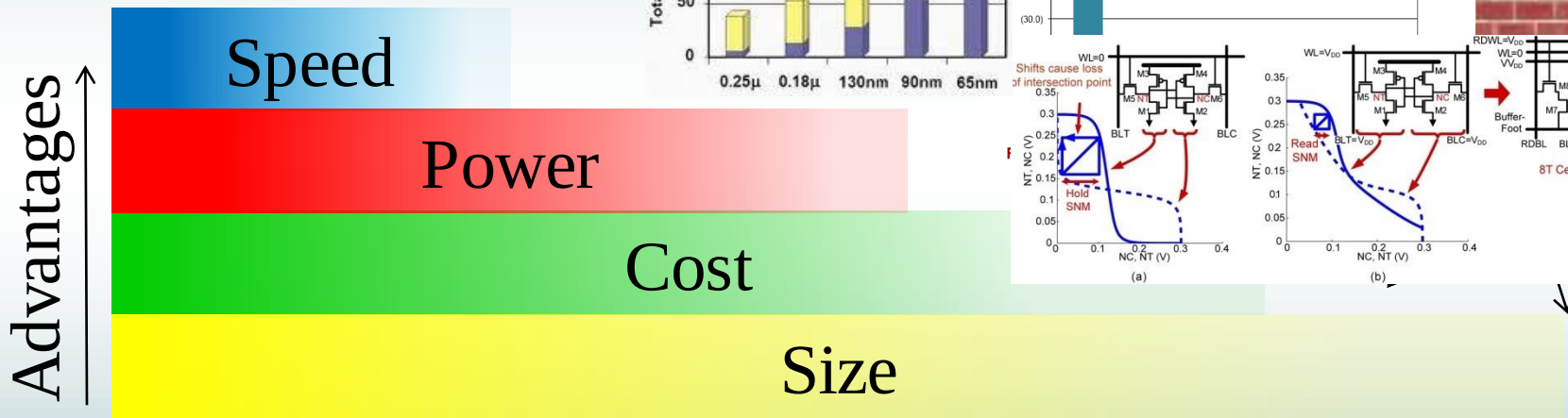
Why We Scale?



p for us?

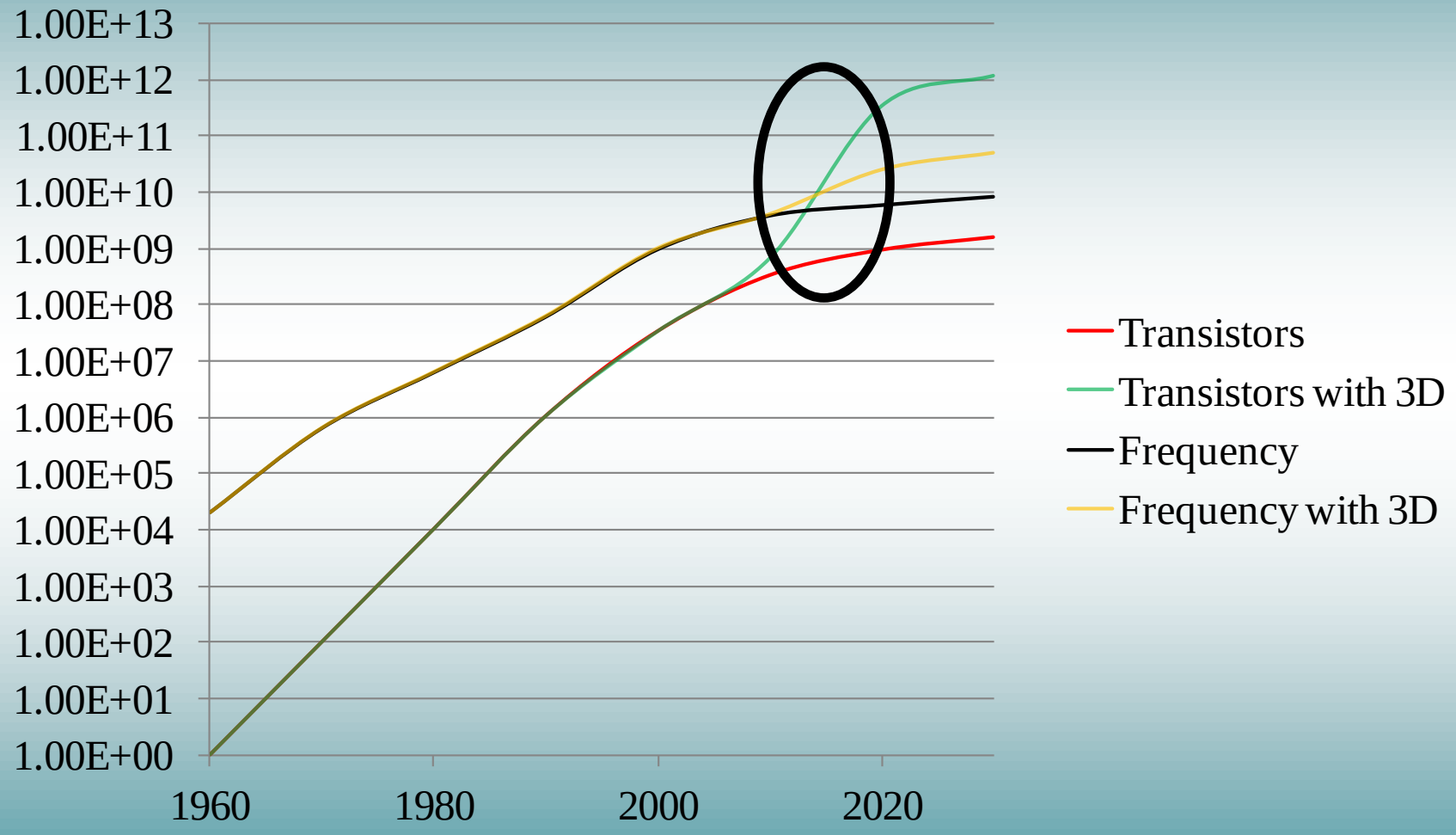






>180nm 130nm 90nm 65nm 45nm 28nm 22nm 16nm

The Effect of 2.5/3D on Devices

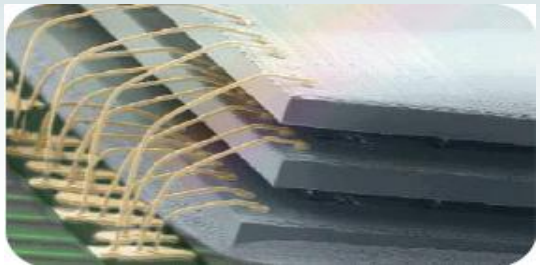


3D Stacking Approaches

Chip Level

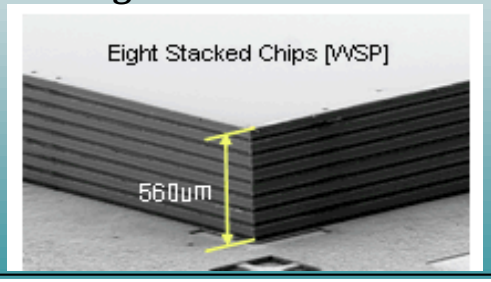
- **Ziptronix**
- **Xan3D**
- **Vertical Circuits**

Amkor : 4S CSP (MCP)



Irvine Sensors : Stacked Flash

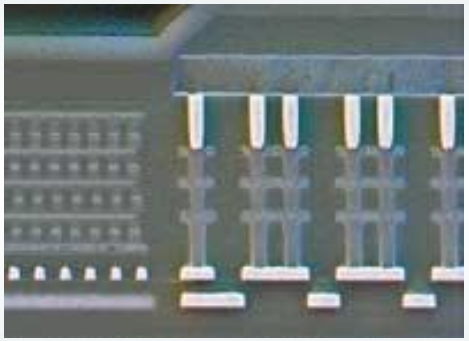
Samsung : Stacked Flash

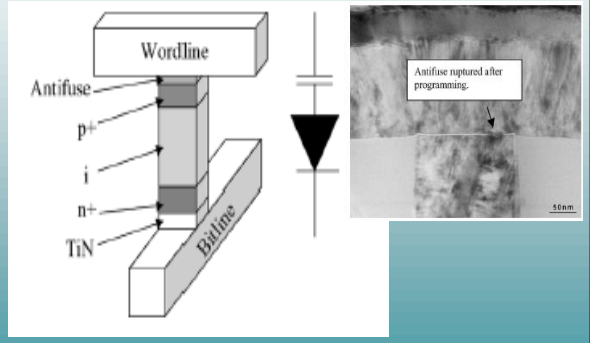


Device Level

- **Stanford**
- **Besang**

Matrix: Vertical TFT

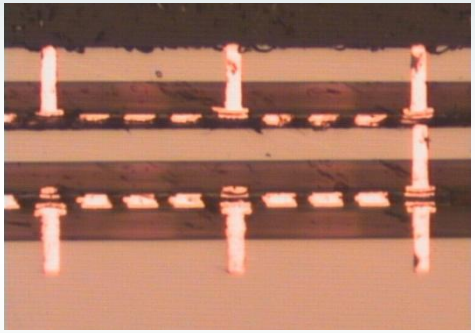


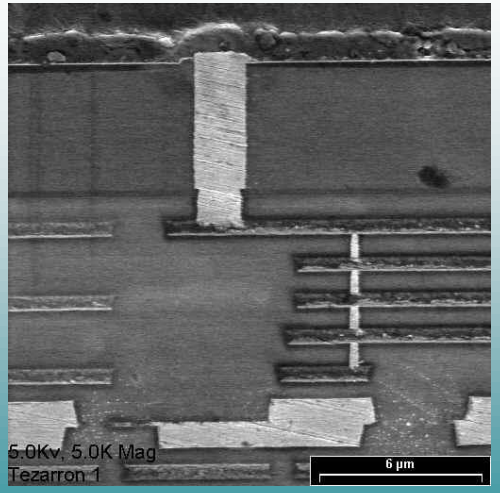


Wafer Level

- **Infineon/IBM**
- **RPI**
- **ZyCube**

Tezzaron

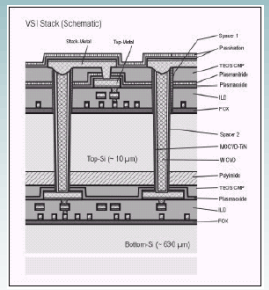


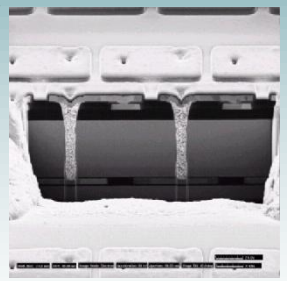


Wafer Level Stacking Approaches

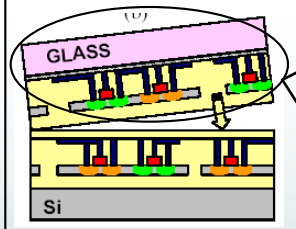
Infineon/IBM

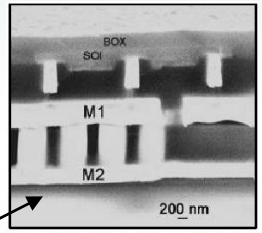
Infineon : W deep via

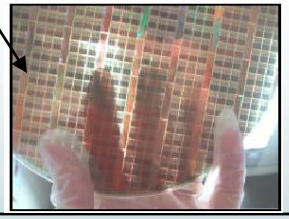




IBM : SOI wafer thinning

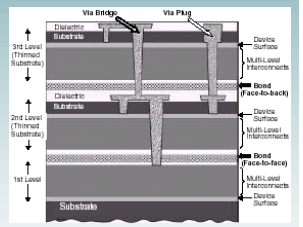


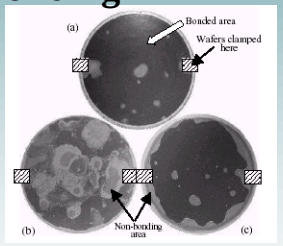




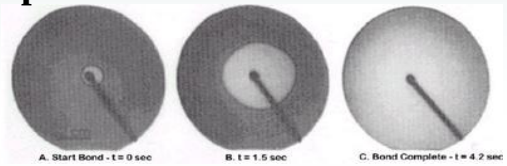
RPI/ Ziptronix/ ZyCube

RPI : Dielectric bonding

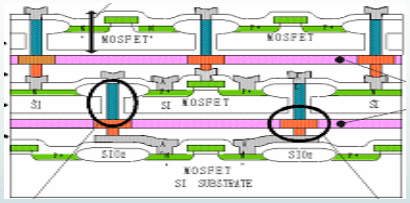




Ziptronix : Covalent bond

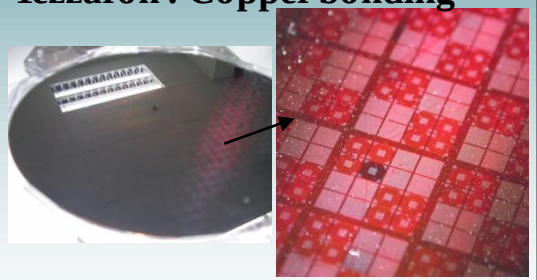


ZyCube : Injection glue bonding

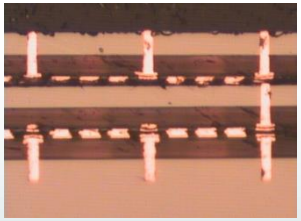


Tezzaron

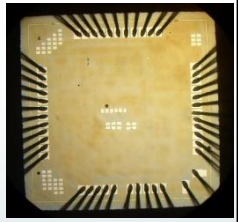
Tezzaron : Copper bonding



Backside of the stacked wafer



3 wafer stack

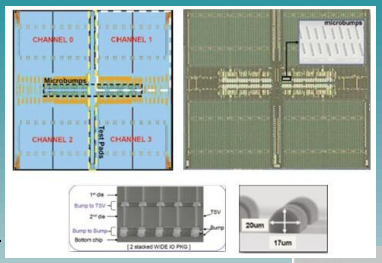


3D Sensor

Market Drivers: 3D

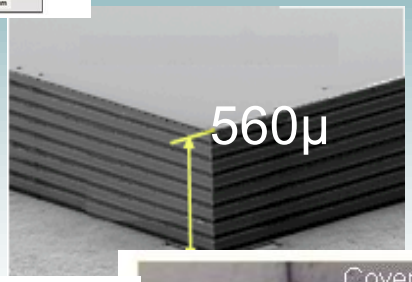
Driver	Functionality	Technical Parameter # 1	Technical Parameter # 2	Value Indicator
Stacked NAND Flash	Cell Phones Hard Drives Flash Drives	Memory density		High packing density
Micro-processor + Memory	Workstations	Latency bandwidth	Power	Execution time
Memory	Multiple	Density	Latency	Varies
Image Sensor	Cell Phones Cameras Automotive	Quantum Efficiency	Number of pixels	Image Quality

There is a lot of 3D today



Samsung

16Gb NAND flash (2Gx8 chips),
Wide Bus DRAM

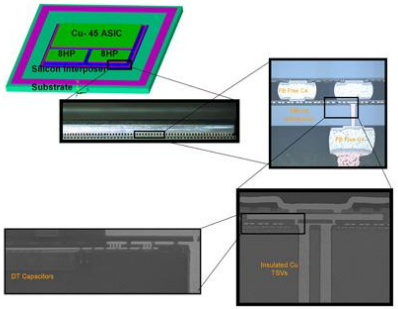


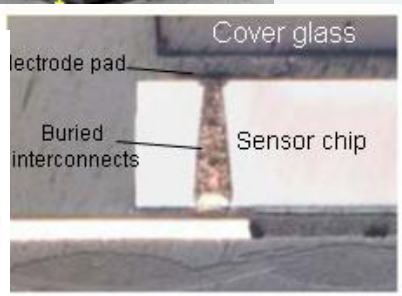
Micron

Wide Bus DRAM

Intel

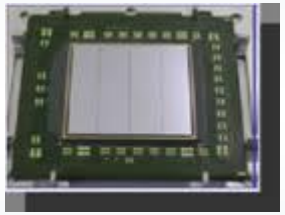
CPU + memory





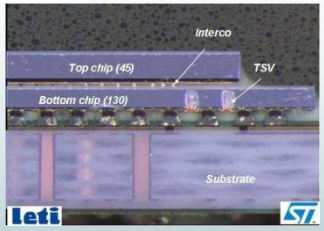
OKI

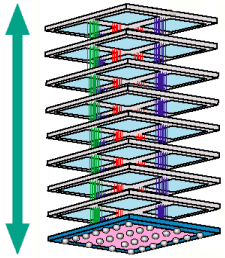
CMOS Sensor

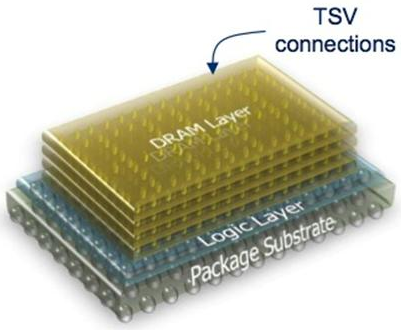


Xilinx

4 die 65nm interposer

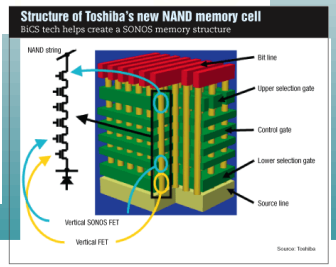


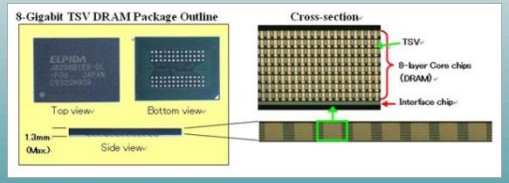




Raytheon/Ziptronix

PIN Detector Device





IBM

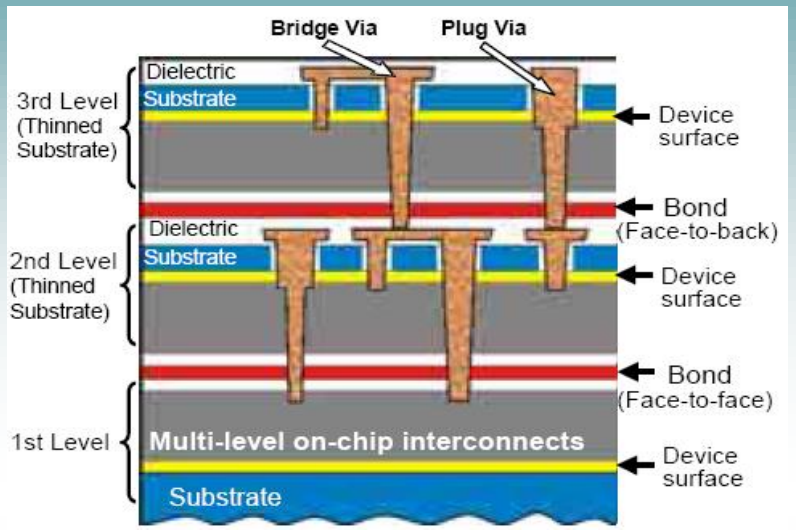
RF Silicon Circuit Board / TSV
Logic & Analog

Toshiba

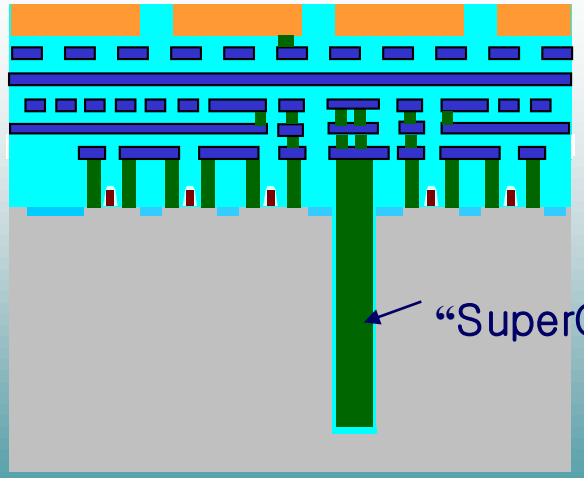
3D NAND

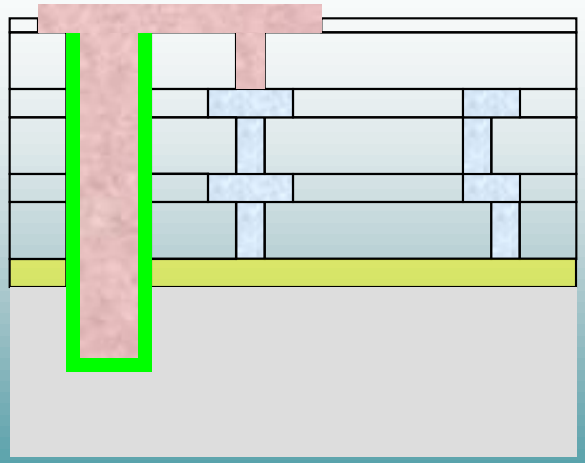
Through-Silicon Via (TSV)

- Via First
- Via Last
- Via at Front end (FEOL)
- Via at Mid line (MOL?)
- Via at Back end (BEOL)



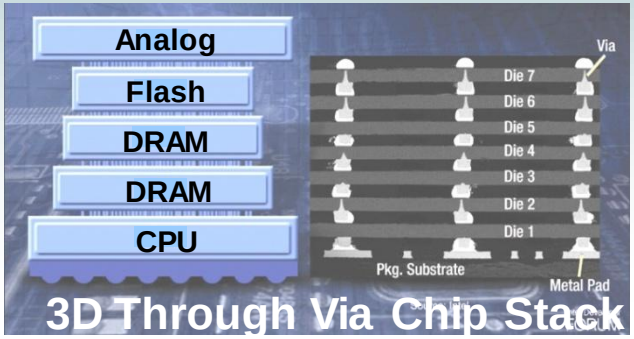
Dr. J.Q. Lu
RPI





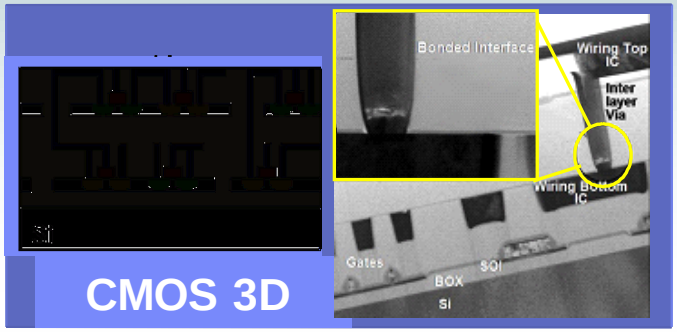
Span of 3D Integration

Packaging



IBM/Samsung

Wafer Fab



IBM

3D-ICs

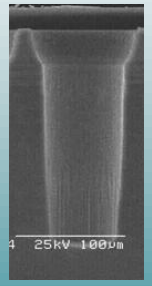
100-1,000,000/sqmm

1000-10M Interconnects/device

1s/sqmm

Peripheral I/O

- Flash, DRAM
- CMOS Sensors



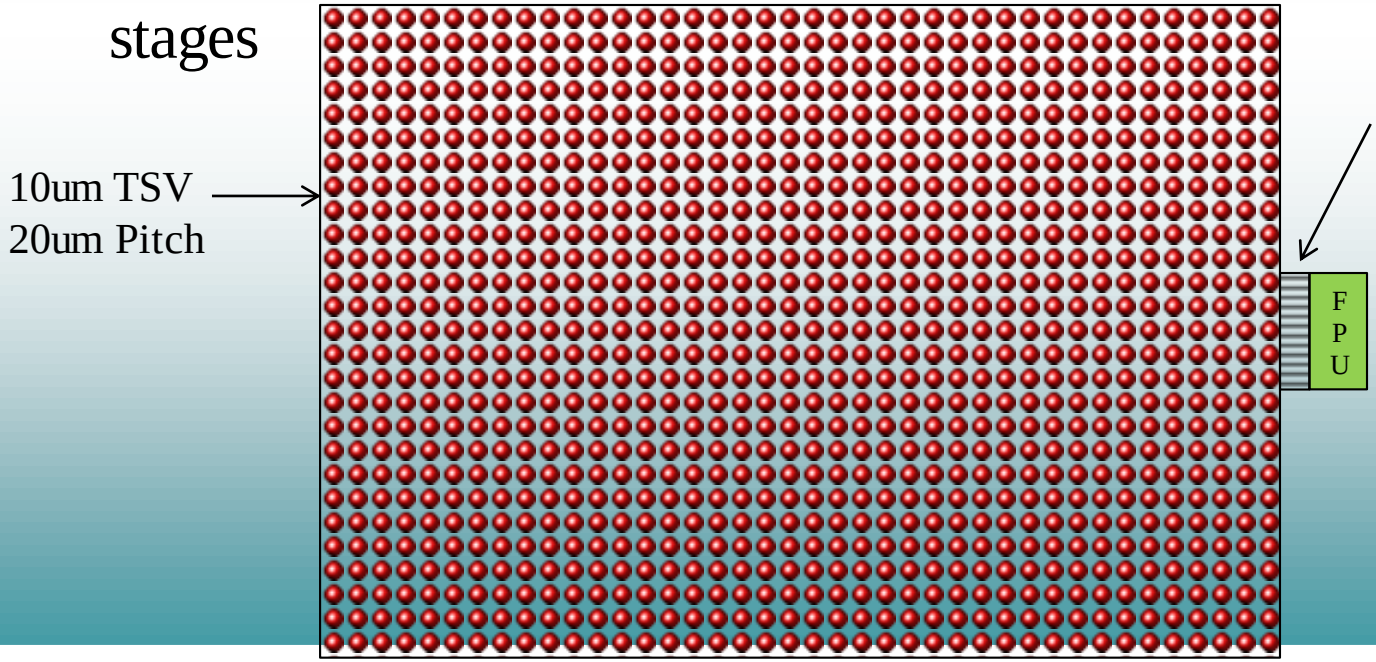
100,000,000s/sqmm

Transistor to Transistor

- Ultimate goal

TSV Pitch ≠ Area ÷ Number of TSVs

- TSV pitch issue example
  - 1024 bit busses require a lot of space with larger TSVs
  - They connect to the heart and most dense area of processing elements
  - The 45nm bus pitch is ~100nm; TSV pitch is >100x greater
  - The big TSV pitch means TOF errors and at least 3 repeater stages



TSV Pitch ≠ Area ÷ Number of TSVs

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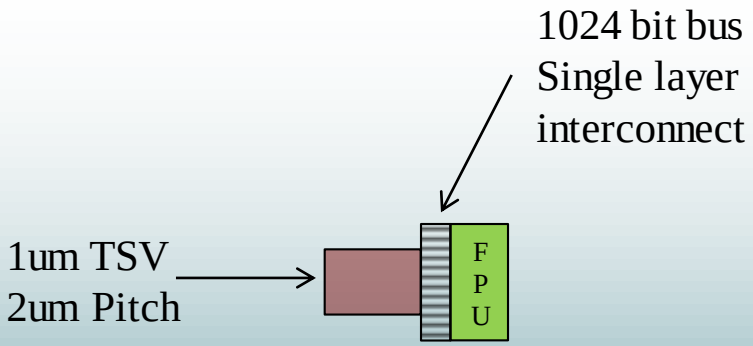
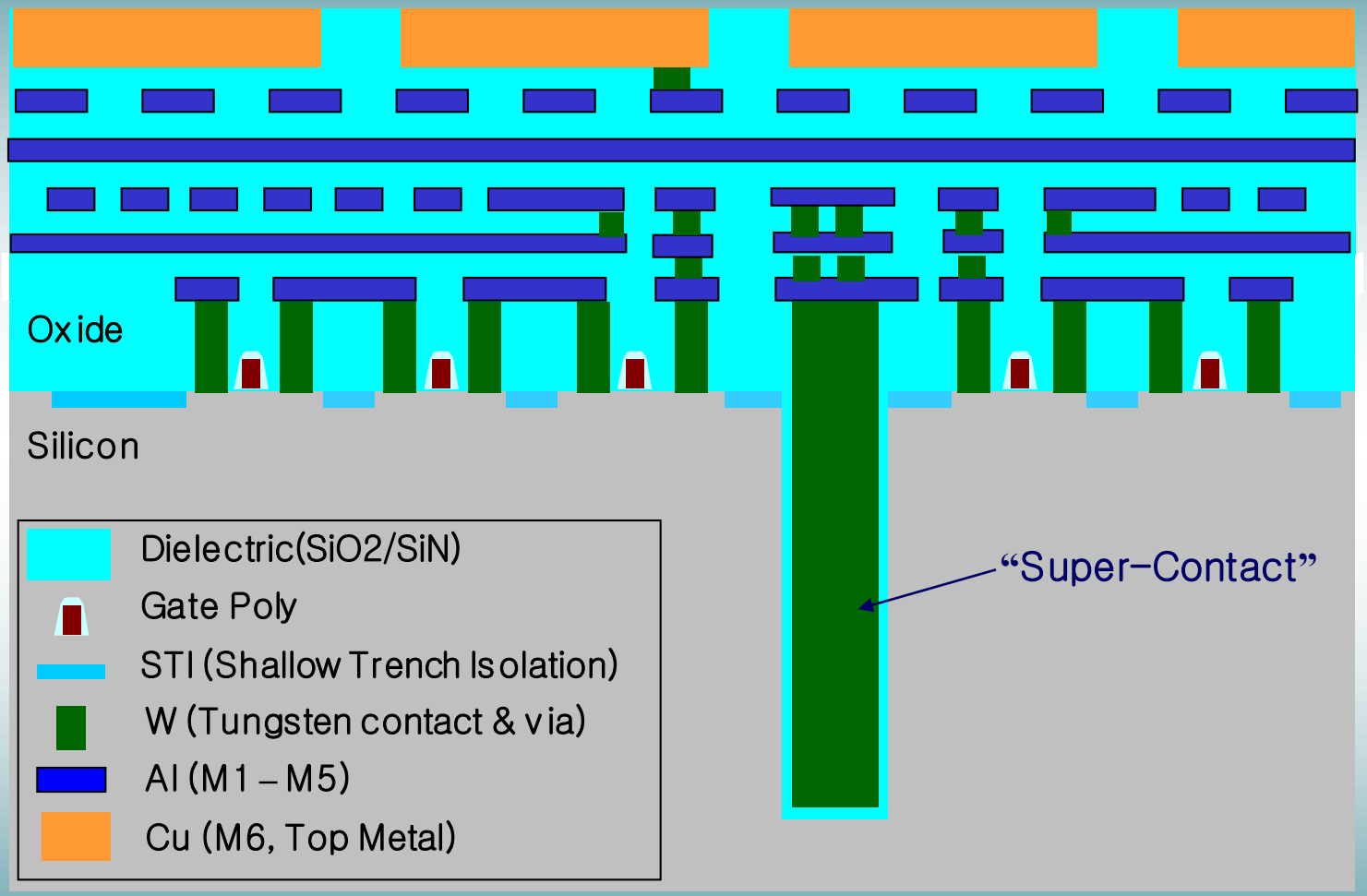


3D Interconnect Characteristics

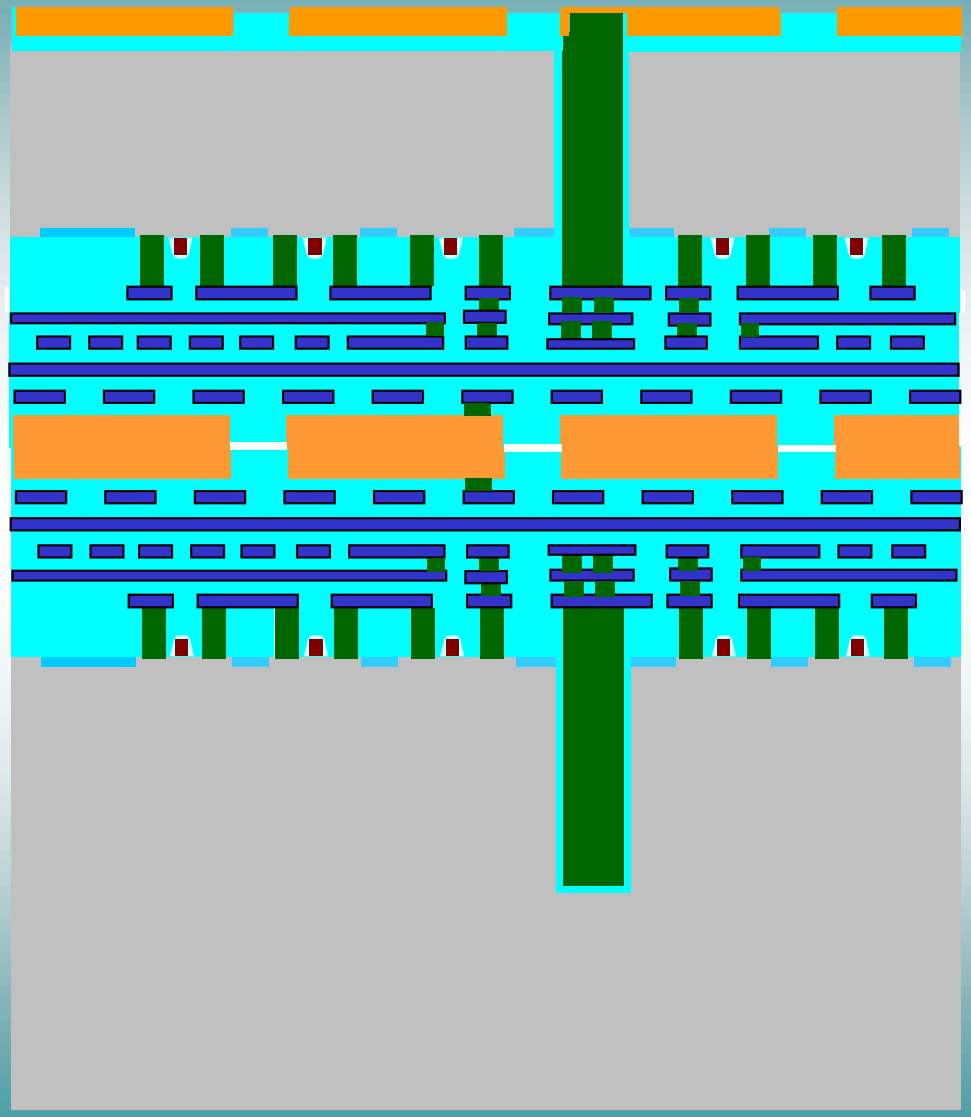
	SuperContact™ I 200mm Via First, FEOL	SuperContact™ III 200mm Via First, FEOL	SuperContact™ IV 200mm Via First, FEOL	Interposer TSV	Bond Points	Die to Wafer
Size L X W X D Material	1.2 µ X 1.2 µ X 6.0µ W in Bulk	0.85 µ X 0.85 µ X 10µ W in Bulk	0.60 µ X 0.60 µ X 2µ W in SOI	10 µ X 10 µ X 100 µ Cu	1.7 µ X 1.7 µ Cu	3 µ X 3 µ Cu
Minimum Pitch	<2.5 µ	1.75 µ	1.2 µ	30/120 µ	2.4 µ	5 µ
Feedthrough Capacitance	2-3fF	3fF	0.2fF	250fF	<<	<25fF
Series Resistance	<1.5 Ω	<3 Ω	<1.75 Ω	<0.5 Ω	<	<

Small fine grain TSVs are fundamental to 3D enablement

A Closer Look at Wafer-Level Stacking



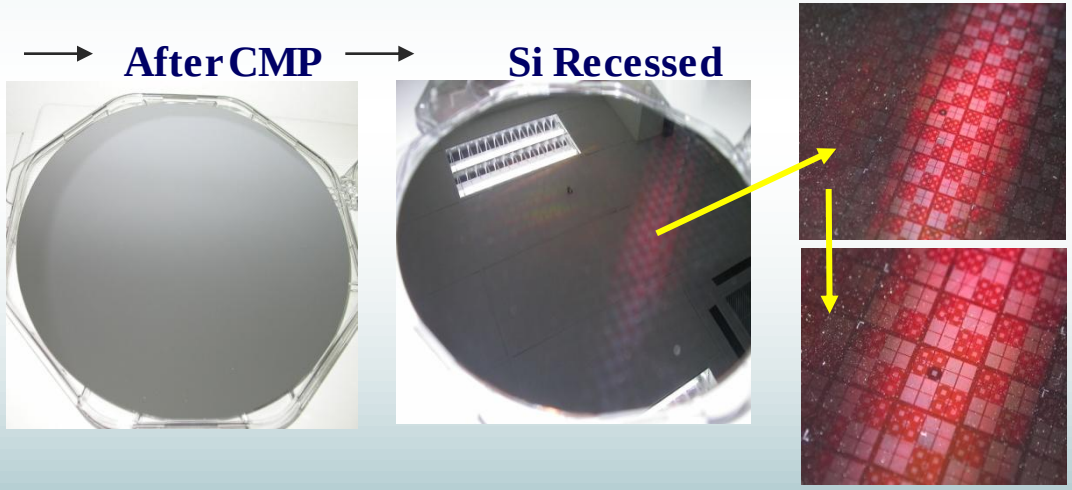
Next, Stack a Second Wafer & Thin:



Stacking Process Sequential Picture

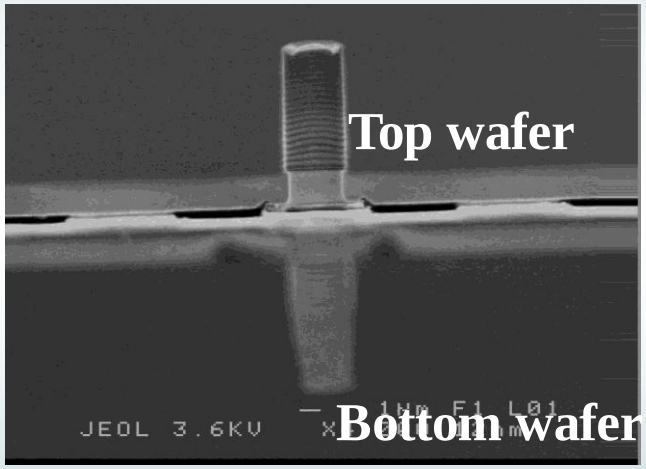
Two wafer Align & Bond → Course Grinded → Fine Grinded

→ After CMP → Si Recessed

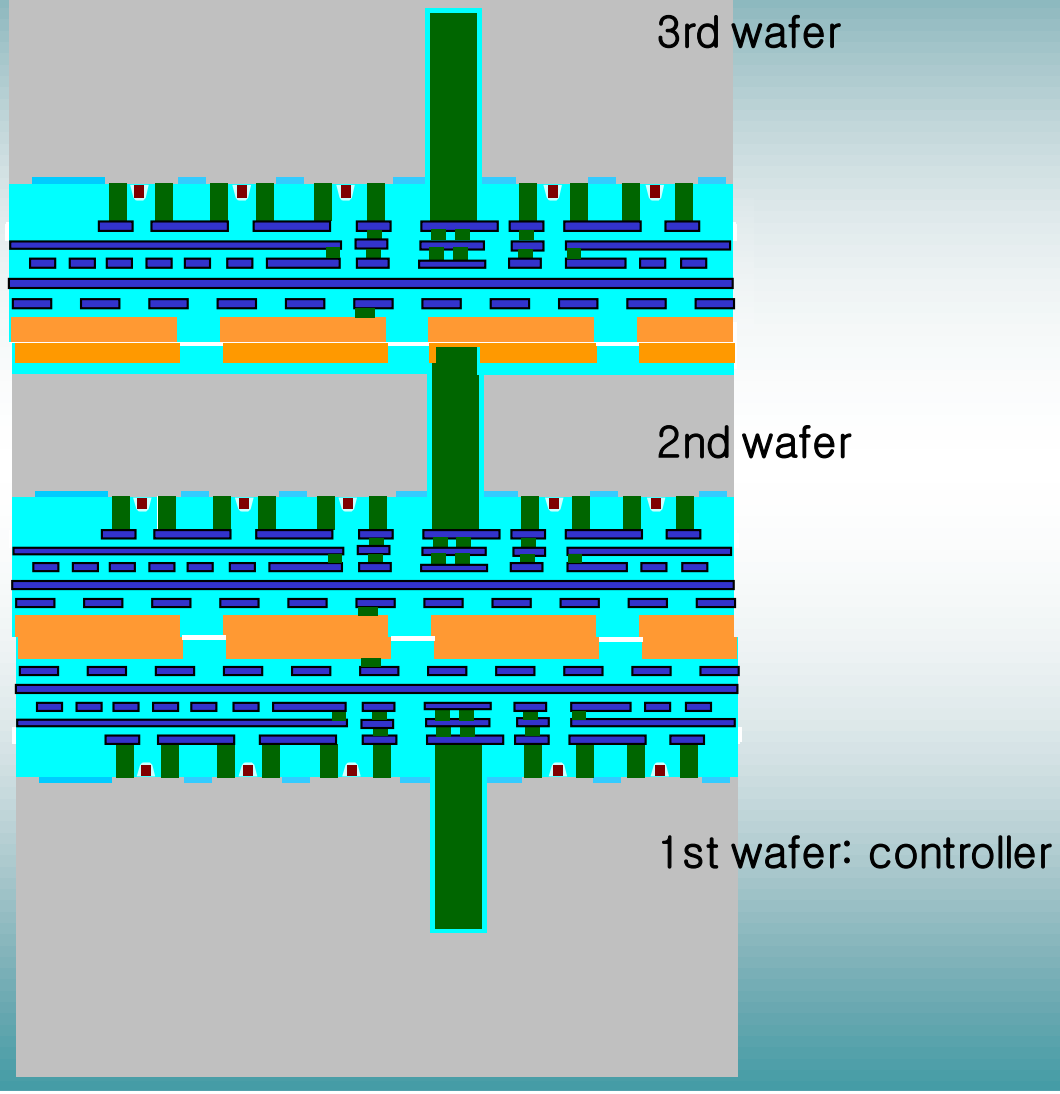


High Precision Alignment

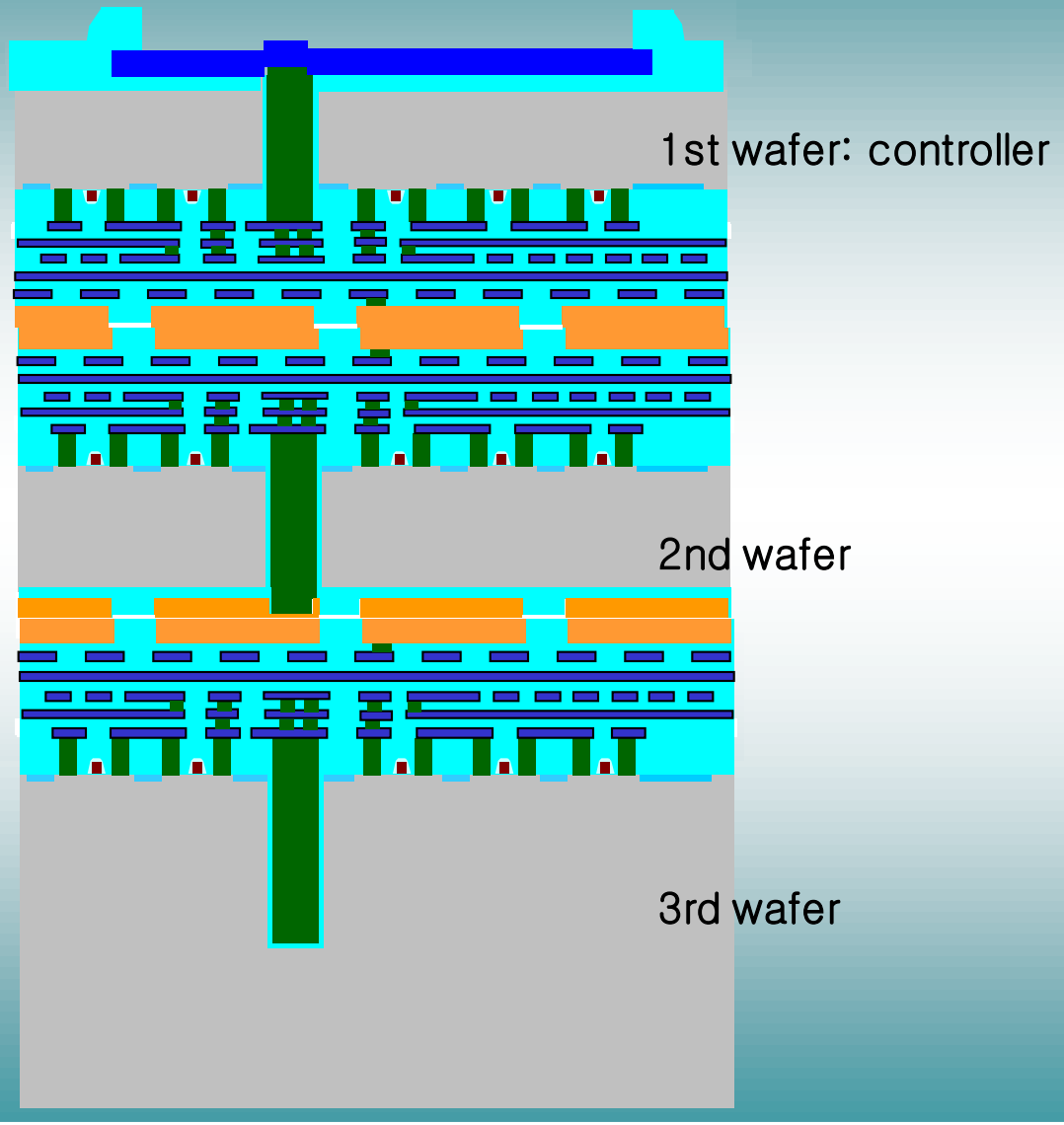
Misalign=0.3um



Then, Stack a Third Wafer:

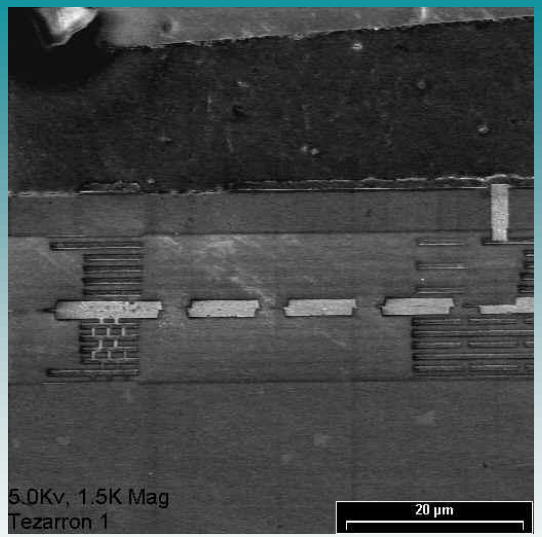


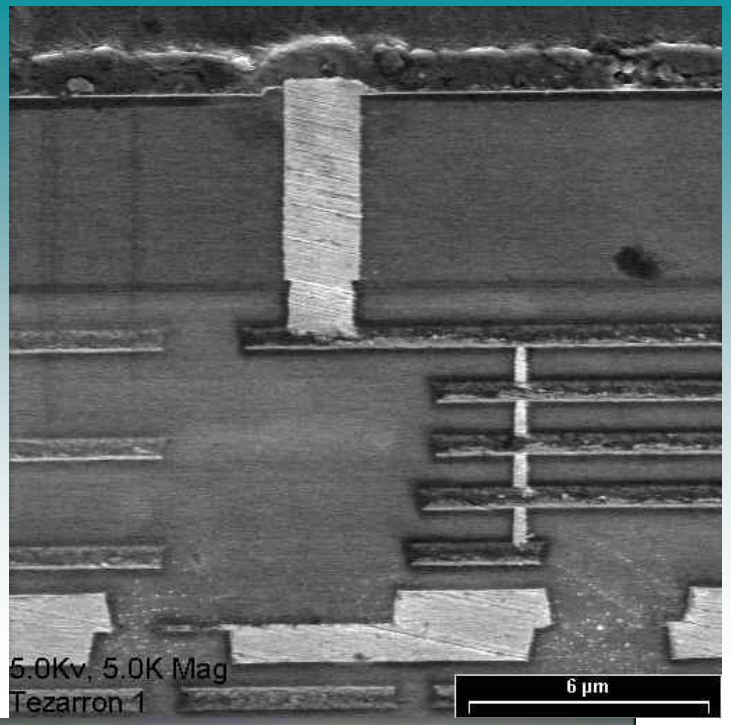
Finally, Flip, Thin & Pad Out:

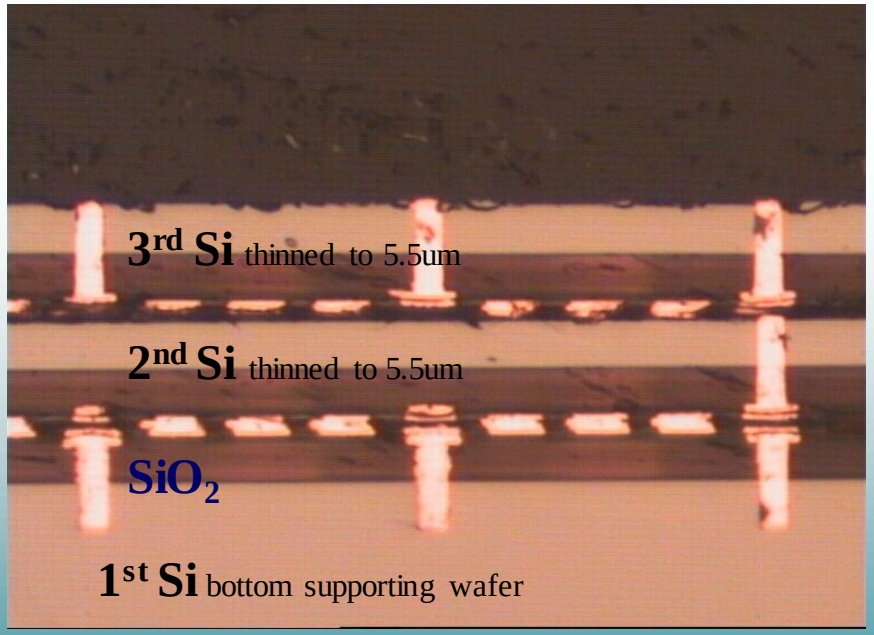


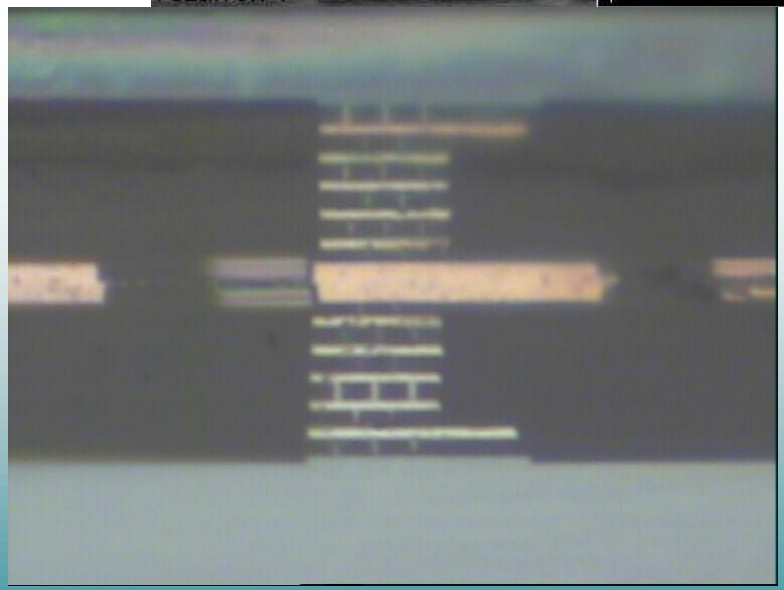
This is the completed stack!

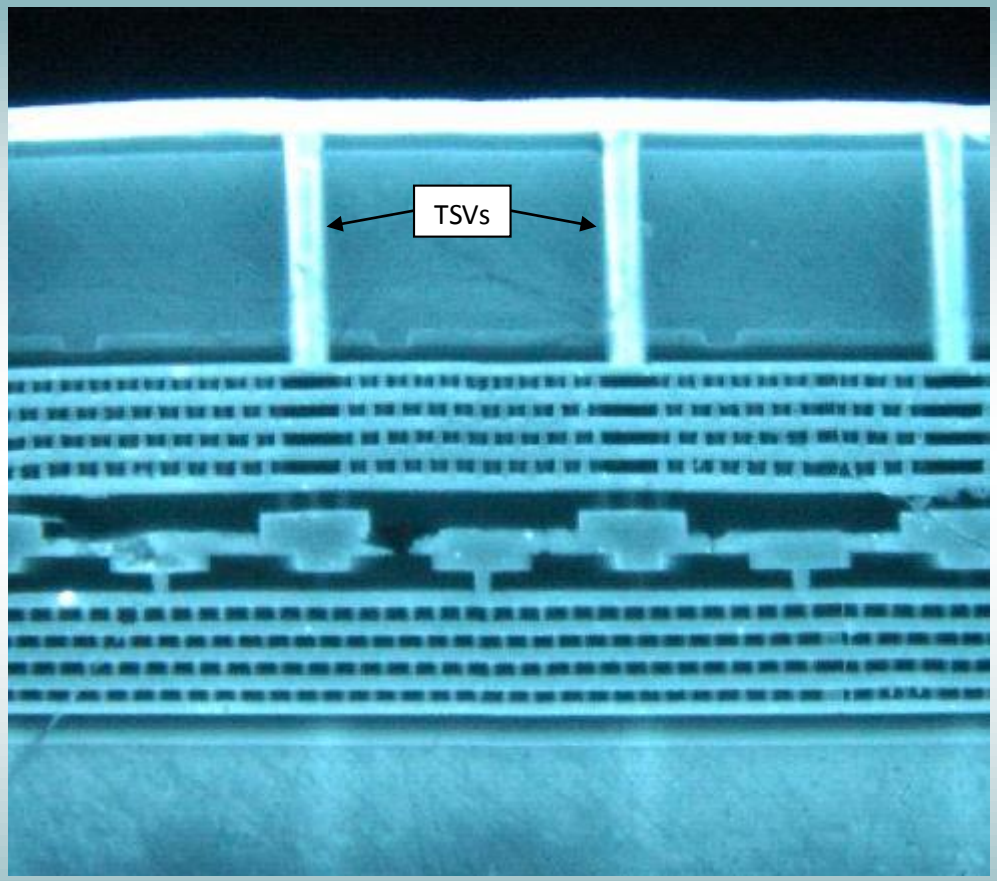
5kV, 800X, Tezzaron
37.5 µm


5.0Kv, 1.5K Mag
Tezarron 1
20 µm

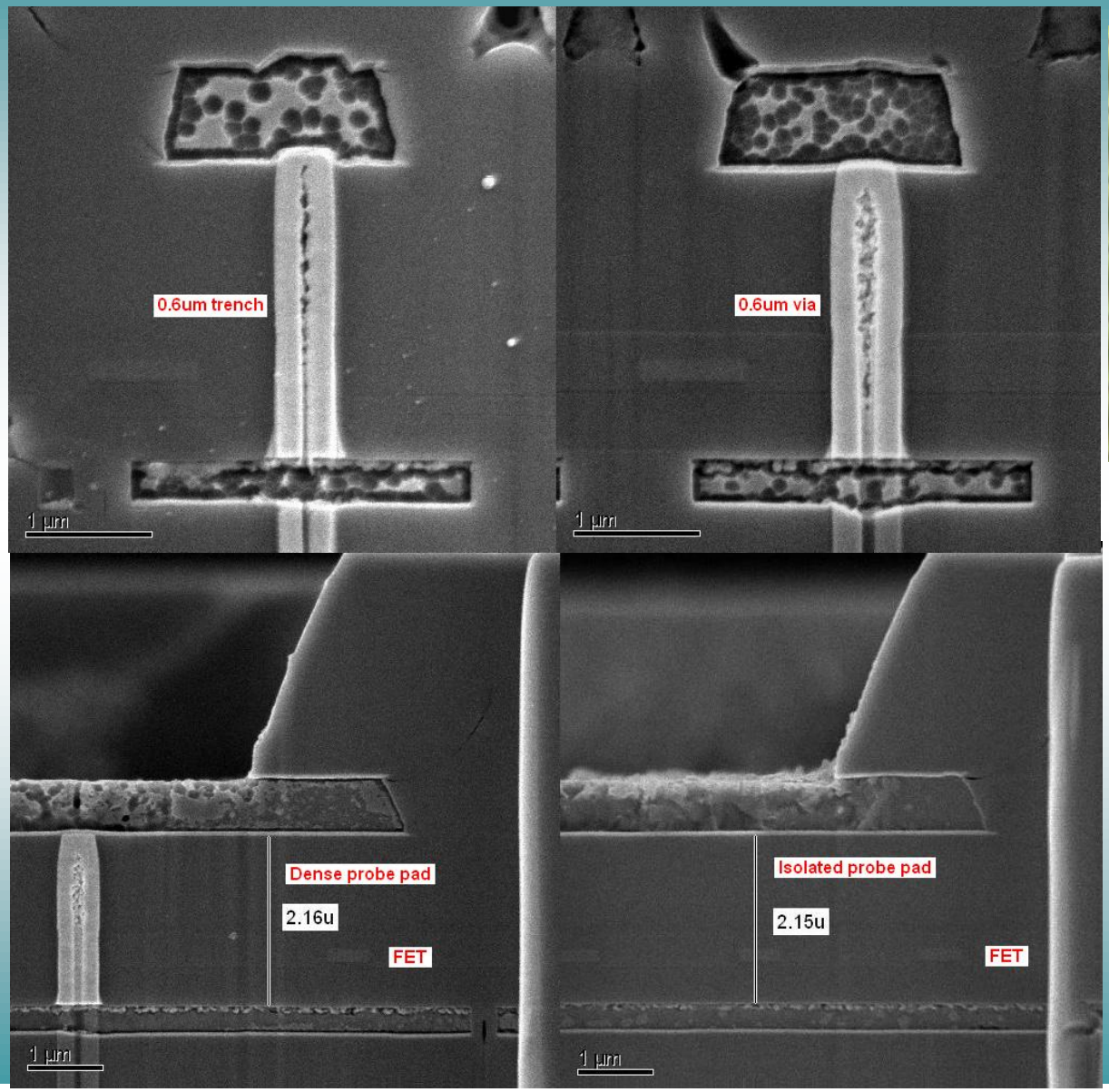

5.0Kv, 5.0K Mag
Tezarron 1
6 µm

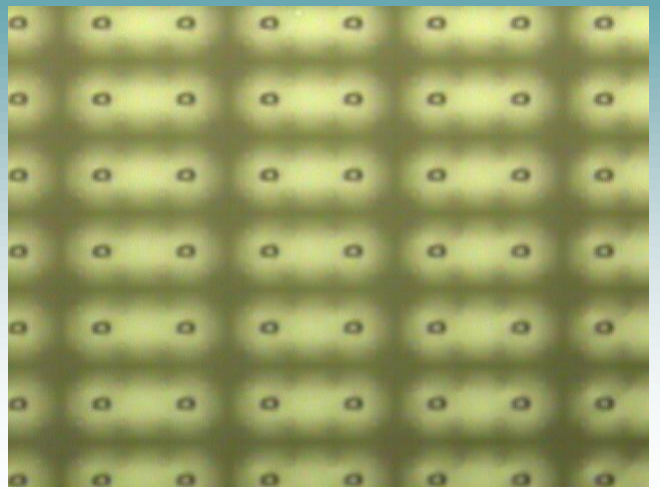

3rd Si thinned to 5.5um
2nd Si thinned to 5.5um
SiO2
1st Si bottom supporting wafer



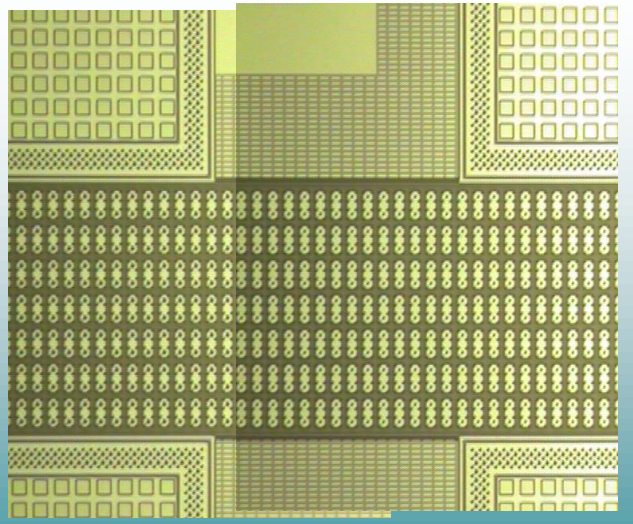

TSVs

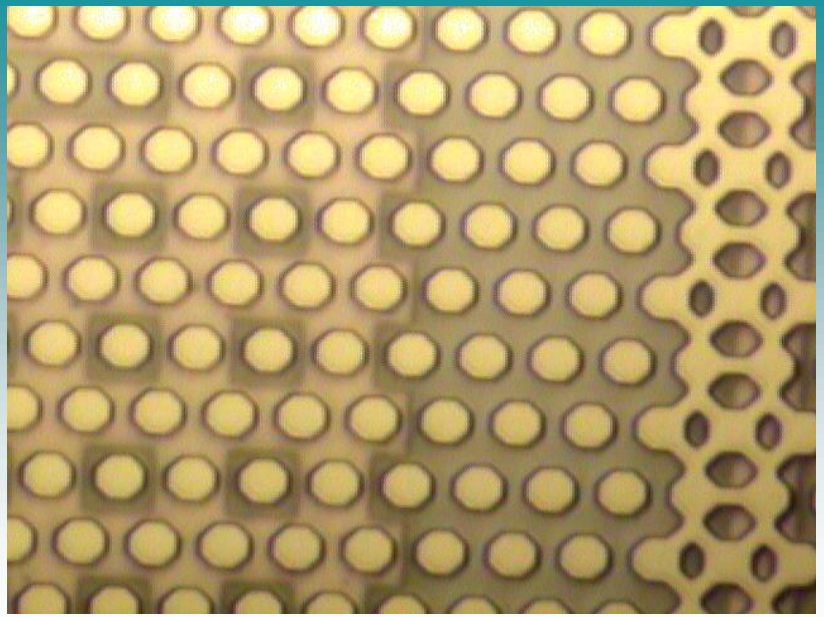
Honeywell 0.6um SOI TSV

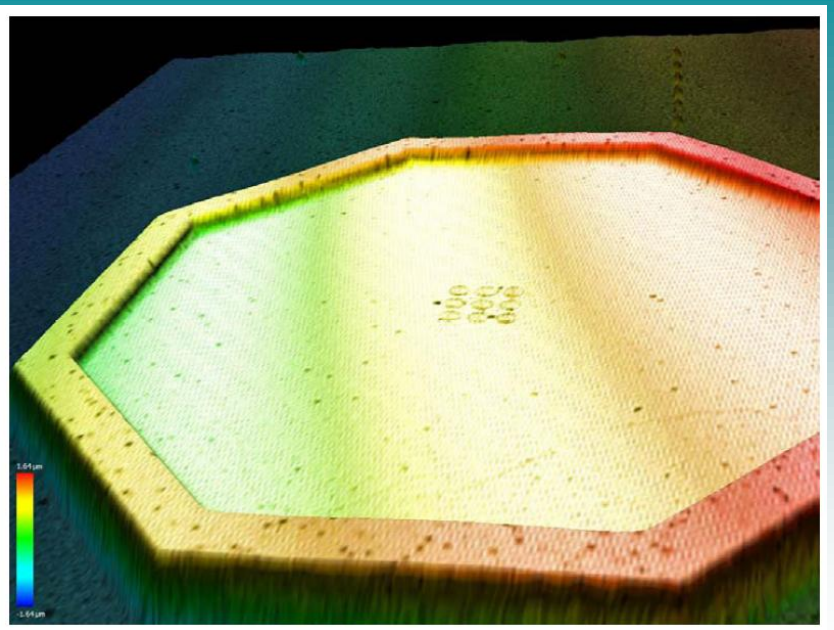


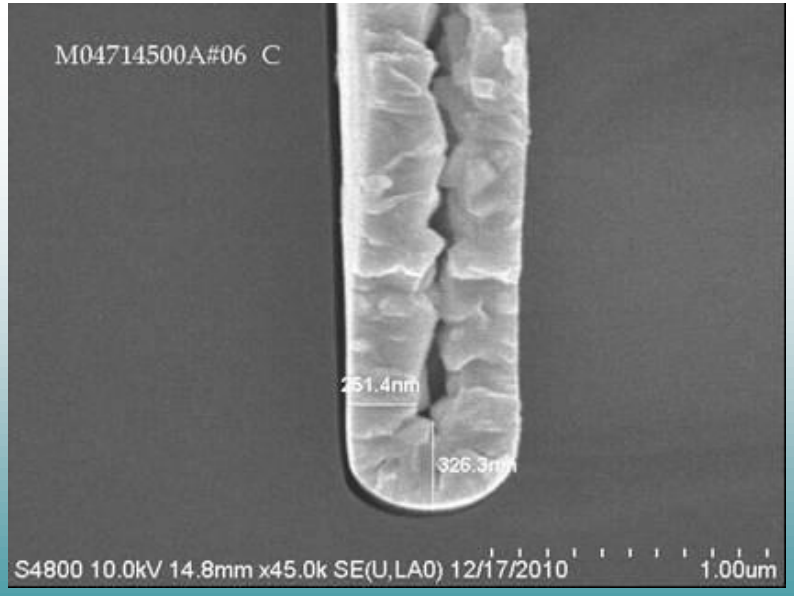


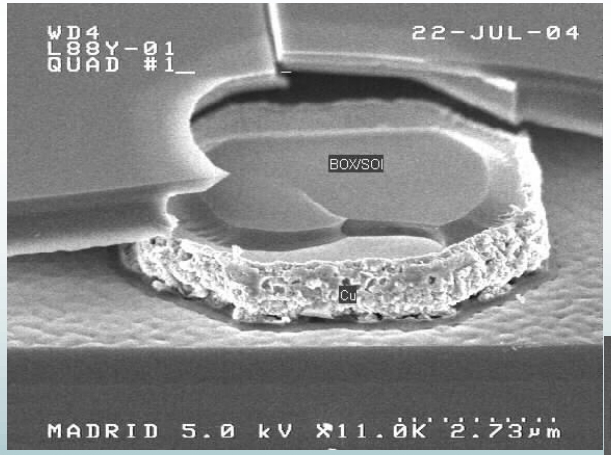
120K TSVs

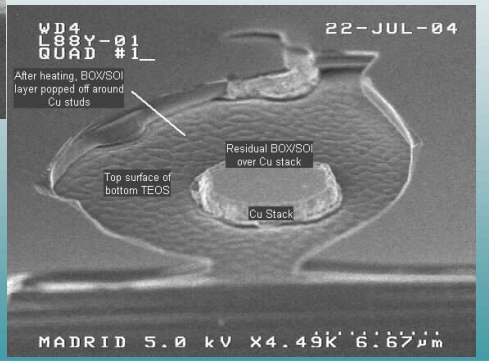







M04714500A#06 C
251.4nm
326.3nm
S4800 10.0kV 14.8mm x45.0k SE(U,LA0) 12/17/2010
1.00um


WD4
L88Y-01
QUAD #1_
22-JUL-04
BOX/SOI
Cu
MADRID 5.0 kV X11.0K 2.73µm


WD4
L88Y-01
QUAD #1_
22-JUL-04
After heating, BOX/SOI layer popped off around Cu studs
Residual BOX/SOI over Cu stack
Top surface of bottom TEOS
Cu Stack
MADRID 5.0 kV X4.49K 6.67µm

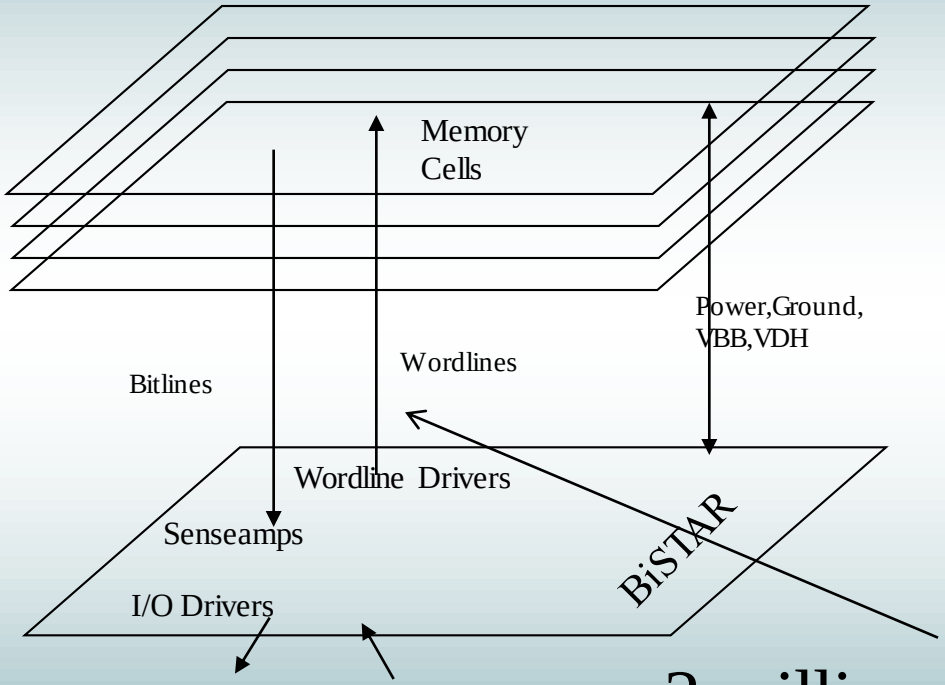
DRAM wants 2 different processes!

Bit cells	Low leakage -slow refresh -low power -low GIDL	High Vt Devices Vneg Well Thick Oxide
Sense Amps Word line drivers Device I/O	High speed -better sensitivity -better bandwidth -lower voltage	Low Vt Devices Copper interconnect Thin Oxides

“Dis-Integrated” 3D Memory

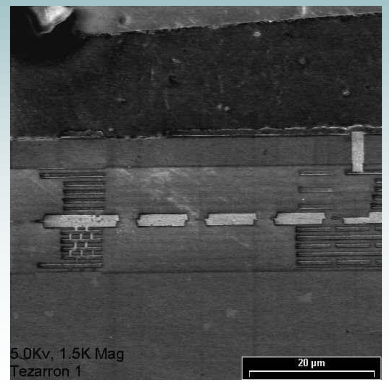
Memory Layers from DRAM fab

Controller Layer from high speed logic fab

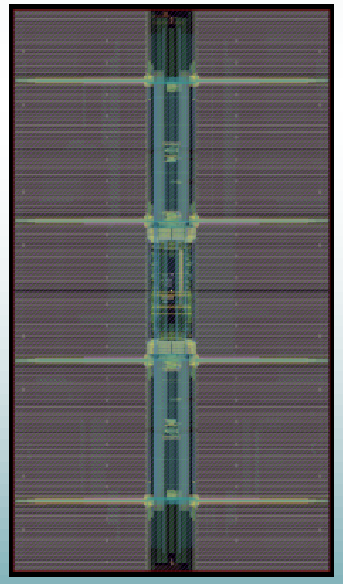


2 million vertical connections per lay per die

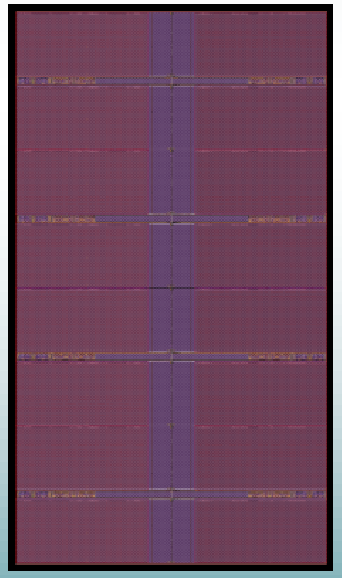
Octopus Stack



2 Layer Stacked Device
(SEM)

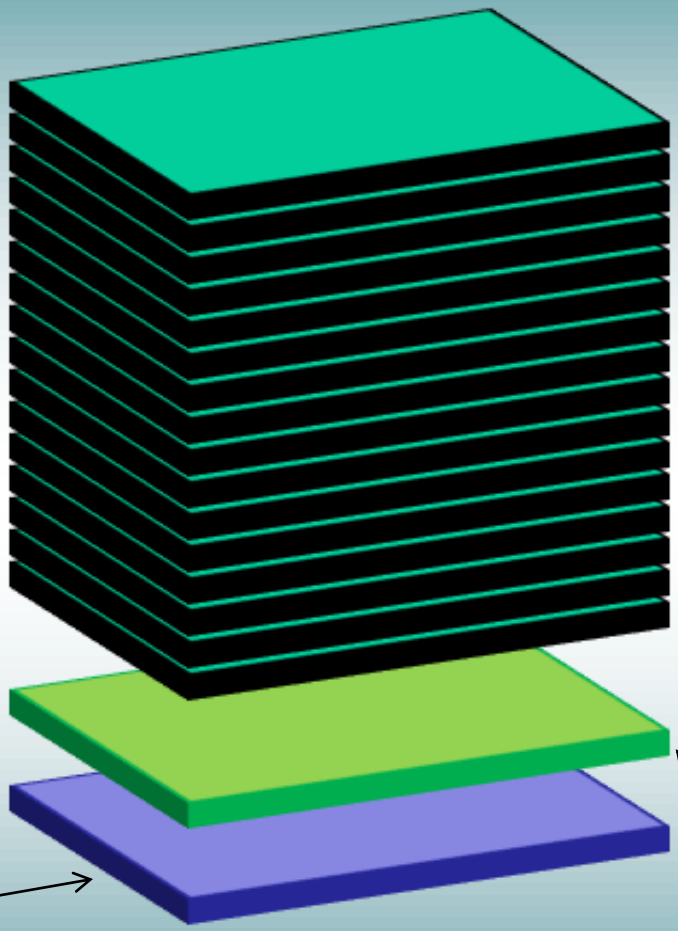


DRAM Control/Logic



DRAM Memory Cells

Gen4 “Dis-Integrated” 3D Memory



DRAM layers
4Xnm node

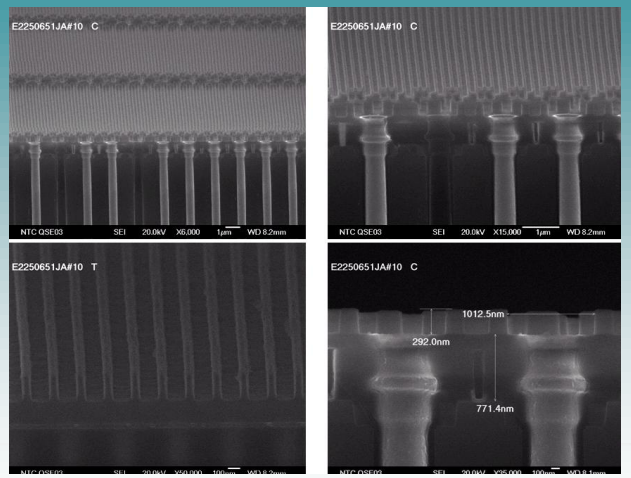
2 million vertical connections per lay per die

I/O layer contains: I/O, interface logic and R&R control CPU. 65nm node

Controller layer contains: senseamps, CAMs, row/column decodes and test engines. 40nm node

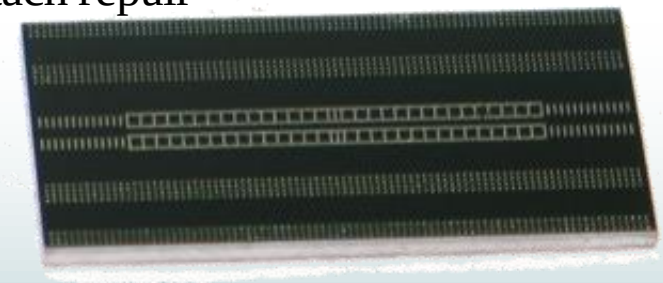
Better yielding than 2D equivalent!

3D DRAMs



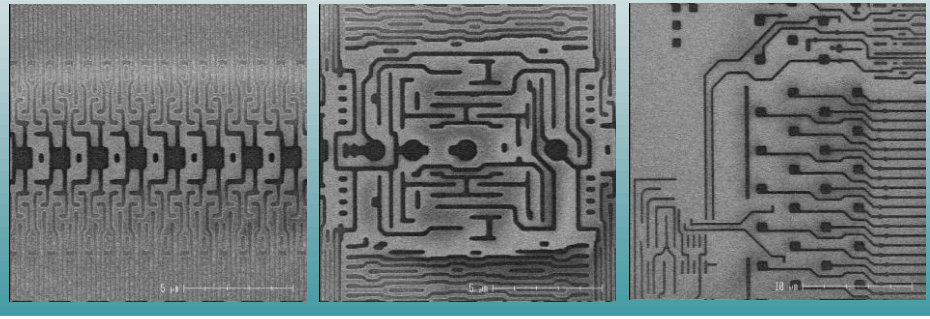
Octopus I

- 1-4Gb
- 16 Ports x 128bits (each way)
- @1GHz
  - CWL=0 CRL=2 SDR format
  - 5ns closed page access to first data (aligned)
  - 12ns full cycle memory time
  - >2Tb/s data transfer rate
- Max clk=1.6GHz
- Internally ECC protected, Dynamic self-repair, Post attach repair
- 115C die full function operating temperature

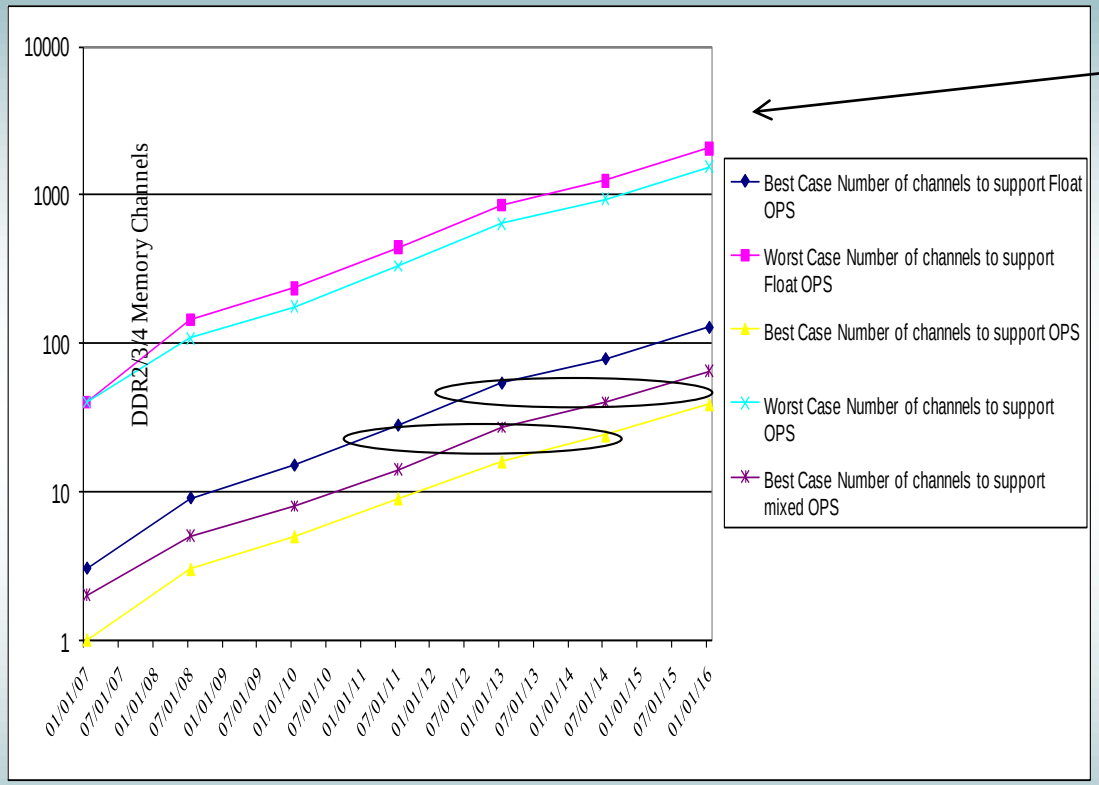


Octopus II

- 4-64Gb
- 64-256 Ports x 64bits (each way)
- @1GHz
  - 5-7ns closed page access to first data (aligned)
  - 12ns full cycle memory time
  - >16Tb/s data transfer rate
  - 4096 banks
  - 2+2pJ/bit



The Industry Issue



Need 50x bandwidth improvement.
Need 10x better cost model than embedded memory.

- To continue to increase CPU performance, exponential bandwidth growth required.
- More than 200 CPU cycles of delay to memory results in cycle for cycle CPU stalls.
- 16 to 64 Mbytes per thread required to hide CPU memory system accesses.
- No current extension of existing IC technology can address requirements.
- Memory I/O power is running away.

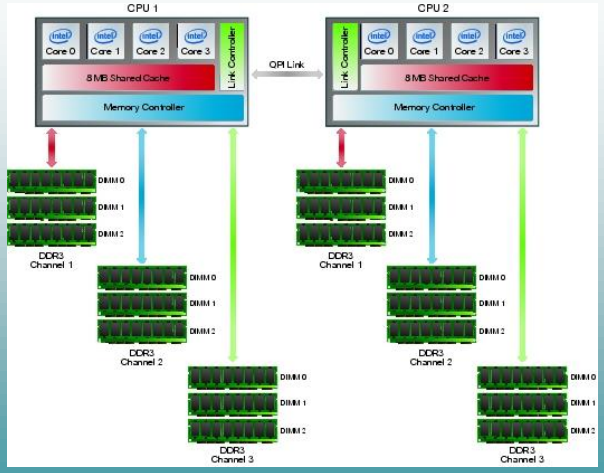
Main Memory Power Cliff

DDR3 ~40mW per pin

1024 Data pins →40W

4096 Data pins →160W

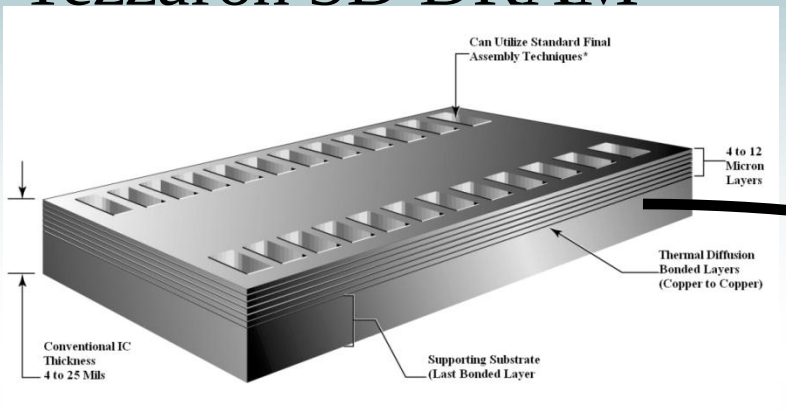
Die on Wafer ~24uW per pin

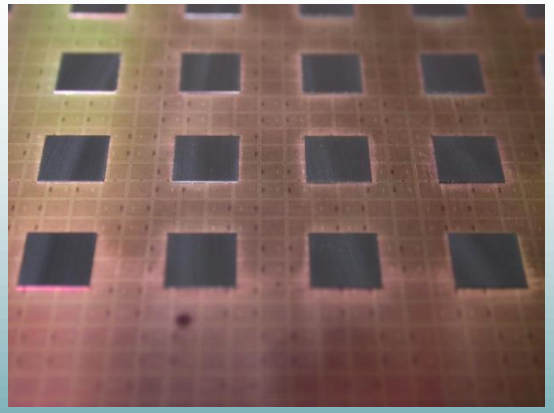


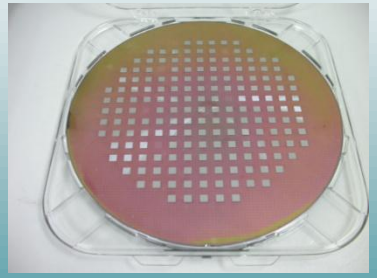
The "Killer" App: Split-Die

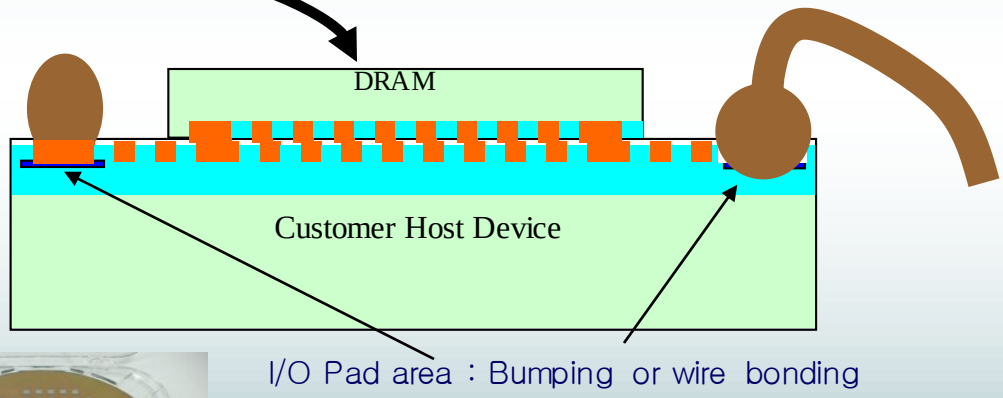
- Embedded Performance with far superior cost/density.
- 110nm DRAM node has better density than 45nm embedded DRAM.
- 1000x reduction in I/O power.

Tezzaron 3D DRAM

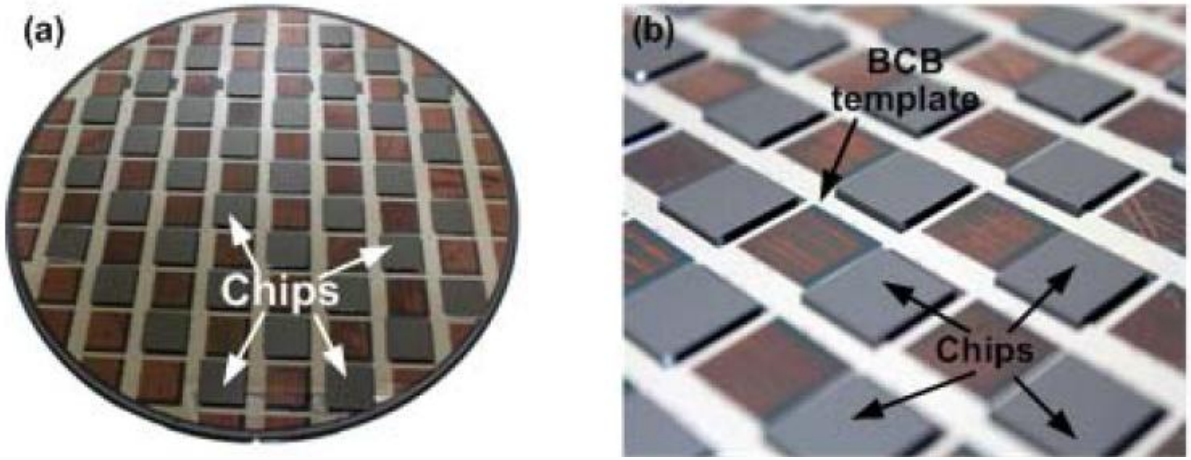






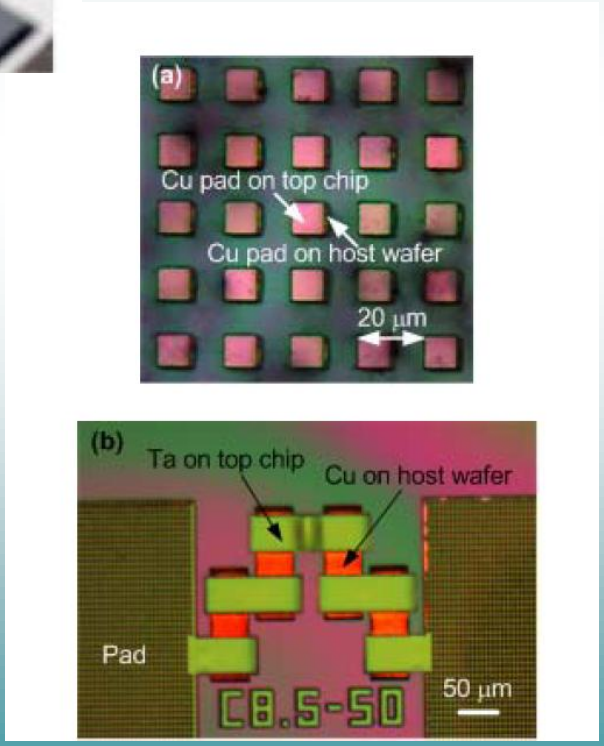


Die to Wafer With BCB Template

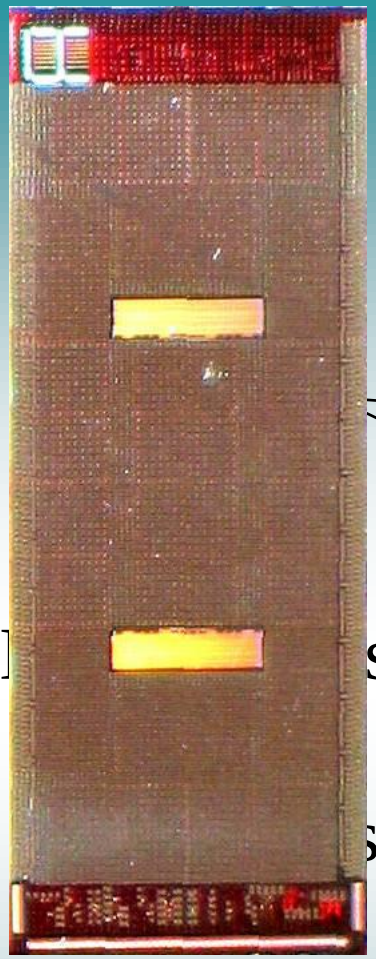


RPI Effort under Dr. James Lu

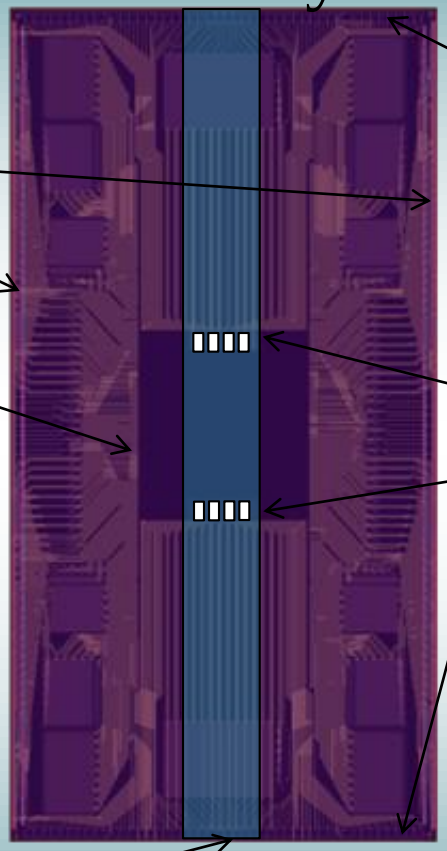
- KGD
- 2um alignment / 5um pitch limit
- Cu-Cu thermo compression bonding
- Multilayer capability



Logic on Memory



Memory

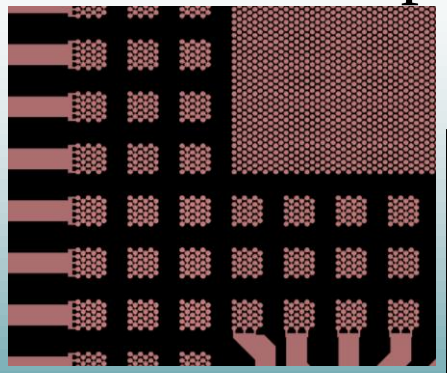


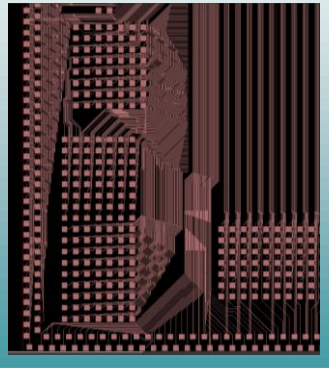
92 pads
(528 total pads at edge, stagger
250um pad, 125um pitch
~1500 available pads)

side

8 DRAM ports
16x21 pad array

so



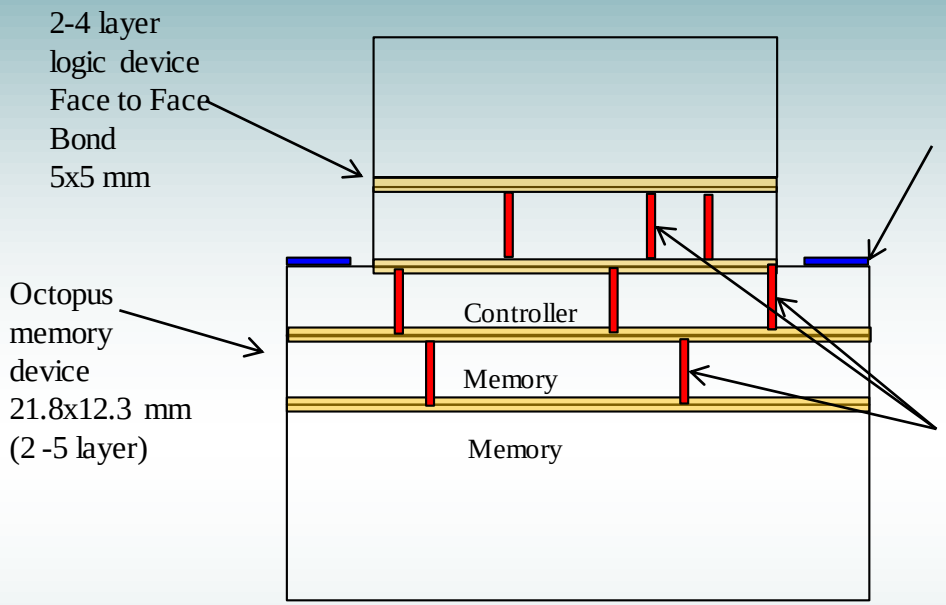


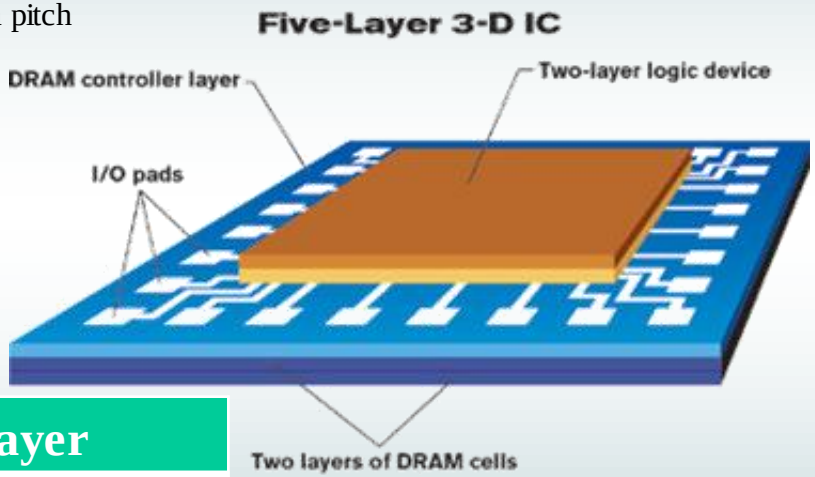
Logic

interposer

>10µf bypass caps
SS ~4,000pf

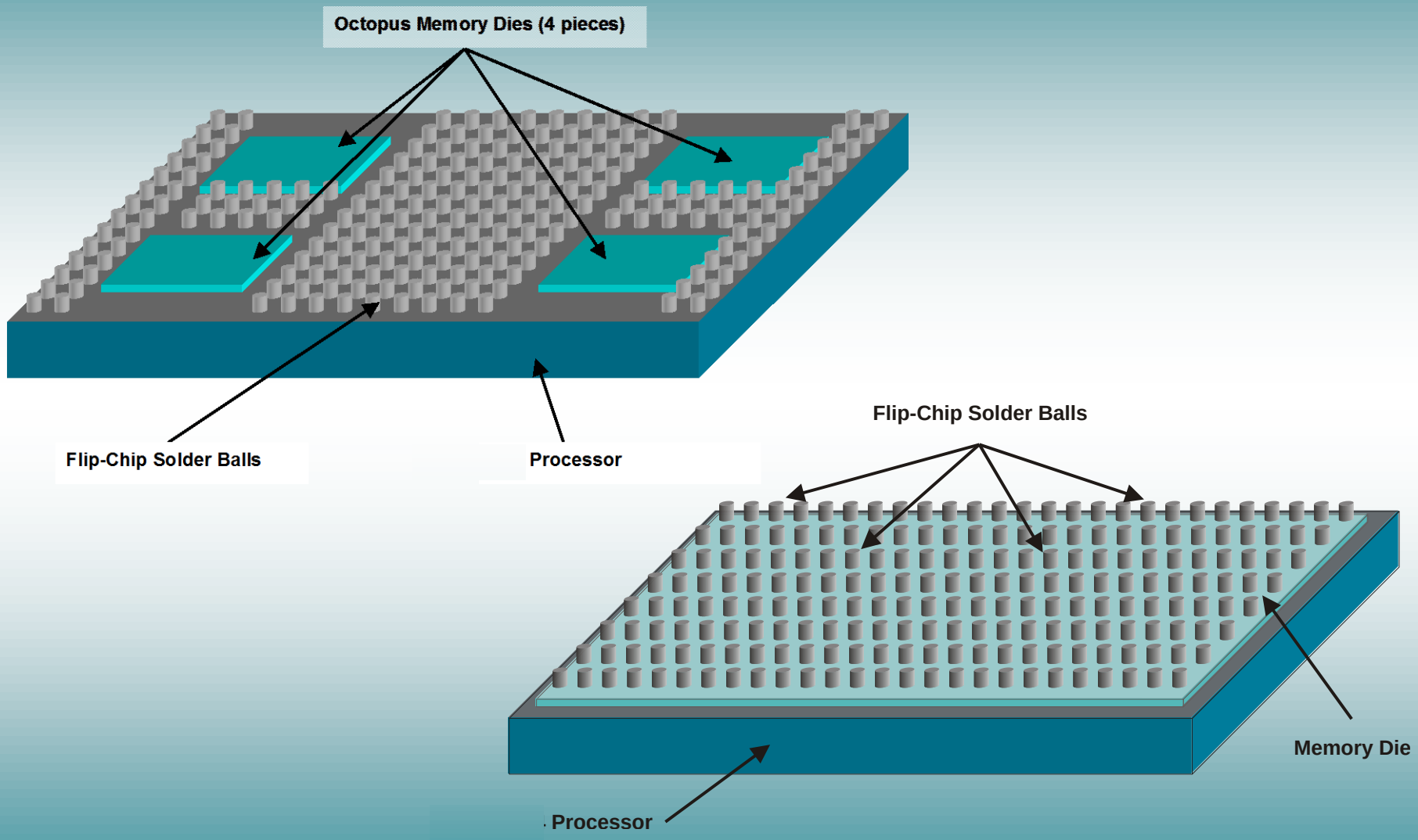
Hyper-Integration
5-9 layer stacks





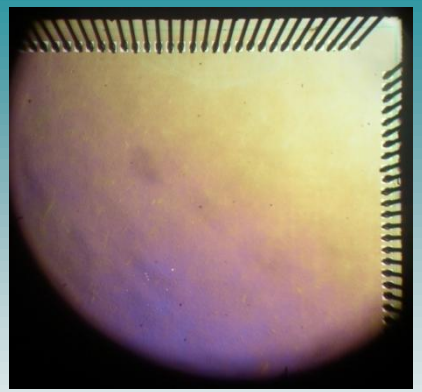
Layer	5 Layer	7 Layer	9 Layer
Poly	9	11	17
Copper Wire	21 (25)	32 (38)	34 (42)
Al/W Wire	7	7	13
Trans. Count	3B	3.1B	5.5B

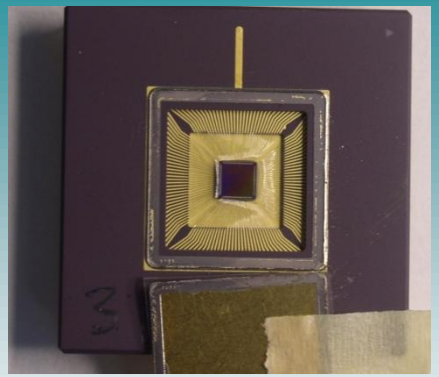
Current Memory Split-Die Projects

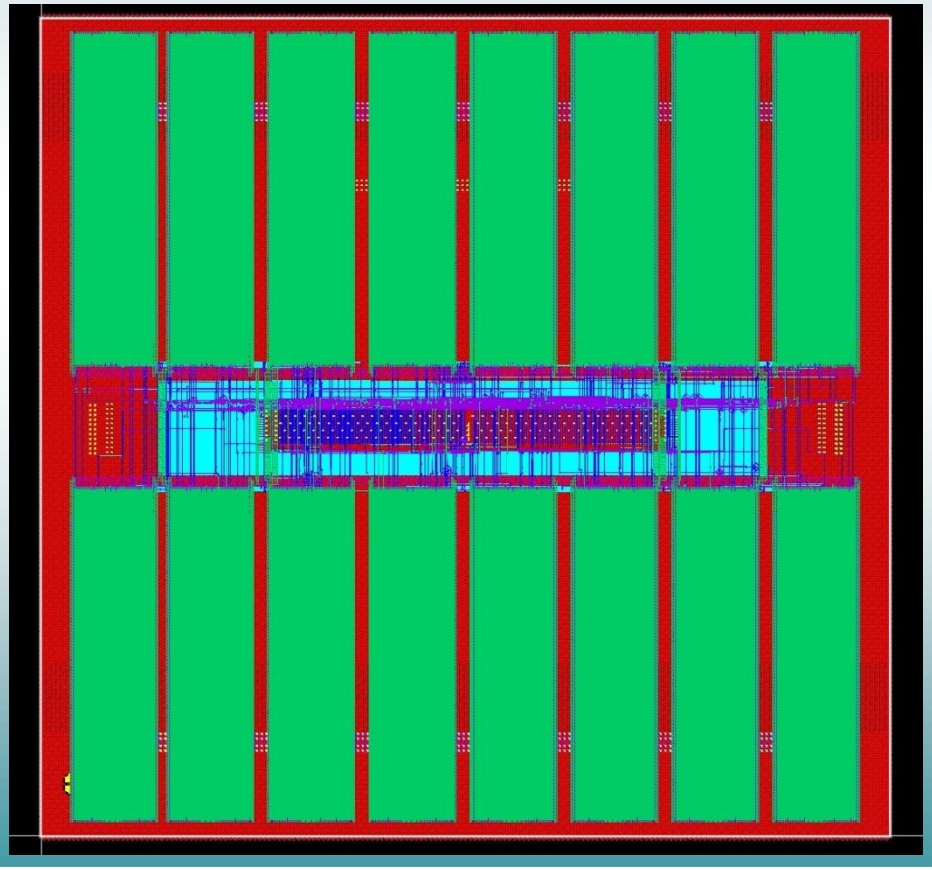


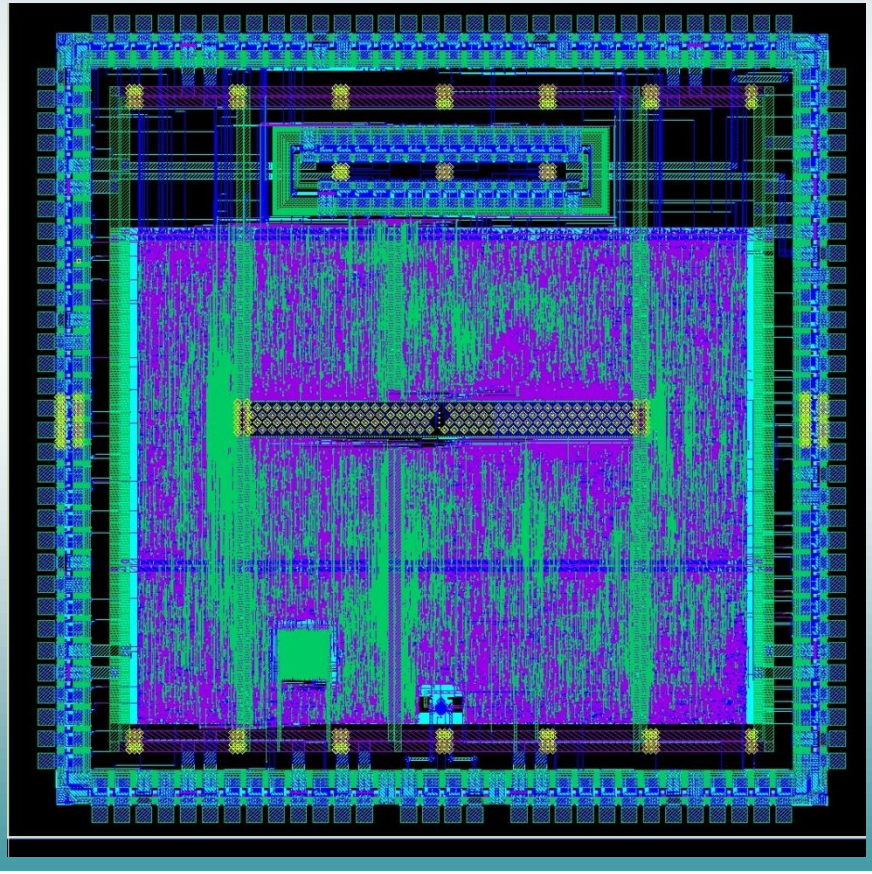
R8051/Memory

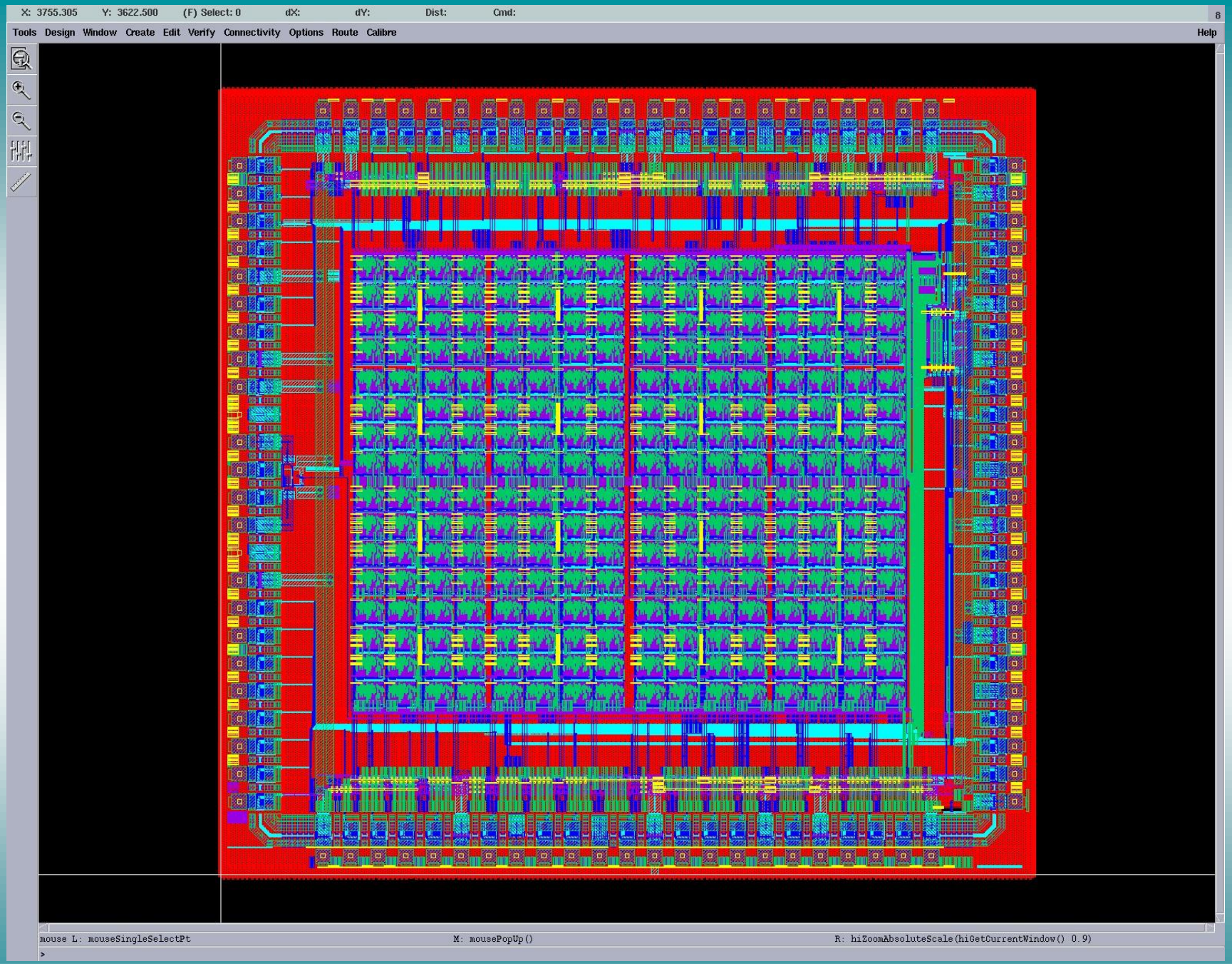
5X Performance
1/10th Power

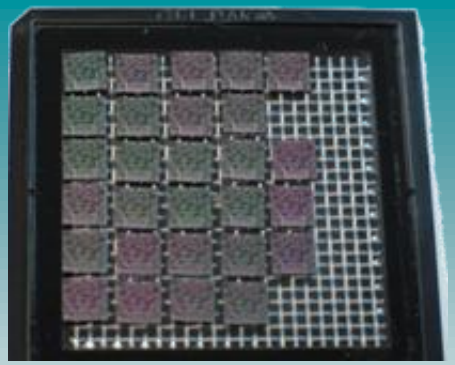


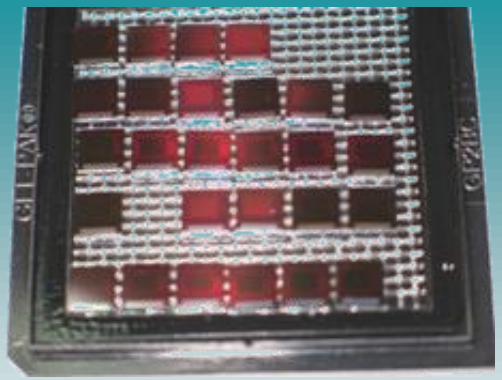
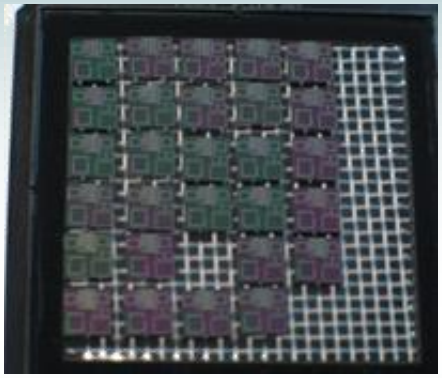
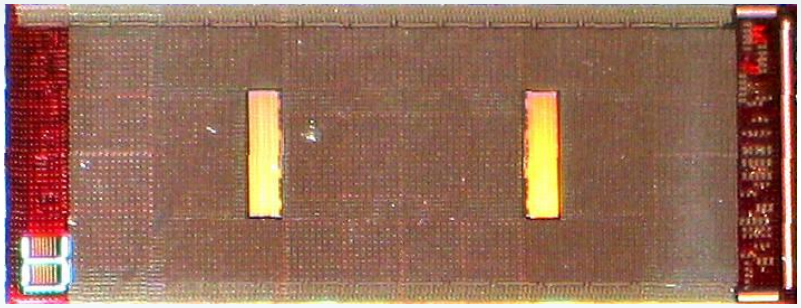
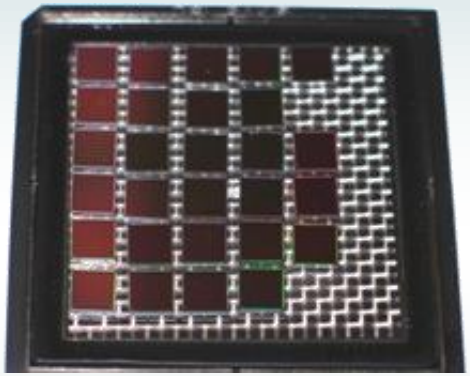


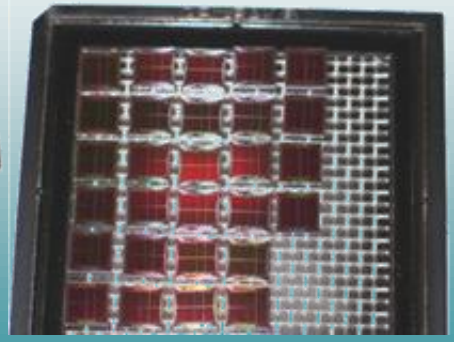
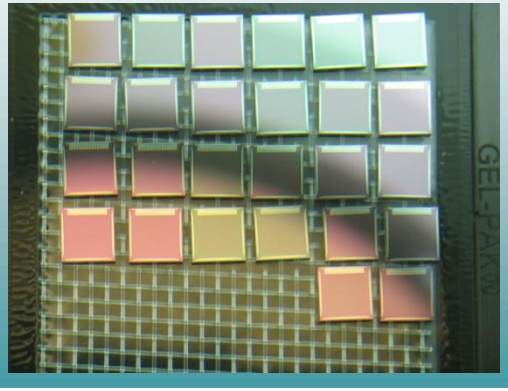


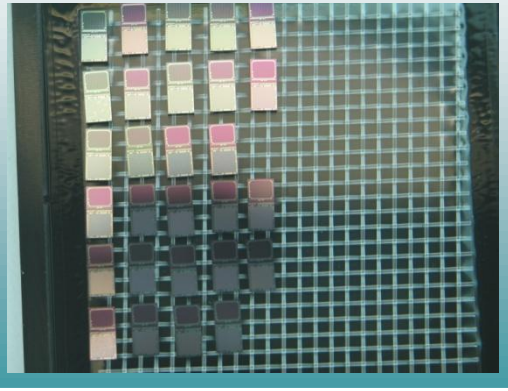



X: 3755.305 Y: 3622.500 (F) Select: 0 dX: dY: Dist: Cmd:
Tools Design Window Create Edit Verify Connectivity Options Route Calibre Help
mouse L: mouseSingleSelectPt M: mousePopUp() R: hiZoomAbsoluteScale(hiGetCurrentWindow() 0.9)



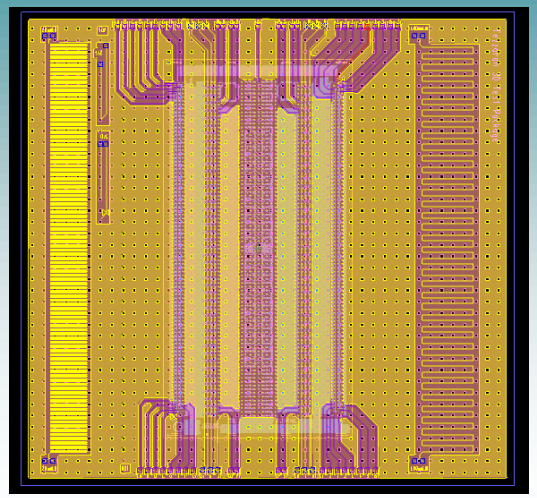



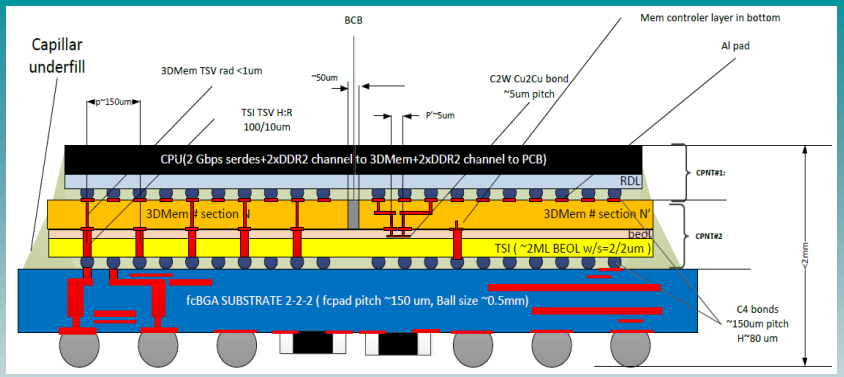


RF, Imaging,
Processing, Analog

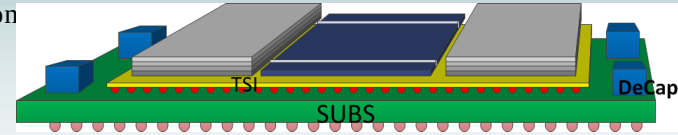
2.5/3D in Combination

IMEA-Star/ Tezzaron Collaboration





IMEA-Star / Tezzaron Collaboration



μBumps

Die to Wafer Cu Thermal Diffusion Bond

C4 Bumps

3 Layer 3D Memory

2 Layer Processor

FPGA (4Xnm)

level#4

level#3

Active Silicon Circuit Board

level#2

Organic Substrate

level#1

level#0

Solder Bumps

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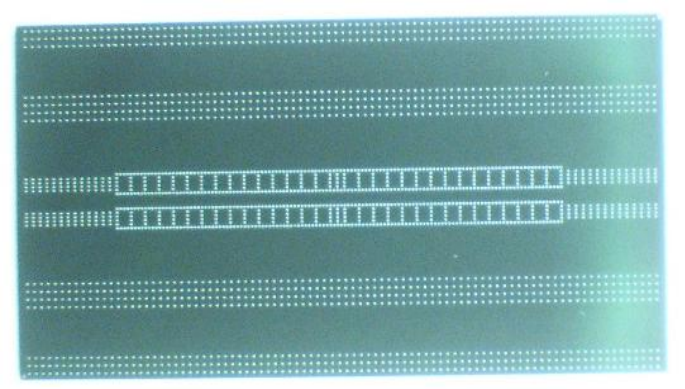
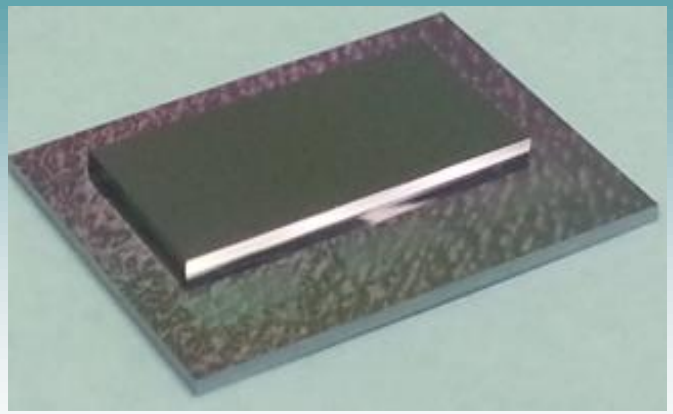
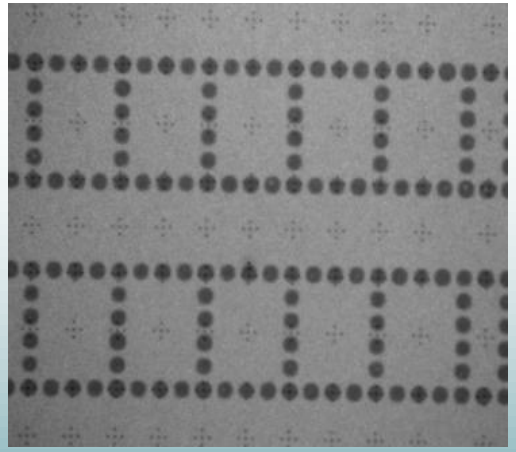
Tezzaron Dummy Chip C2C Assembly



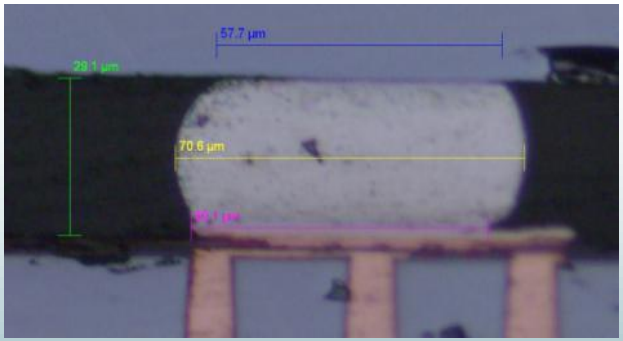
Memory die



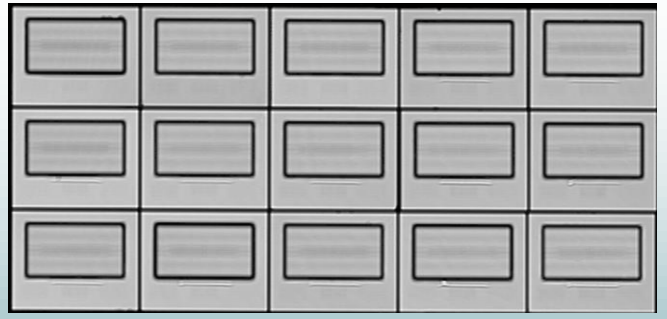
C2C sample



X-ray inspection indicated no significant solder voids

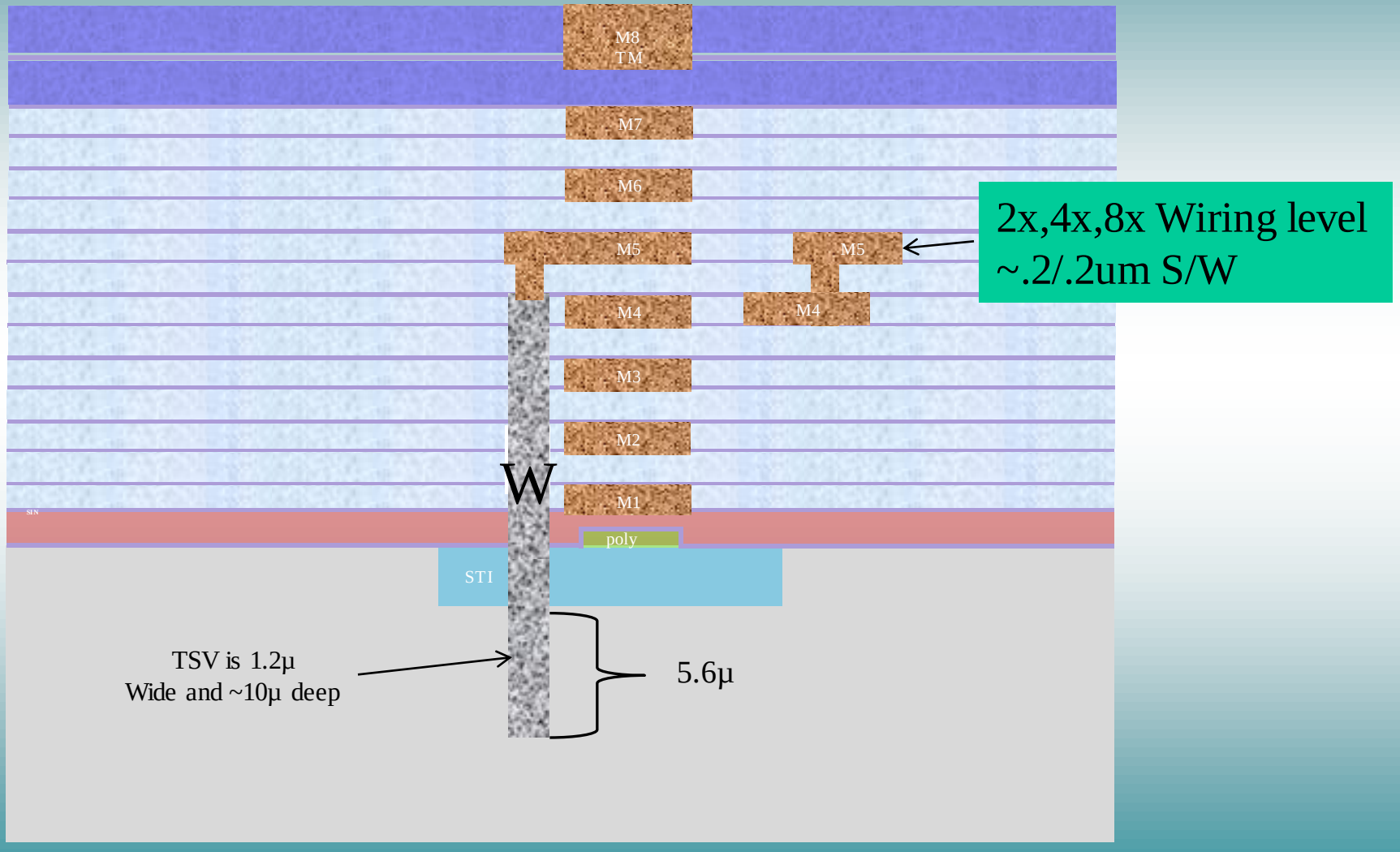


X-section of good micro bump

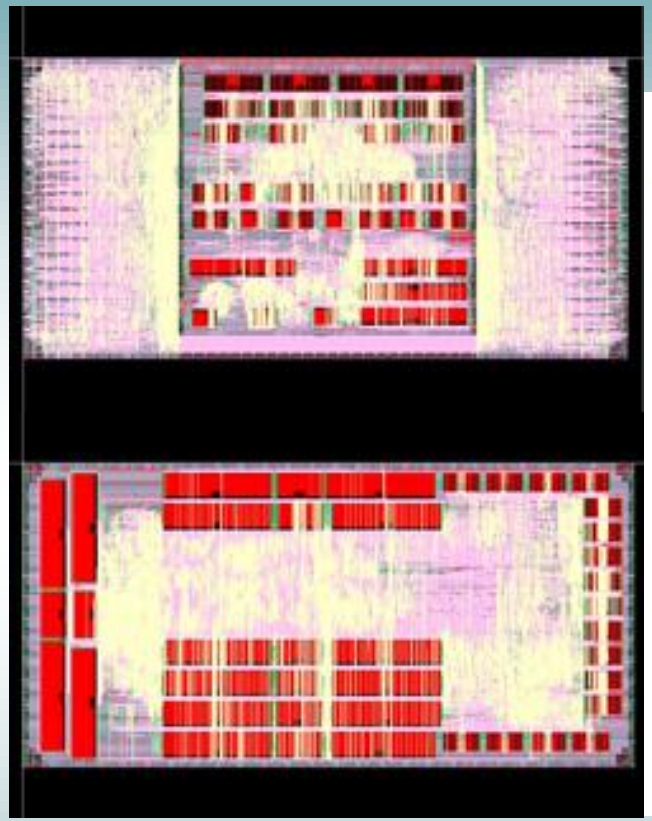


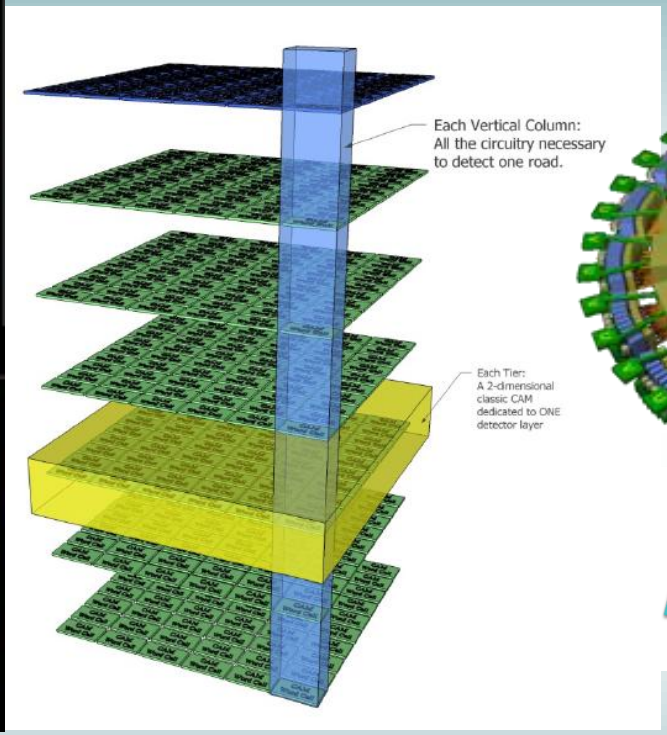
CSCAN showed no underfill voids (UF: Namics 8443-14)

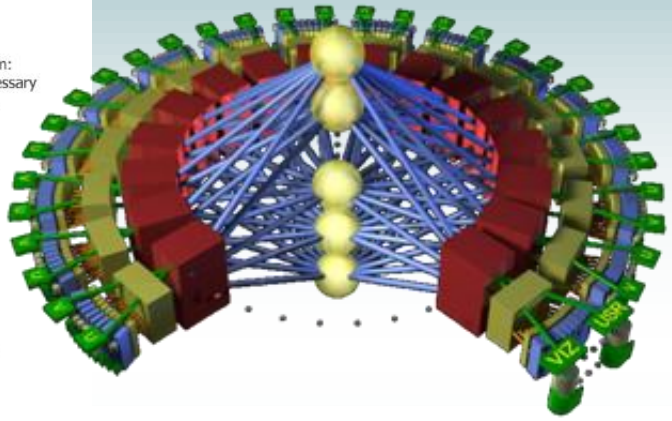
Near End-of-Line

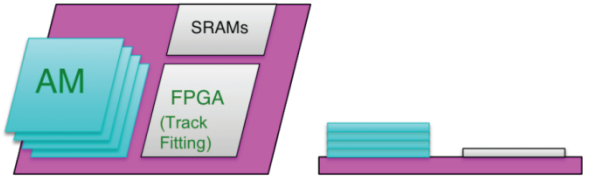


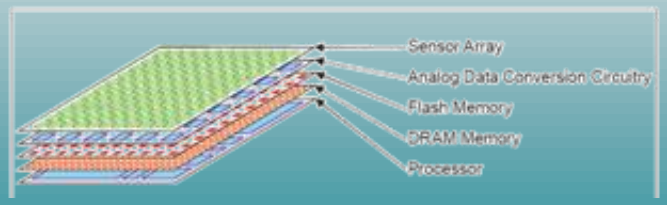
New Apps – New Architectures





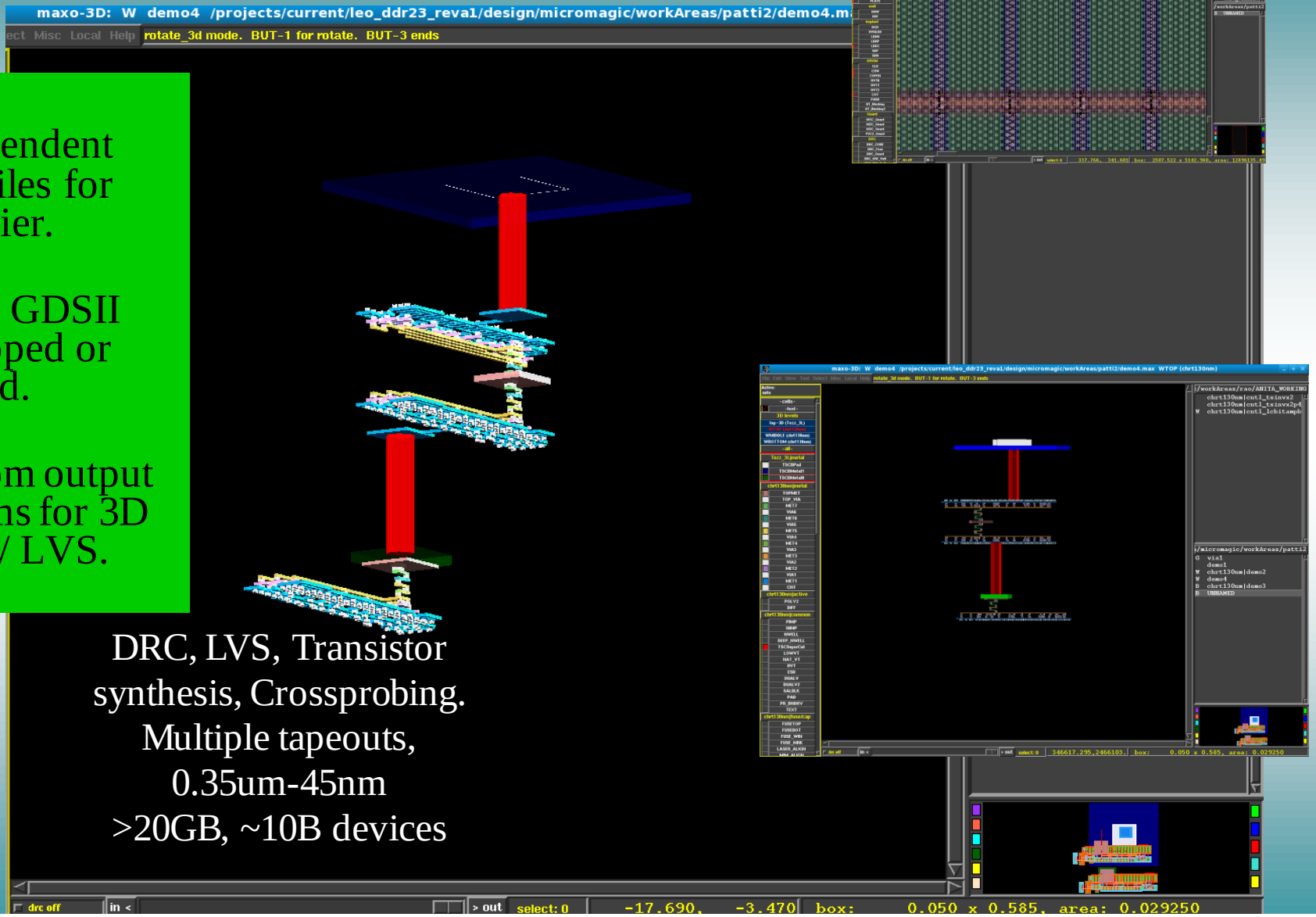






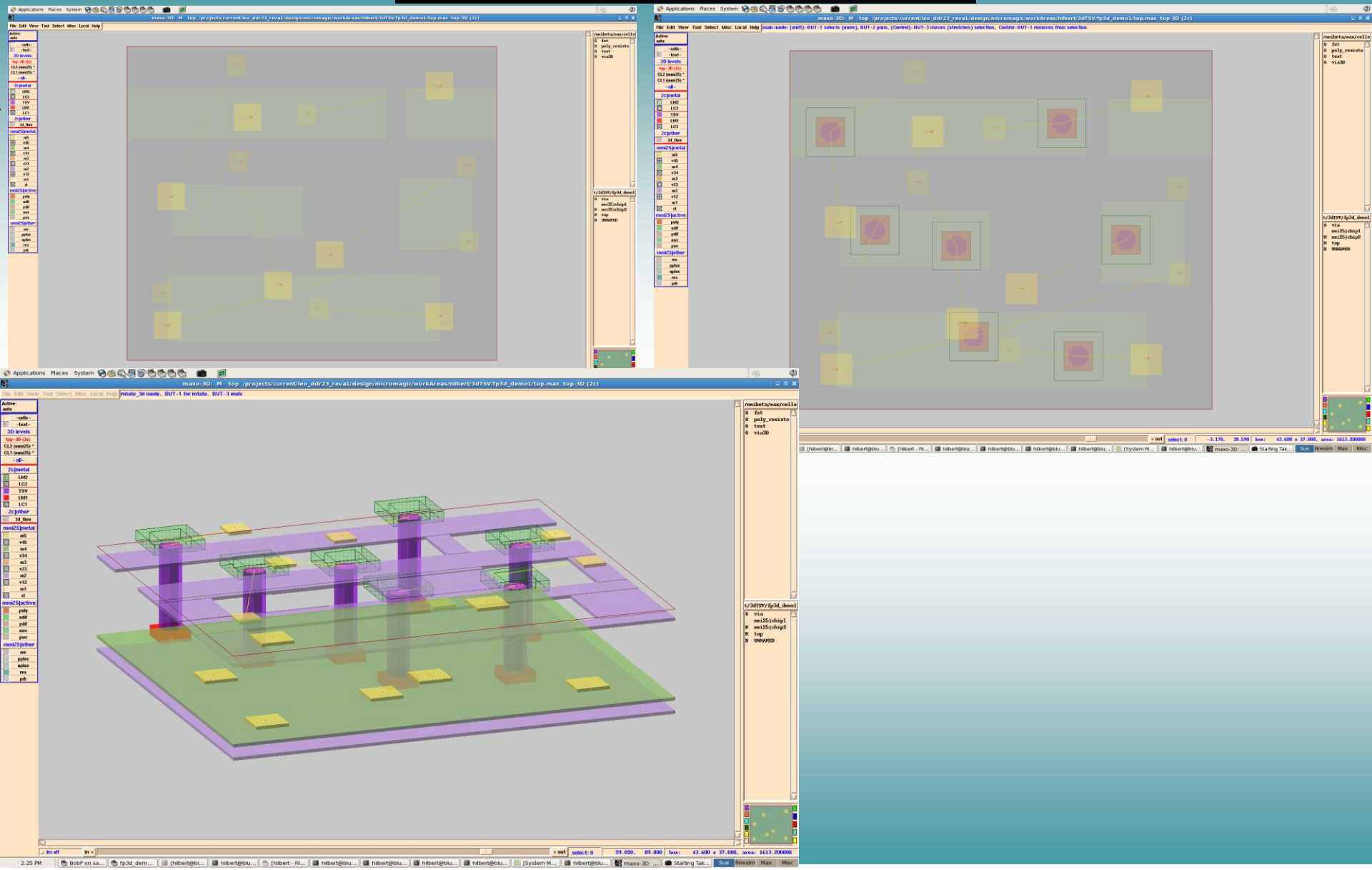
MAX-3D by Micro Magic, Inc.
Fully functional 3D layout editor.

- Independent tech files for each tier.
- Saves GDSII as flipped or rotated.
- Custom output streams for 3D DRC / LVS.



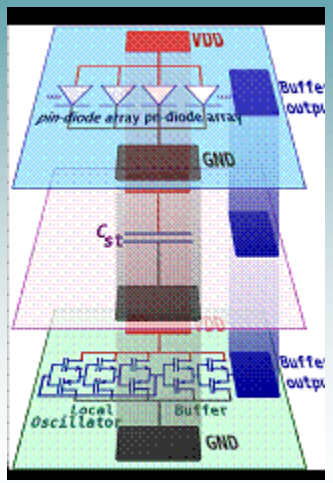
DRC, LVS, Transistor synthesis, Crossprobing.
Multiple tapeouts,
0.35um-45nm
>20GB, ~10B devices

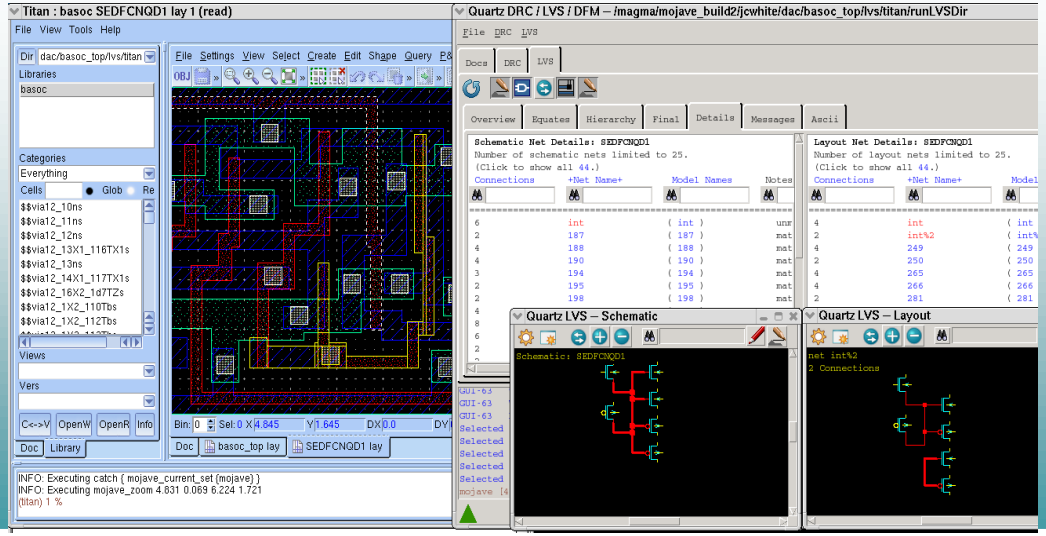
3D Place & Route



3D LVS using QuartzLVS from Magma

- Key features
  - LVS each of the 2D designs as well as the 3D interconnections between them in a single run
  - Driven by a 3D “tech file” that specifies the number and order of layers, interconnect material, etc
  - TSV aware LVS extraction
  - Full debug environment to analyze any LVS mismatch






```
# 3D LVS Tech file
WAFER: 1
   LAYOUT TOP BLOCK: lvslayer1_1
   SCHEMATIC TOP BLOCK: lvslayer1
   GDSII FILE: lvslayer1_1.gds
   SCHEMATIC NETLIST: lvslayer1.sp
   INTERFACE UP METAL: 1;0
   INTERFACE UP TEXT: 1;101
...
INTERFACE:
   LAYOUT TOP BLOCK: lvstop
   SCHEMATIC TOP BLOCK: lvstop
   GDSII FILE: lvstop_ALL.gds
   SCHEMATIC NETLIST: lvstop.sp
   BOND OUT METAL: 5;0
   BOND OUT TEXT: 5;101
```

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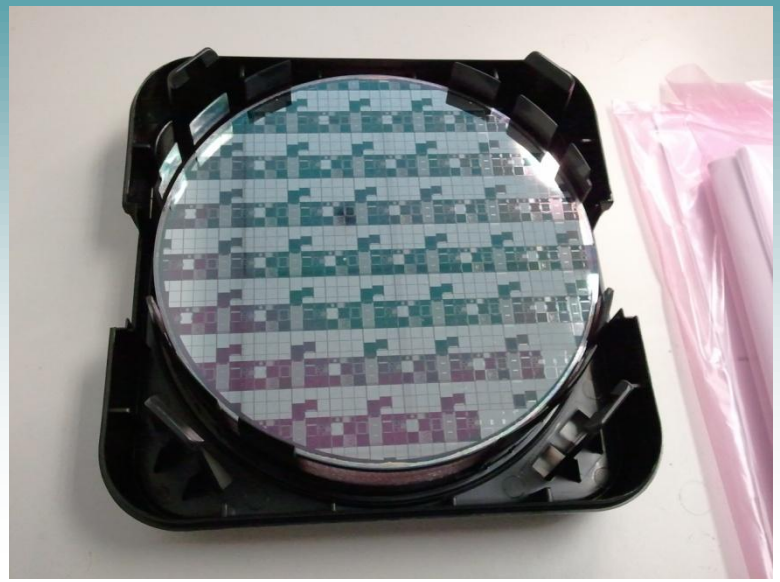
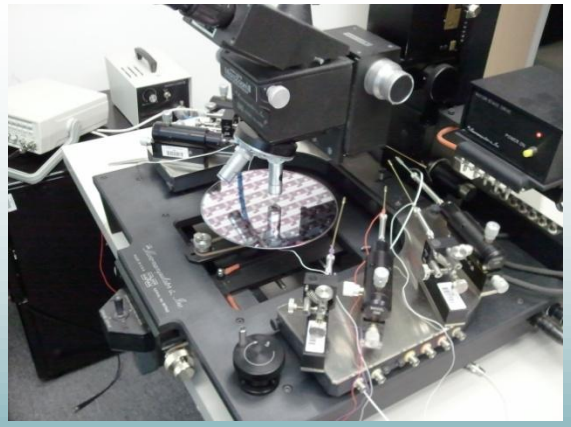
Challenges

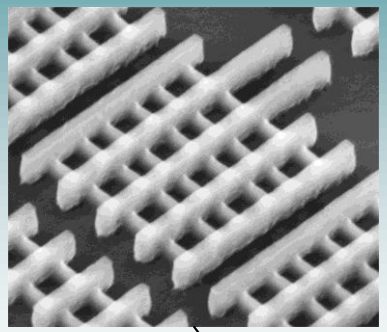
- Tools
  - Partitioning tools
  - 3D P&R
- Access
- Heat
- Testing
  - IEEE 1500
  - IEEE 1149
- Standards
  - Die level
    - JEDEC JC-11 Wide bus memory
  - Foundry interface

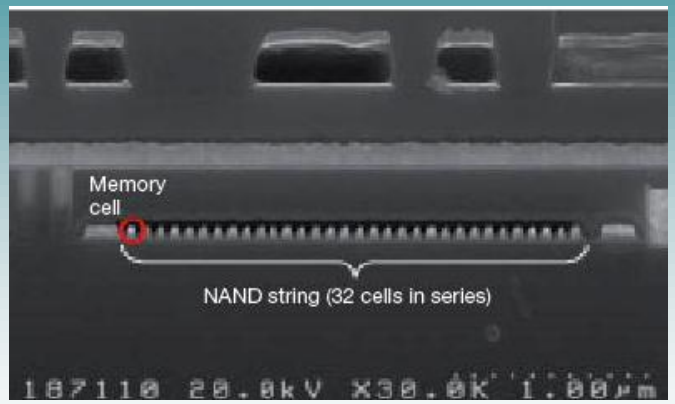




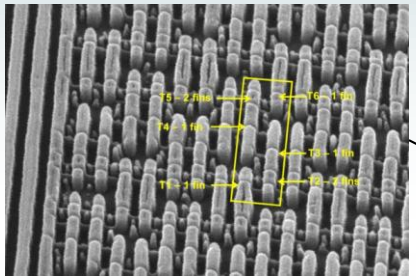
3D Key to Enable Next Gen

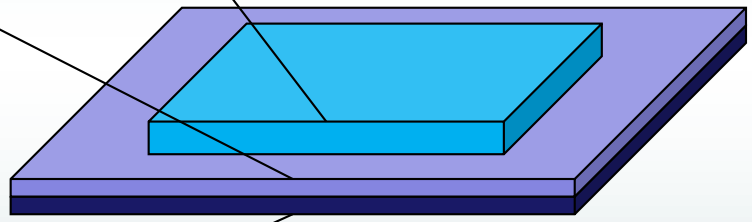
16nm Sea-of-Gates

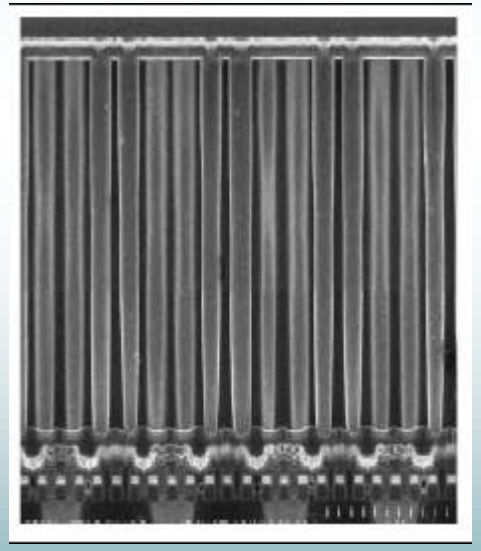


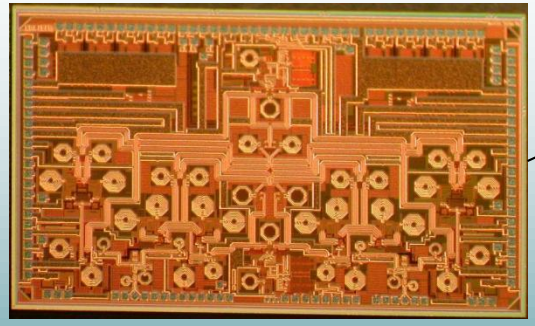


14nm Sea-of-SRAM









65nm Analog and I/O

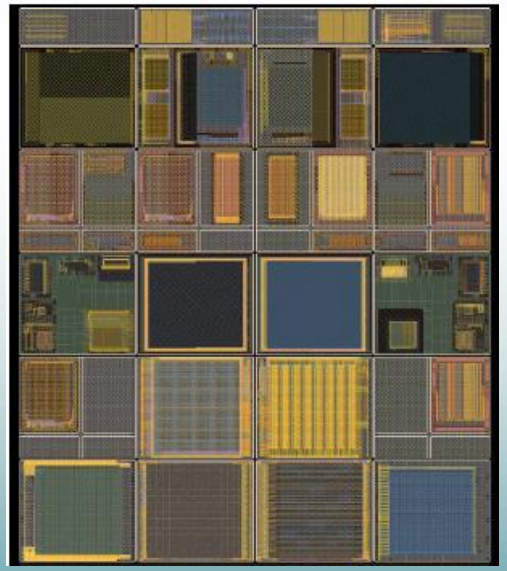
IP isolation Optimized Process Simplified Technology Real Reuse

Tezzaron/Novati 3D Technologies

- "Volume" 2.5D and 3D Manufacturing in 2013
- Interposers
- Future interposers with
  - High K Caps
  - Photonics
  - Passives
  - Power transistors
- Wholly owned Tezzaron subsidiary
- Cu-Cu, DBI®, Oxide, IM 3D assembly

2.5/3D Design Enablement

- Complete 3D PDK 8th Release
  - GF 130nm
  - Synopsys, Hspice, Cadence, MicroMagic 3D physical editor
  - Calibre 3D DRC/LVS
  - Artisan standard cell libraries
- MOSIS, CMP, and CMC MPW support
  - 130nm, coming soon 65nm
  - Silicon Workbench
- Honeywell 150nm SOI
- NEOL TSV insertion
- 40→28nm 3D logic
- Silicon interposers, active, photonics
- Organic interposers
- >100 devices in process
- >500 users

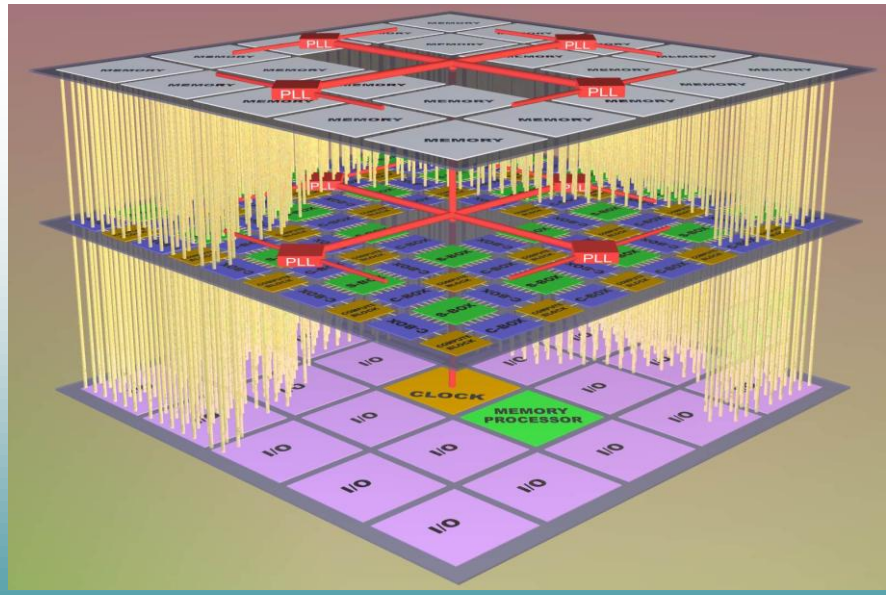


Summary

- 3D has numerous and vast opportunities!!
  - New design approaches
  - New ways of thinking
  - Best of class integration of
    - Memory
    - Logic
    - RF
    - MEMS

Sensors

Computing

MEMS

Communications