3D Integration:

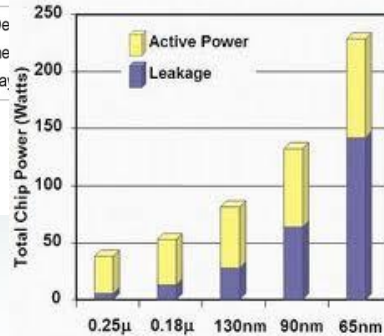# New Opportunities for Speed, Power and Performance

Robert Patti, CTO
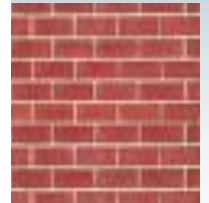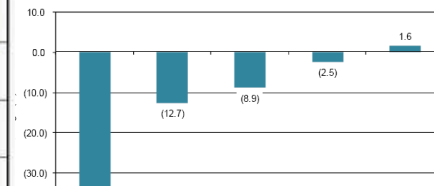
rpatti@tezzaron.com

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Why We Scale?

Speed
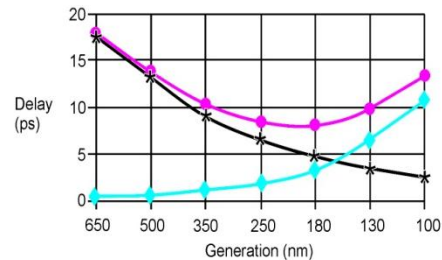
Power

Cost

Size

Advantages
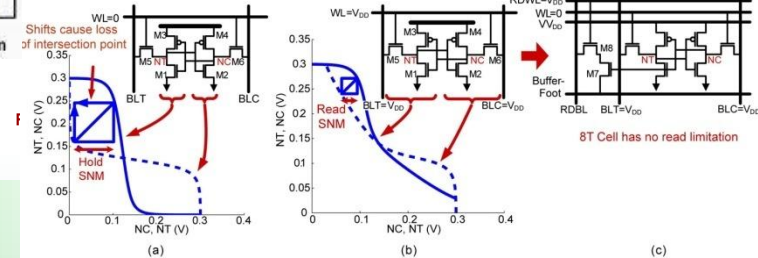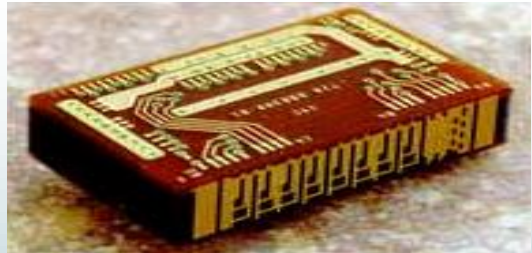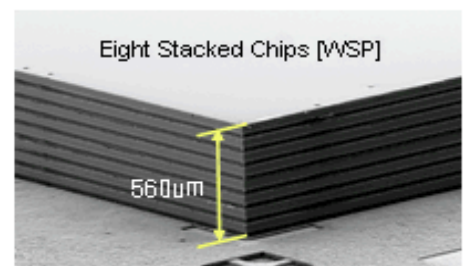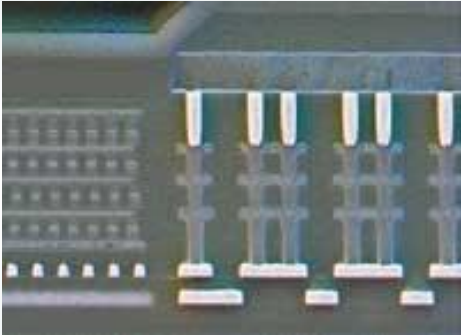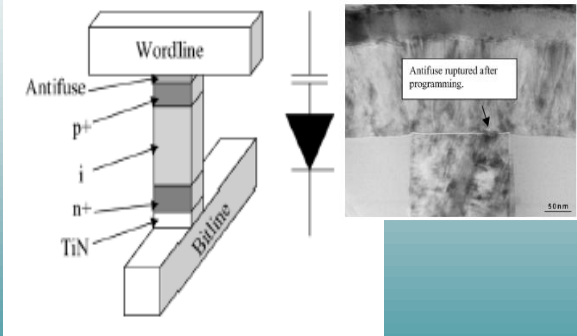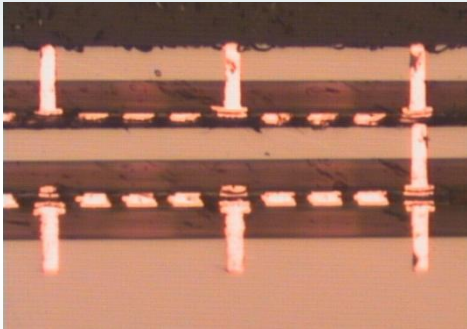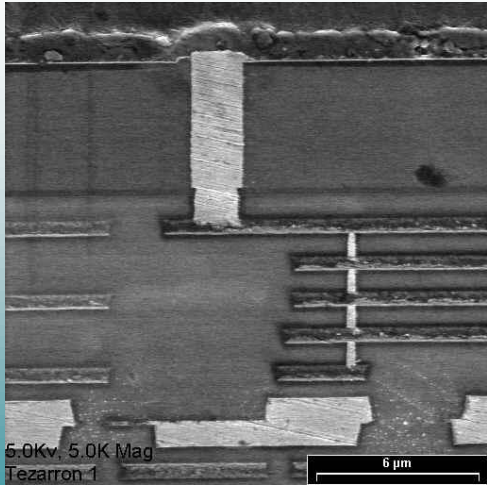
>180nm   130nm   90nm   65nm   45nm   28nm   22nm   16nm

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The Effect of 2.5/3D on Devices

Legend:
- Transistors
- Transistors with 3D
- Frequency
- Frequency with 3D

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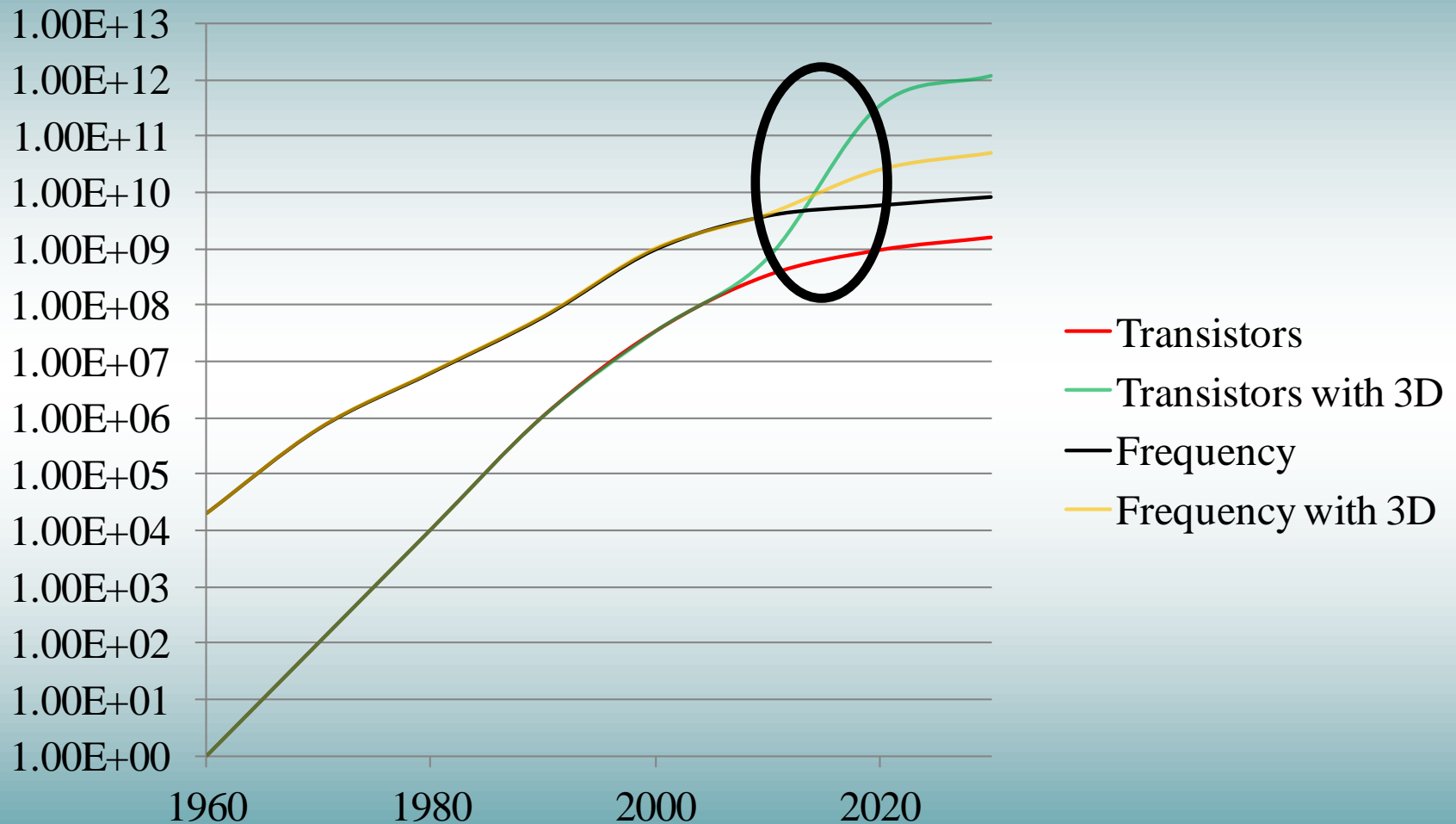
3D Stacking Approaches

Chip Level	Device Level	Wafer Level
• **Ziptronix** • **Xan3D** • **Vertical Circuits**	• **Stanford** • **Besang**	• **Infineon/IBM** • **RPI** • **ZyCube**

Amkor : 4S CSP (MCP)

Matrix: Vertical TFT

Tezzaron

Irvine Sensors : Stacked Flash

Samsung : Stacked Flash

Eight Stacked Chips [WSP]

560um

Wordline
Antifuse
p+
i
n+
TiN
Bitline

Antifuse ruptured after programming.

5.0Kv. 5.0K Mag
Tezarron 1
6 µm

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Wafer Level Stacking Approaches

Infineon/IBM	RPI/ Ziptronix/ ZyCube	Tezzaron

Infineon : W deep via
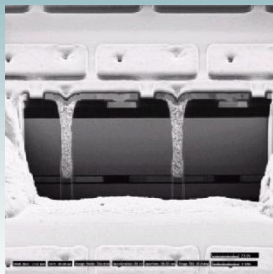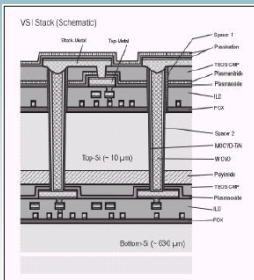
IBM : SOI wafer thinning
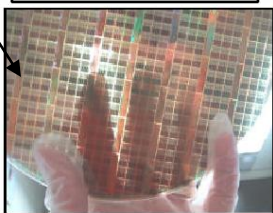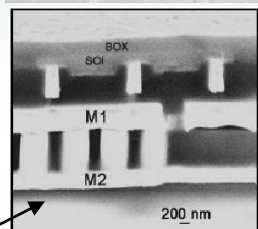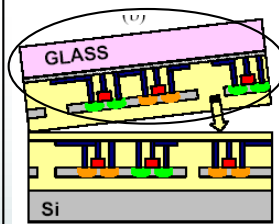
RPI : Dielectric bonding
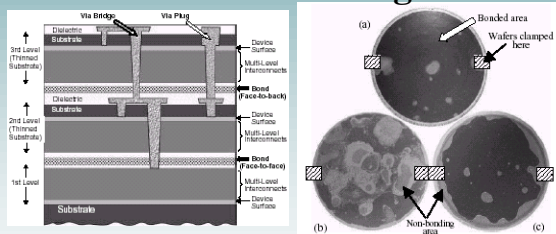
Ziptronix : Covalent bond

A. Start Bond - t = 0 sec   B. t = 1.5 sec   C. Bond Complete - t = 4.2 sec
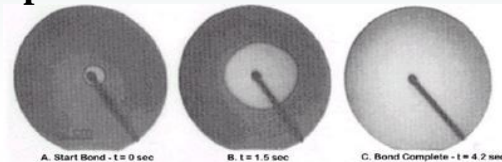
ZyCube : Injection glue bonding
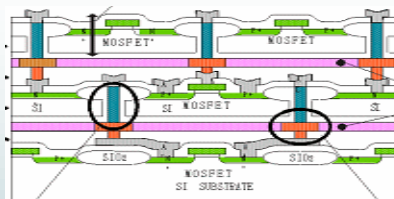
Tezzaron : Copper bonding
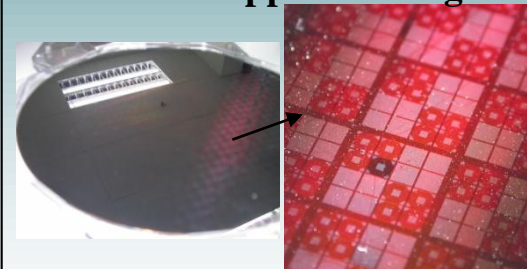
Backside of the stacked wafer
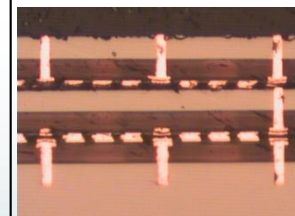
3 wafer stack   **3D Sensor**

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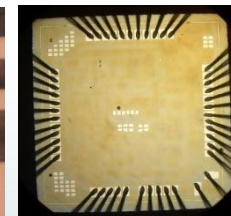
Market Drivers: 3D

Driver	Functionality	Technical Parameter # 1	Technical Parameter # 2	Value Indicator
Stacked NAND Flash	Cell Phones Hard Drives Flash Drives	Memory density		High packing density
Micro-processor + Memory	Workstations	Latency bandwidth	Power	Execution time
Memory	Multiple	Density	Latency	Varies
Image Sensor	Cell Phones Cameras Automotive	Quantum Efficiency	Number of pixels	Image Quality

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There is a lot of 3D today

Samsung
16Gb NAND flash (2Gx8 chips),
Wide Bus DRAM

560µ

Micron
Wide Bus DRAM

Intel
CPU + memory

Cover glass
Electrode pad
Buried interconnects
Sensor chip

OKI
CMOS Sensor

TSV connections

Xilinx
4 die 65nm interposer

Top chip (45)
Interco
TSV
Bottom chip (130)
Substrate
Leti ST

Raytheon/Ziptronix
PIN Detector Device

Structure of Toshiba's new NAND memory cell
BiCS tech helps create a SONOS memory structure

8-Gigabit TSV DRAM Package Outline   Cross-section

IBM
RF Silicon Circuit Board / TSV
Logic & Analog

Toshiba
3D NAND
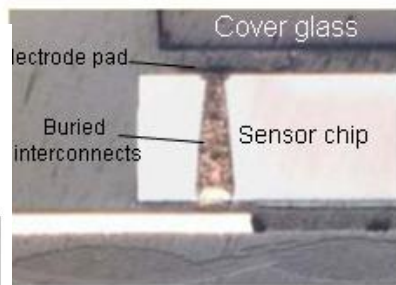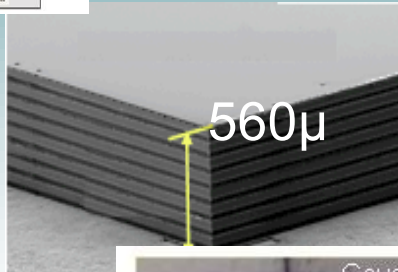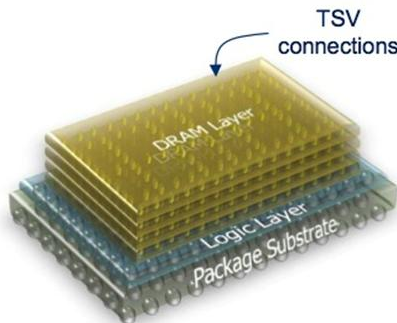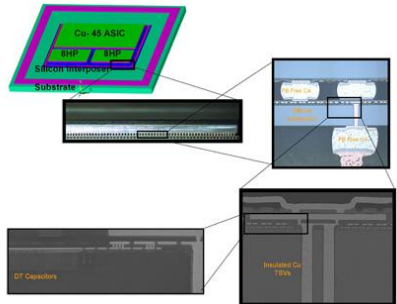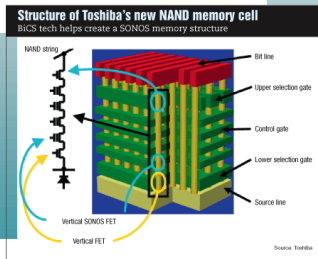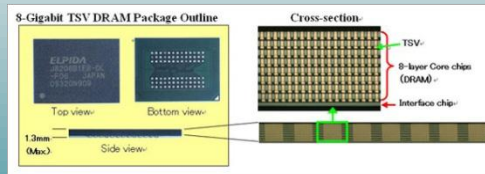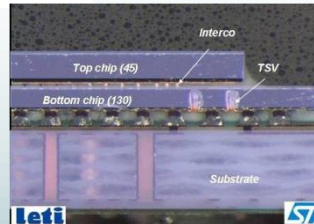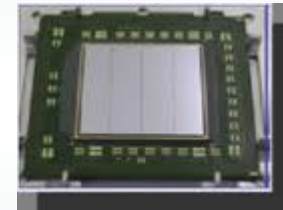
Through-Silicon Via (TSV)

- Via First

- Via Last

- Via at Front end (FEOL)

- Via at Mid line (MOL?)

- Via at Back end (BEOL)

Dr. J.Q. Lu
RPI

"SuperContact"

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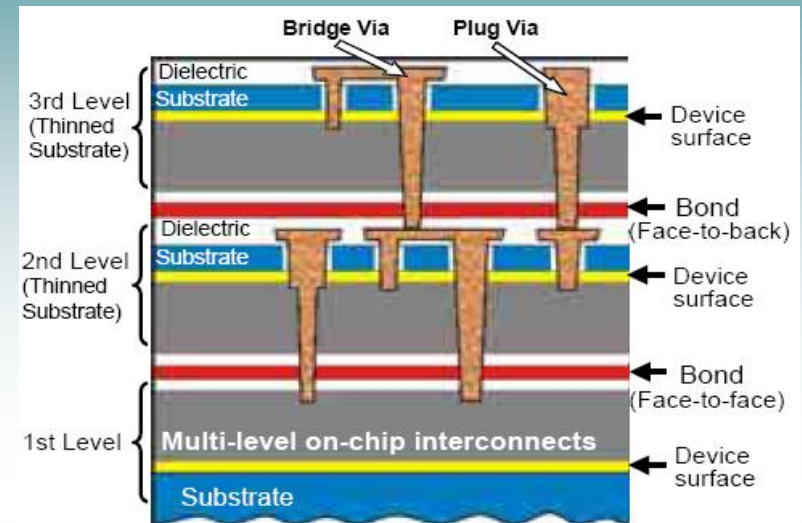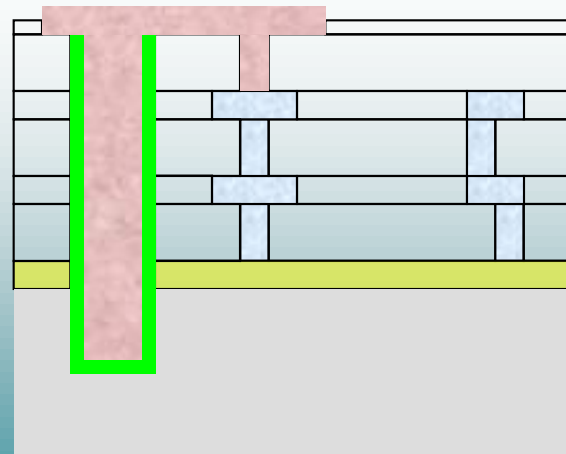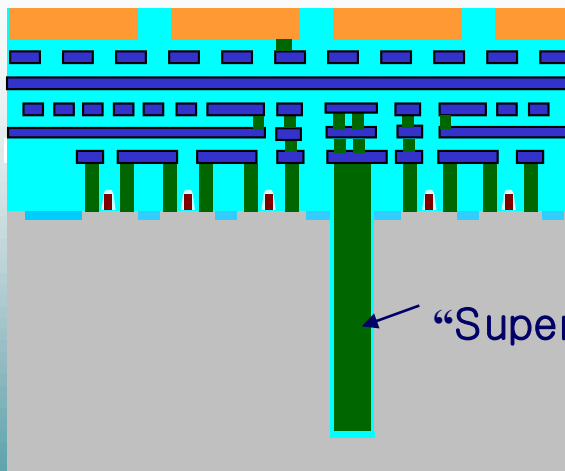
Span of 3D Integration

Packaging

Analog
Flash
DRAM
DRAM
CPU

3D Through Via Chip Stack

IBM/Samsung

Wafer Fab

CMOS 3D

IBM
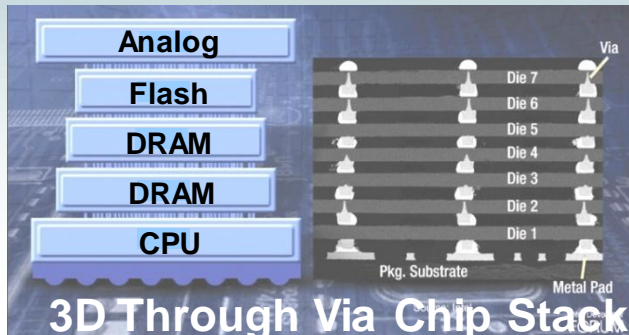
3D-ICs

100-1,000,000/sqmm

1000-10M Interconnects/device
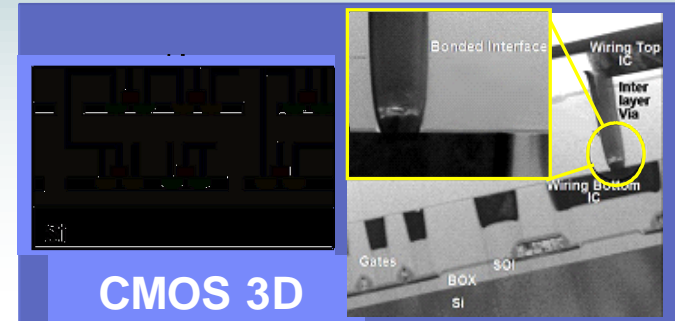
1s/sqmm

Peripheral I/O

- Flash, DRAM

- CMOS Sensors
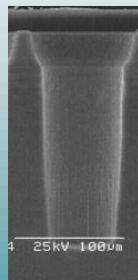
100,000,000s/sqmm

Transistor to Transistor

- Ultimate goal

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TSV Pitch ≠ Area ÷ Number of TSVs

- TSV pitch issue example
  - 1024 bit busses require a lot of space with larger TSVs
  - They connect to the heart and most dense area of processing elements
  - The 45nm bus pitch is ~100nm; TSV pitch is >100x greater
  - The big TSV pitch means TOF errors and at least 3 repeater stages

10um TSV
20um Pitch

1024 bit bus
Single layer
interconnect

F
P
U

07/07/2013

TSV Pitch ≠ Area ÷ Number of TSVs

- TSV pitch issue example
  - 1024 bit busses require a lot of space with larger TSVs
  - They connect to the heart and most dense area of processing elements
  - The 45nm bus pitch is ~100nm; TSV pitch is >100x greater
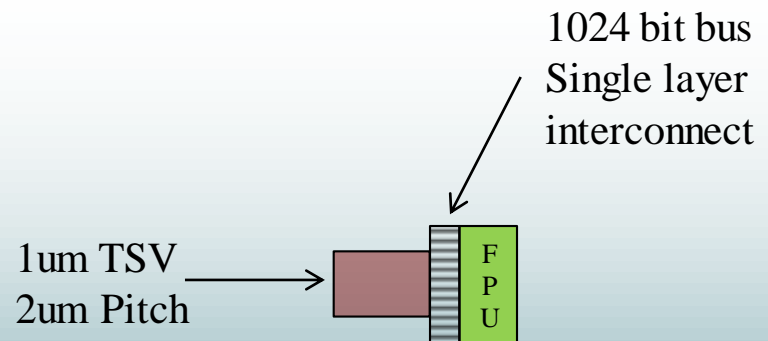 - The big TSV pitch means TOF errors and at least 3 repeater stages

1024 bit bus
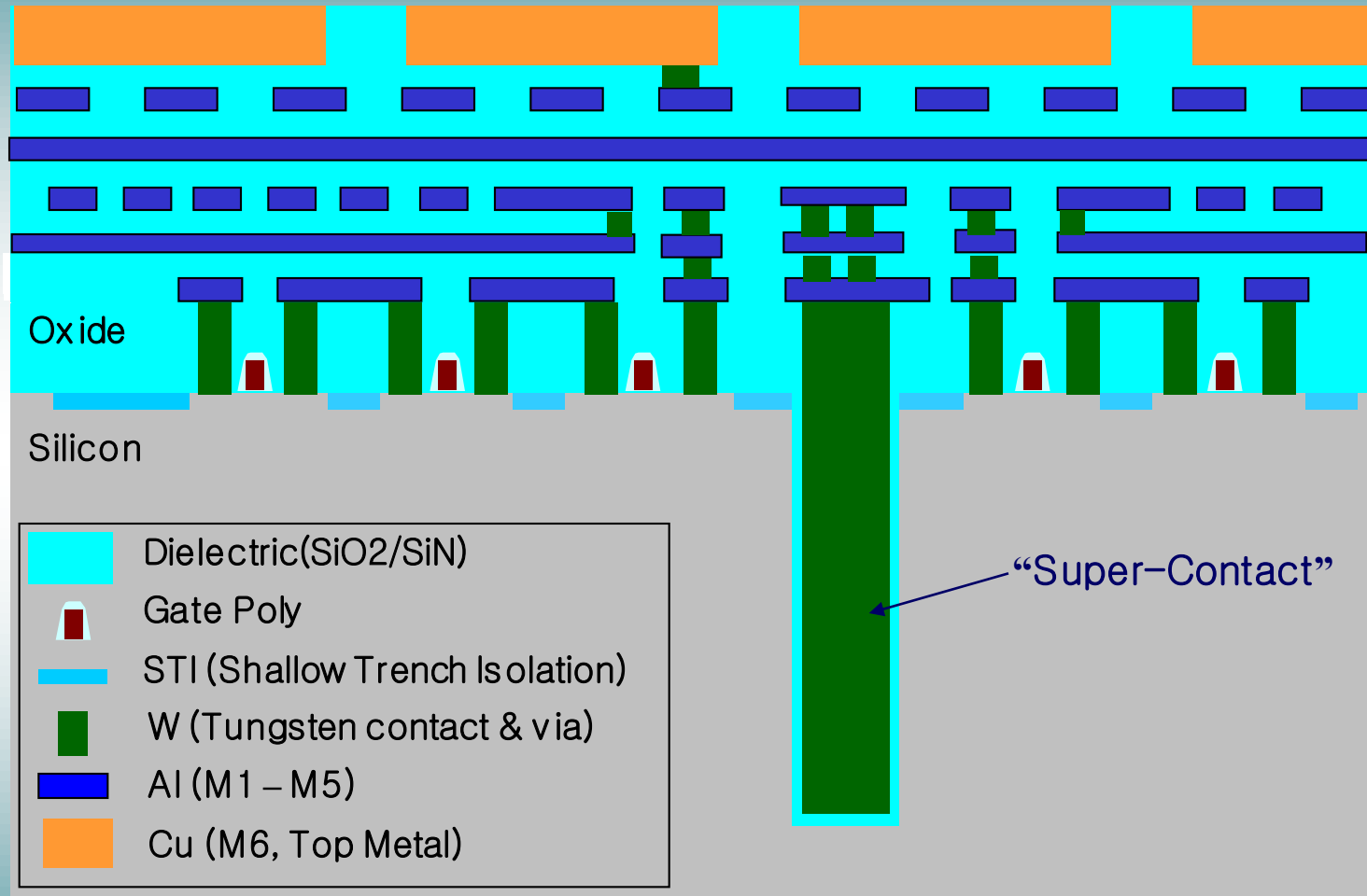Single layer
interconnect

1um TSV
2um Pitch

F
P
U

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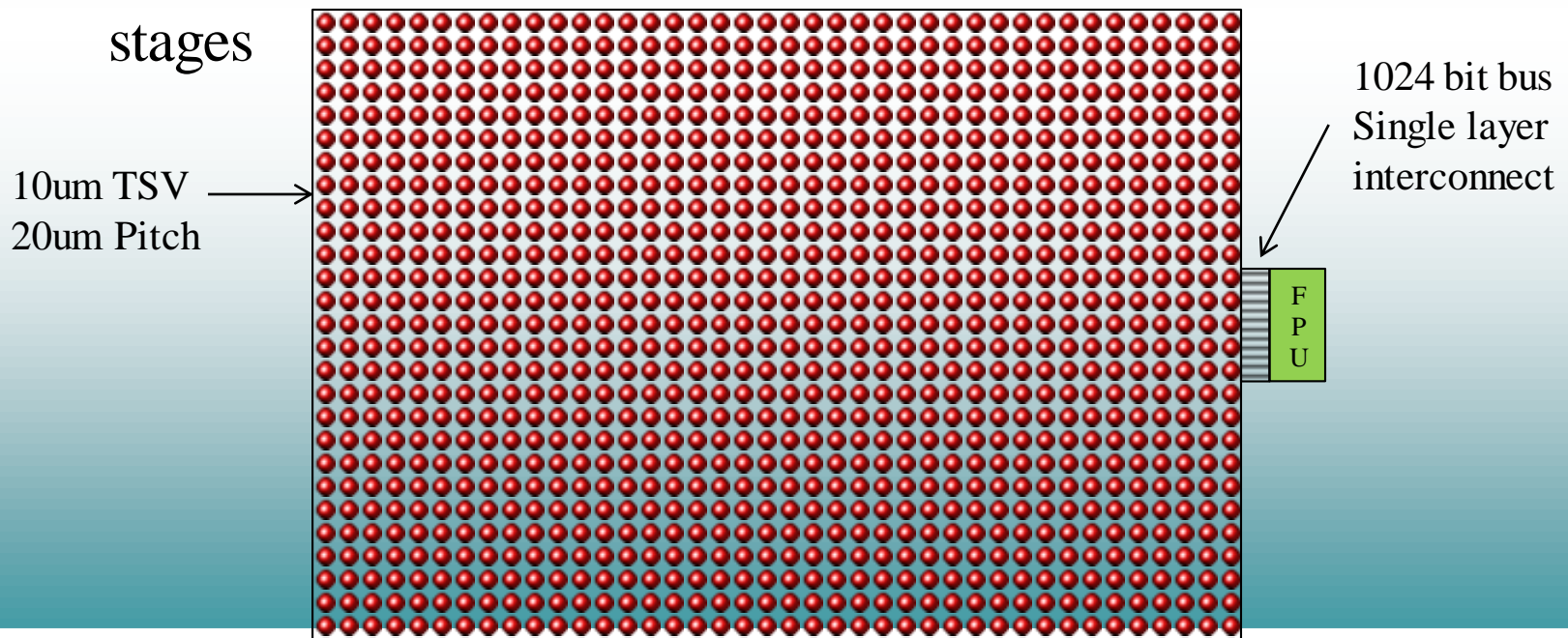
3D Interconnect Characteristics
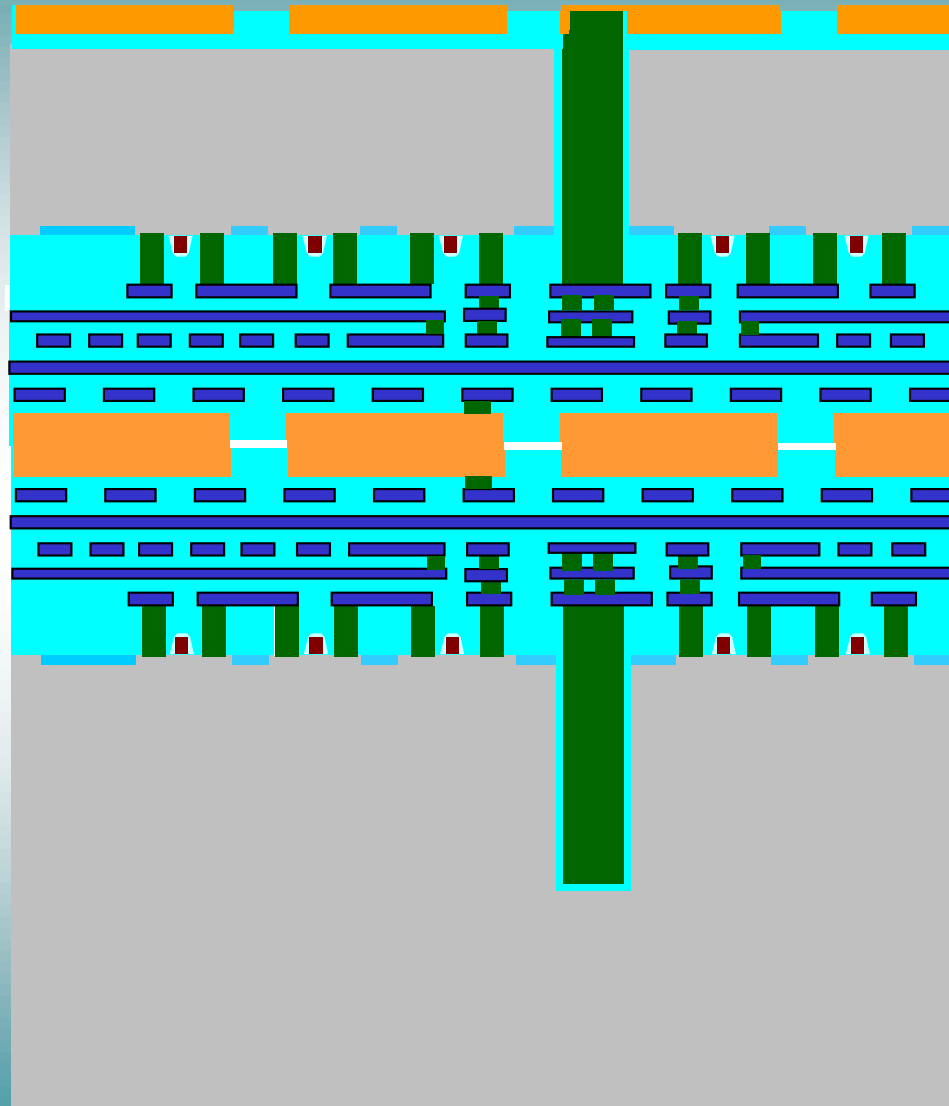
	SuperContact^{TM} I 200mm Via First, FEOL	SuperContact^{TM} III 200mm Via First, FEOL	SuperContact^{TM} IV 200mm Via First, FEOL	Interposer TSV	Bond Points	Die to Wafer
Size L X W X D Material	1.2 μ X 1.2 μ X 6.0μ W in Bulk	0.85 μ X 0.85 μ X 10μ W in Bulk	0.60 μ X 0.60 μ X 2μ W in SOI	10 μ X 10 μ X 100 μ Cu	1.7 μ X 1.7 μ Cu	3 μ X 3 μ Cu
Minimum Pitch	<2.5 μ	1.75 μ	1.2 μ	30/120 μ	2.4 μ	5 μ
Feedthrough Capacitance	2-3fF	3fF	0.2fF	250fF	<<	<25fF
Series Resistance	<1.5 Ω	<3 Ω	<1.75 Ω	<0.5 Ω	<	<

Small fine grain TSVs are fundamental to 3D enablement

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A Closer Look at Wafer-Level Stacking

Oxide

Silicon

Legend:
- Dielectric(SiO2/SiN)
- Gate Poly
- STI (Shallow Trench Isolation)
- W (Tungsten contact & via)
- Al (M1 – M5)
- Cu (M6, Top Metal)

"Super-Contact"

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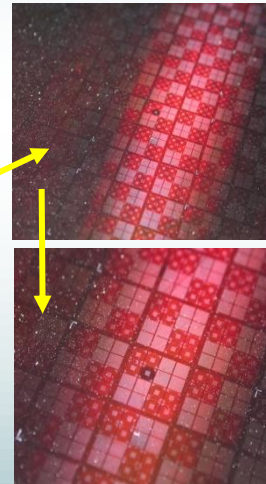
Next, Stack a Second Wafer & Thin:

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Stacking Process Sequential Picture

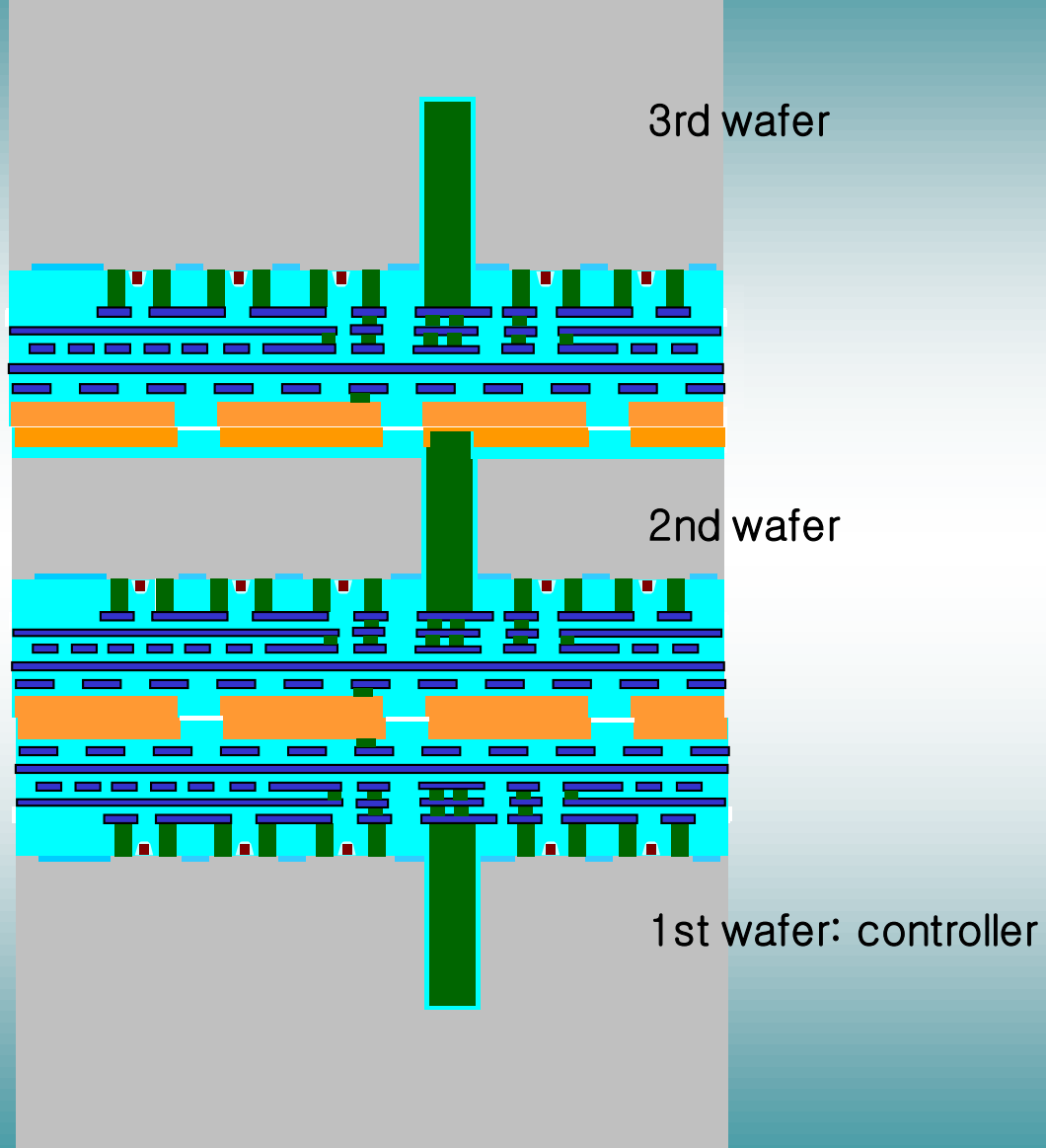**Two wafer Align & Bond** → **Course Grinded** → **Fine Grinded**

High Precision Alignment

Misalign=0.3um
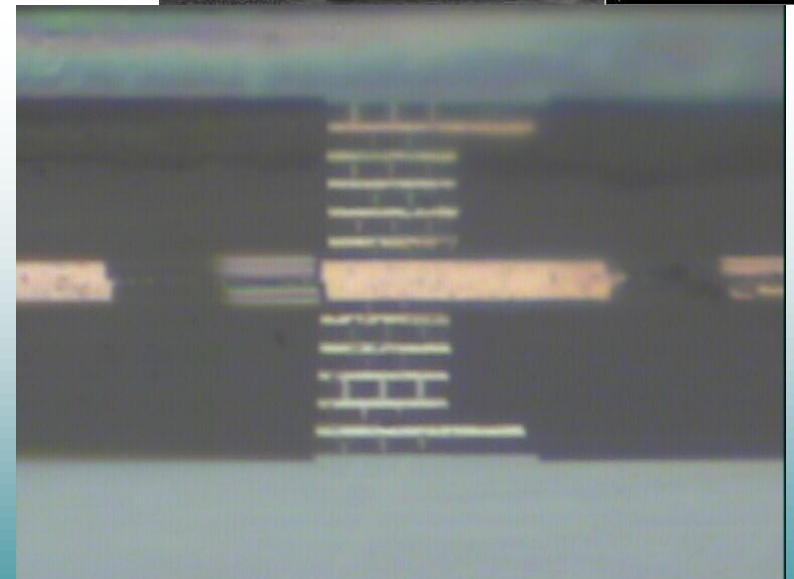
→ **After CMP** → **Si Recessed**

Top wafer

Bottom wafer

JEOL 3.6KV

Then, Stack a Third Wafer:

3rd wafer

2nd wafer

1st wafer: controller

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16
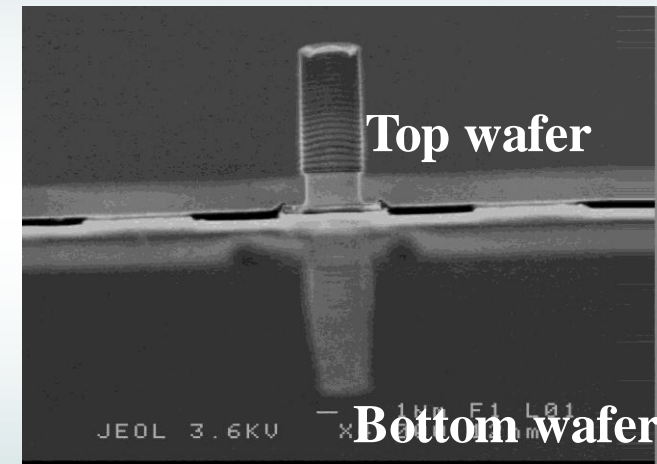
Finally, Flip, Thin & Pad Out:

1st wafer: controller

2nd wafer

3rd wafer
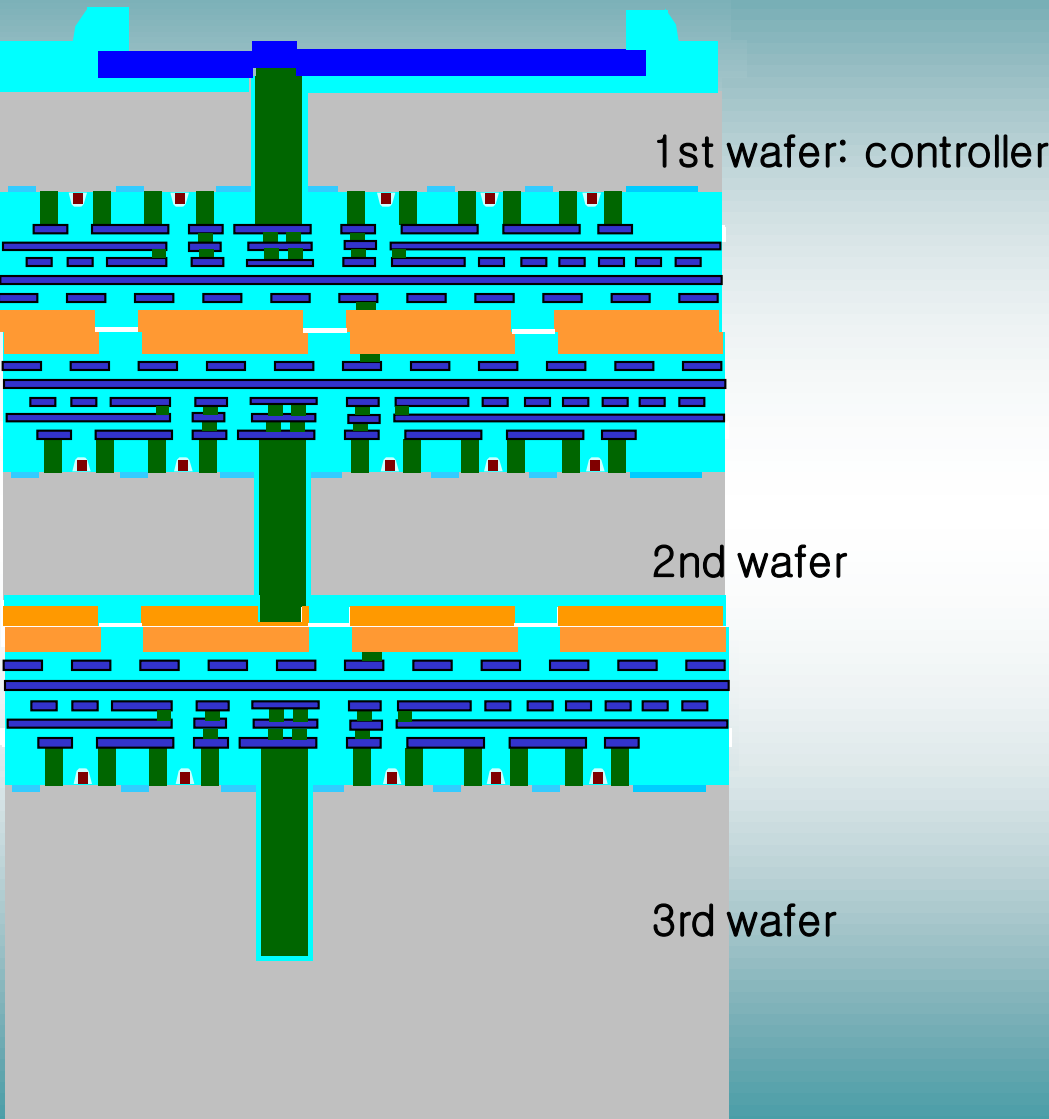
This is the
completed stack!

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17

5kV, 800X, Tezzaron
37.5 μm

5.0Kv, 1.5K Mag
Tezarron 1
20 μm

5.0Kv, 5.0K Mag
Tezarron 1
6 μm

3rd Si thinned to 5.5um

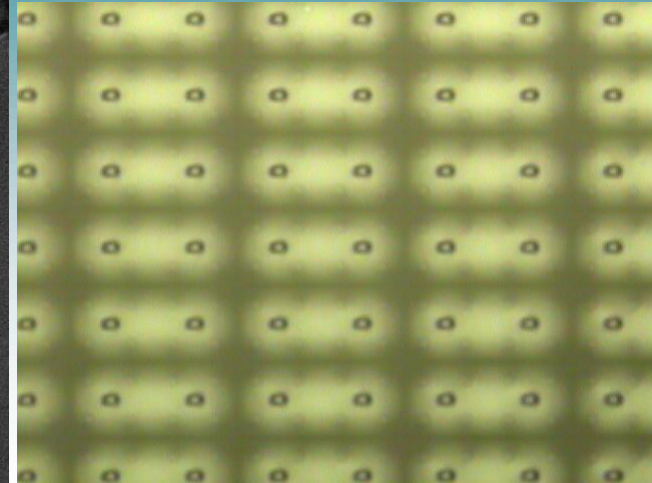**2nd Si** thinned to 5.5um

SiO₂

1st Si bottom supporting wafer

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TSVs

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Honeywell 0.6um SOI TSV

0.6um trench

0.6um via

1 µm

Dense probe pad

2.16u

FET

Isolated probe pad

2.15u

FET

1 µm

120K TSVs

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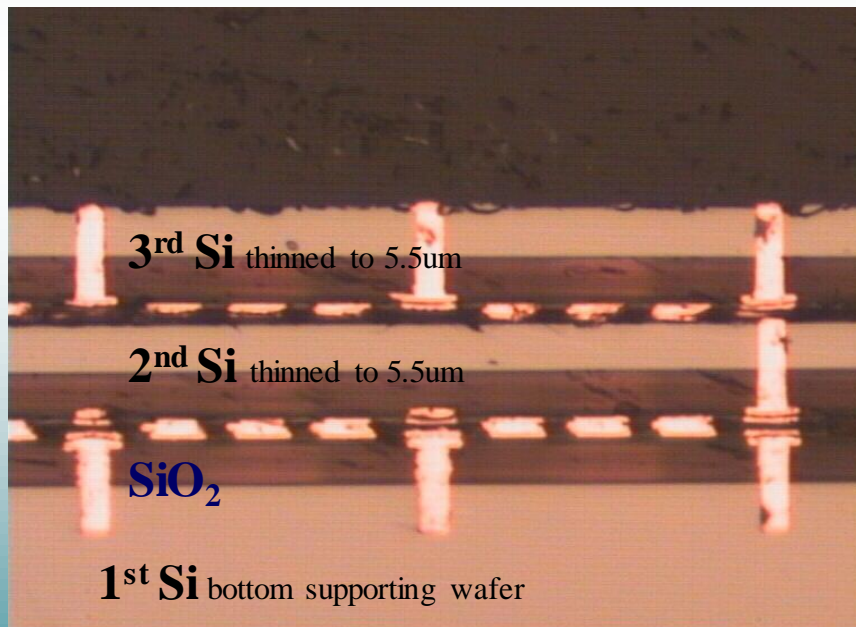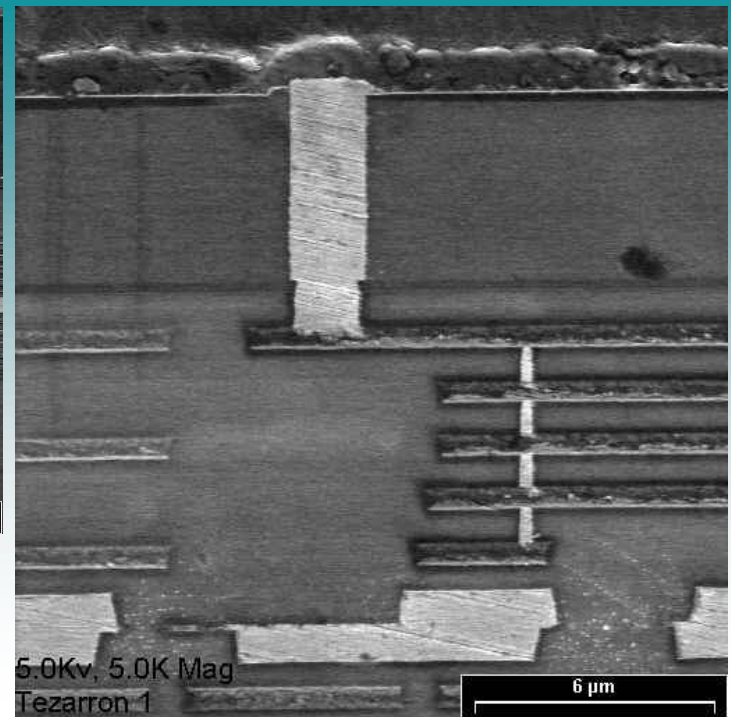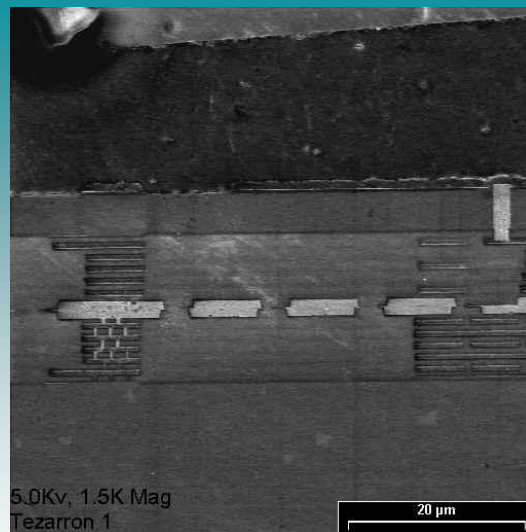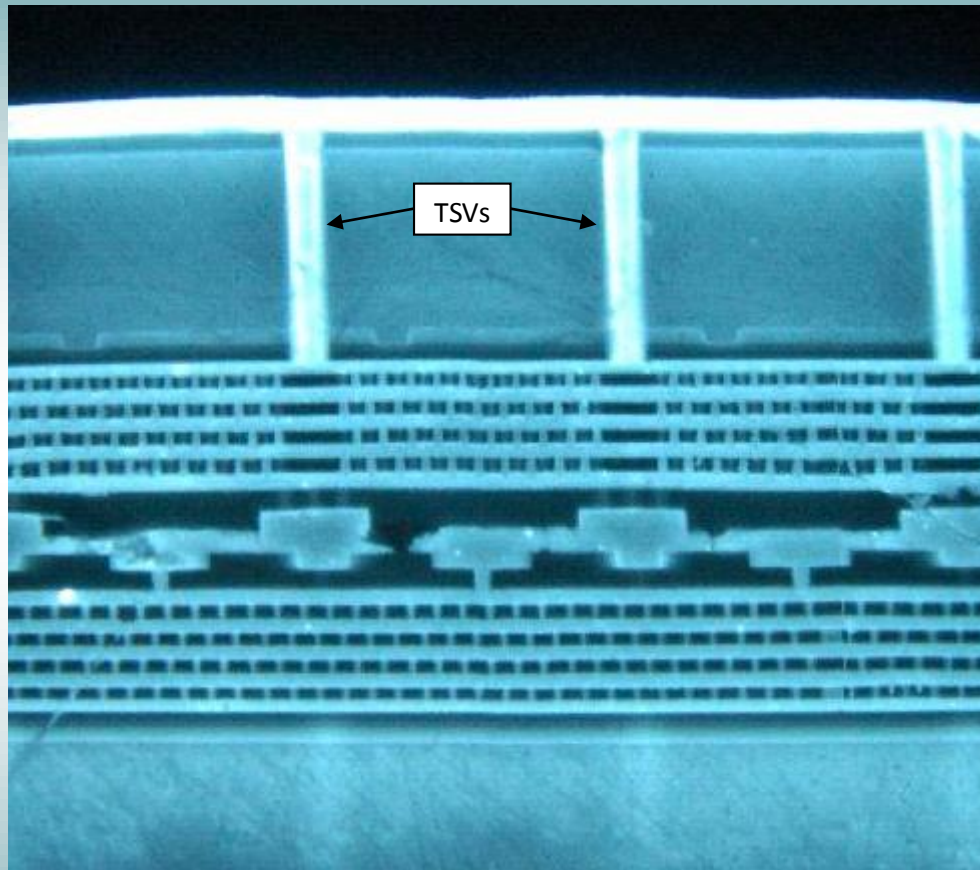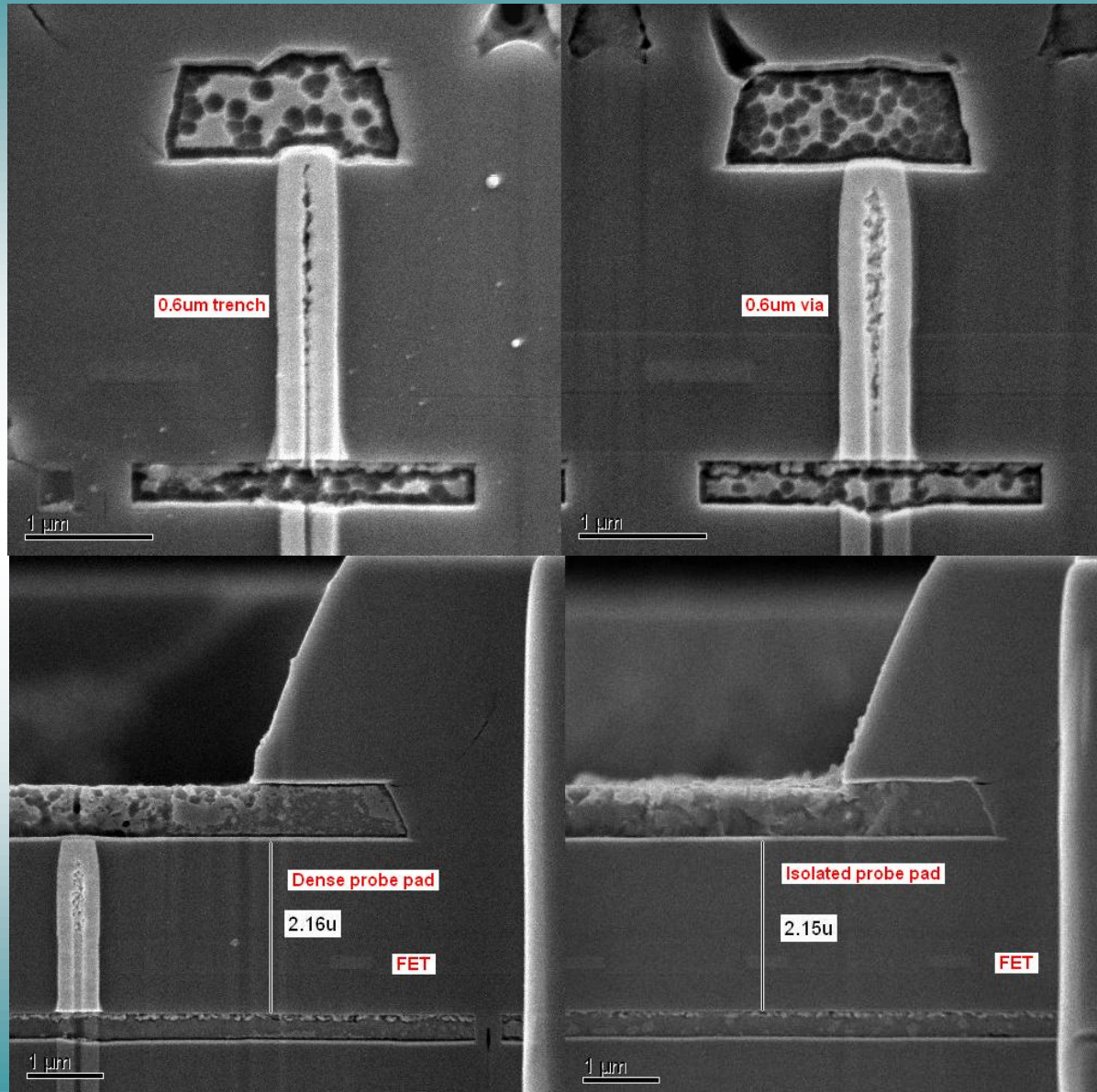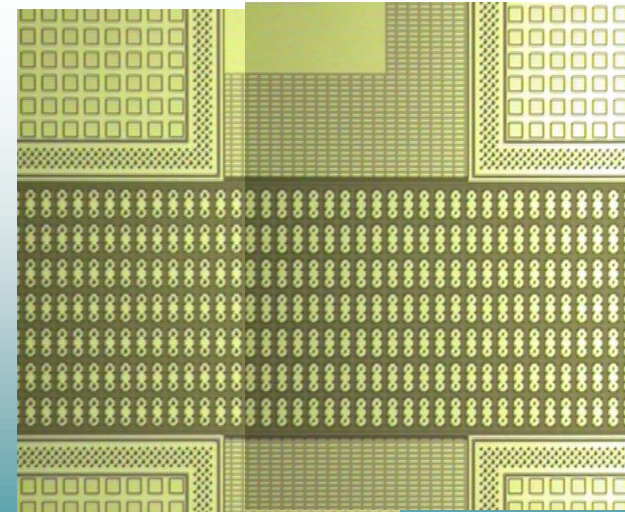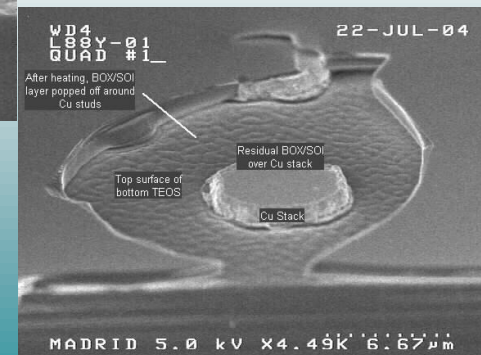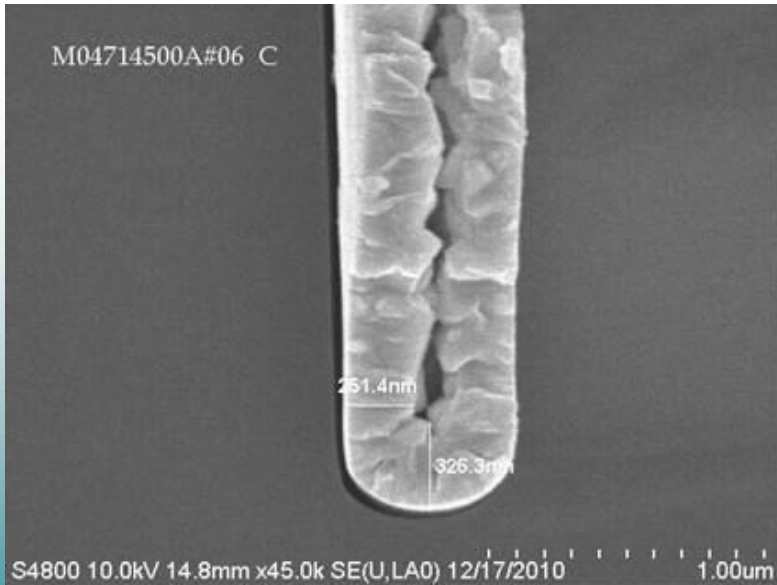
DRAM wants 2 different processes!

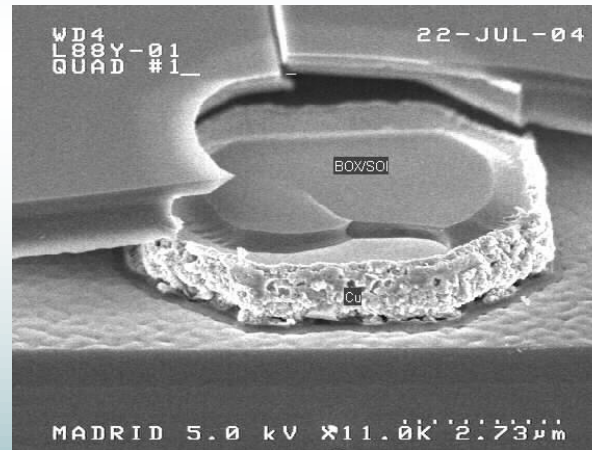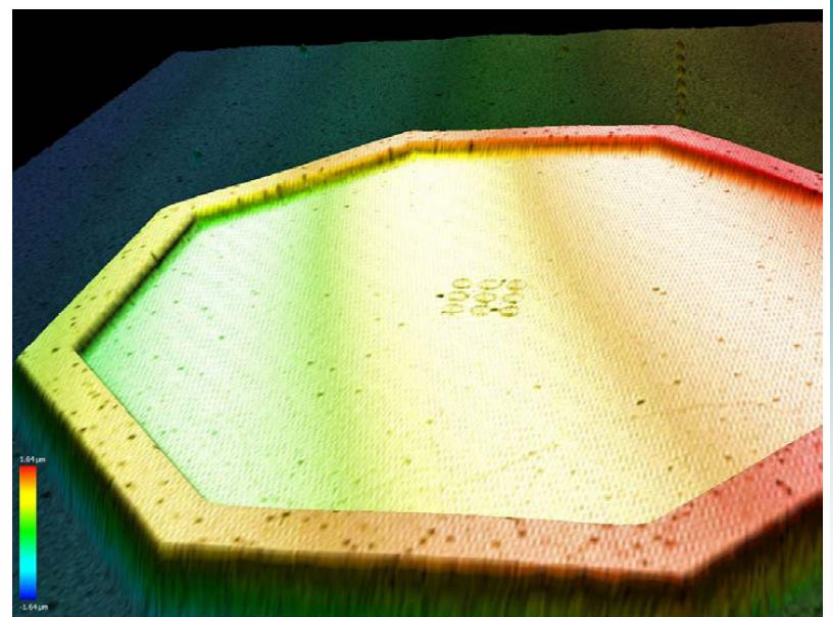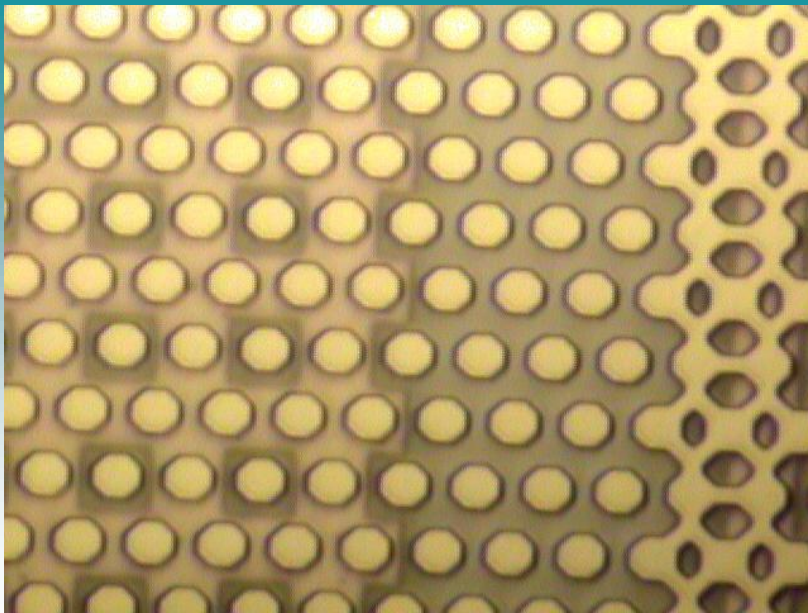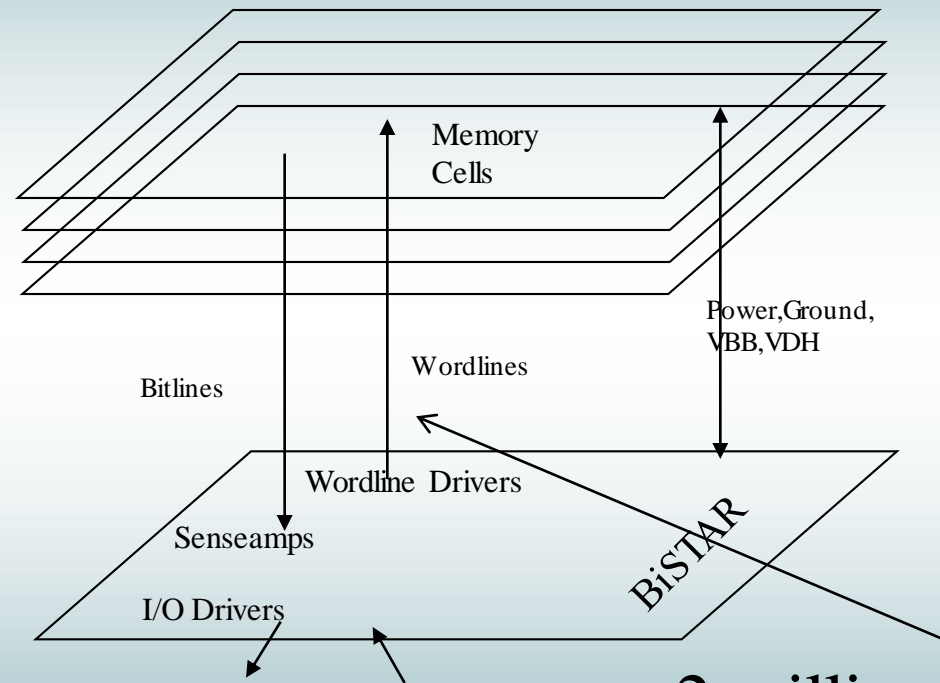| Bit cells	Low leakage -slow refresh -low power -low GIDL	High Vt Devices Vneg Well Thick Oxide
Sense Amps Word line drivers Device I/O	High speed -better sensitivity -better bandwidth -lower voltage	Low Vt Devices Copper interconnect Thin Oxides

"Dis-Integrated" 3D Memory

Memory Layers from DRAM fab

Controller Layer from high speed logic fab

Memory Cells

Power,Ground, VBB,VDH

Bitlines

Wordlines

Wordline Drivers

Senseamps

BiSTAR

I/O Drivers

2 million vertical connections per lay per die

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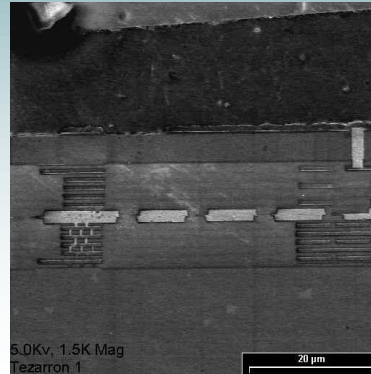
Octopus Stack

2 Layer Stacked Device
(SEM)

DRAM Control/Logic

DRAM Memory Cells

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Gen4 "Dis-Integrated" 3D Memory

DRAM layers
4Xnm node
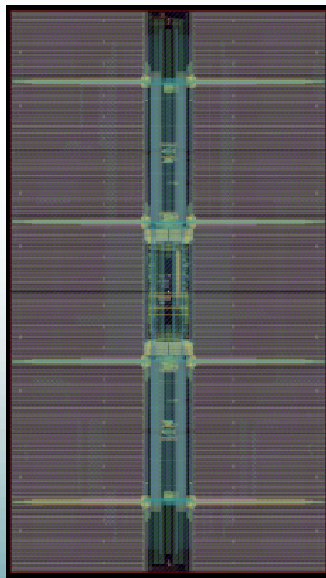
2 million vertical connections per lay per die

I/O layer contains: I/O, interface logic and R&R control CPU. 65nm node

Controller layer contains: senseamps, CAMs, row/column decodes and test engines. 40nm node

Better yielding than 2D equivalent!

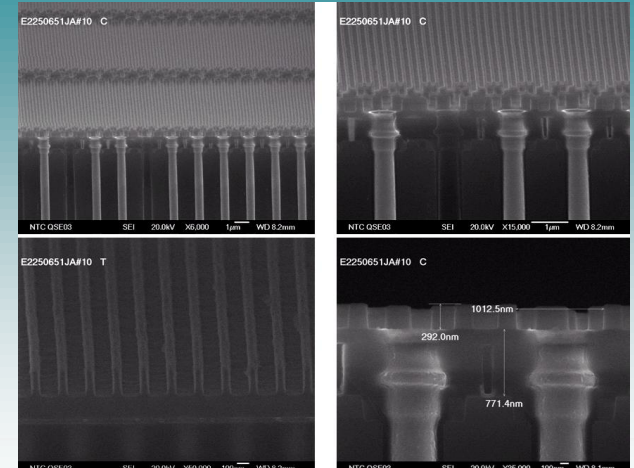*INFIERI 2013*
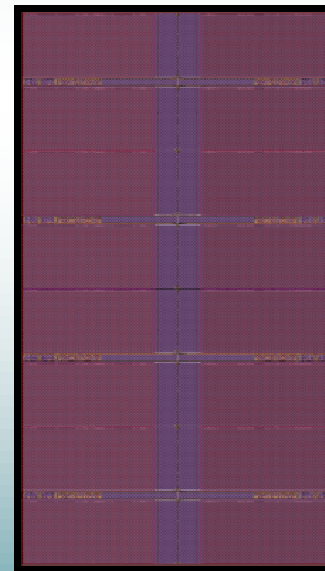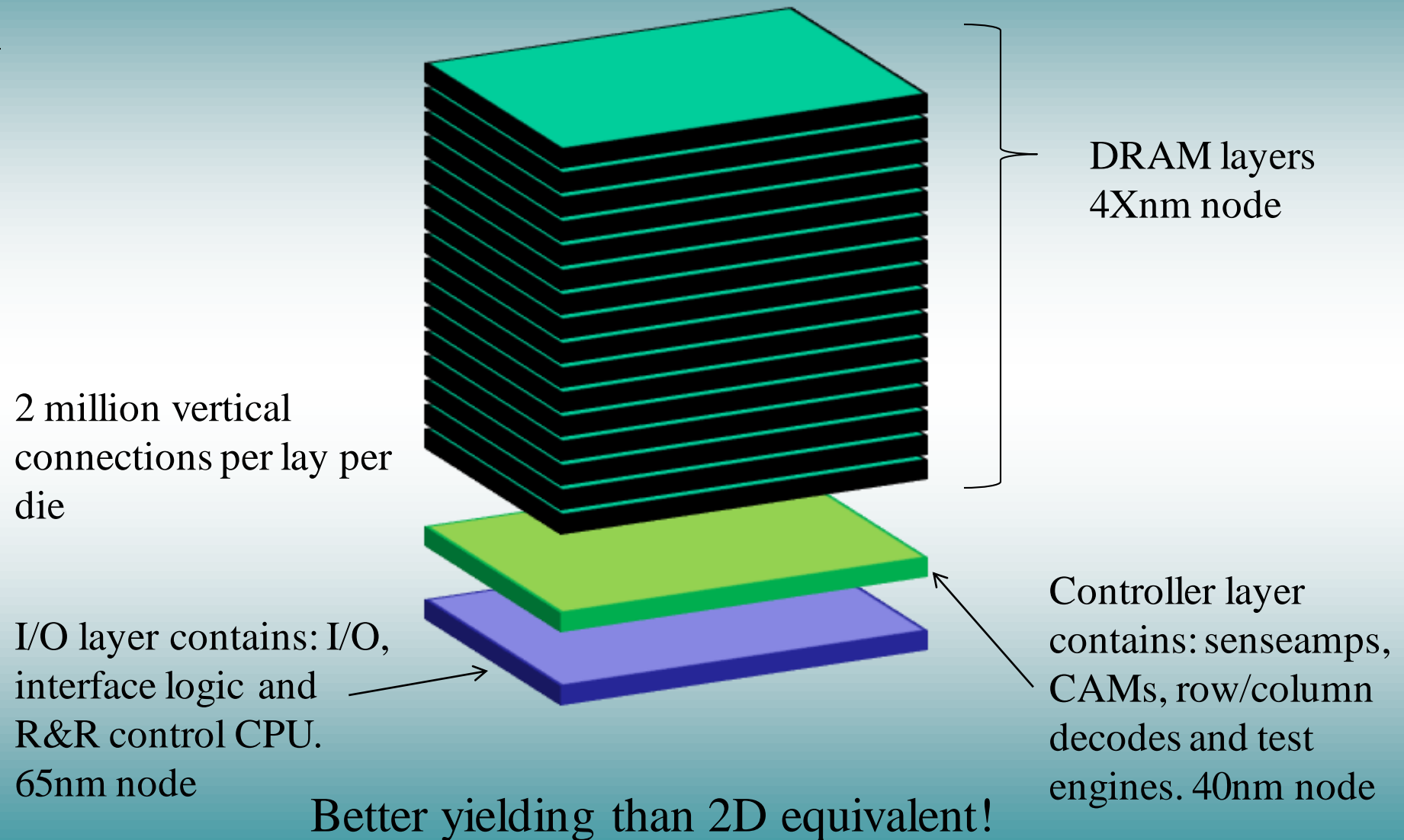
3D DRAMs

Octopus I

- 1-4Gb
- 16 Ports x 128bits (each way)
- @1GHz
  - CWL=0 CRL=2 SDR format
  - 5ns closed page access to first data (aligned)
  - 12ns full cycle memory time
  - >2Tb/s data transfer rate
- Max clk=1.6GHz
- Internally ECC protected, Dynamic self-repair, Post attach repair
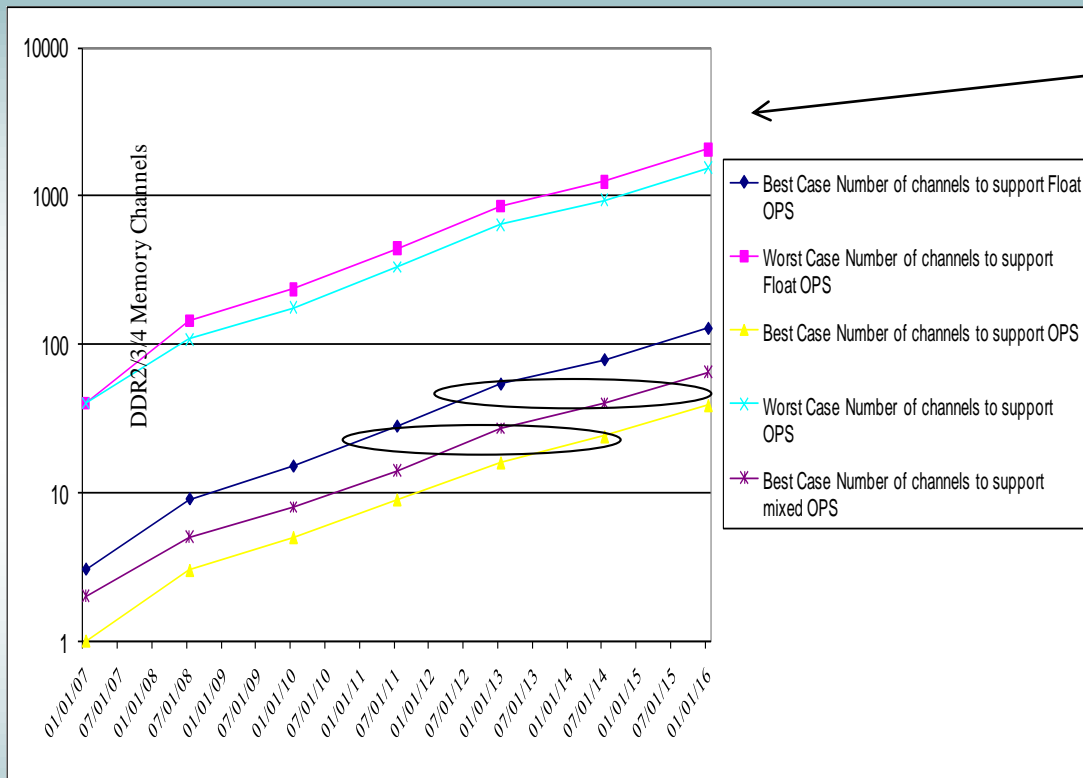- 115C die full function operating temperature

Octopus II

- 4-64Gb
- 64-256 Ports x 64bits (each way)
- @1GHz
  - 5-7ns closed page access to first data (aligned)
  - 12ns full cycle memory time
  - >16Tb/s data transfer rate
  - 4096 banks
  - 2+2pJ/bit

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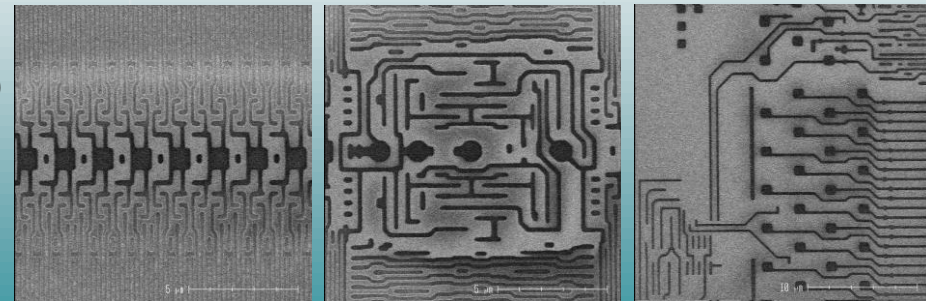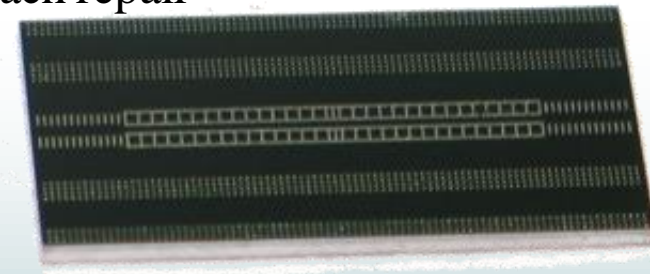
The Industry Issue

Need 50x bandwidth improvement.
Need 10x better cost model than embedded memory.

➤ To continue to increase CPU performance, exponential bandwidth growth required.

➤ More than 200 CPU cycles of delay to memory results in cycle for cycle CPU stalls.

➤ 16 to 64 Mbytes per thread required to hide CPU memory system accesses.

➤ No current extension of existing IC technology can address requirements.

➤ Memory I/O power is running away.

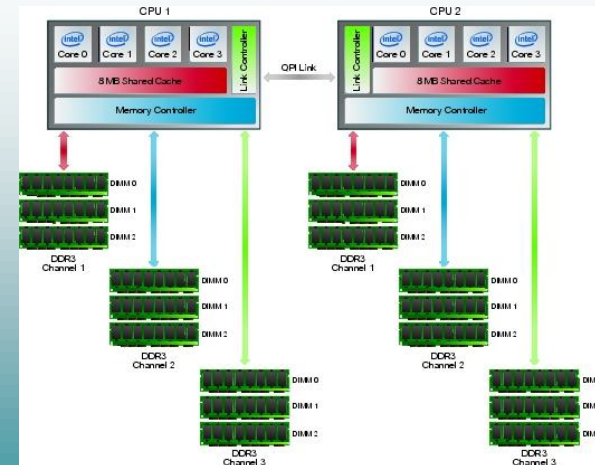# Main Memory Power Cliff

DDR3 ~40mW per pin

1024 Data pins →40W

4096 Data pins →160W

Die on Wafer ~24uW per pin

07/07/2013

# The "Killer" App: Split-Die

Tezzaron 3D DRAM

Can Utilize Standard Final Assembly Techniques*

4 to 12 Micron Layers

Thermal Diffusion Bonded Layers (Copper to Copper)

Conventional IC Thickness 4 to 25 Mils

Supporting Substrate (Last Bonded Layer)
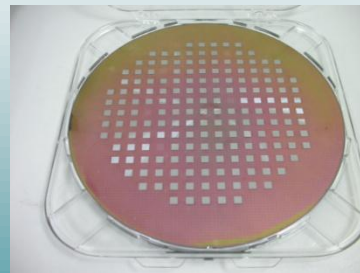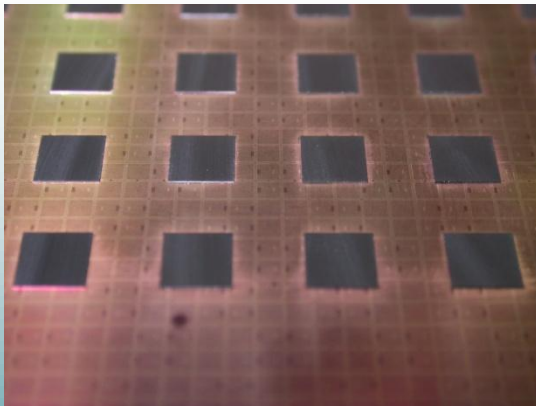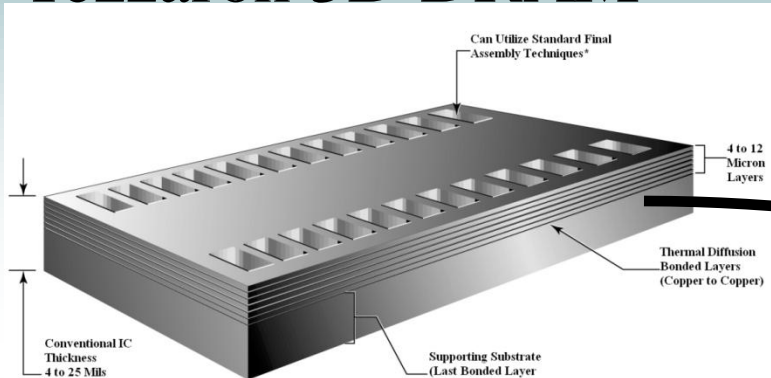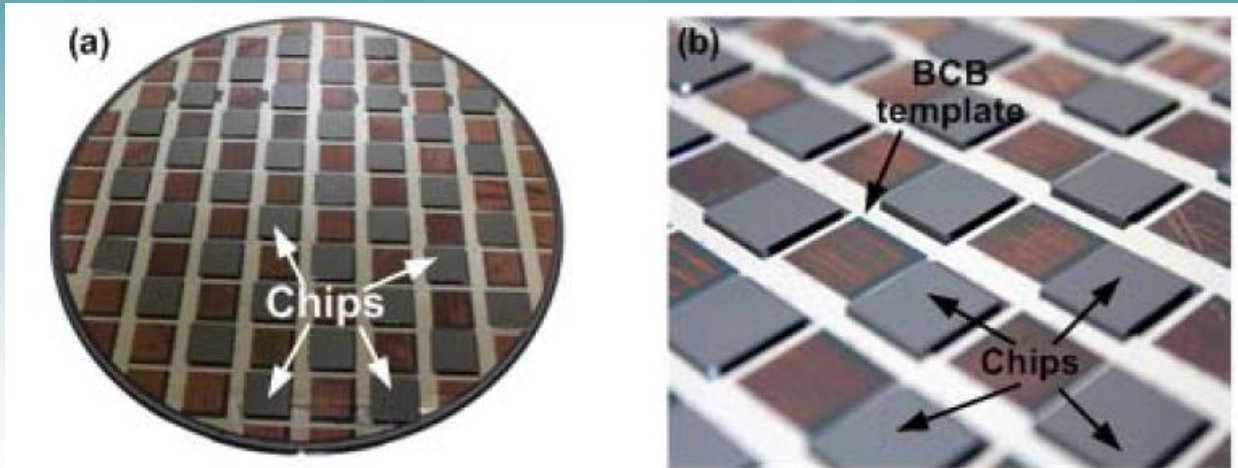
➢ Embedded Performance with far superior cost/density.

➢ 110nm DRAM node has better density than 45nm embedded DRAM.

➢ 1000x reduction in I/O power.

DRAM

Customer Host Device

I/O Pad area : Bumping or wire bonding
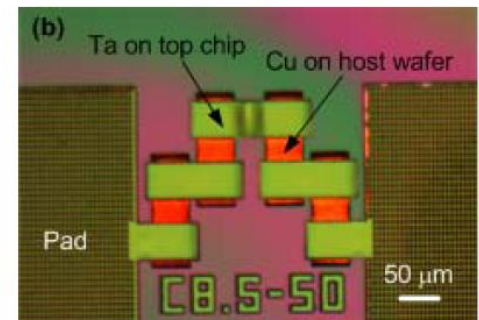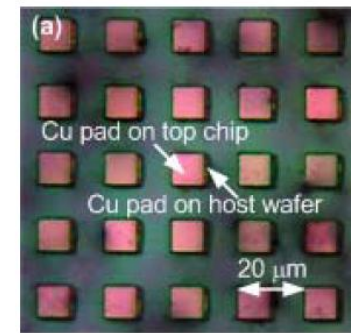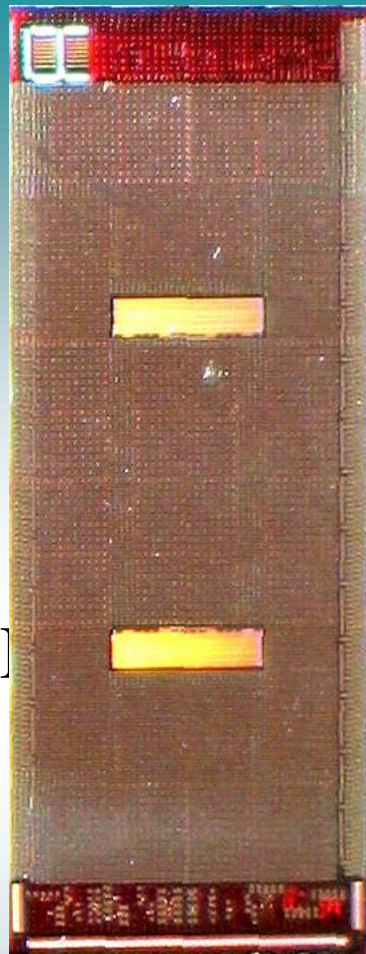
INFIERI 2013
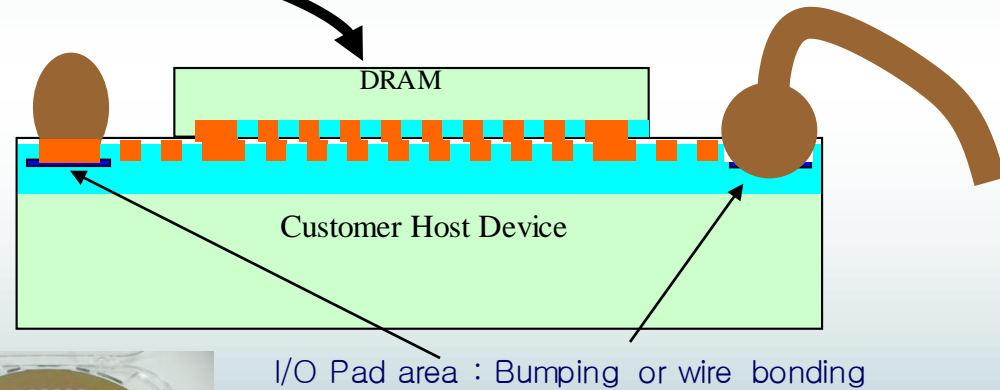
Die to Wafer With BCB Template
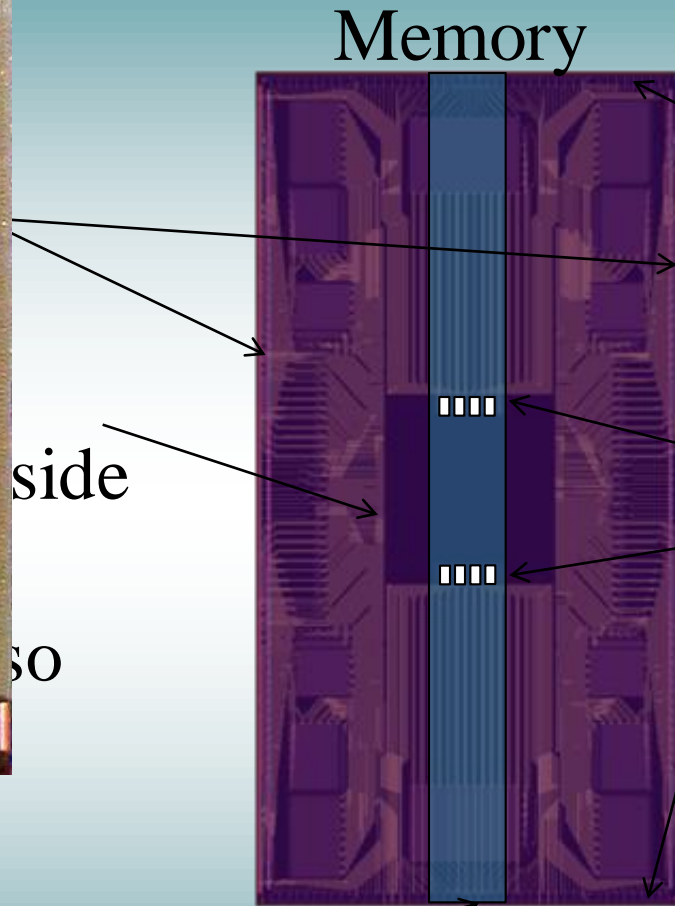

RPI Effort under Dr. James Lu

- KGD
- 2um alignment / 5um pitch limit
- Cu-Cu thermo compression bonding
- Multilayer capability

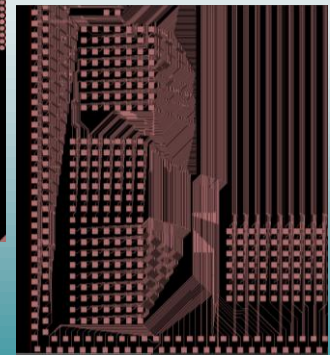*INFIERI 2013*

Logic on Memory
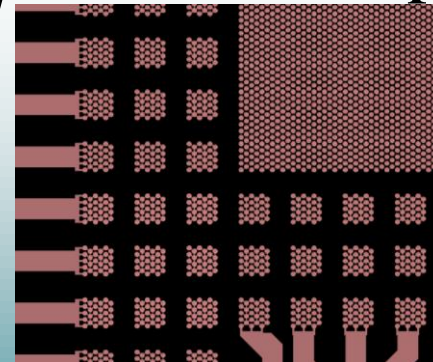
Memory

92 pads

(528 total pads at edge, stagger
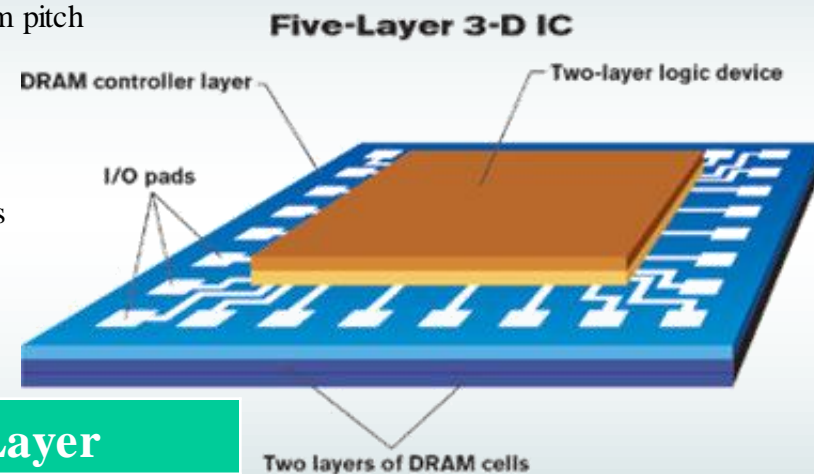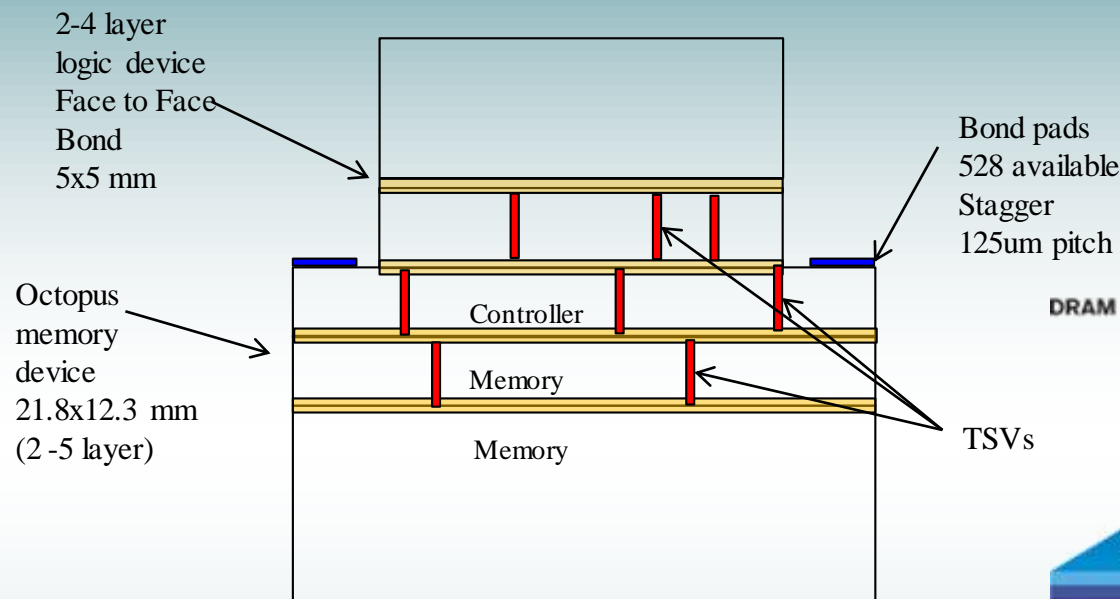250um pad, 125um pitch
~1500 available pads)

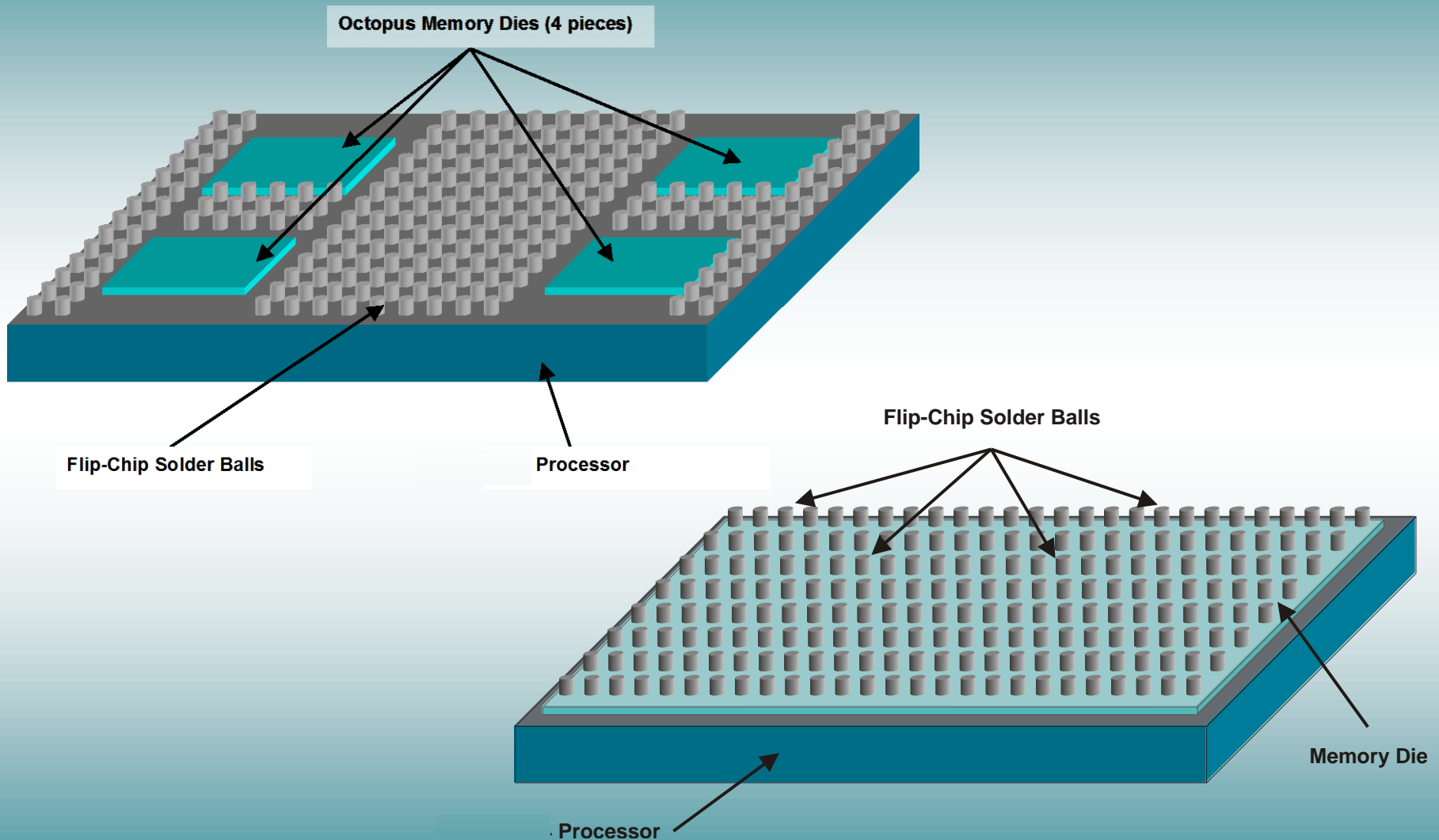8 DRAM ports
16x21 pad array

side

so

Logic
interposer

>10μf bypass caps
SS ~4,000pf

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Hyper-Integration
5-9 layer stacks

2-4 layer
logic device
Face to Face
Bond
5x5 mm

Bond pads
528 available
Stagger
125um pitch

Octopus
memory
device
21.8x12.3 mm
(2 -5 layer)

Controller

Memory

Memory

TSVs

Five-Layer 3-D IC

DRAM controller layer

Two-layer logic device

I/O pads

Two layers of DRAM cells

Layer	5 Layer	7 Layer	9 Layer
Poly	9	11	17
Copper Wire	21 (25)	32 (38)	34 (42)
Al/W Wire	7	7	13
Trans. Count	3B	3.1B	5.5B

Current Memory Split-Die Projects

Octopus Memory Dies (4 pieces)

Flip-Chip Solder Balls

Processor

Flip-Chip Solder Balls

Memory Die

Processor

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R8051/Memory

5X Performance
1/10th Power

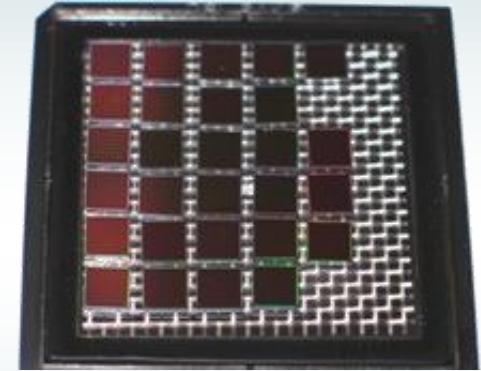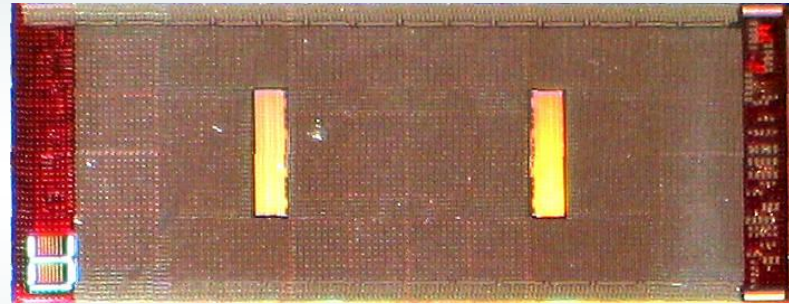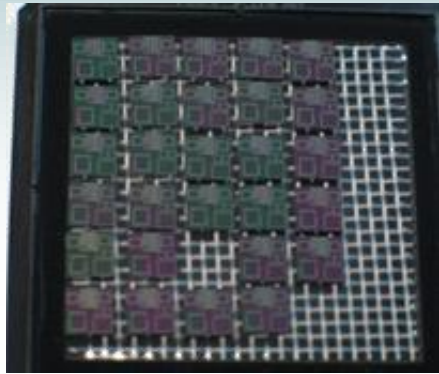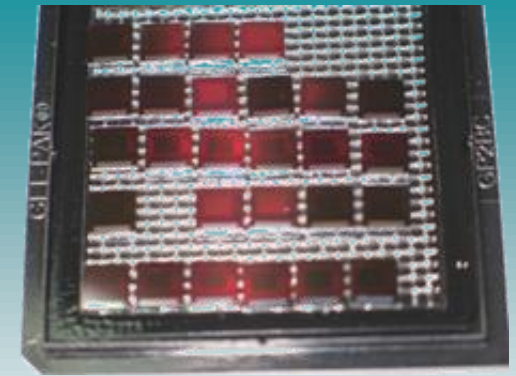Tools Design Window Create Edit Verify Connectivity Options Route Calibre   Help
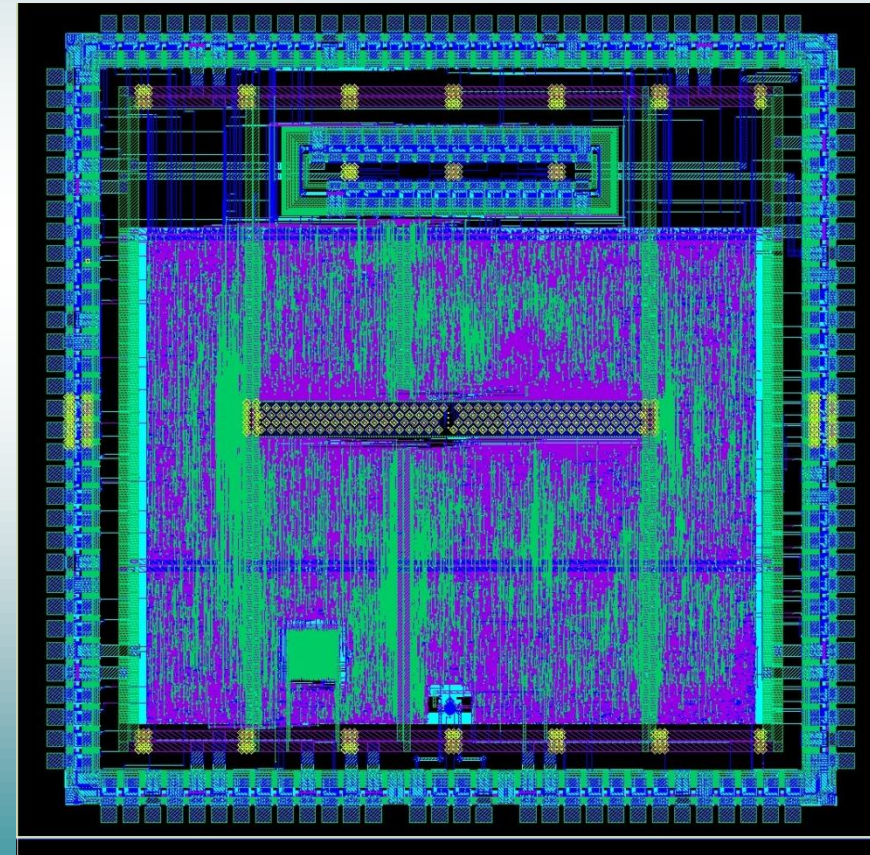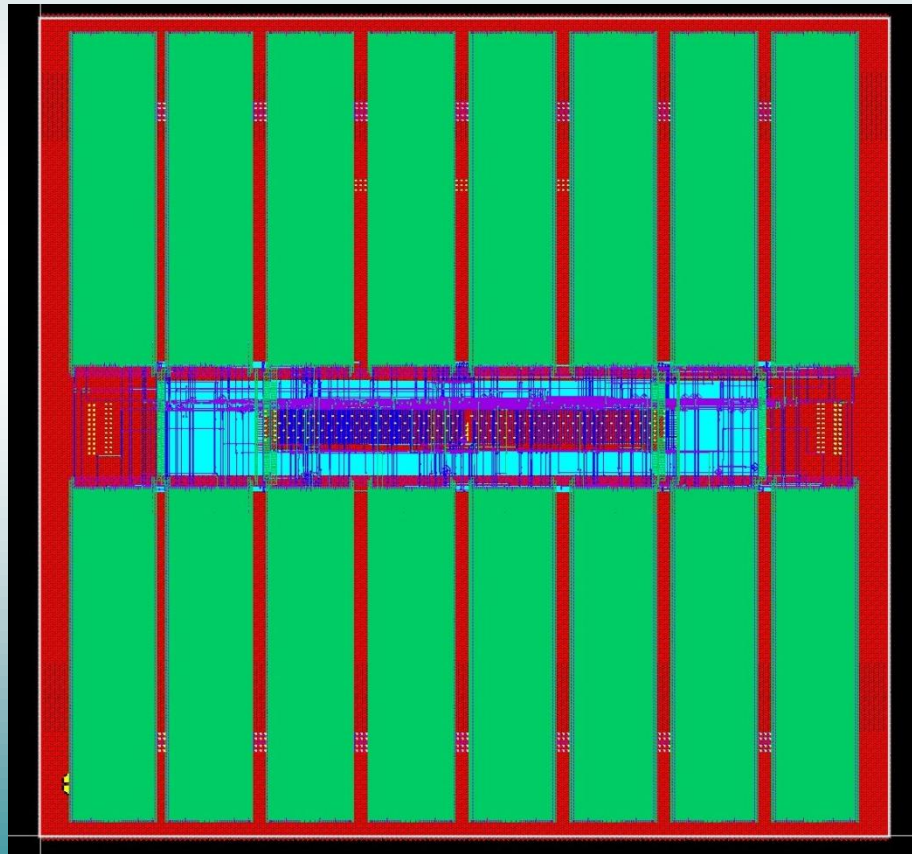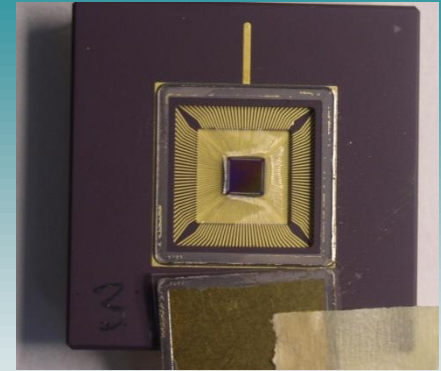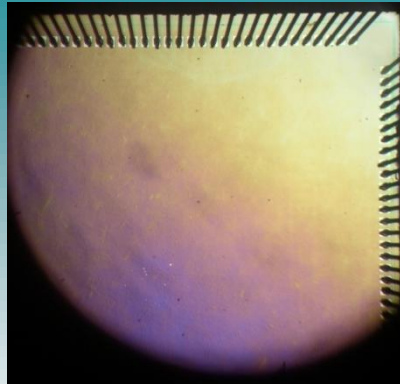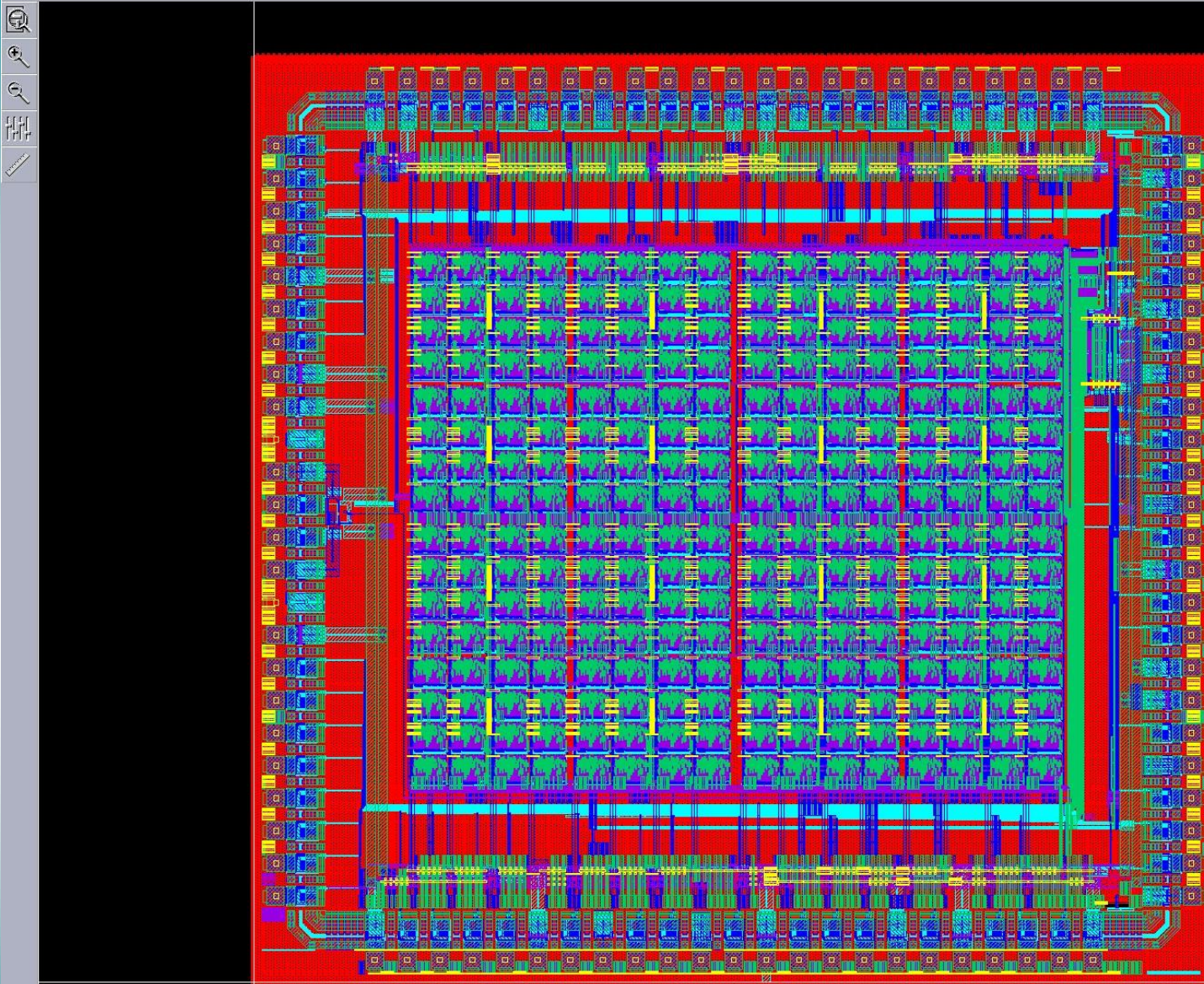
mouse L: mouseSingleSelectPt   M: mousePopUp()   R: hiZoomAbsoluteScale(hiGetCurrentWindow() 0.9)
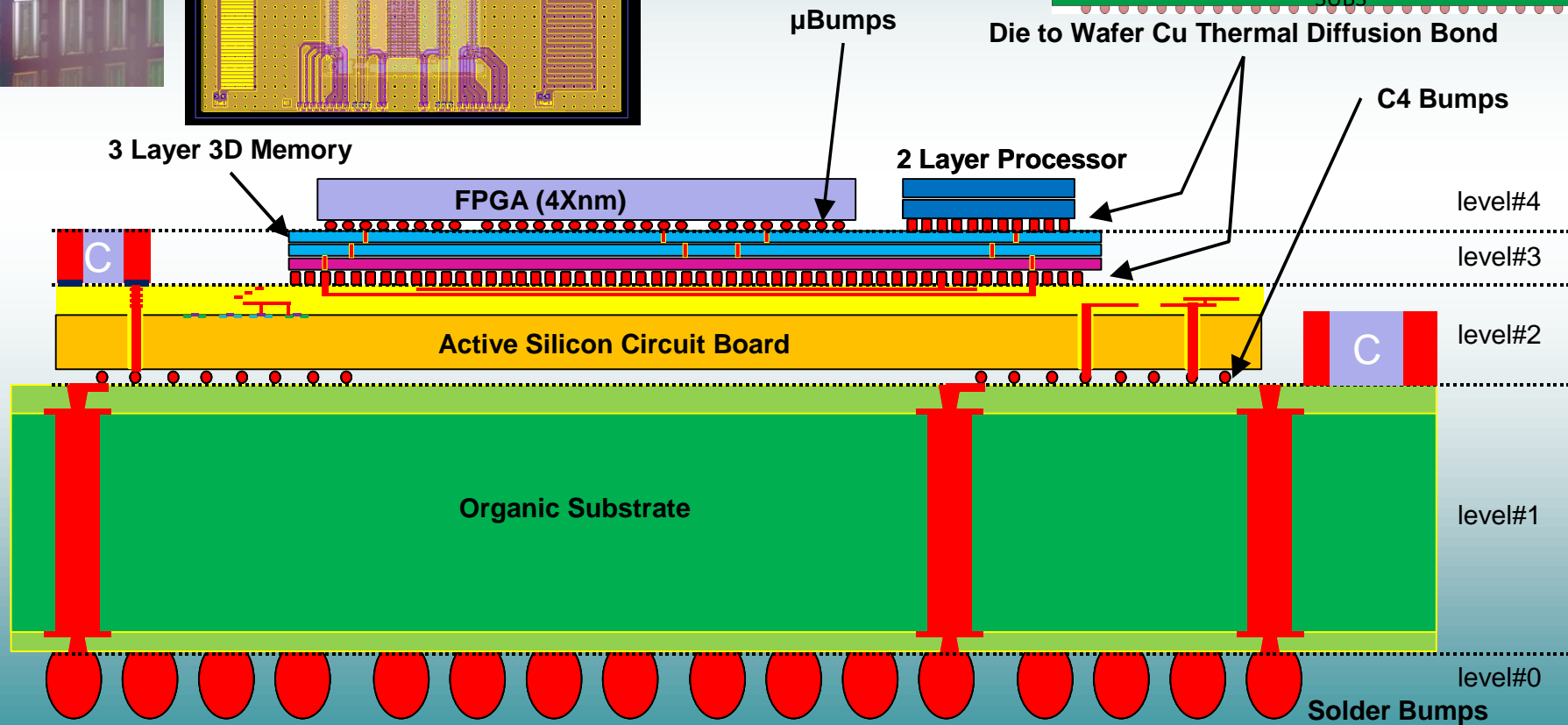>

© Tezzaron Semiconductor   *INFIERI2013*   07/07/2013   35
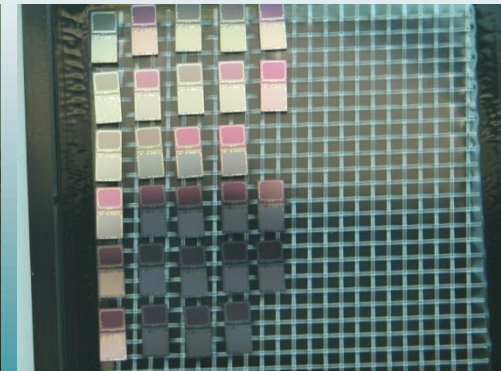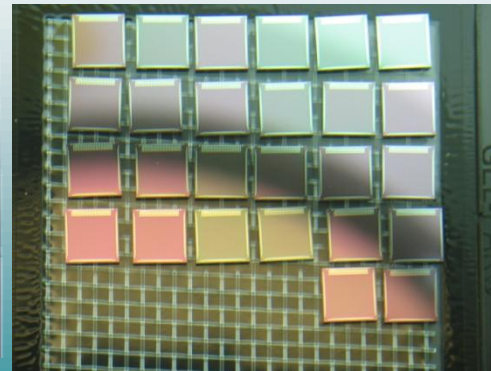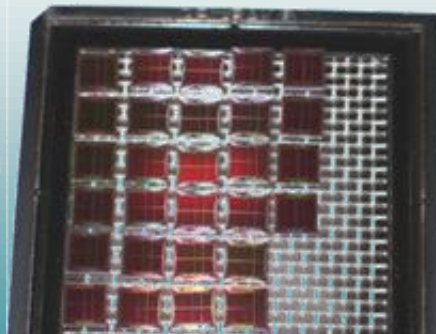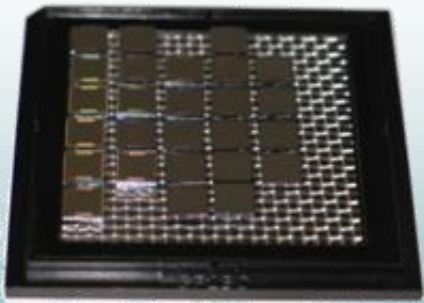
RF, Imaging,
Processing, Analog

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2.5/3D in Combination

IMEA-Star/
Tezzaron
Collaboration

Capillar underfill

BCB

Mem controler layer in bottom

3DMem TSV rad <1um

TSI TSV H:R 100/10um

~50um

C2W Cu2Cu bond ~5um pitch

Al pad

p~150um

P'~5um

CPU(2 Gbps serdes+2xDDR2 channel to 3DMem+2xDDR2 channel to PCB)

RDL

CPNT#1:

3DMem # section N

3DMem # section N'

beol

CPNT#2

TSI (~2ML BEOL w/s=2/2um)

fcBGA SUBSTRATE 2-2-2 (fcpad pitch ~150 um, Ball size ~0.5mm)

C4 bonds ~150um pitch H~80 um

IMEA-Star / Tezzaron Collaboration

µBumps

Die to Wafer Cu Thermal Diffusion Bond

TSI

SUBS

DeCap

C4 Bumps

3 Layer 3D Memory

2 Layer Processor

FPGA (4Xnm)

level#4

level#3

C

Active Silicon Circuit Board

level#2

C

Organic Substrate

level#1

level#0

Solder Bumps

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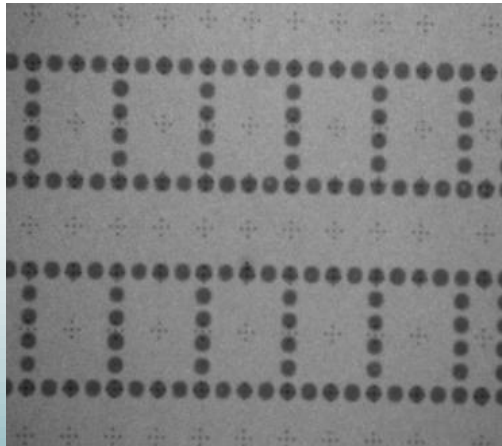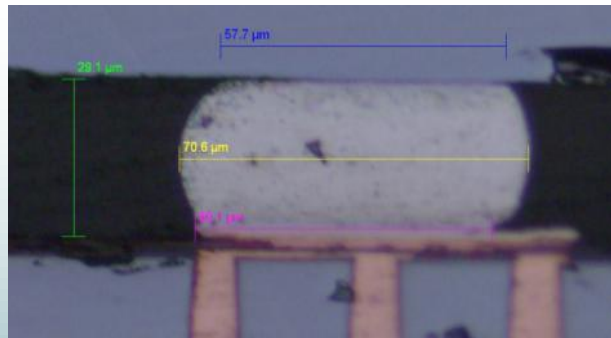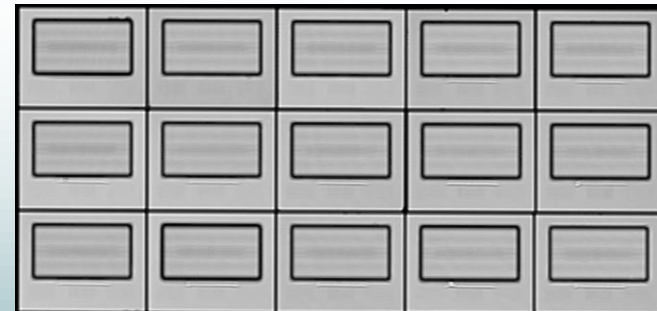
Tezzaron Dummy Chip C2C Assembly
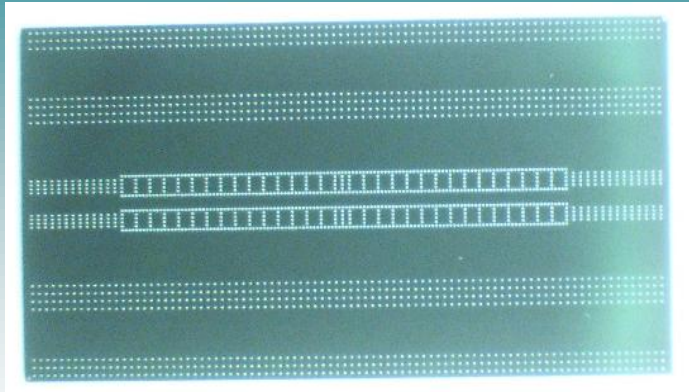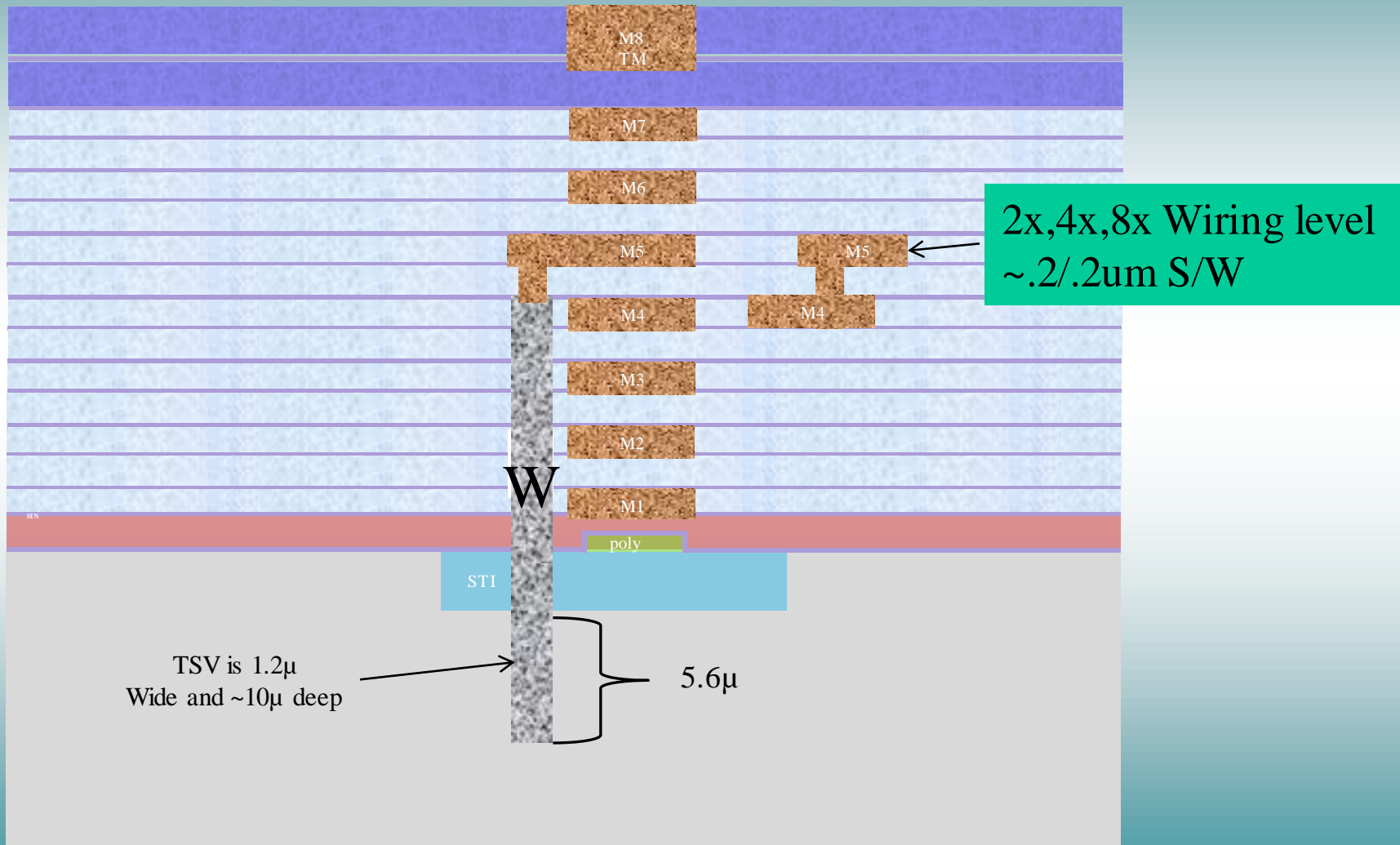

Memory die
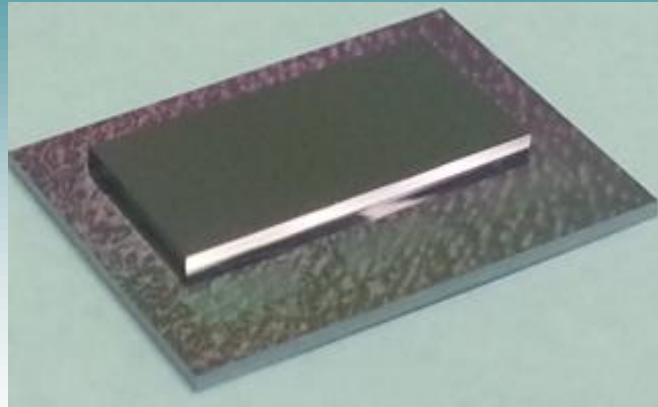
C2C sample

X-ray inspection indicated
no significant solder voids

X-section of good
micro bump
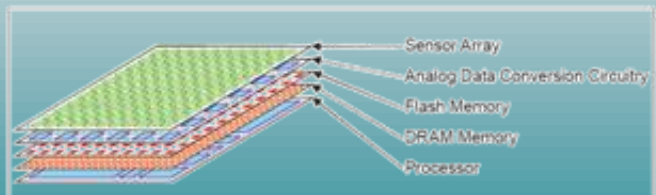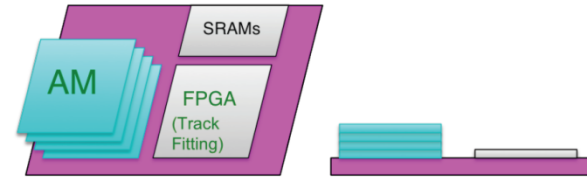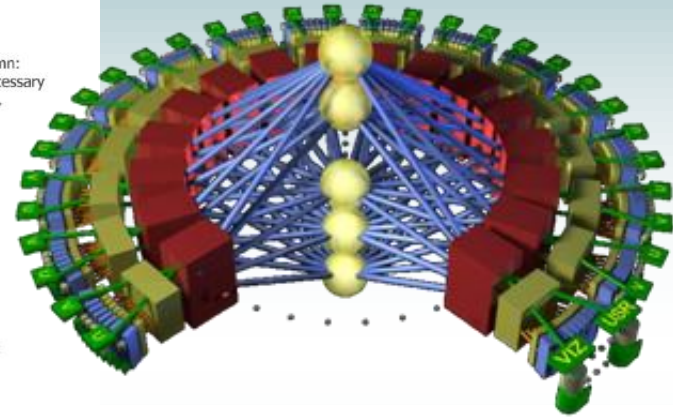

CSCAN showed no
underfill voids (UF:
Namics 8443-14)

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Near End-of-Line

2x,4x,8x Wiring level ~.2/.2um S/W

M8 TM

M7

M6

M5   M5

M4   M4

M3

M2

W

M1

poly

SIN

STI

TSV is 1.2μ
Wide and ~10μ deep

5.6μ

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New Apps – New Architectures

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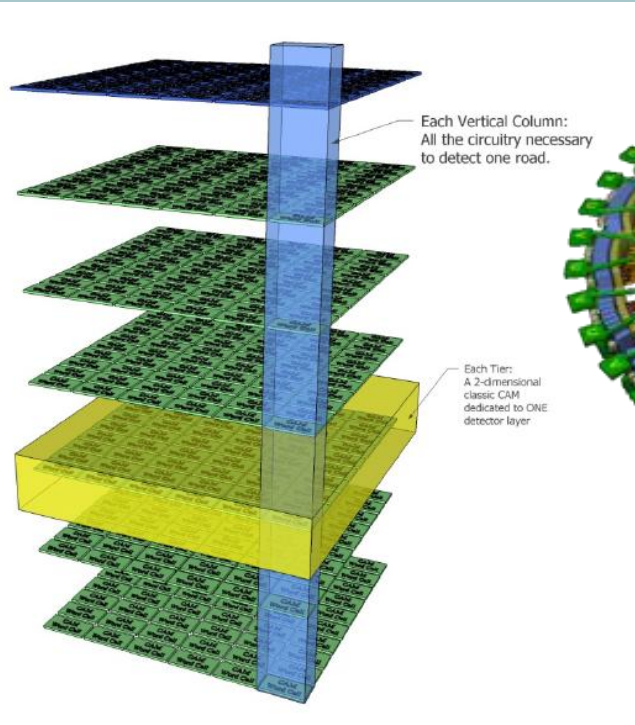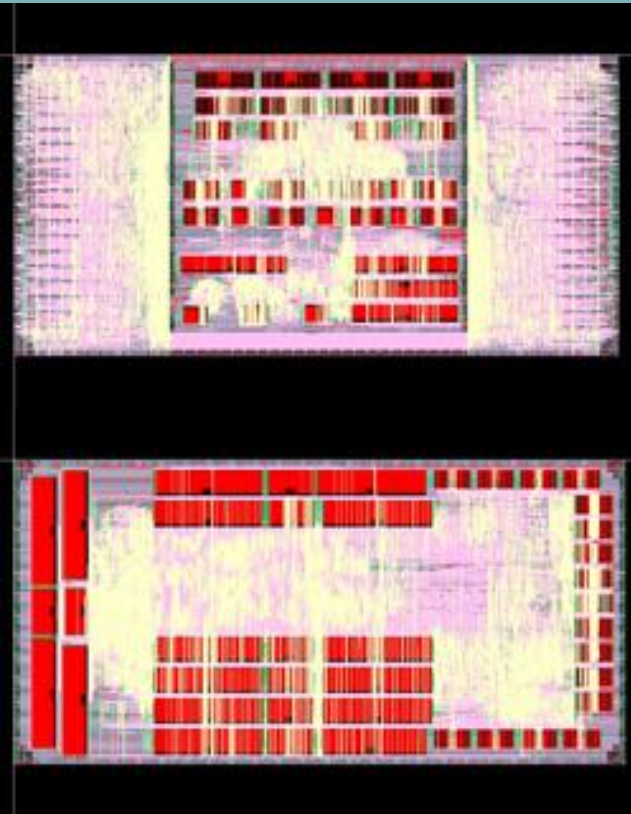
MAX-3D by Micro Magic, Inc.
Fully functional 3D layout editor.

- Independent tech files for each tier.

- Saves GDSII as flipped or rotated.

- Custom output streams for 3D DRC / LVS.

DRC, LVS, Transistor synthesis, Crossprobing.
Multiple tapeouts,
0.35um-45nm
>20GB, ~10B devices

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3D Place & Route
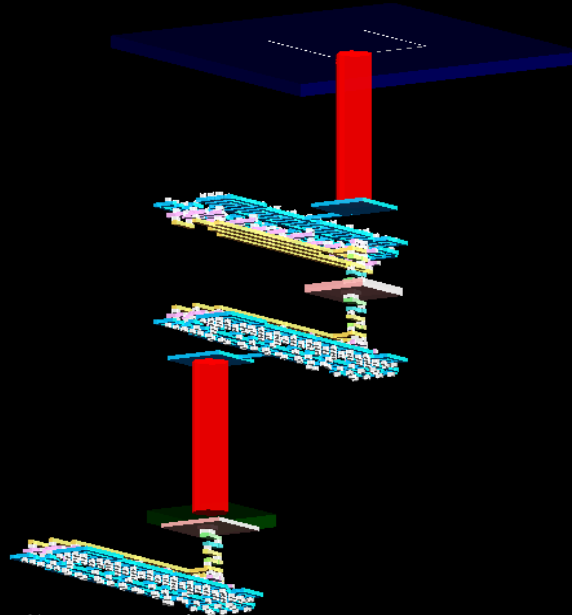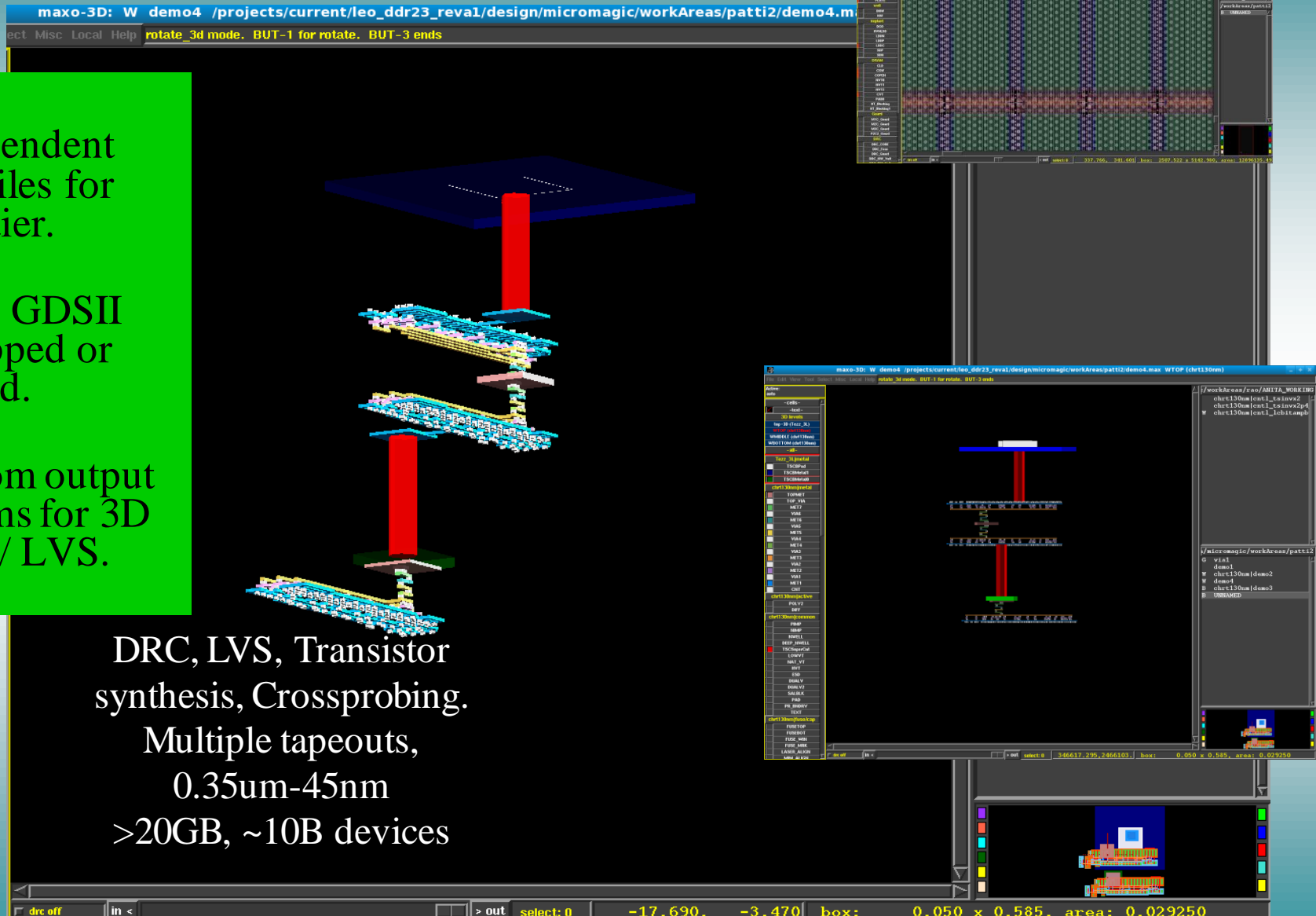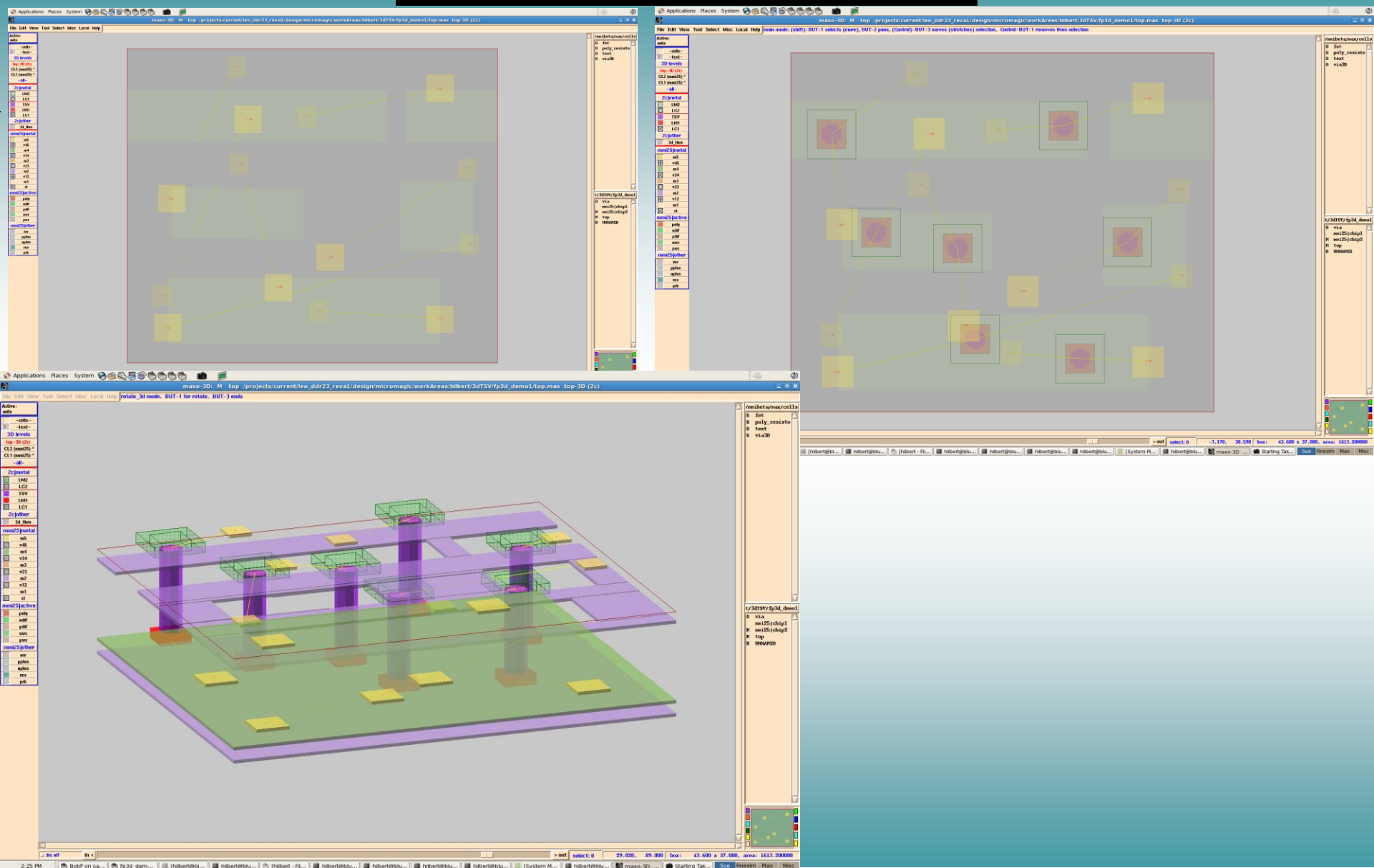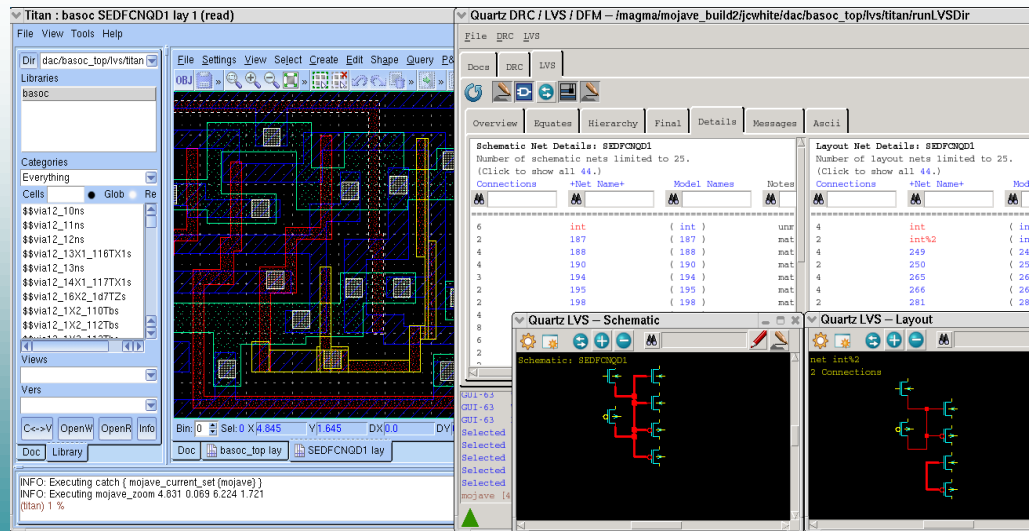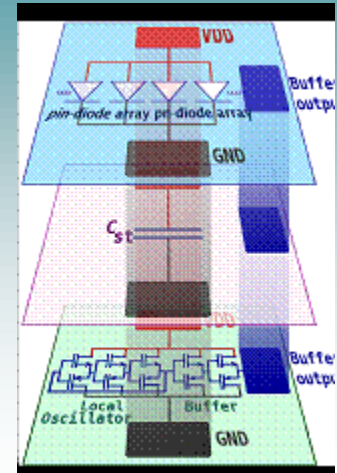
3D LVS using QuartzLVS from Magma

- ## Key features
  - LVS each of the 2D designs as well as the 3D interconnections between them in a single run
  - Driven by a 3D "tech file" that specifies the number and order of layers, interconnect material, etc
  - TSV aware LVS extraction
  - Full debug environment to analyze any LVS mismatch


```
# 3D LVS Tech file
WAFER: 1
    LAYOUT TOP BLOCK: lvslayer1_1
    SCHEMATIC TOP BLOCK: lvslayer1
    GDSII FILE: lvslayer1_1.gds
    SCHEMATIC NETLIST: lvslayer1.sp
    INTERFACE UP METAL: 1;0
    INTERFACE UP TEXT: 1;101
...
INTERFACE:
    LAYOUT TOP BLOCK: lvstop
    SCHEMATIC TOP BLOCK: lvstop
    GDSII FILE: lvstop_ALL.gds
    SCHEMATIC NETLIST: lvstop.sp
    BOND OUT METAL: 5;0
    BOND OUT TEXT: 5;101
```
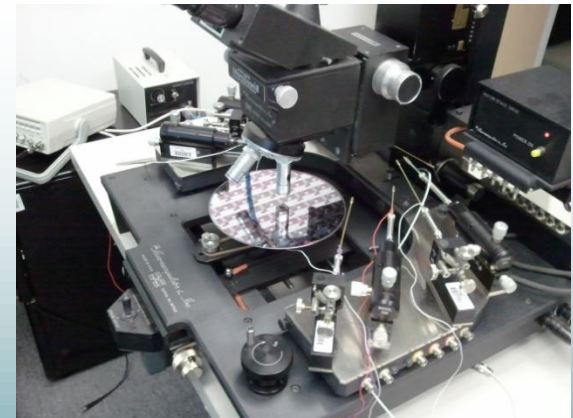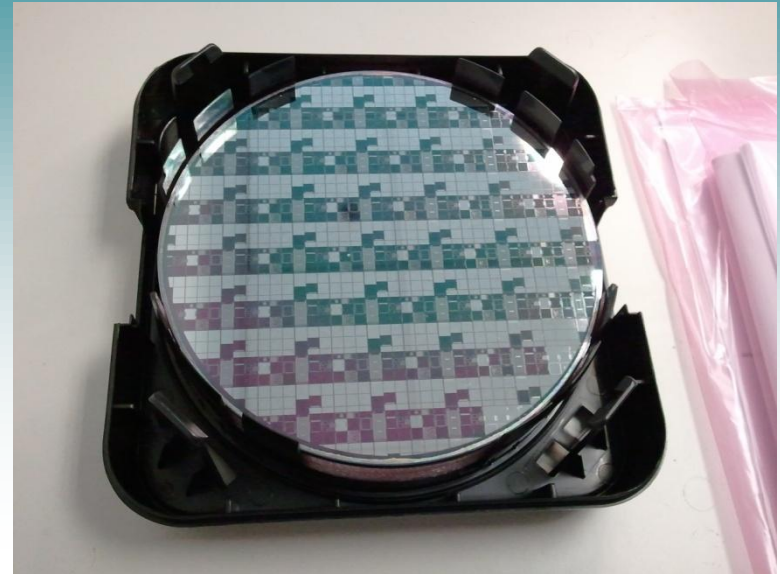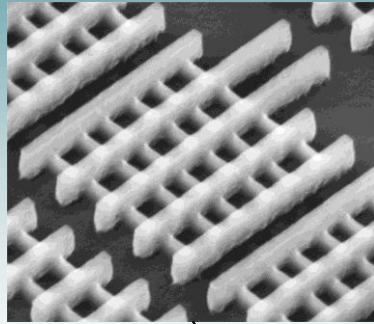
Challenges

- Tools
  - Partitioning tools
  - 3D P&R
- Access
- Heat
- Testing
  - IEEE 1500
  - IEEE 1149
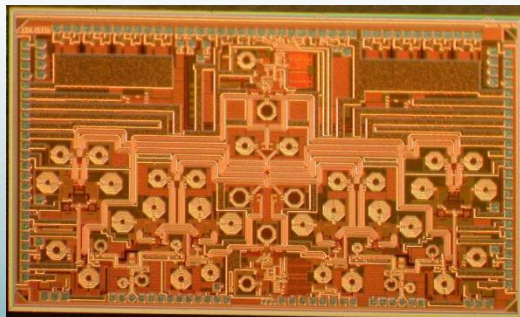- Standards
  - Die level
    - JEDEC JC-11 Wide bus memory
  - Foundry interface

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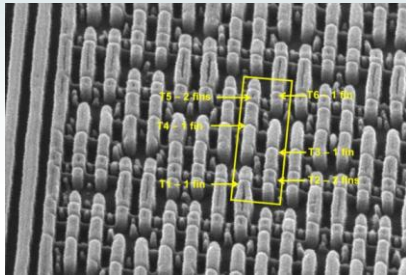# 3D Key to Enable Next Gen

16nm Sea-of-Gates

14nm Sea-of-SRAM

Memory cell

NAND string (32 cells in series)

187110   20.0kV X30.0K 1.00μm
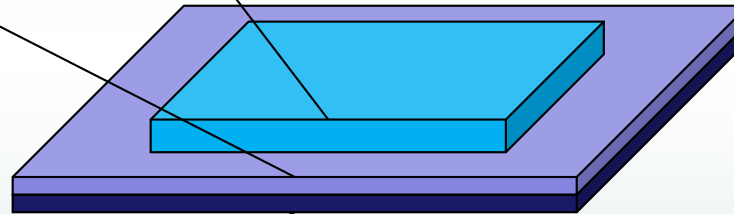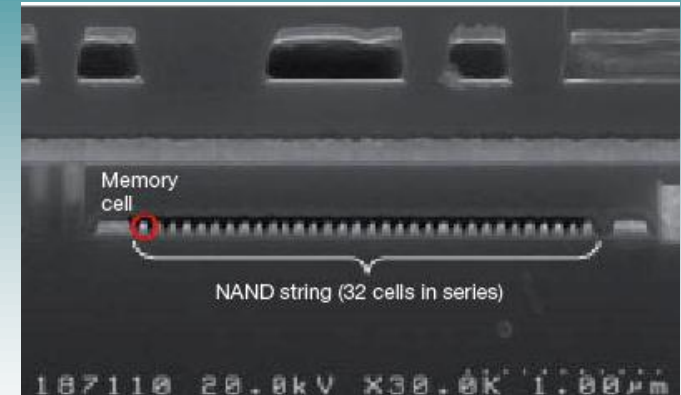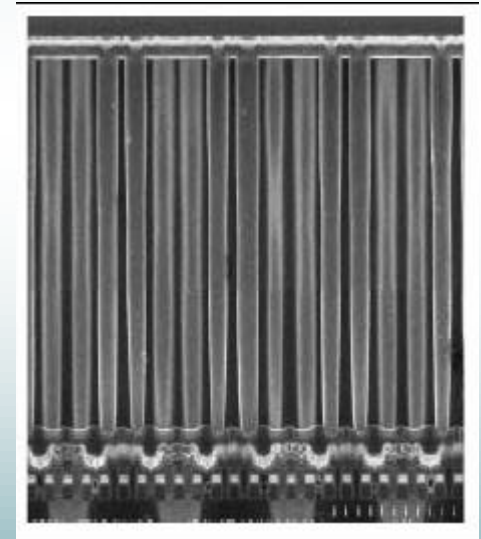

65nm Analog and I/O

IP isolation   Optimized Process   Simplified Technology   Real Reuse

Tezzaron/Novati 3D Technologies

- "Volume" 2.5D and 3D Manufacturing in 2013
- Interposers
- Future interposers with
  - High K Caps
  - Photonics
  - Passives
  - Power transistors
- Wholly owned Tezzaron subsidiary
- Cu-Cu, DBI®, Oxide, IM 3D assembly

07/07/2013

2.5/3D Design Enablement

- Complete 3D PDK 8th Release
  - GF 130nm
  - Synopsys, Hspice, Cadence, MicroMagic 3D physical editor
  - Calibre 3D DRC/LVS
  - Artisan standard cell libraries
- MOSIS, CMP, and CMC MPW support
  - 130nm, coming soon 65nm
  - Silicon Workbench
- Honeywell 150nm SOI
- NEOL TSV insertion
- 40→28nm 3D logic
- Silicon interposers, active, photonics
- Organic interposers
- >100 devices in process
- >500 users

07/07/2013
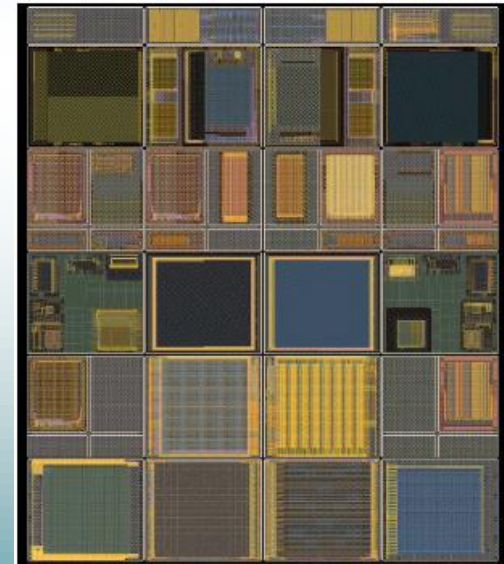
Summary

- ## 3D has numerous and vast opportunities!!
  - ### New design approaches
  - ### New ways of thinking
  - ### Best of class integration of
    - Memory
    - Logic
    - RF
    - MEMS

Sensors

Computing

MEMS

Communications

07/07/2013

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