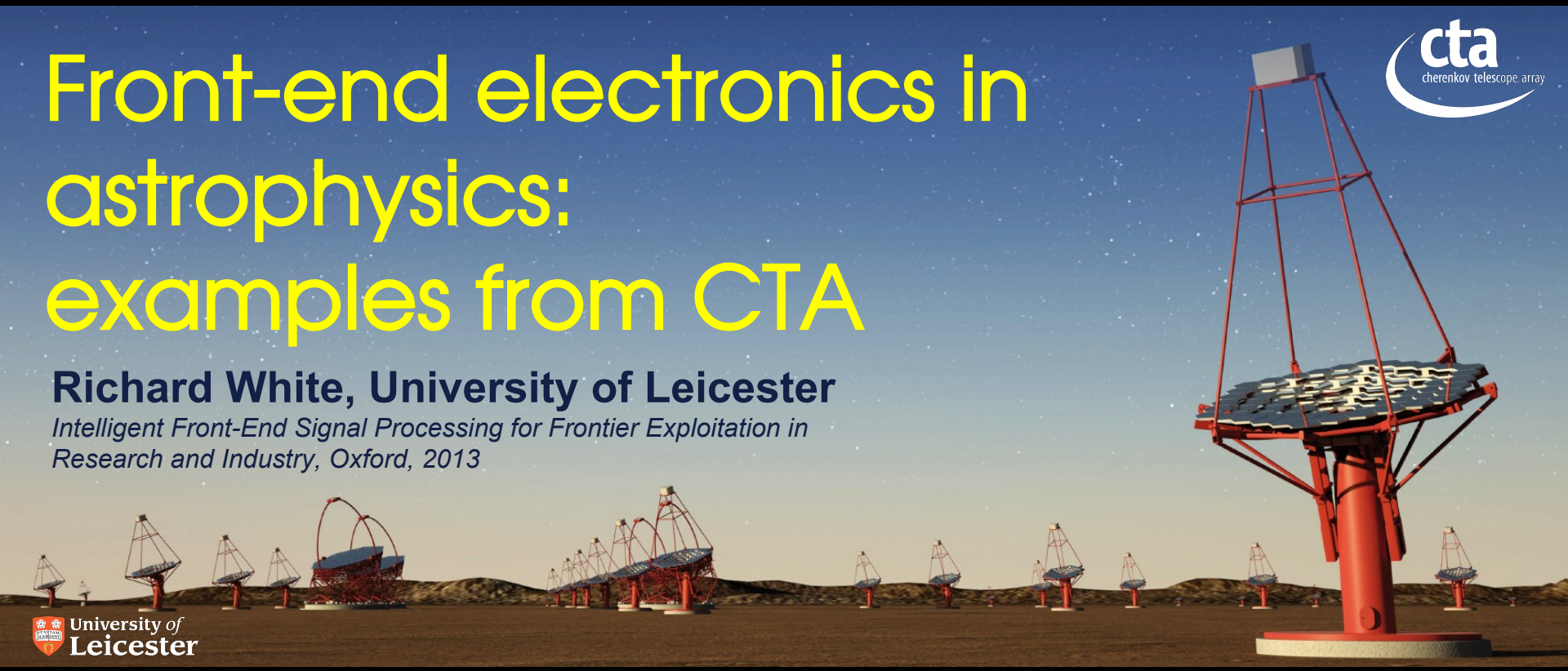
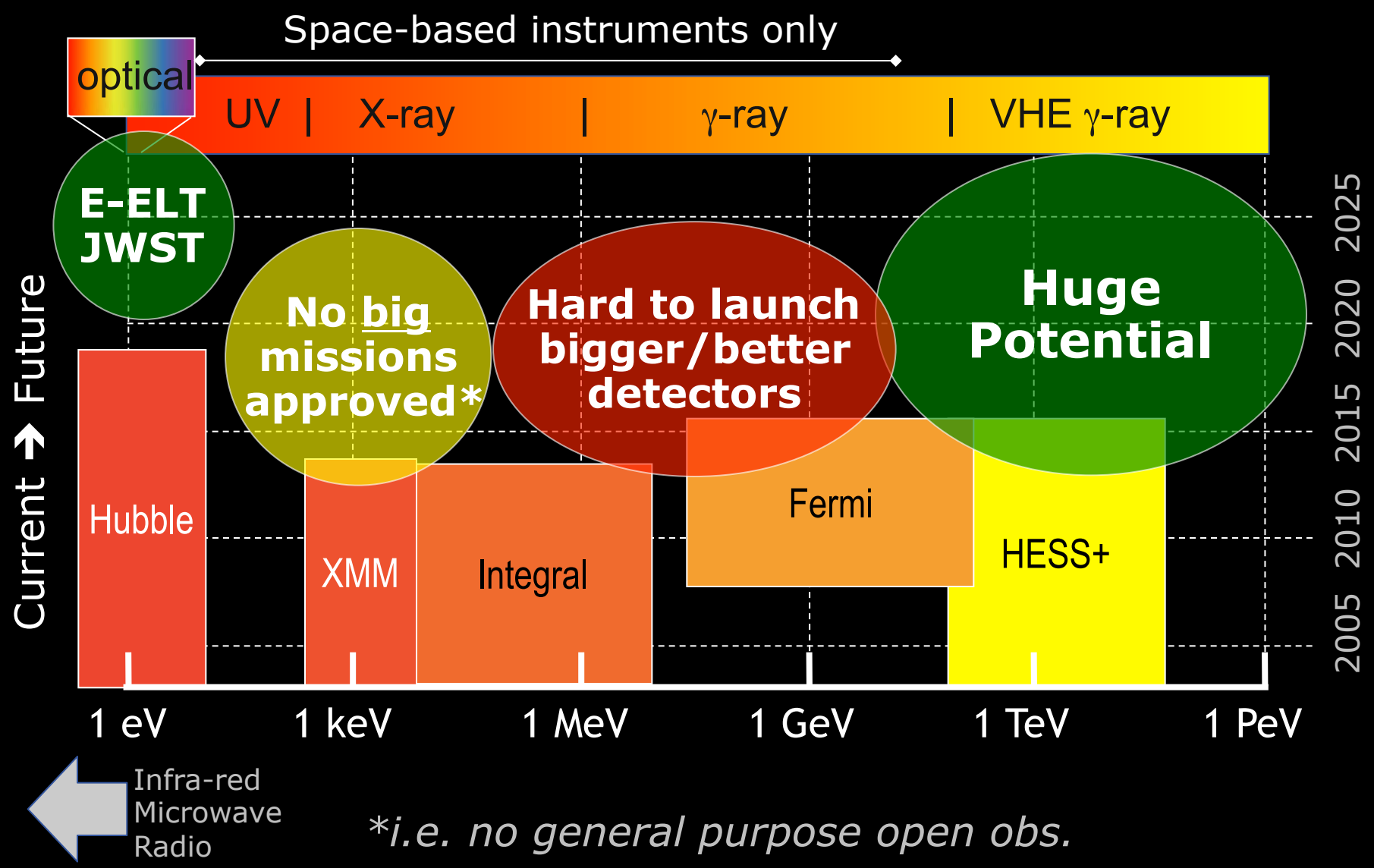
Front-end electronics in astrophysics: examples from CTA

Richard White, University of Leicester

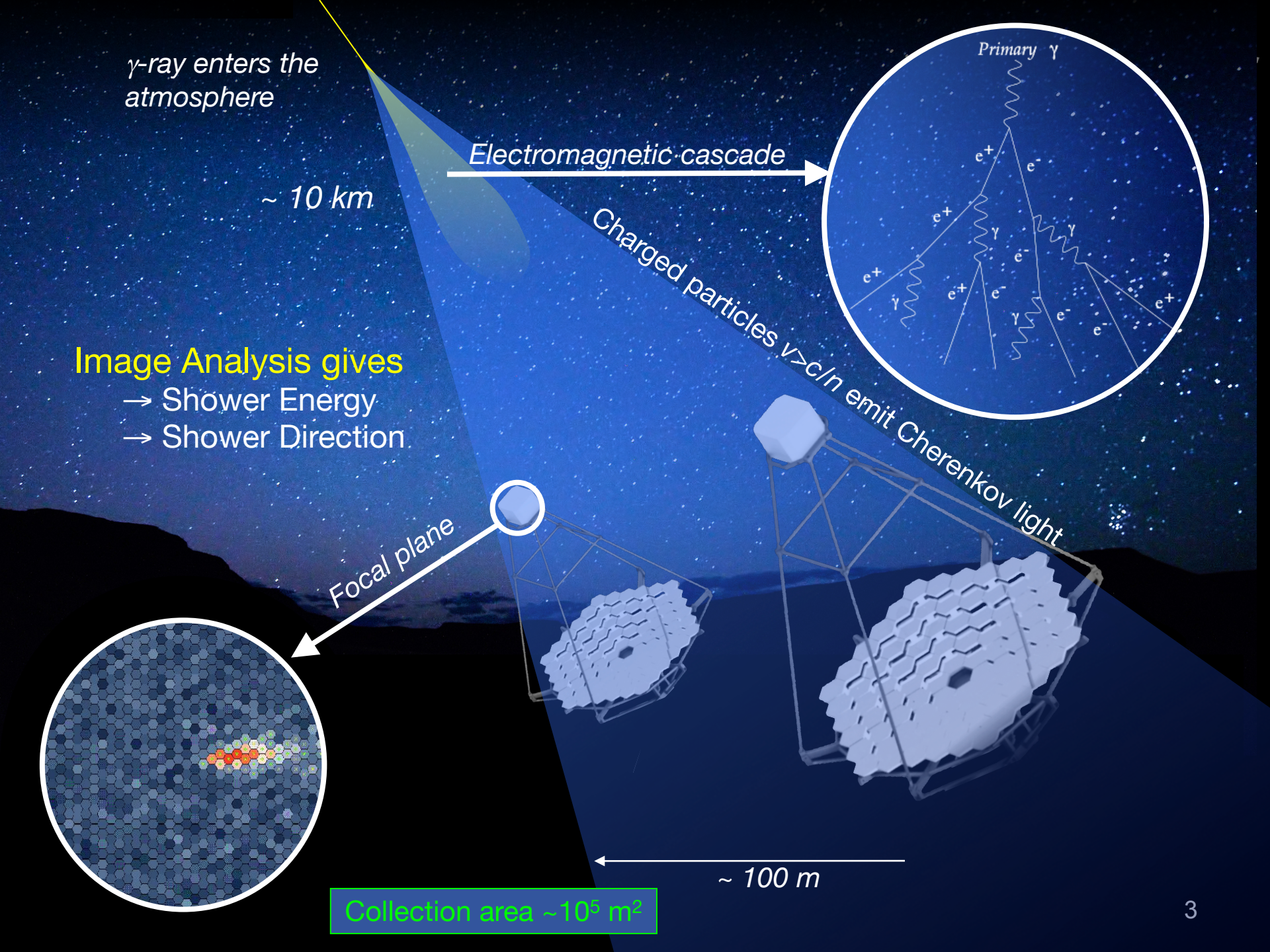
Intelligent Front-End Signal Processing for Frontier Exploitation in Research and Industry, Oxford, 2013

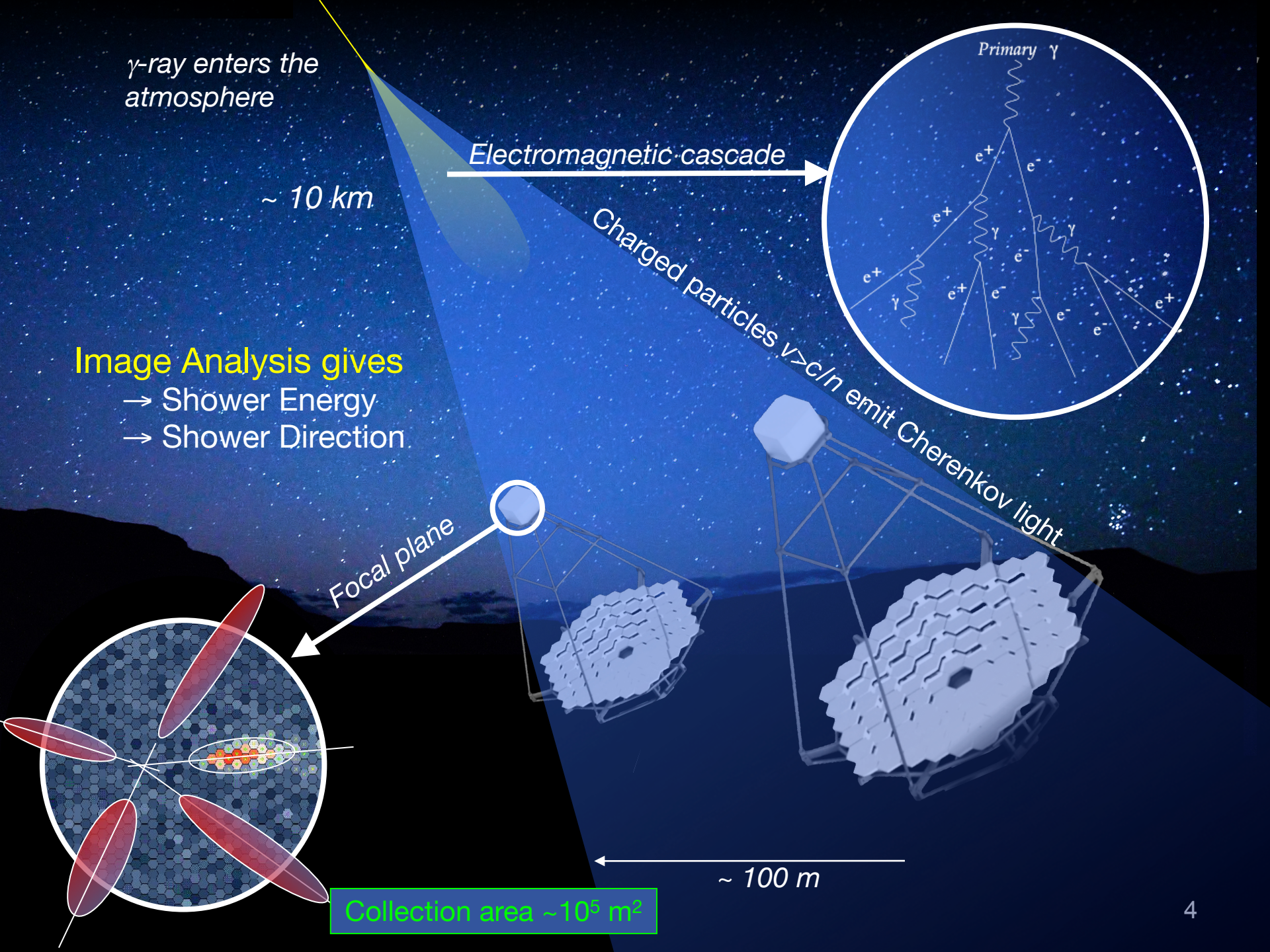


High Energy Future?



*i.e. no general purpose open obs.


γ-ray enters the atmosphere
~ 10 km
Electromagnetic cascade
Primary γ
Charged particles v>c/n emit Cherenkov light
Image Analysis gives
→ Shower Energy
→ Shower Direction
Focal plane
~ 100 m
Collection area ~10^5 m^2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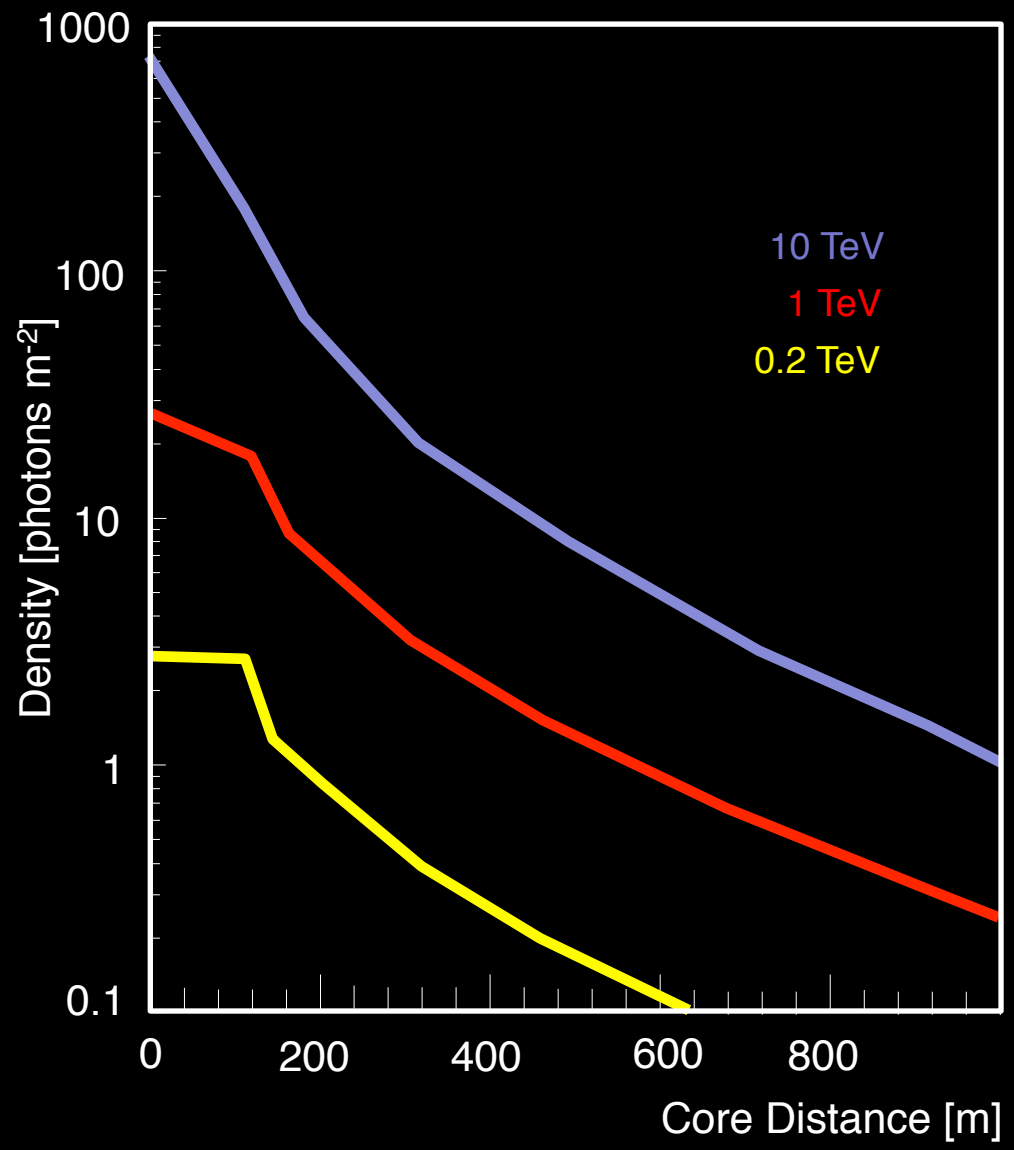
Technique
signal

- Cherenkov light:
  - Faint
    - 1 TeV gamma-ray → ~ 10 photons / m^2 @ 200 m from impact
    - → Big dishes
  - Fast
    - Lasts a few ns
    - → Fast photosensors and electronics
  - Blue
    - Peaks at 350 nm
    - → Blue sensitive photosensors

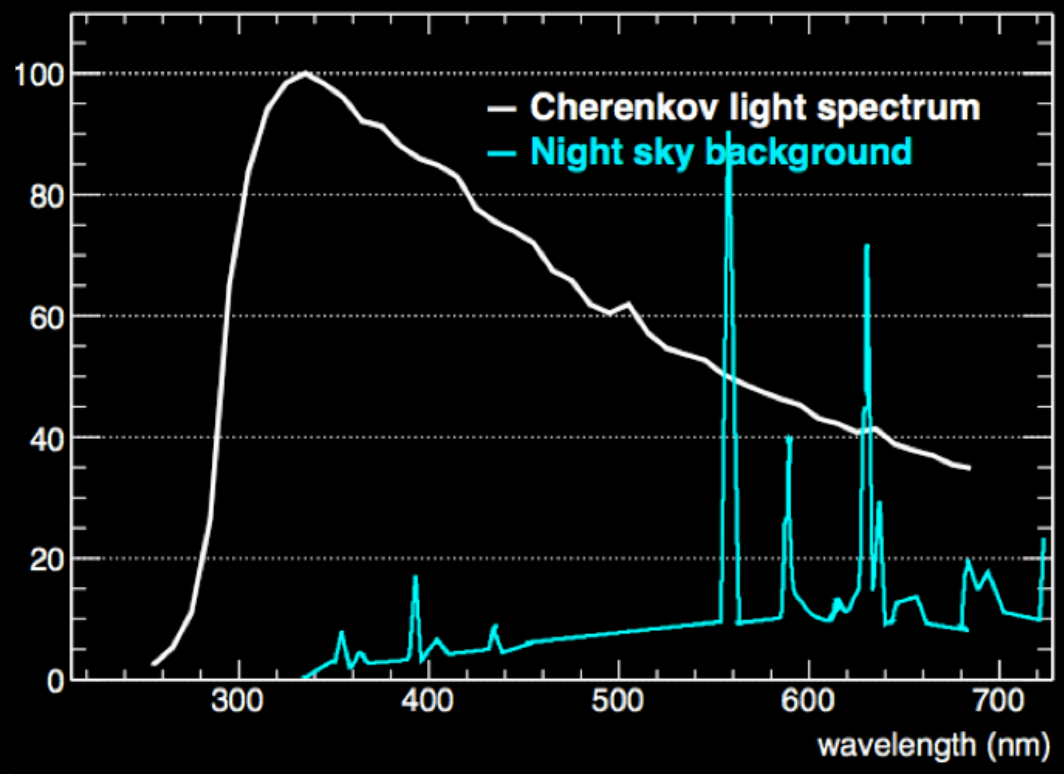


Adapted from de La Calle Perez, Biller, 2006

Technique
background

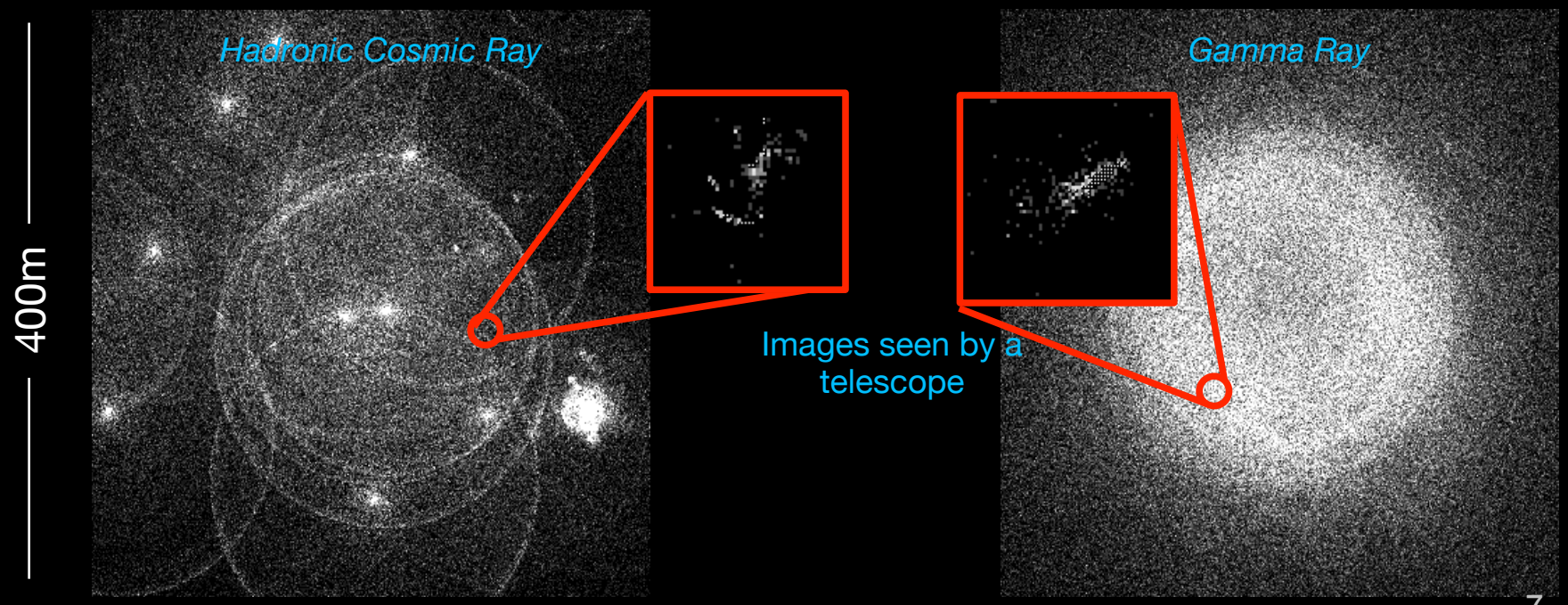
University of Leicester

- Night Sky Background (NSB)
  - Stars, air-glow, Zodiacal light...
  - Extra-galactic rate ~100 MHz (for 100m^2 dish, 0.15^o pix)
  - → Can reduce using online triggering



Technique
background

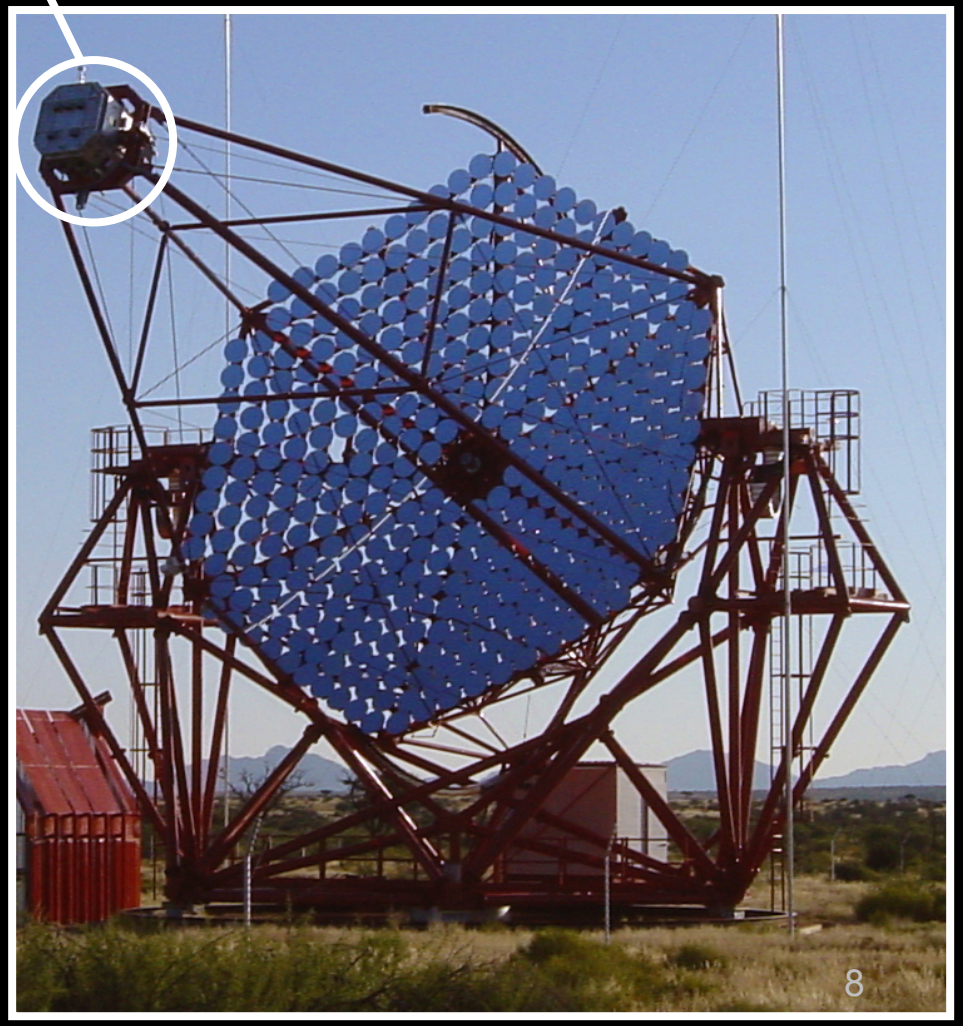
- Cosmic rays
  - Rate dominates gamma-ray rate, even after NSB is reduced
  - ~100 kHz for ~100 GeV threshold
  - → Offline image analysis



from Jamie Holder

Key Technology

the camera: an example from HESS



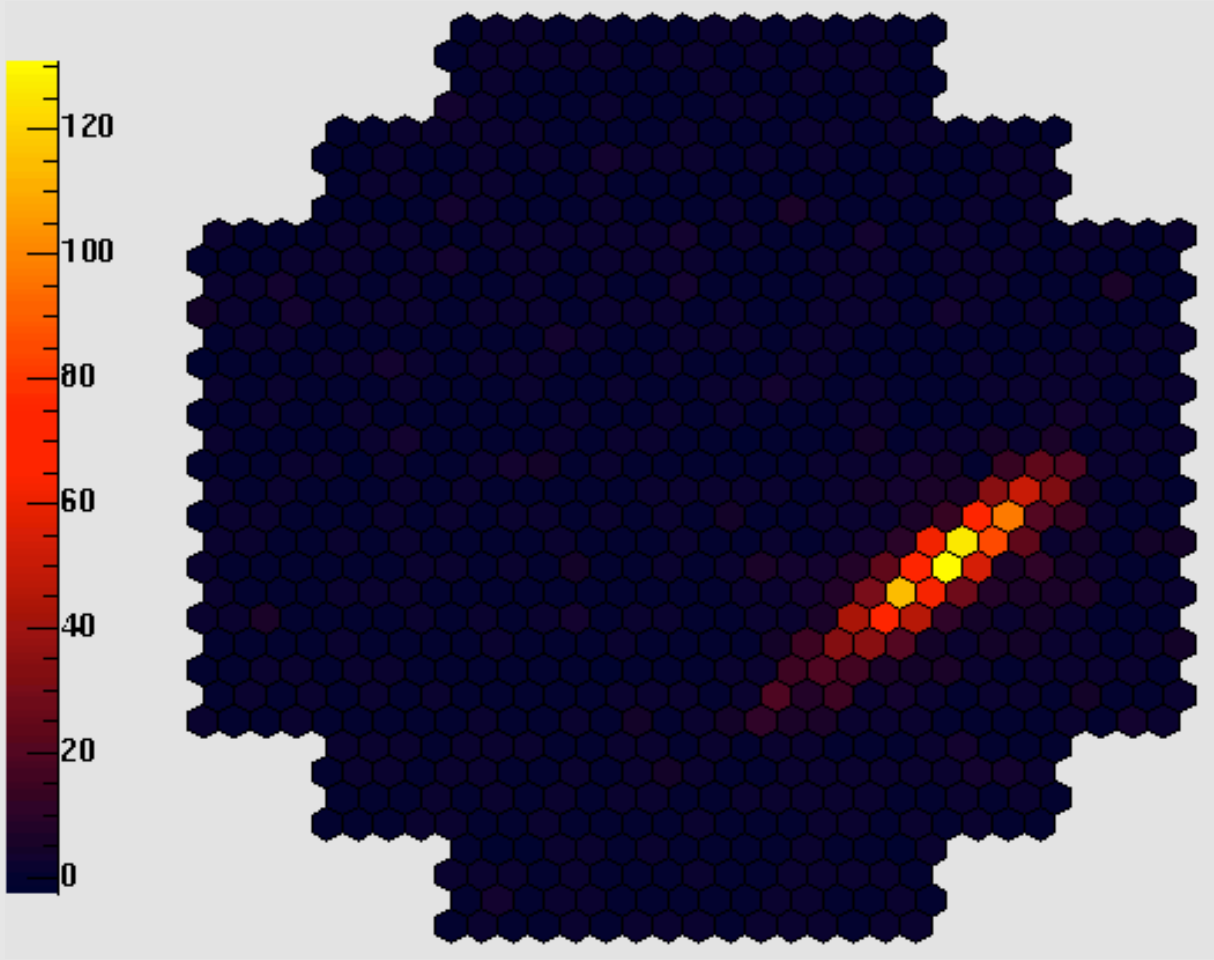
960 PMT pixels

Angular pixel size: 0.16°

Camera diameter: 5° FoV (1.4 m)

Key Technology

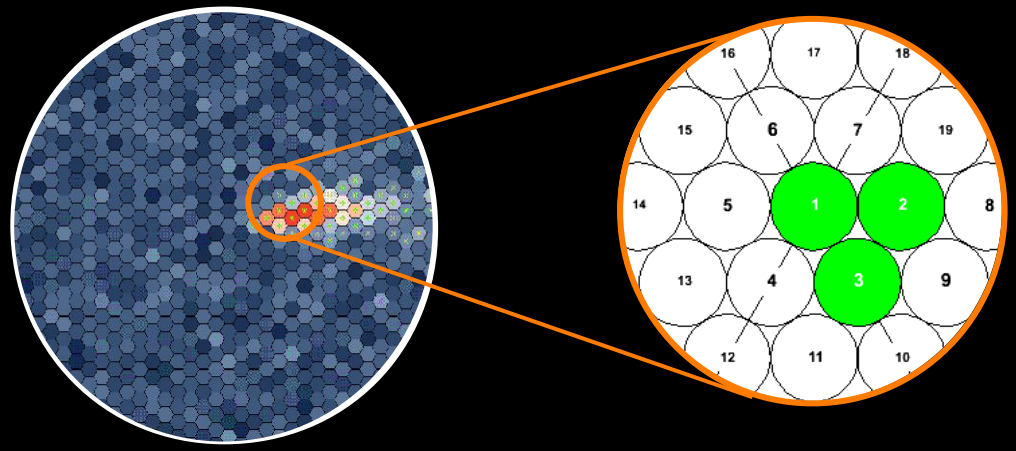
the camera: an example from HESS

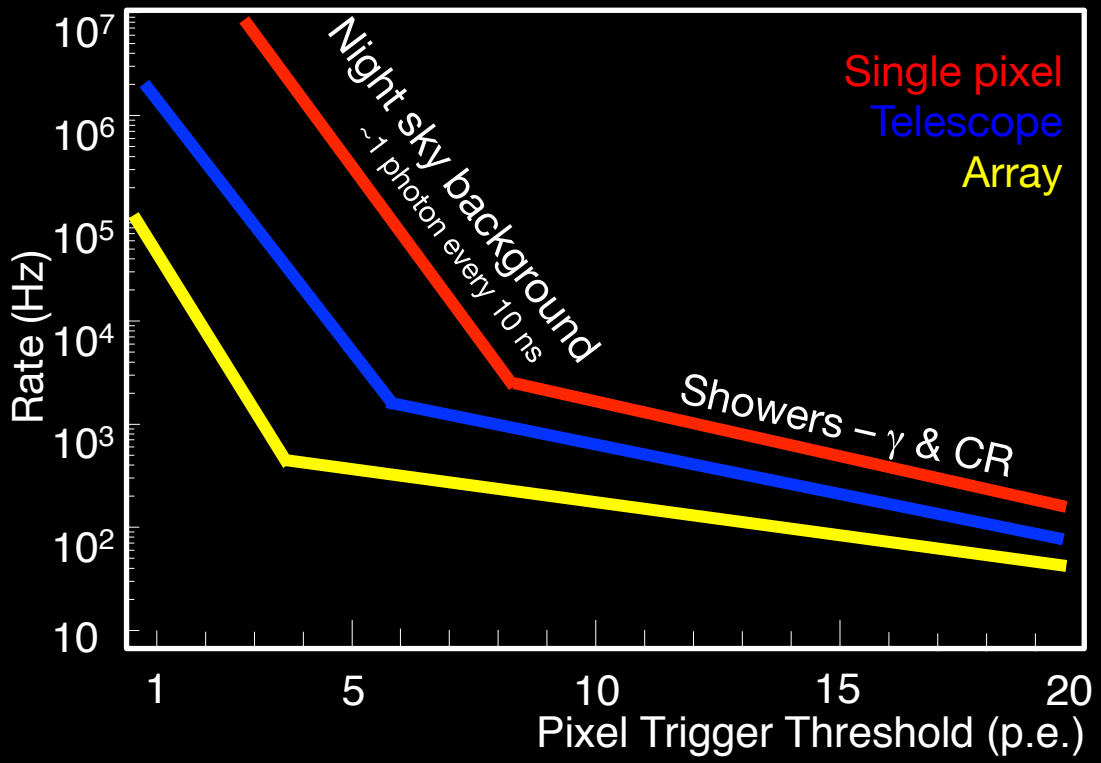


Highly pixelated, fixed (16 ns) exposures

Triggering

- Pixel level:
  - Threshold on every pixel
  - → 1 – 10 MHz
- Camera level:
  - Time coincidence between neighbouring pixels
  - At least 3 in <5 ns
  - → 1 – 10 kHz
- Array level:
  - At least 3 telescopes in <70 ns
  - → ~few hundred Hz

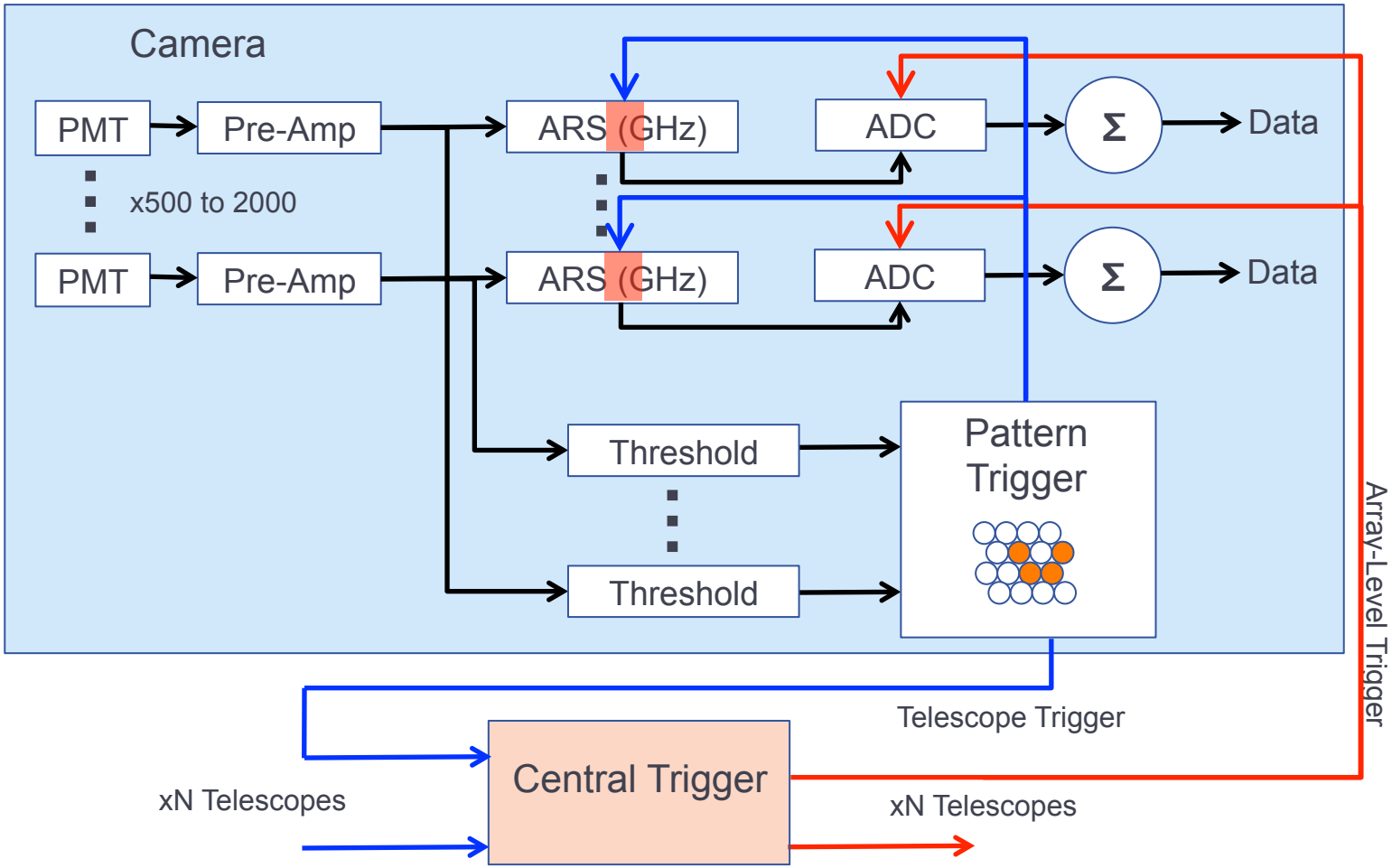




Front End Electronics

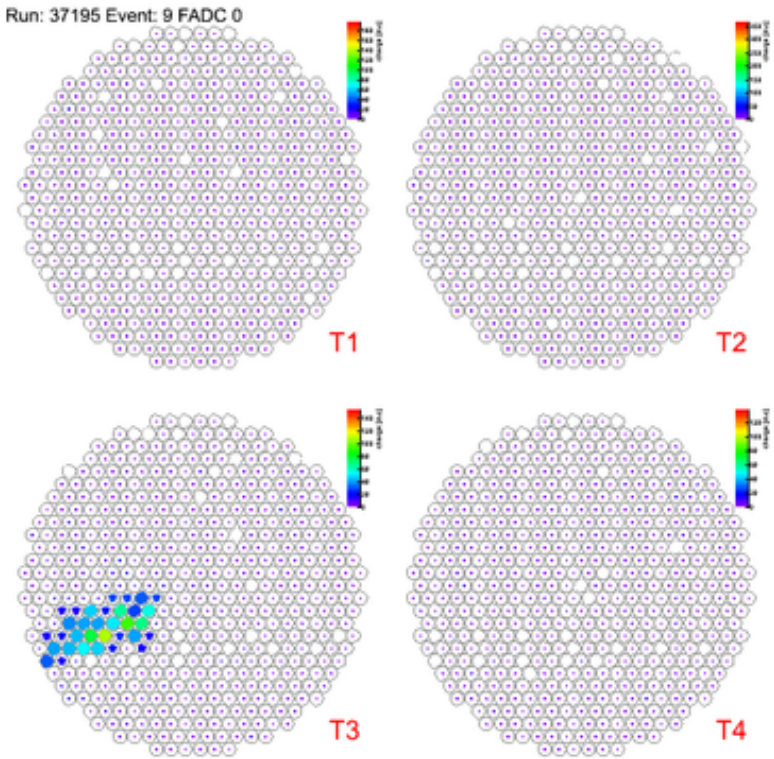
Waveform Sampling ASICs

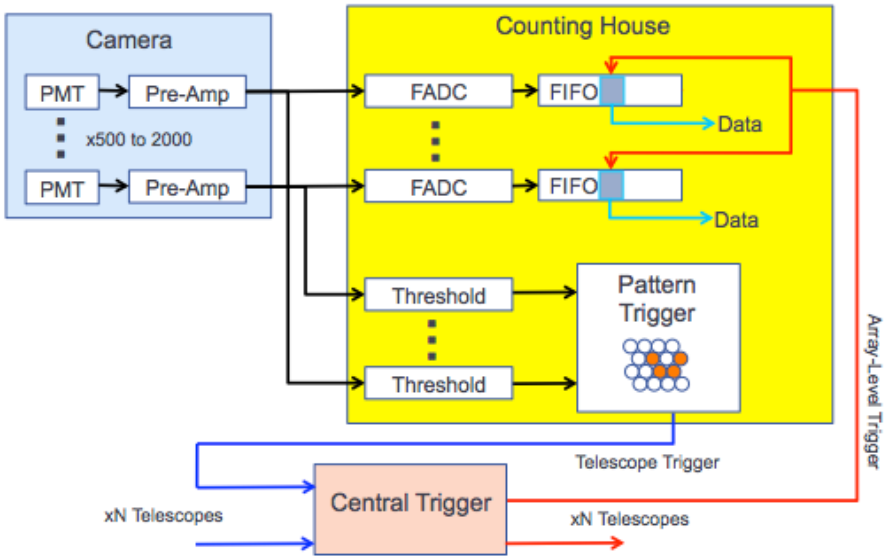
- Capacitor array
- Slow ADC digitises signal
- Compact and low power
- Data output is the integrated signal

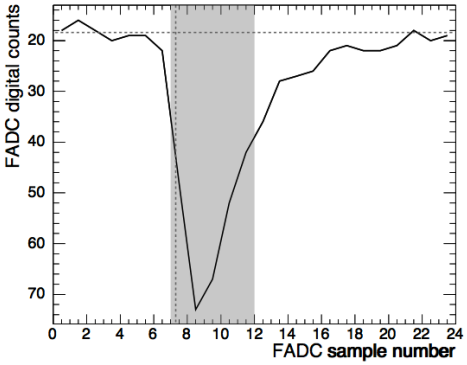


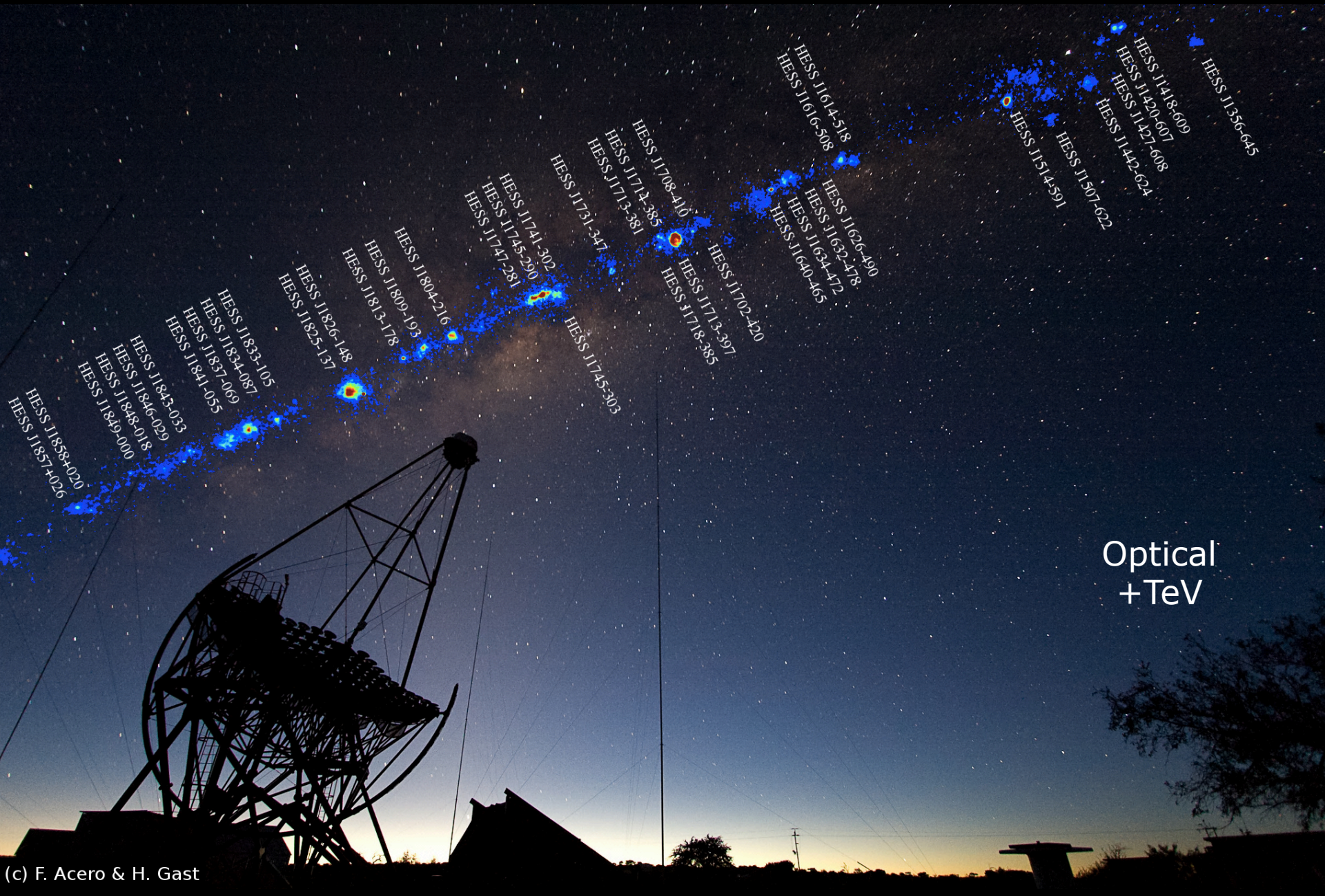
Front End Electronics

FADC Pipeline








HESS J1858+020
HESS J1857+026
HESS J1849-000
HESS J1848-018
HESS J1846-029
HESS J1843-033
HESS J1841-055
HESS J1837-069
HESS J1834-087
HESS J1833-105
HESS J1825-137
HESS J1826-148
HESS J1813-178
HESS J1809-193
HESS J1804-216
HESS J1747-281
HESS J1745-290
HESS J1741-302
HESS J1745-303
HESS J1731-347
HESS J1713-381
HESS J1714-385
HESS J1708-410
HESS J1718-385
HESS J1713-397
HESS J1702-420
HESS J1640-465
HESS J1634-472
HESS J1632-478
HESS J1626-490
HESS J1616-508
HESS J1614-518
HESS J1514-591
HESS J1507-622
HESS J1442-624
HESS J1427-608
HESS J1420-607
HESS J1418-609
HESS J1356-645
Optical
+TeV
(c) F. Acero & H. Gast

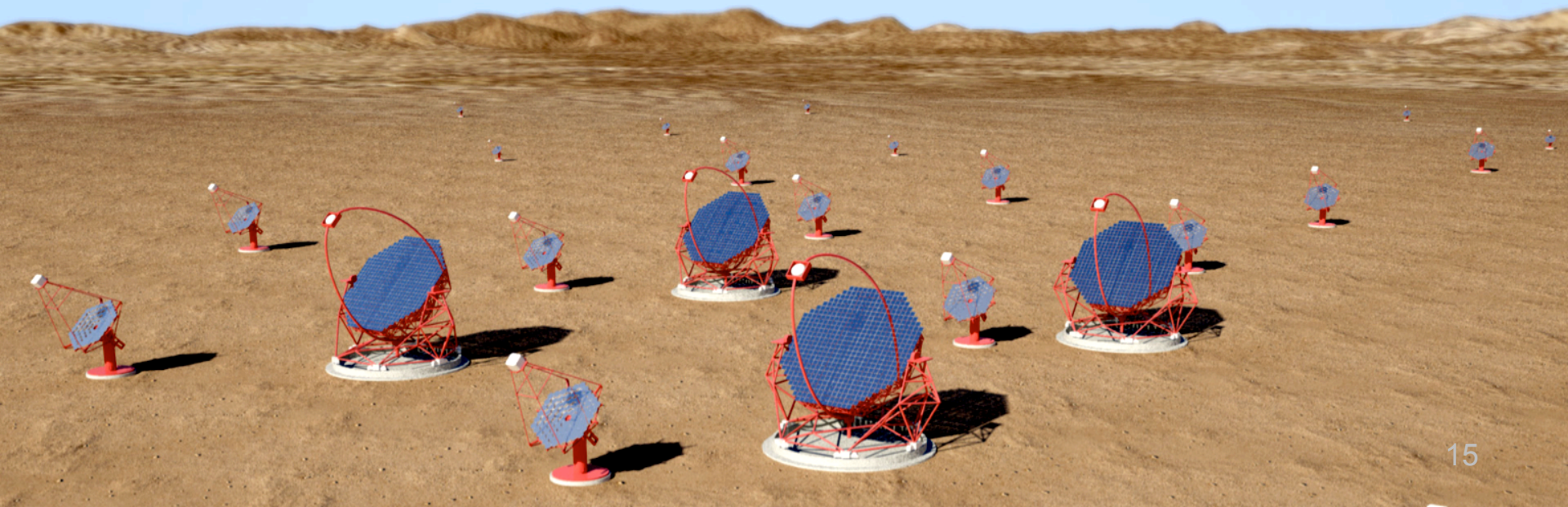
THE STATE OF THE ART:

HESS-2

HESS-1: 4 x 12m tels
HESS-2: +28m tel

The Cherenkov Telescope Array

- A huge improvement in all aspects of performance
- A user facility / proposal-driven observatory
  - With two sites and a total of >100 telescopes
- A global ~€200M project
  - Including everyone from HESS, MAGIC and VERITAS
  - >1000 scientists and engineers across 27 countries



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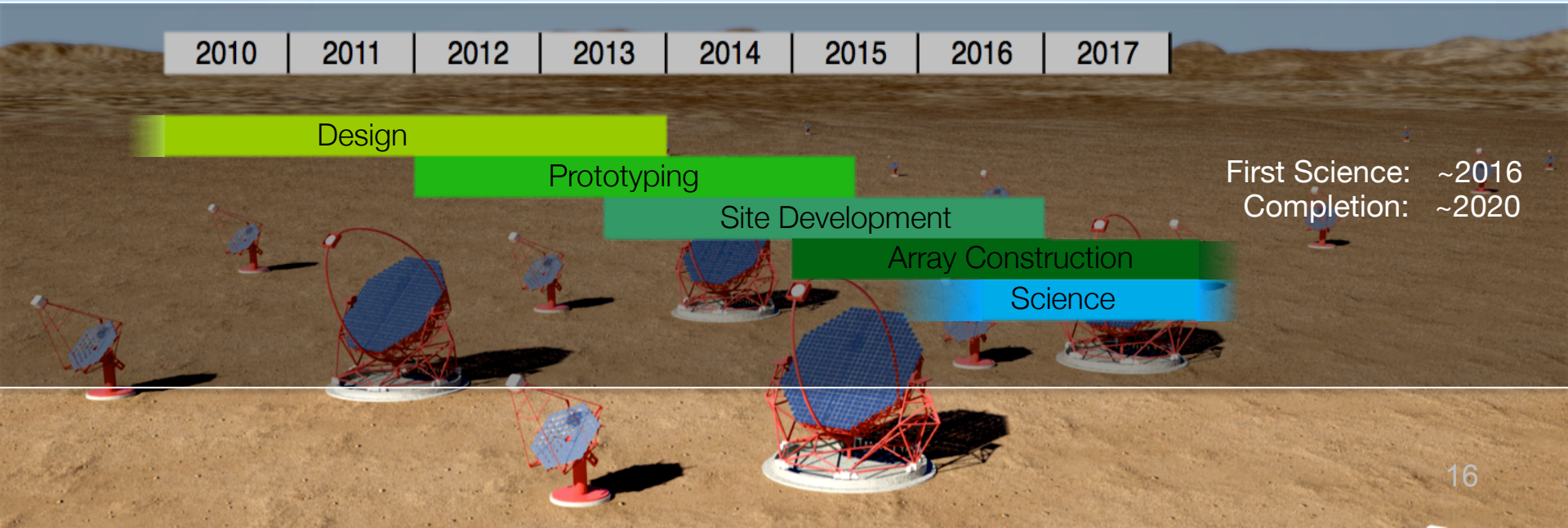
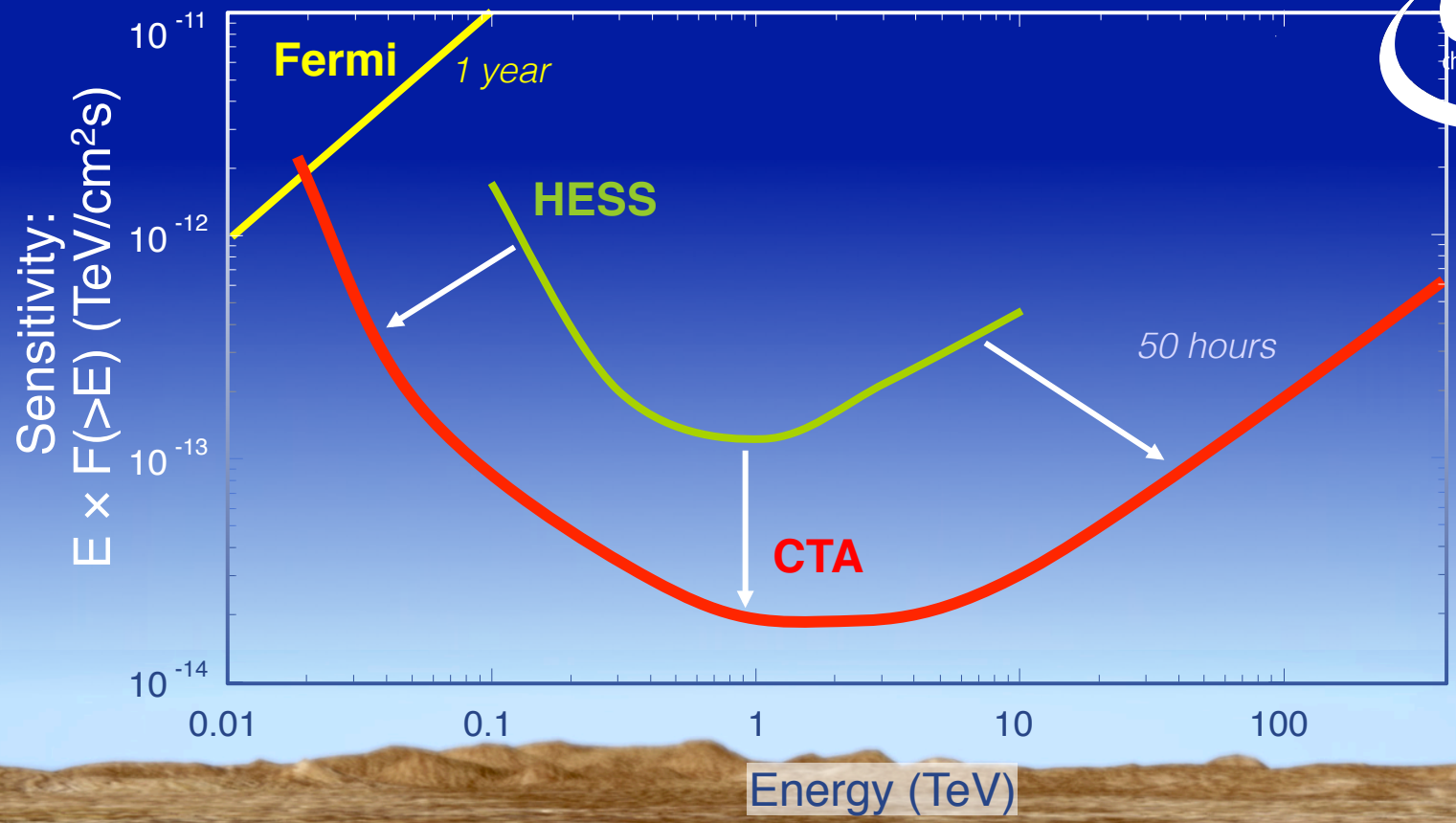
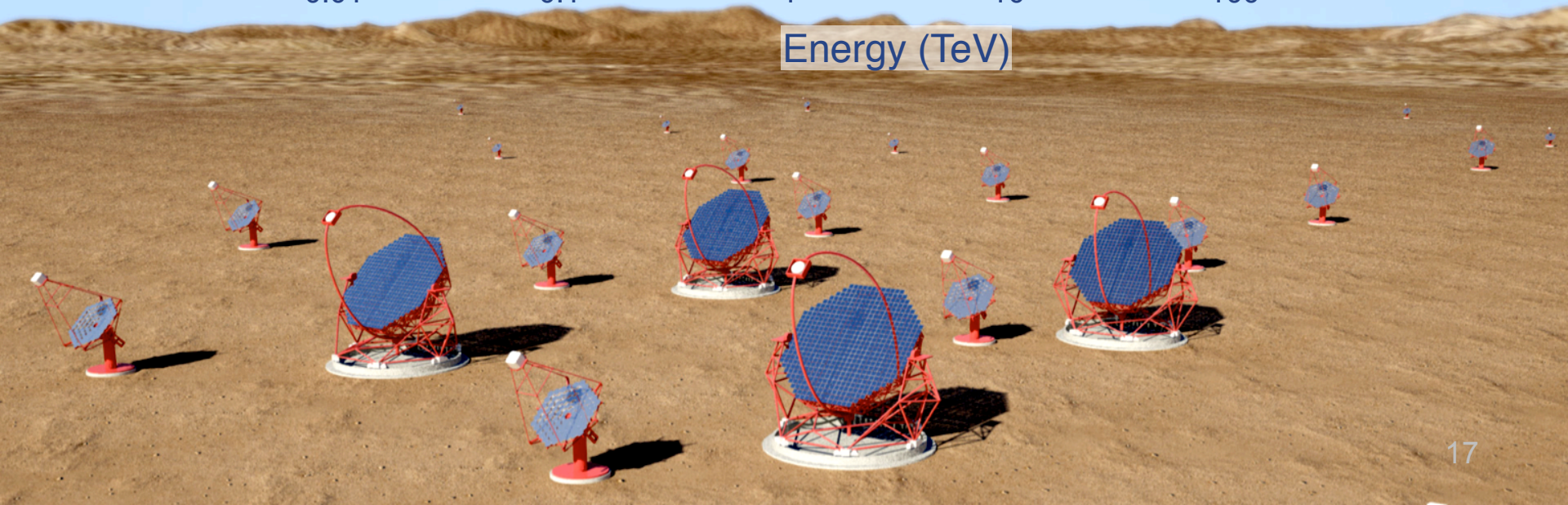
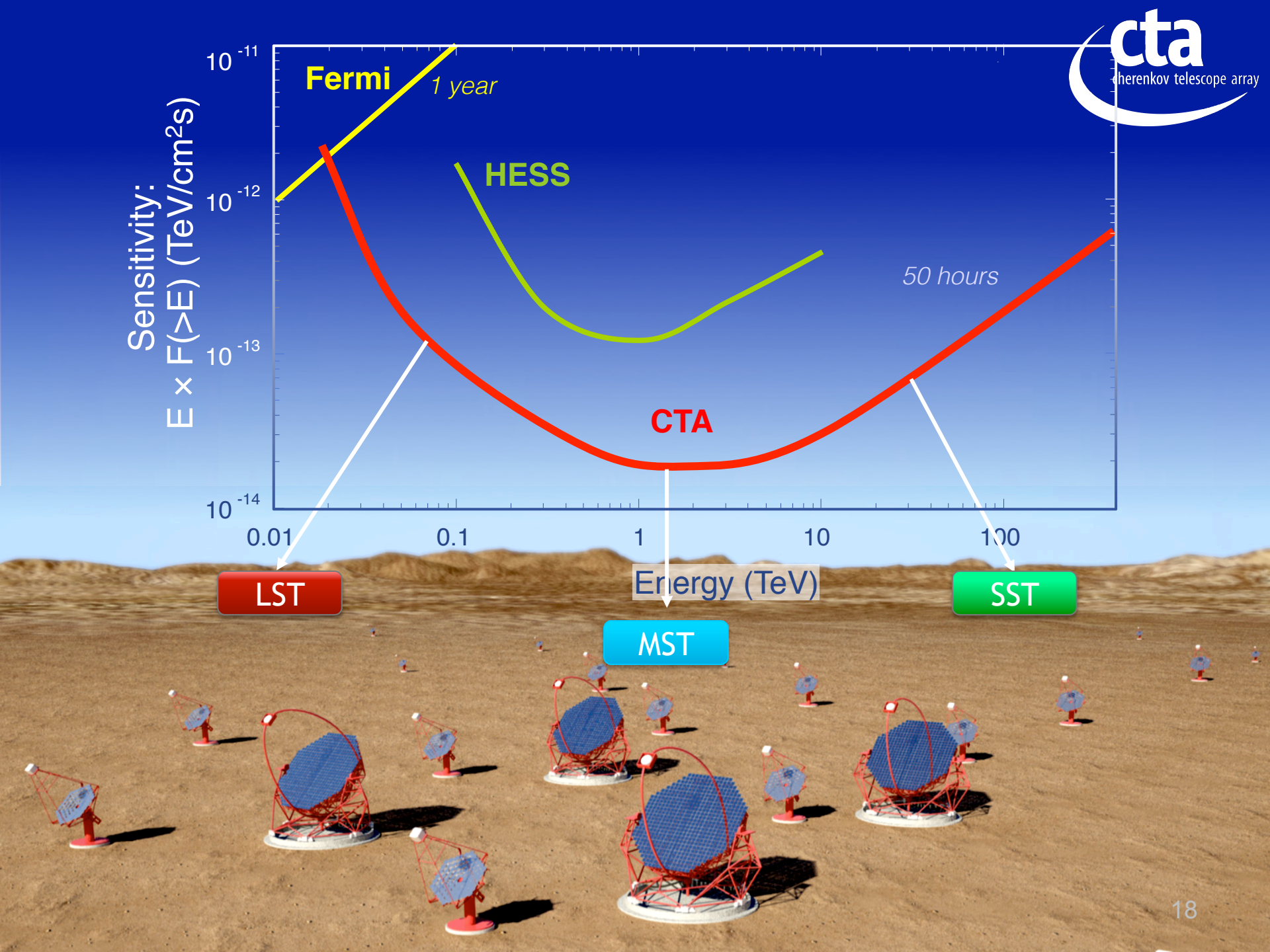



Fermi
1 year
HESS
50 hours
CTA
Sensitivity:
E × F(>E) (TeV/cm²s)
10 -11
10 -12
10 -13
10 -14
0.01
0.1
1
10
100
Energy (TeV)

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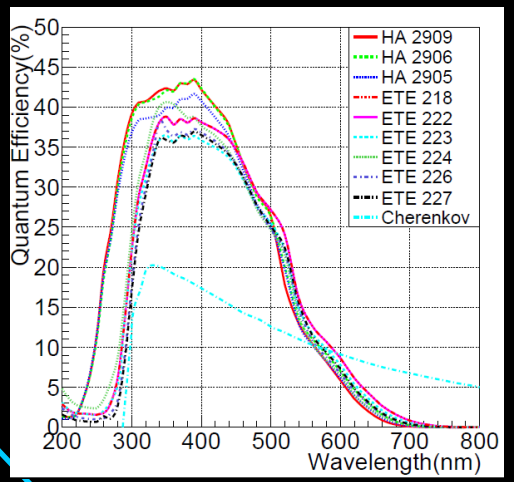
100
Energy (TeV)
LST
MST
SST

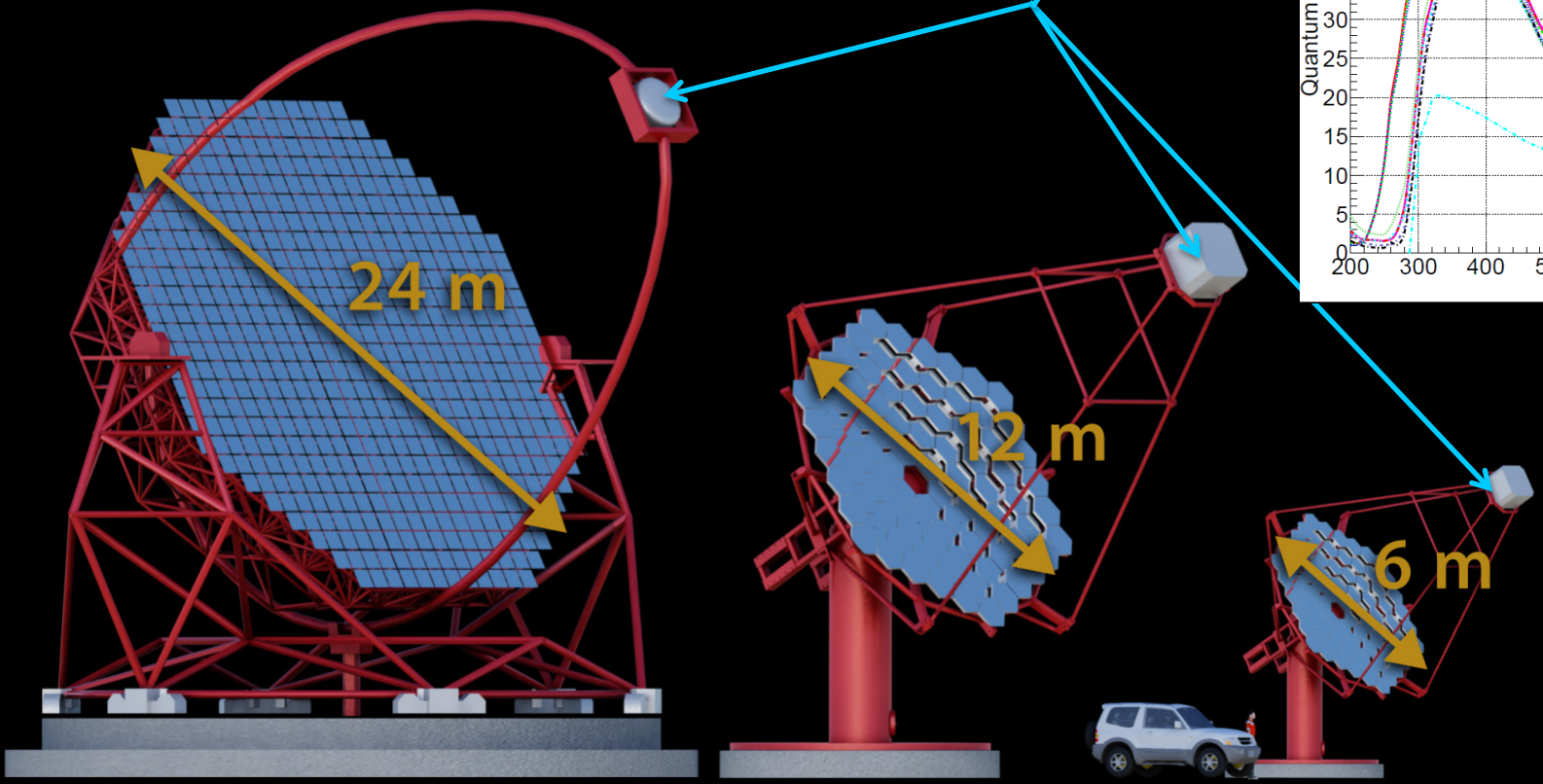
The Telescopes

University of Leicester

Baseline photosensors:
Hamamatsu 1.5" photomultipliers (R11920-100-20)

- Developed by Hamamatsu & MPI Munich for CTA
- Super Bialkali (Sba) photocathode
- ~20% of Cherenkov photons 300-600 nm





The Telescopes

University of Leicester

LST

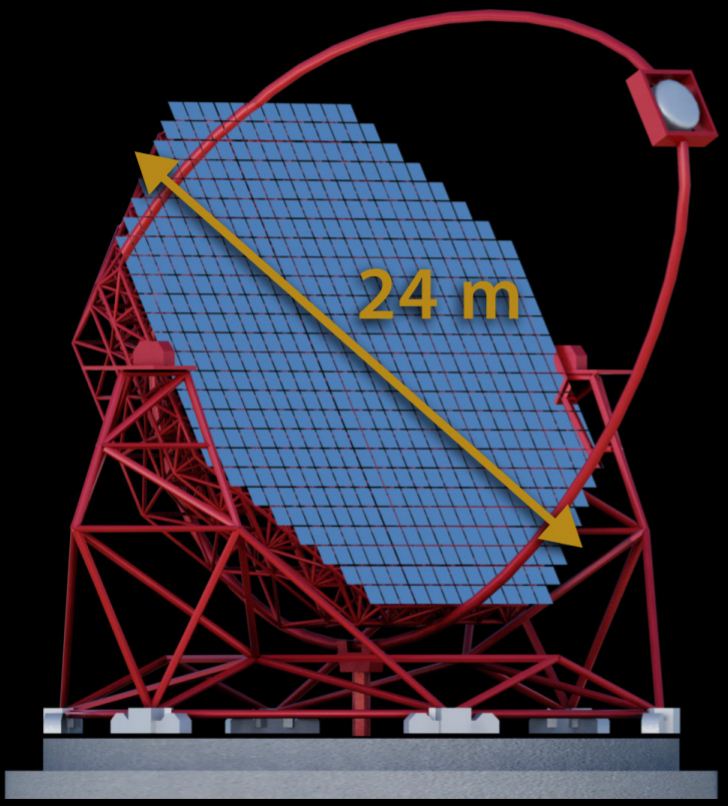
- ~4
- threshold ~30 GeV
- ~2.2 m Camera
- 4.5° FoV
- 1700 Pixels

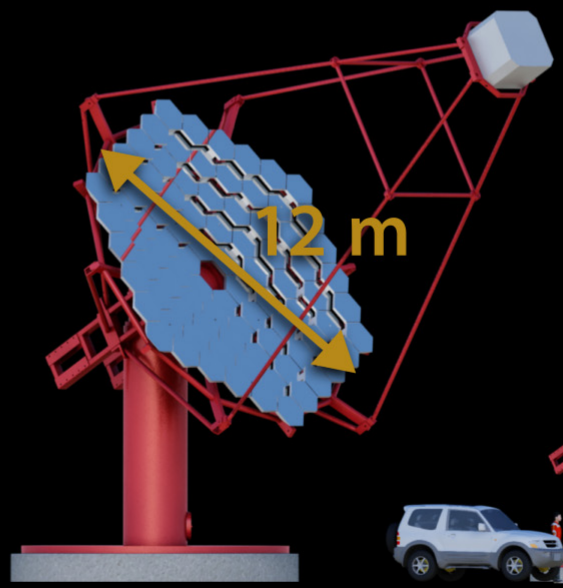
MST

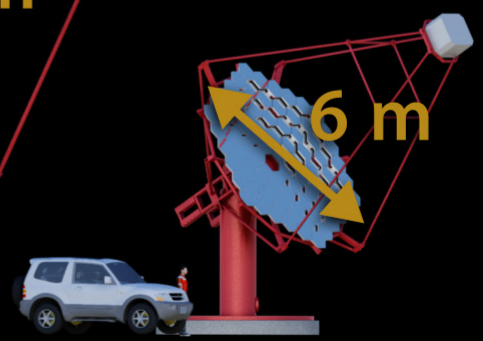
- ~25
- 200 GeV– 5 TeV
- ~2 m Camera
- 7-8° FoV
- 1500-2000 Pixels

SST

- ~35
- 3 km^2 area
- ~1 TeV - 300 TeV
- ~1.5 m Camera
- 7-10° FoV
- 600-1300 Pixels







CTA FEE Technology

University of Leicester

SPARTAN 6

VIRTEX5

VIRTEX6

KINTEX7

...STARTING TO THINK ABOUT IT ANY WAY

VIRTEX7

CTA FEE Technology

Field

Programmable

Gate

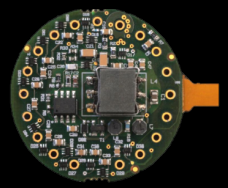
Array

- Trigger
  - ~2000 pixels in parallel, ns coincidence windows
  - Many different algorithms possible on the camera and array level.
- Data processing
  - Buffering
  - Serialisation, (up to 2.5 Gbps x 32 per FPGA)
- Time stamping / clock synchronisation
  - ~2 ns accuracy needed across 10 km^2
- Control

CTA FEE Technology

ASICs

- Preamplifiers
  - PACTA
    - 2 channels HG, LG
    - Differential output
    - 130 mW
    - 450 MHz



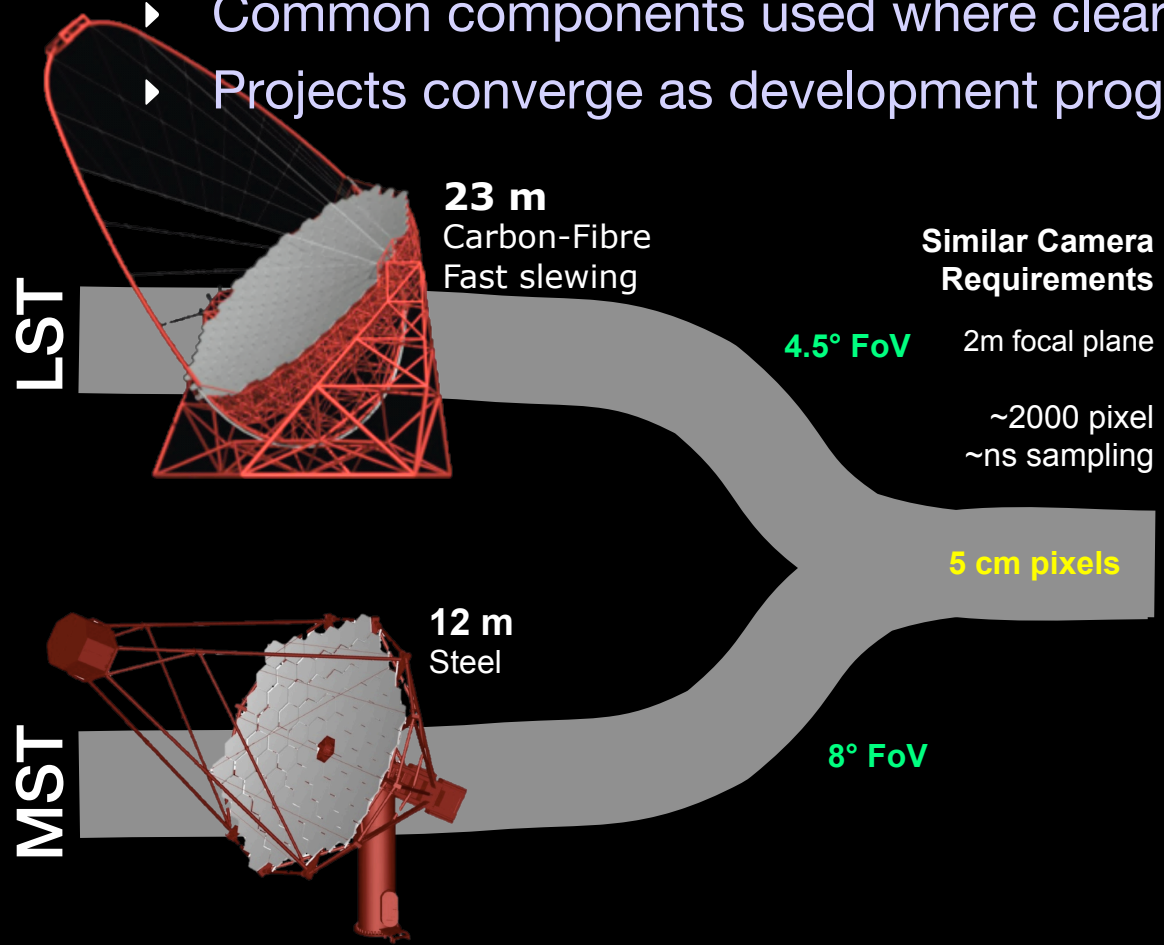
PACTA

- Waveform Sampling
  - NECTAr
    - 2 ch, 0.5 – 3.2 GSa/s
    - Includes 20 MHz ADC
  - DRS4
    - 8 ch, 0.7 – 5 GSa/s
    - No ADC
  - TARGET
  - EASIROC

Camera Development

University of Leicester

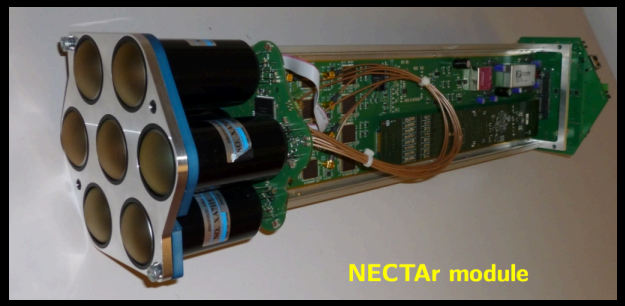
- Development strategy:
  - Several prototyping projects
  - Provides test beds for different technology and mitigates risk
  - Common components used where clear/possible
  - Projects converge as development progresses

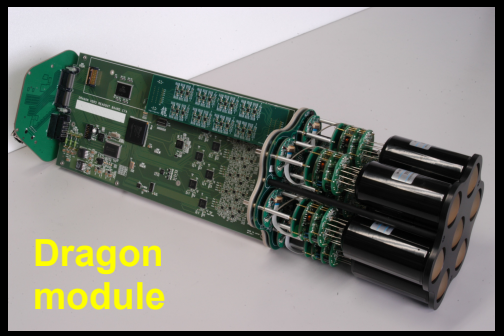


Similar Camera Requirements

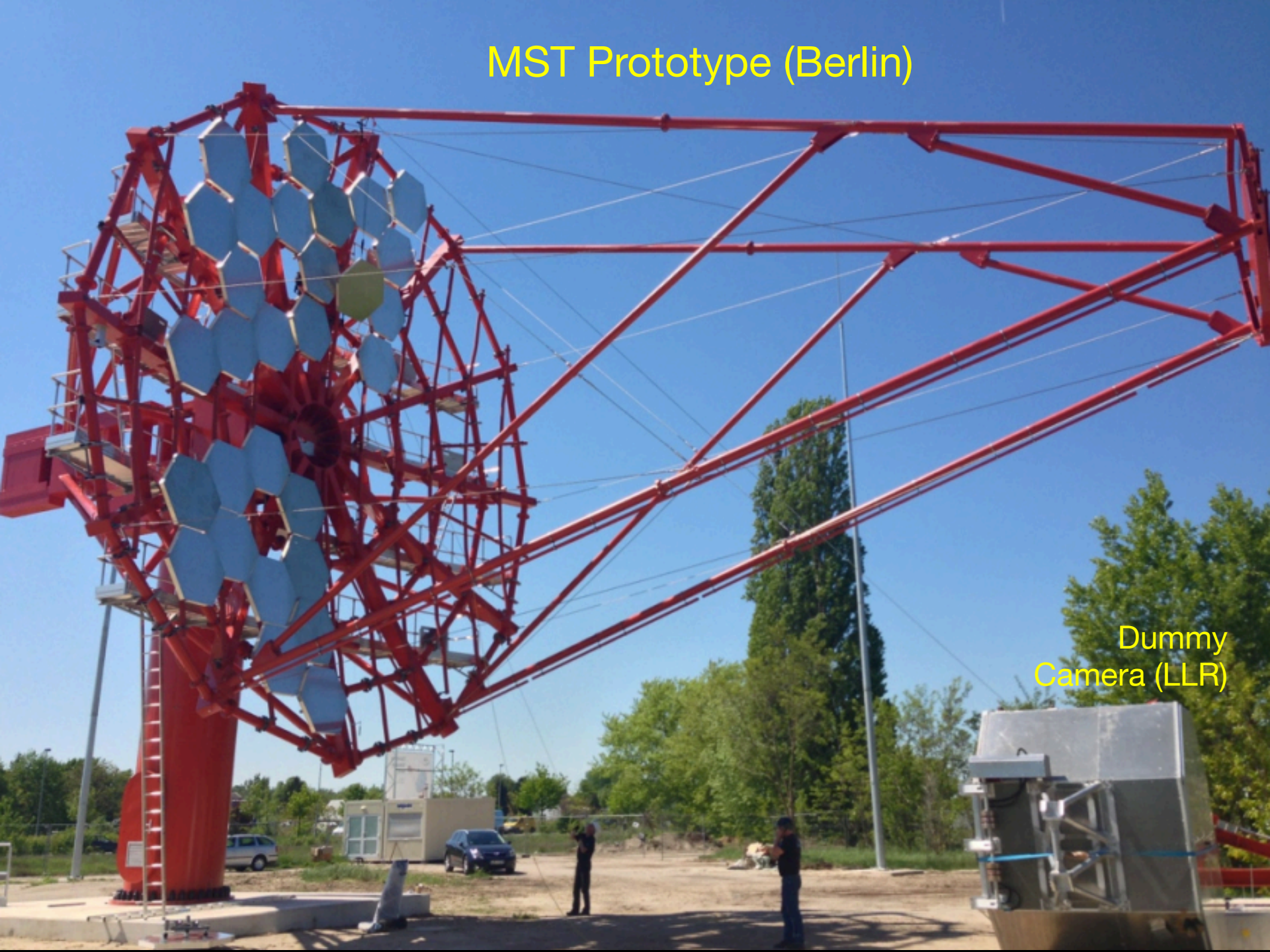
2m focal plane

~2000 pixel
~ns sampling





MST Prototype (Berlin)



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University of Leicester

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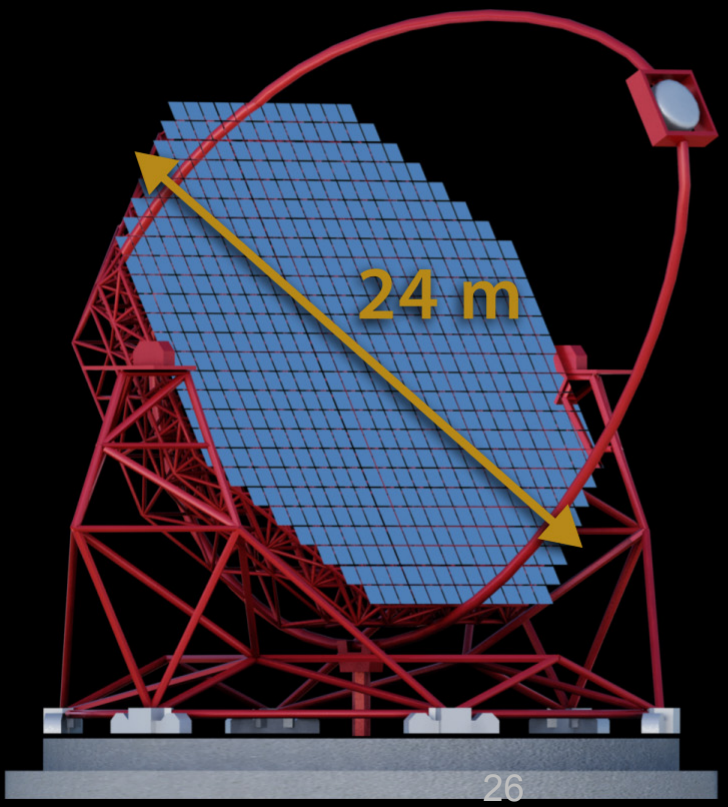

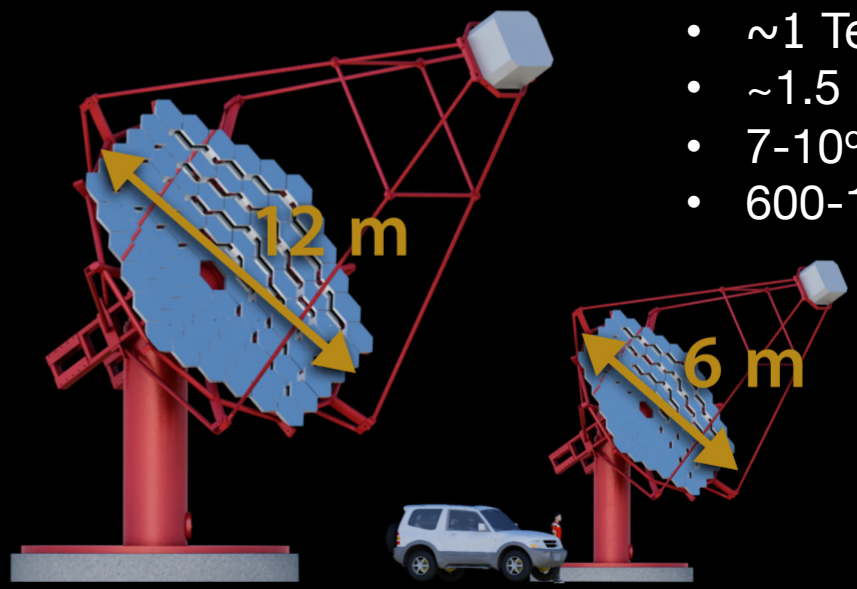

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The Telescopes

University of Leicester

LST

- ~4

Majority of the cost is in the structure (carbon fibre).

- 1700 Pixels

MST

- ~25

Camera and structure cost approximately the same.

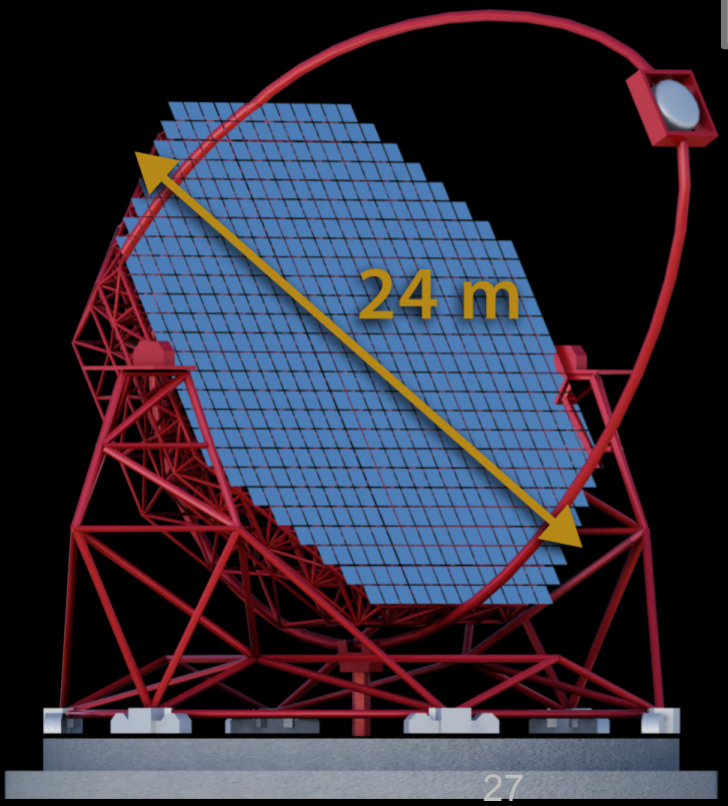
- 1500-2000 Pixels

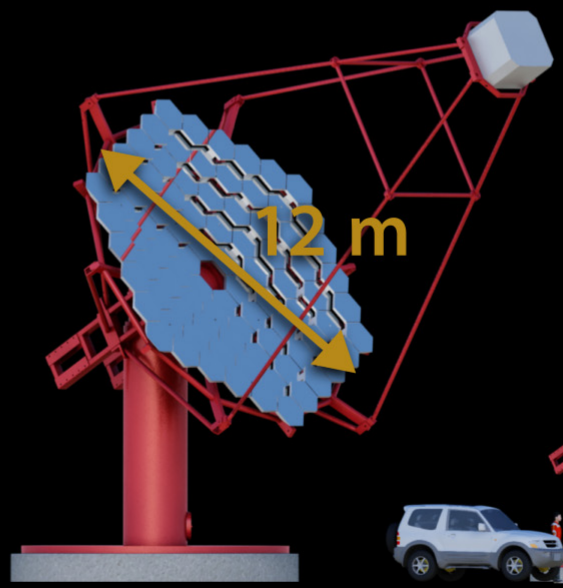
SST

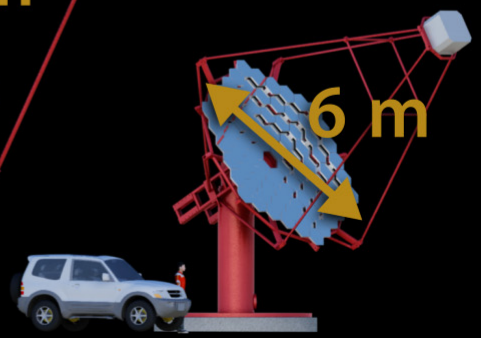
- ~35

Majority of the cost is in the camera…

- 7-10° FoV
- 600-1300 Pixels







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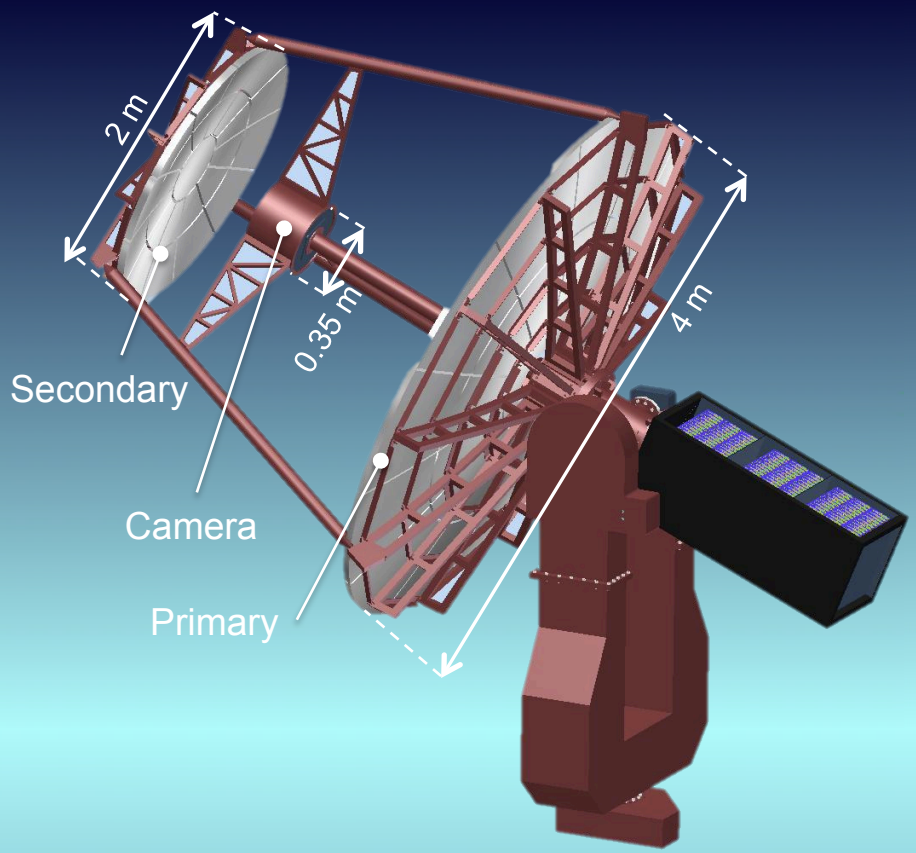
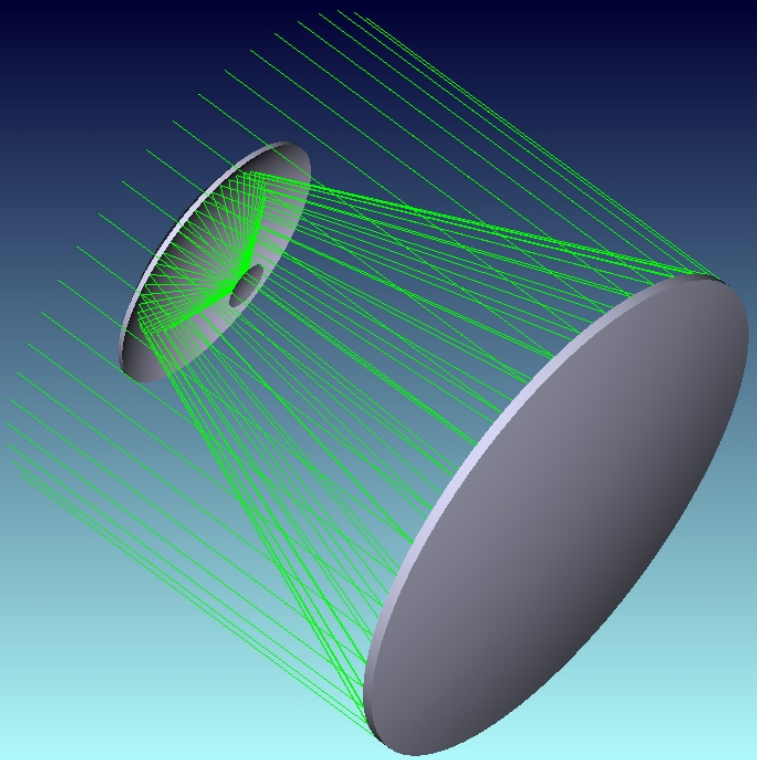
SST Dual Mirror Design

an option for the highest energies





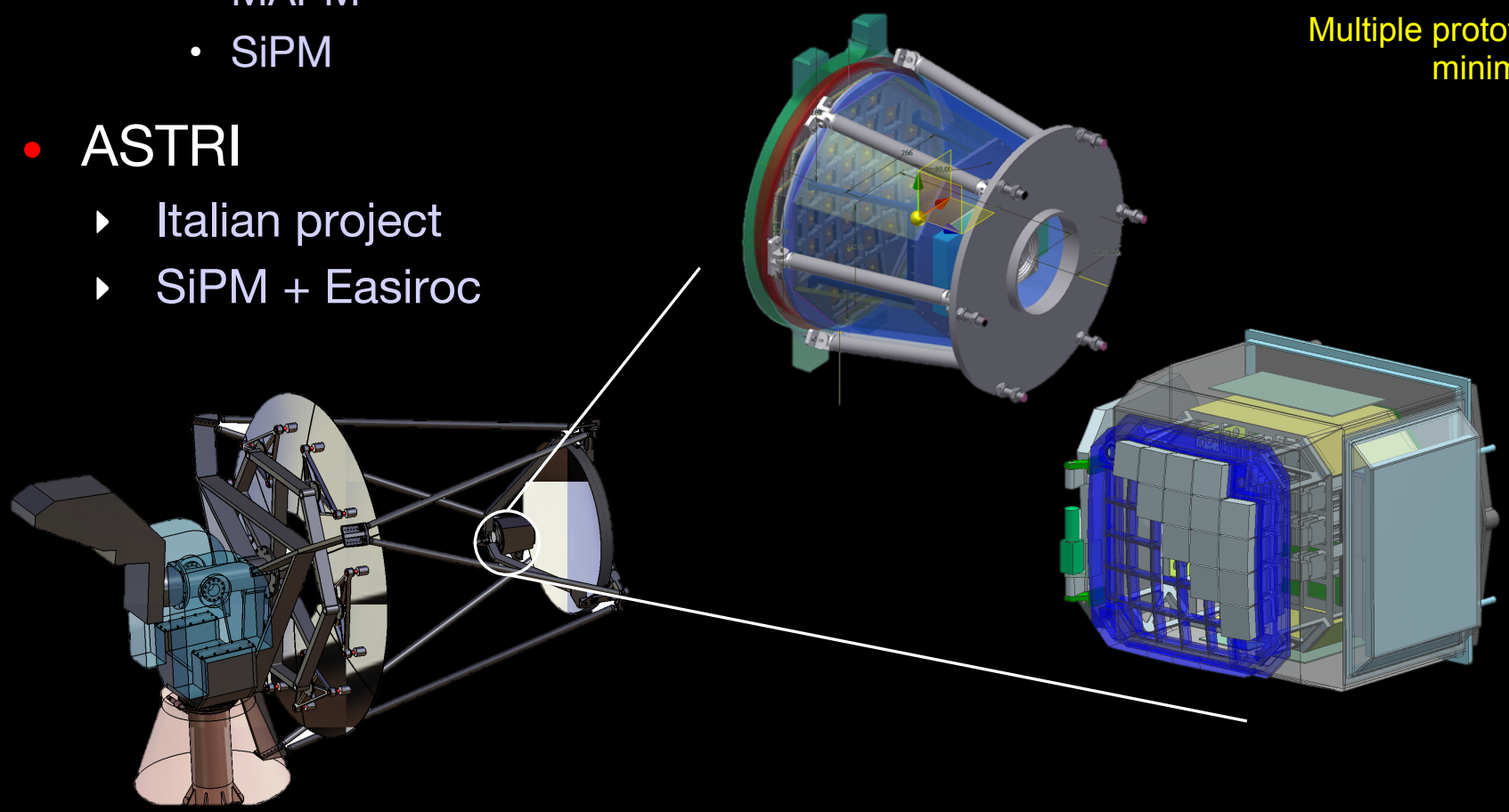
- Secondary optics reduces the plate scale:
  - Cheaper photosensors
  - The camera becomes 0.35 m across
  - ~70 SSTs become possible

Camera's for dual mirror SST

University of Leicester

- CHEC (Compact High Energy Camera)
  - UK, US, Japan, Netherlands
  - Funding in place for 2 prototype cameras with the same electronics but different photosensors
    - MAPM
    - SiPM
- ASTRI
  - Italian project
  - SiPM + Easiroc

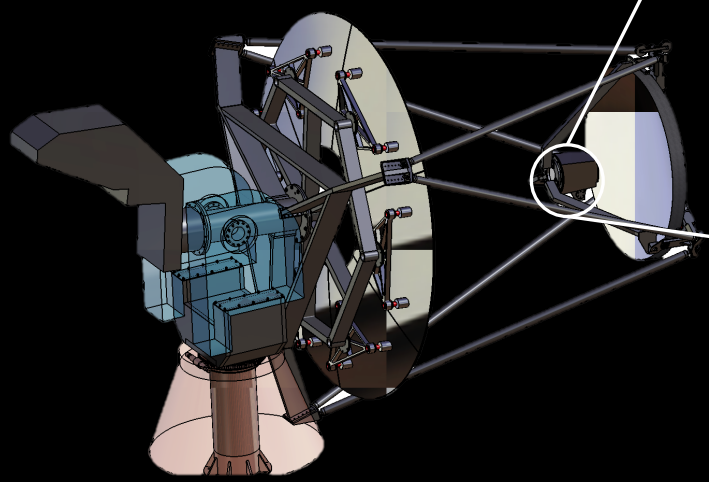
Multiple prototypes to minimise risk

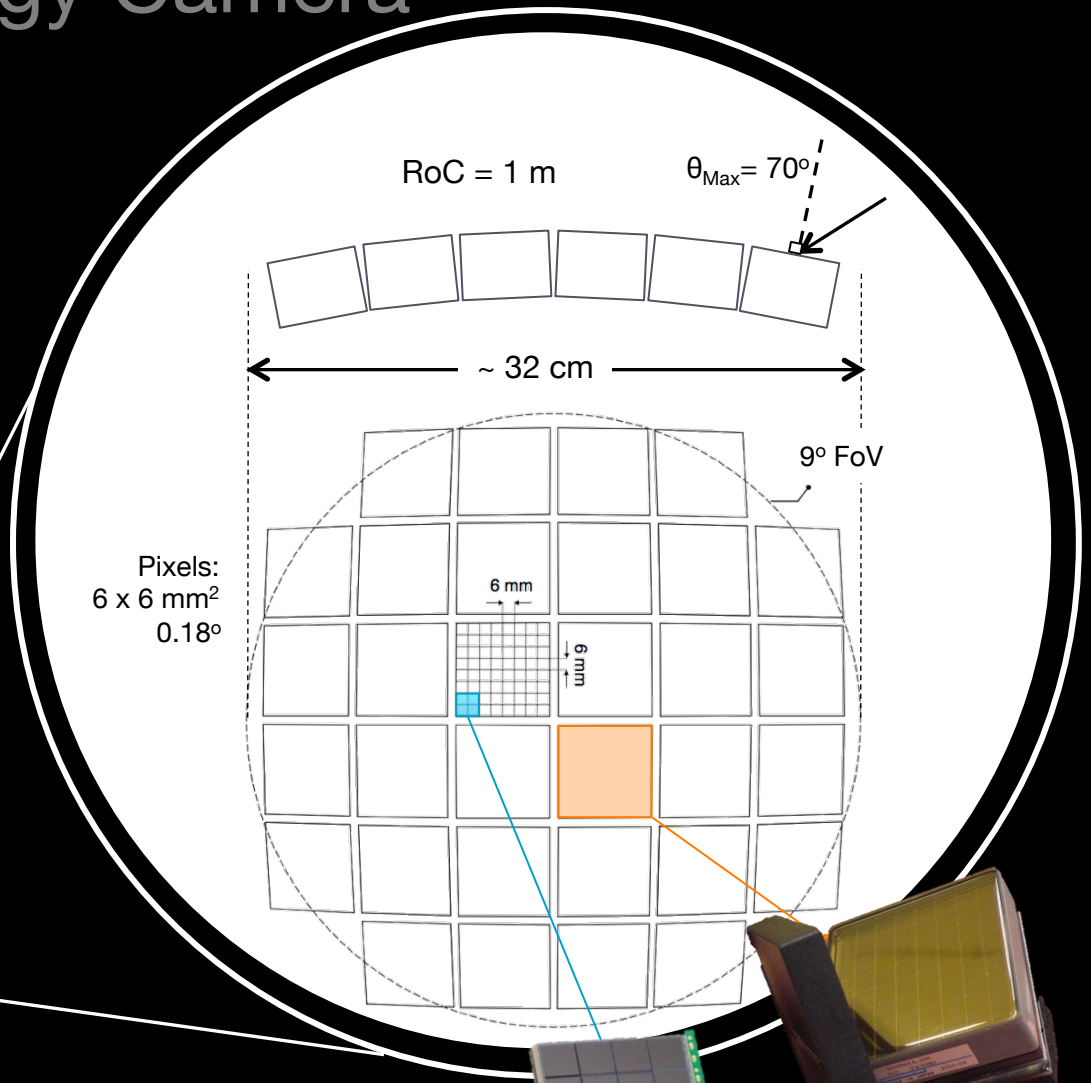


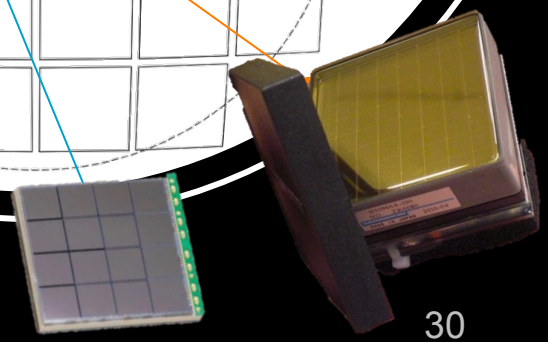
CHEC
Compact High Energy Camera

University of Leicester

- Focal Plane:
  - 9° FoV, 0.18° pixels
  - 32 cm diameter
- Challenges:
  - Curved focal plane
  - Incident light from large angles
  - Compact electronics

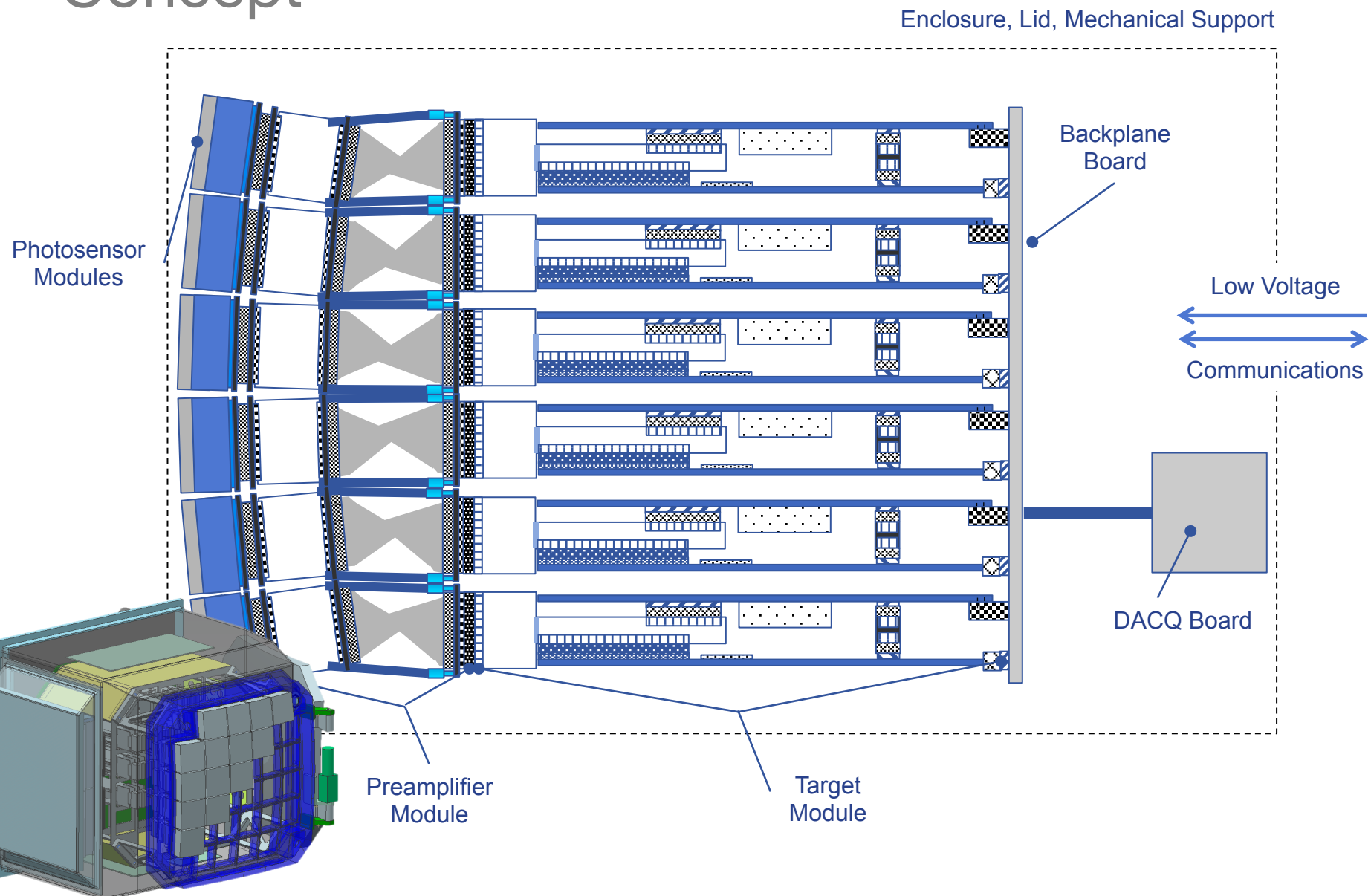






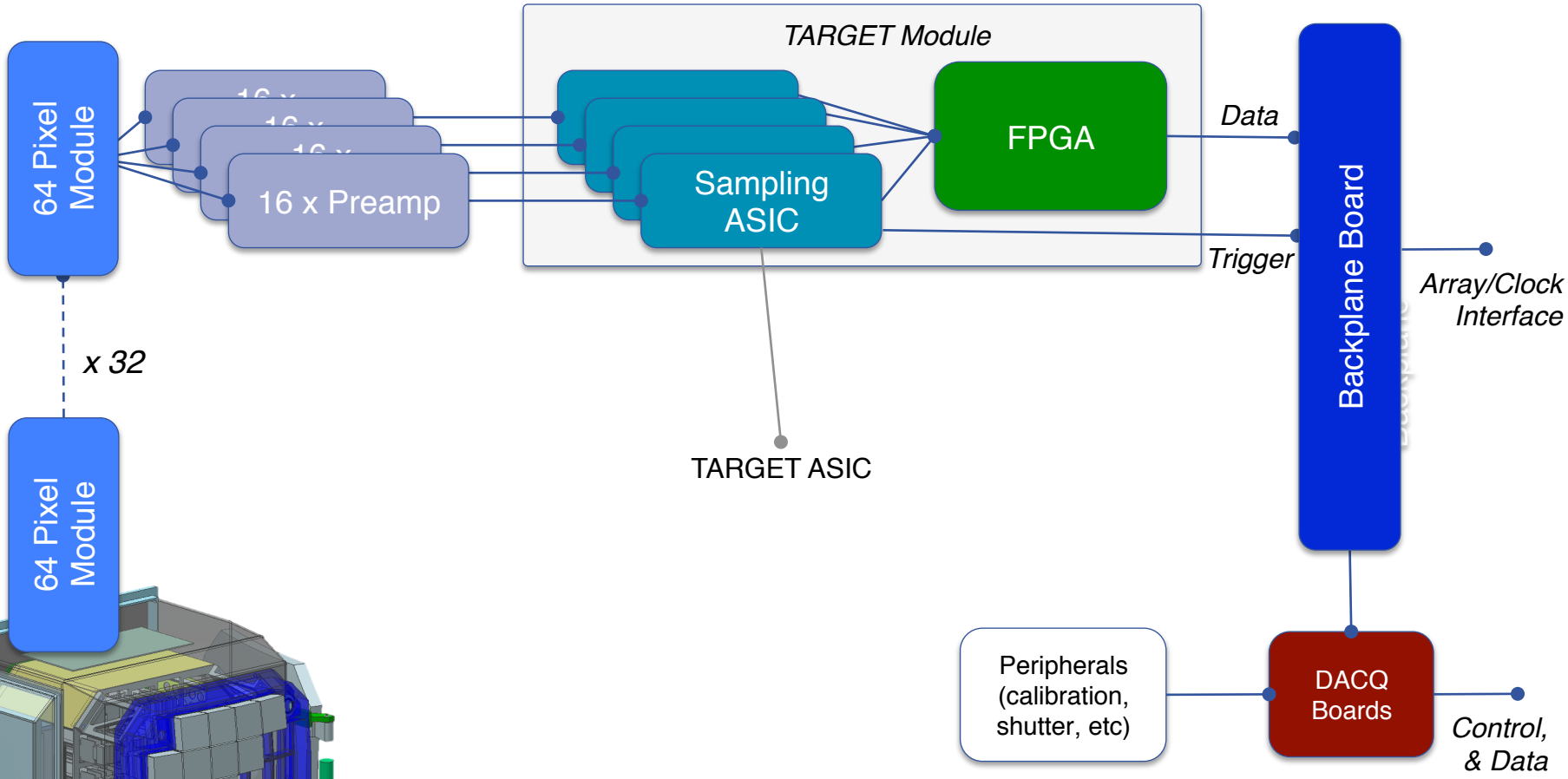
CHEC

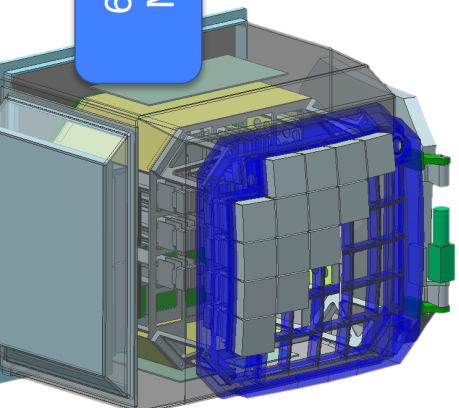
Concept



CHEC

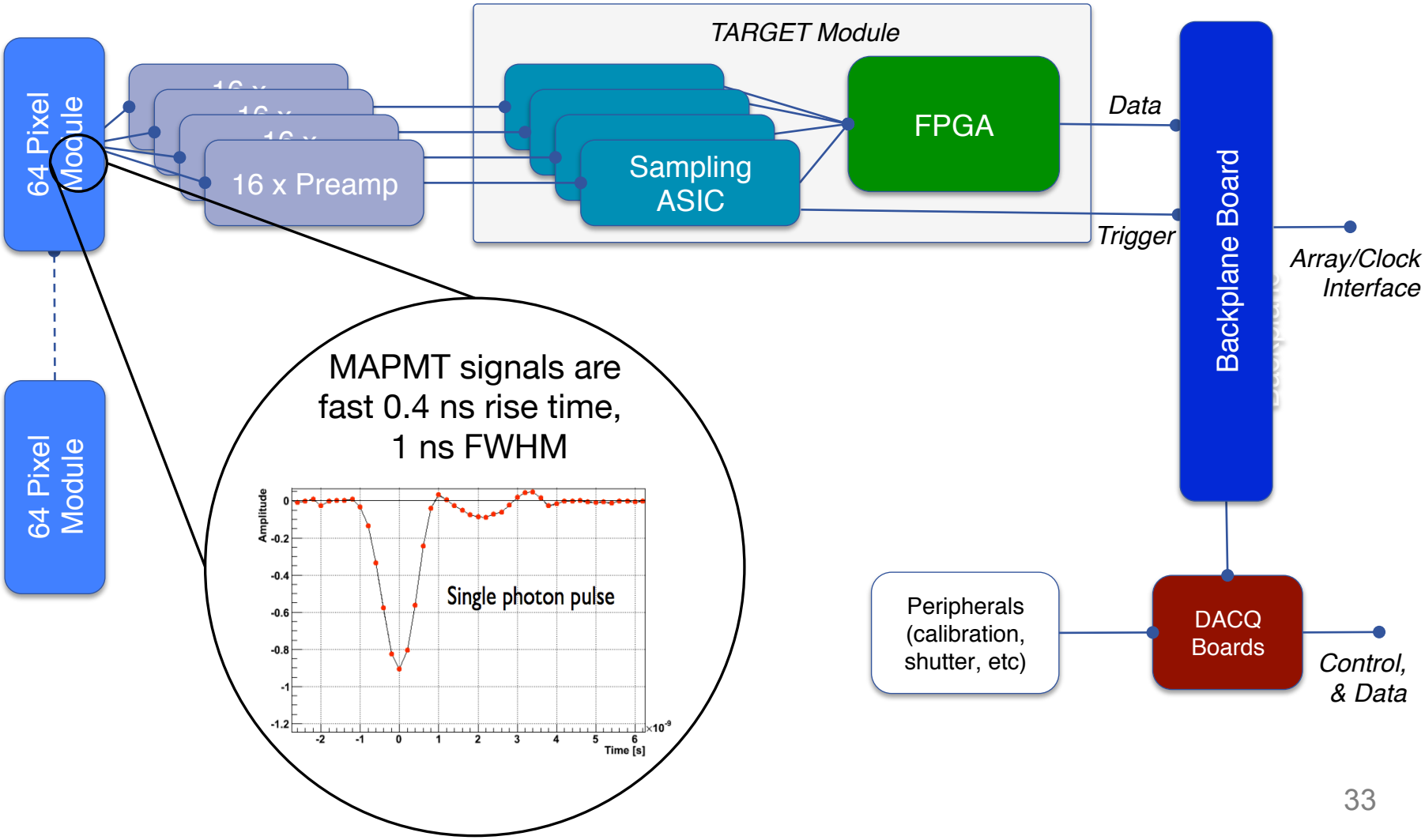
electronics & readout





CHEC

electronics & readout



CHEC Trigger Simulations

University of Leicester

- Pulse Shape Optimisation:
  - T_r = 3.5 – 6.0 ns
  - FWHM = 5.5 – 10.5 ns
  - …at TARGET input

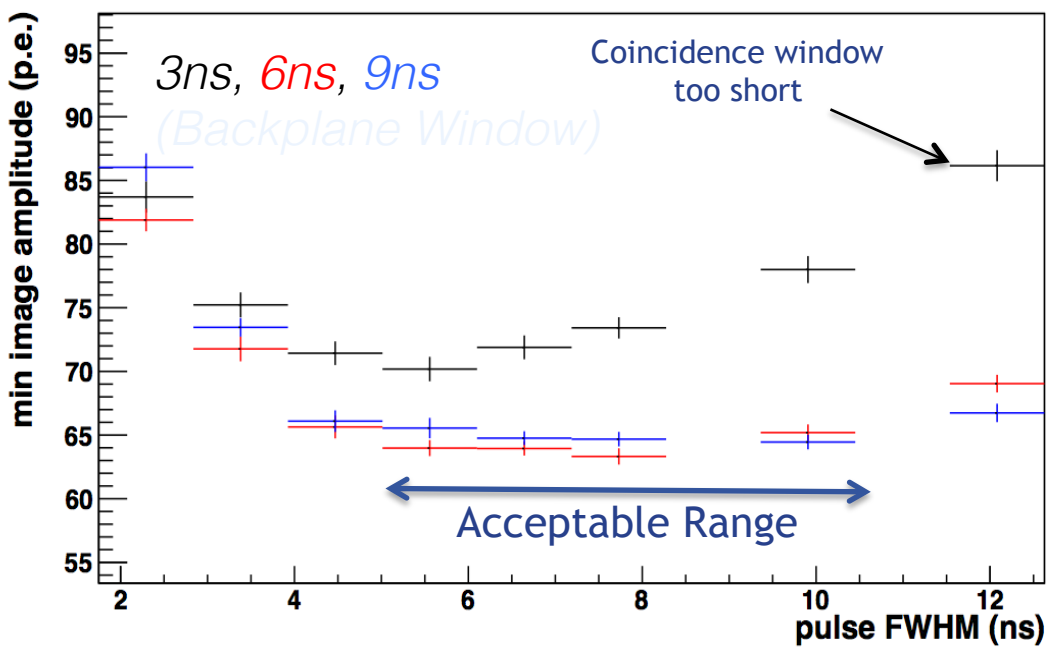
Pre-amplifier Requirements

- Trigger Logic:
  - Analogue sum of 4 pixels, then multiplicity of 2 patches

TARGET ASIC Requirements

Backplane Board Requirements (Neighbouring Patches)

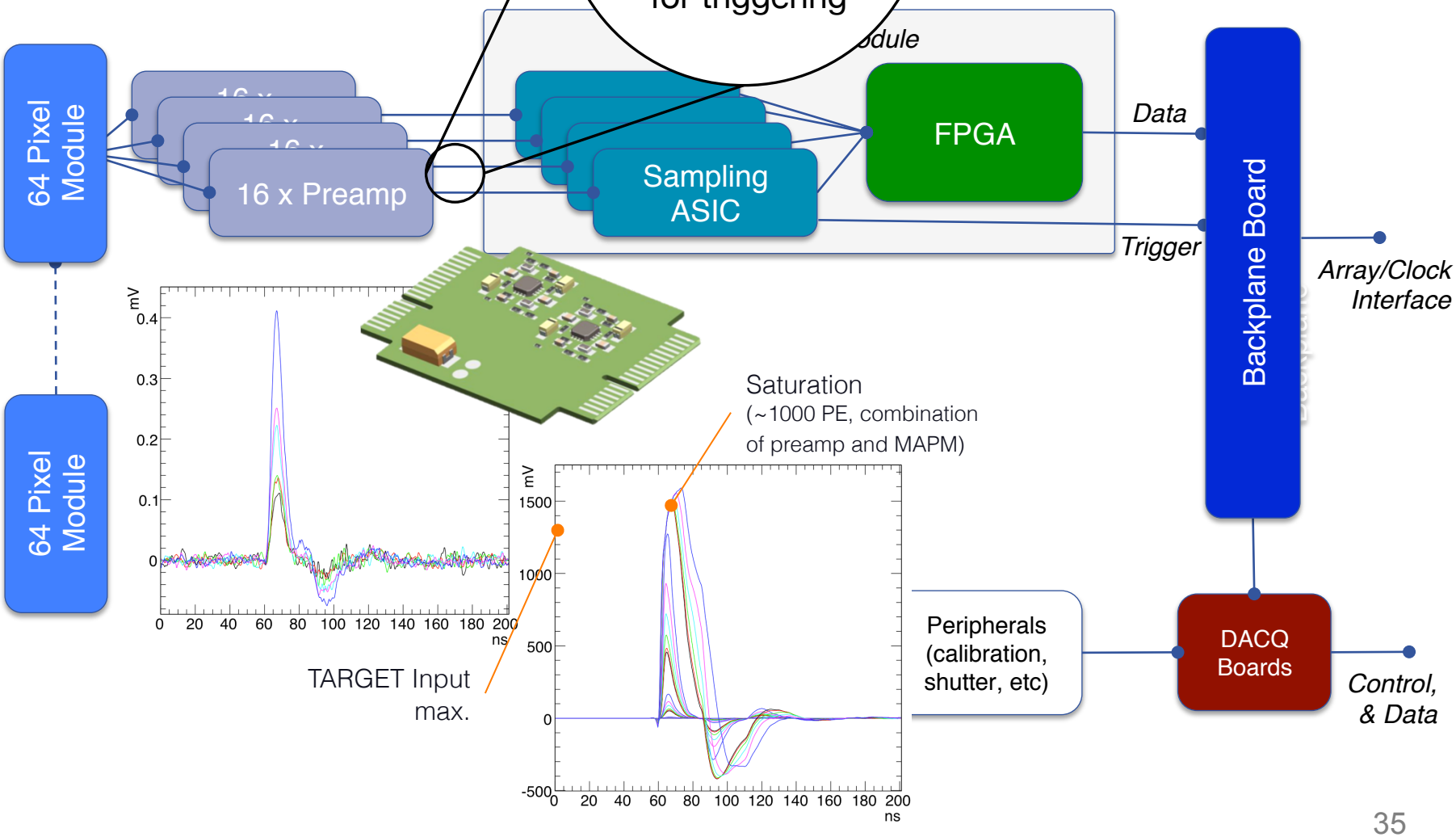
50% trigger prob. (Requirement is 100 pe)

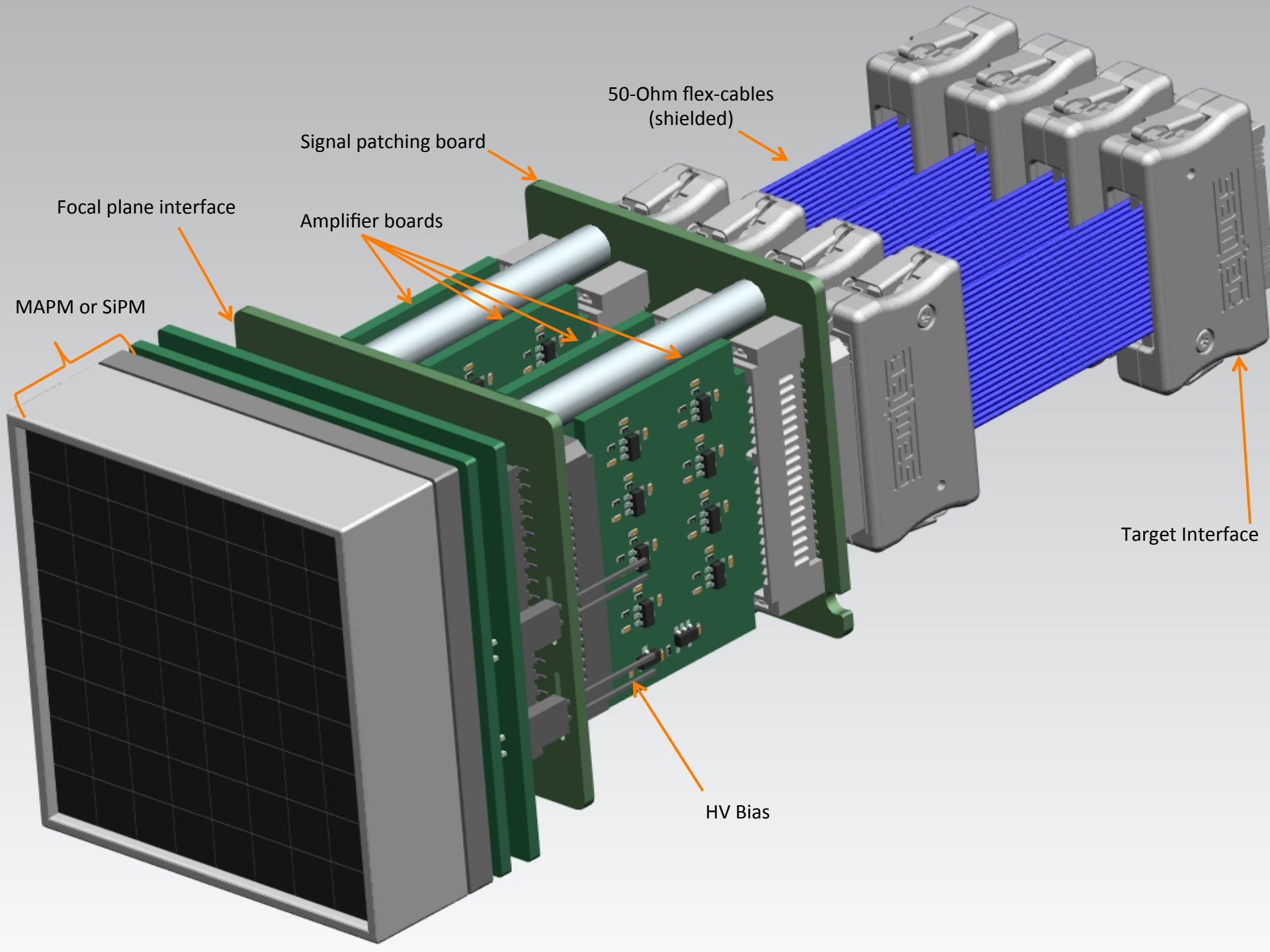


i.e. 0.34° trigger pixels

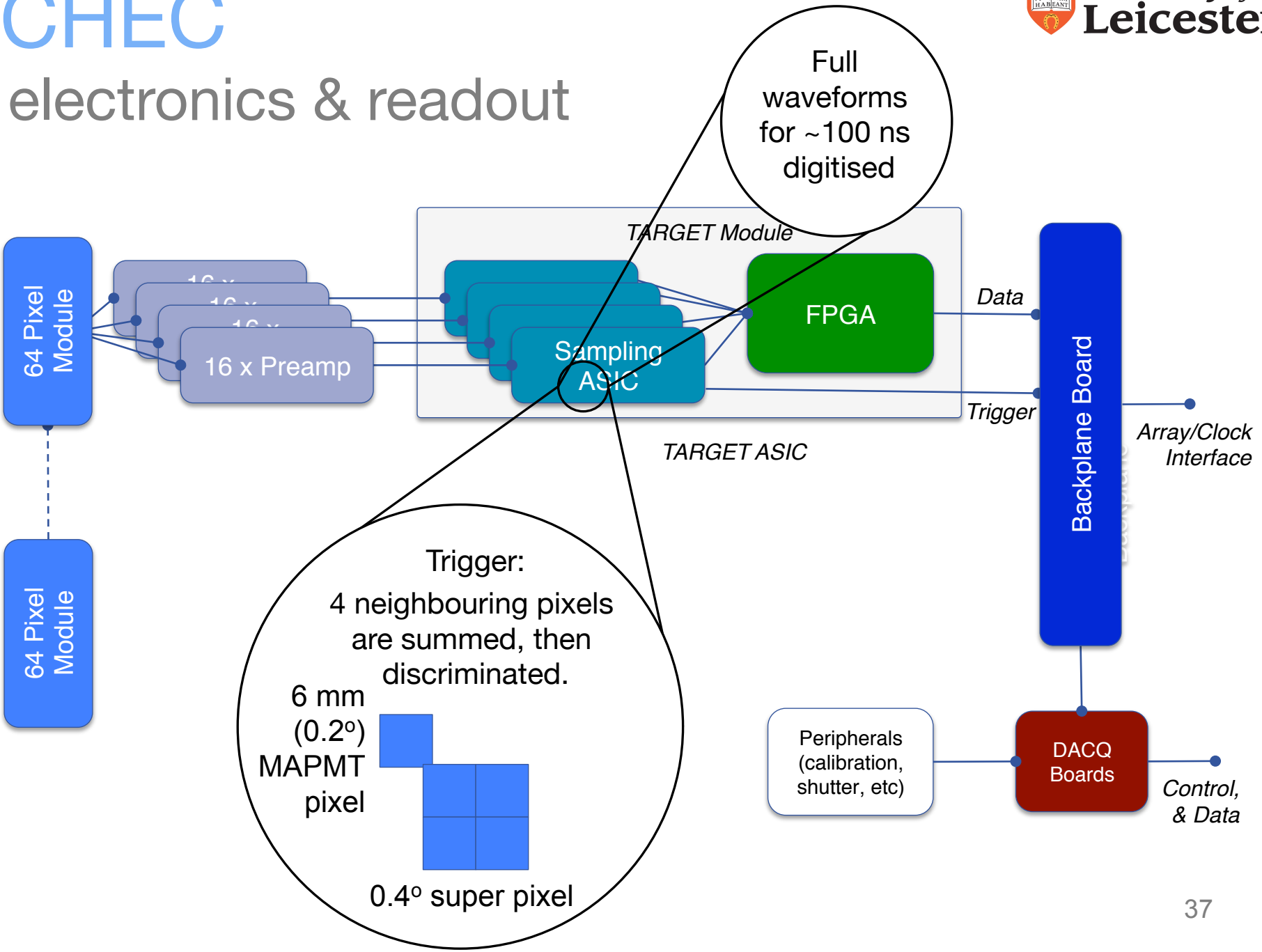
CHEC
electronics & read

Simulations show that for >TeV energies ~ 6 ns FWHM is optimal for triggering




50-Ohm flex-cables
(shielded)
Signal patching board
Focal plane interface
Amplifier boards
MAPM or SiPM
Target Interface
HV Bias

CHEC
electronics & readout

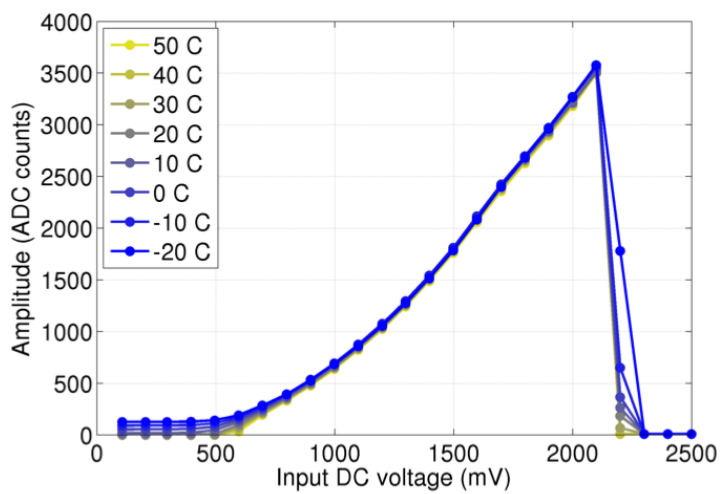


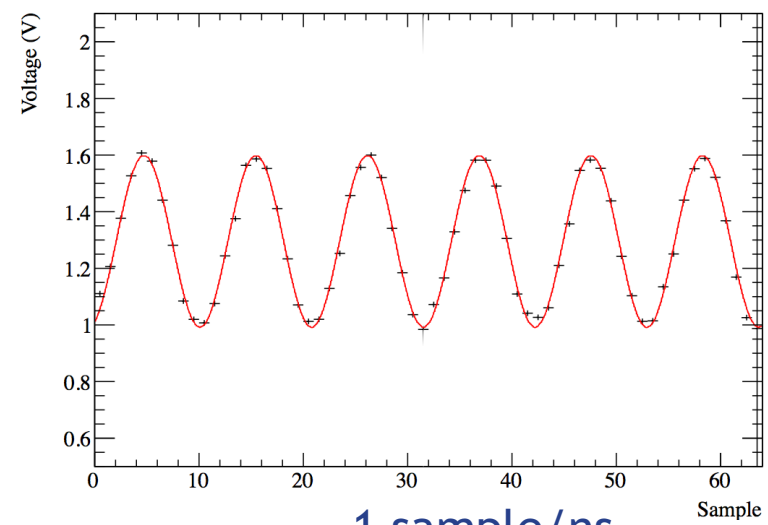
TARGET ASIC

University of Leicester

TARGET	1	5
Channels	16	16
Storage Cells per	4,096	**16,384**
Pre-amplifier	No	No
Single-ended or (Pseudo) Differential	SE	SE
Bandwidth (MHz)	150	**> 380**
Crosstalk at 3 dB Frequency	< 4%	**< 1%**
AC Saturation	Yes	**No**
Int/Ext Control Voltages	Ext	**Int**
Trigger	OR of 16	**4 Each Analog Sum of 4**
Wilkinson ADCs (Ch × Samples)	2 × 16	**16 × 32**
Dead Time for 10 Bit, 16 Ch, 48 Samples (μs)	48	**10**

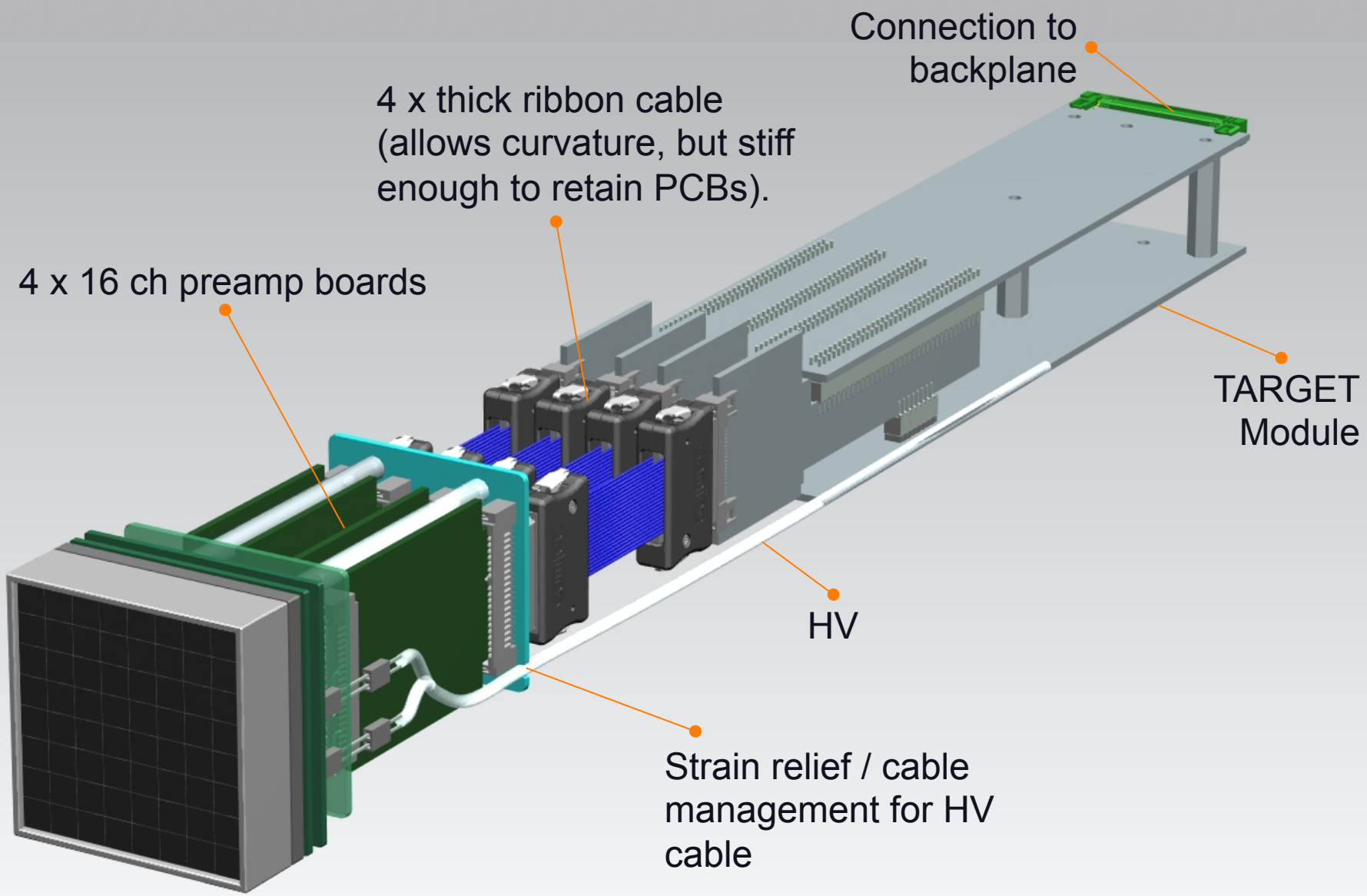
- Analog buffering
- Switched cap array
- Digitisation using Wilkinson ramp
- TARGET 5:
  - <0.6 mV noise or ENOB = 11
  - Sampling 0.5 – 1 GS/s
  - Analogue sum of 4



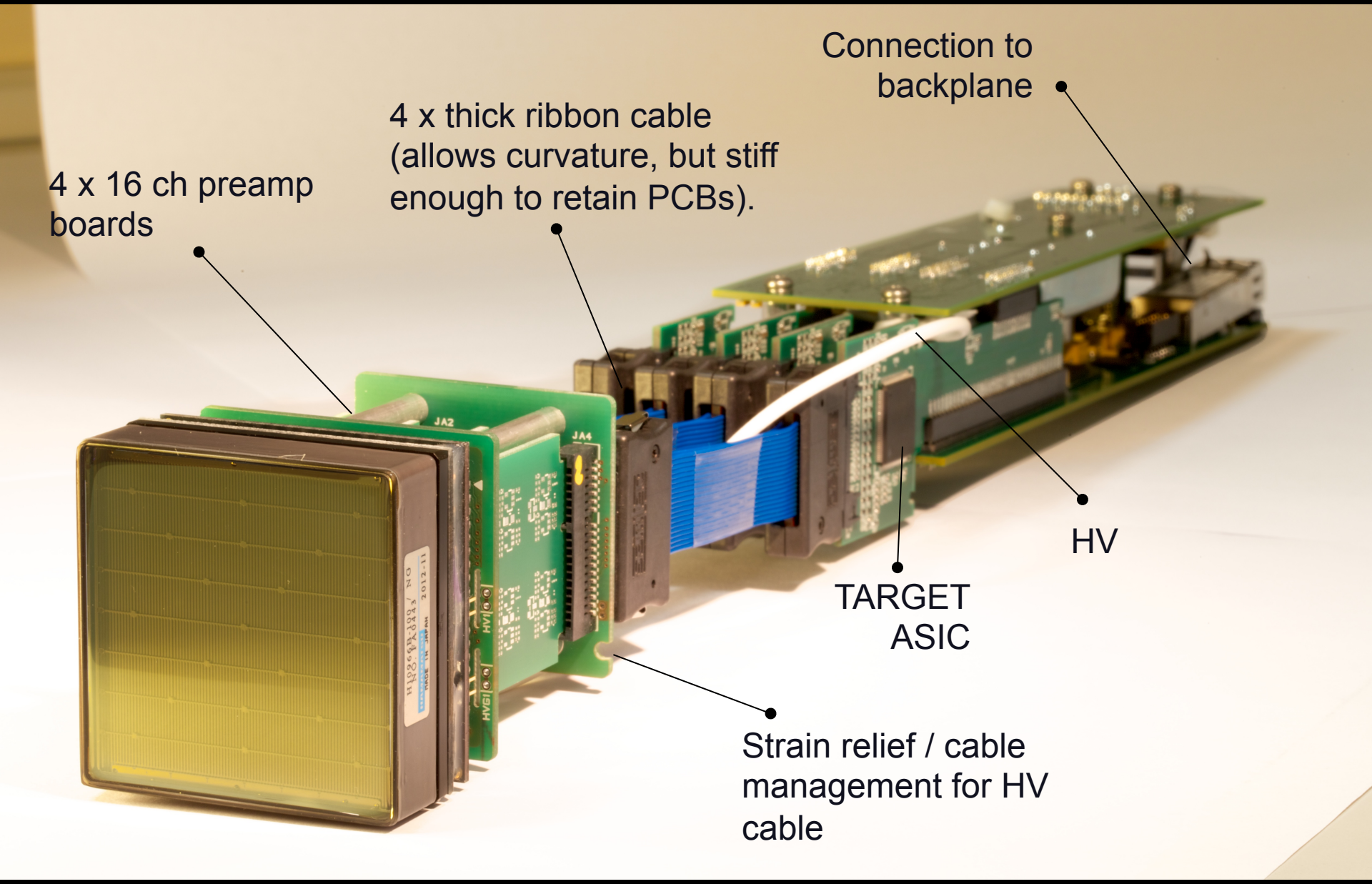


1 sample/ns

CHEC Module


Connection to backplane
4 x thick ribbon cable (allows curvature, but stiff enough to retain PCBs).
4 x 16 ch preamp boards
TARGET Module
HV
Strain relief / cable management for HV cable

CHEC Module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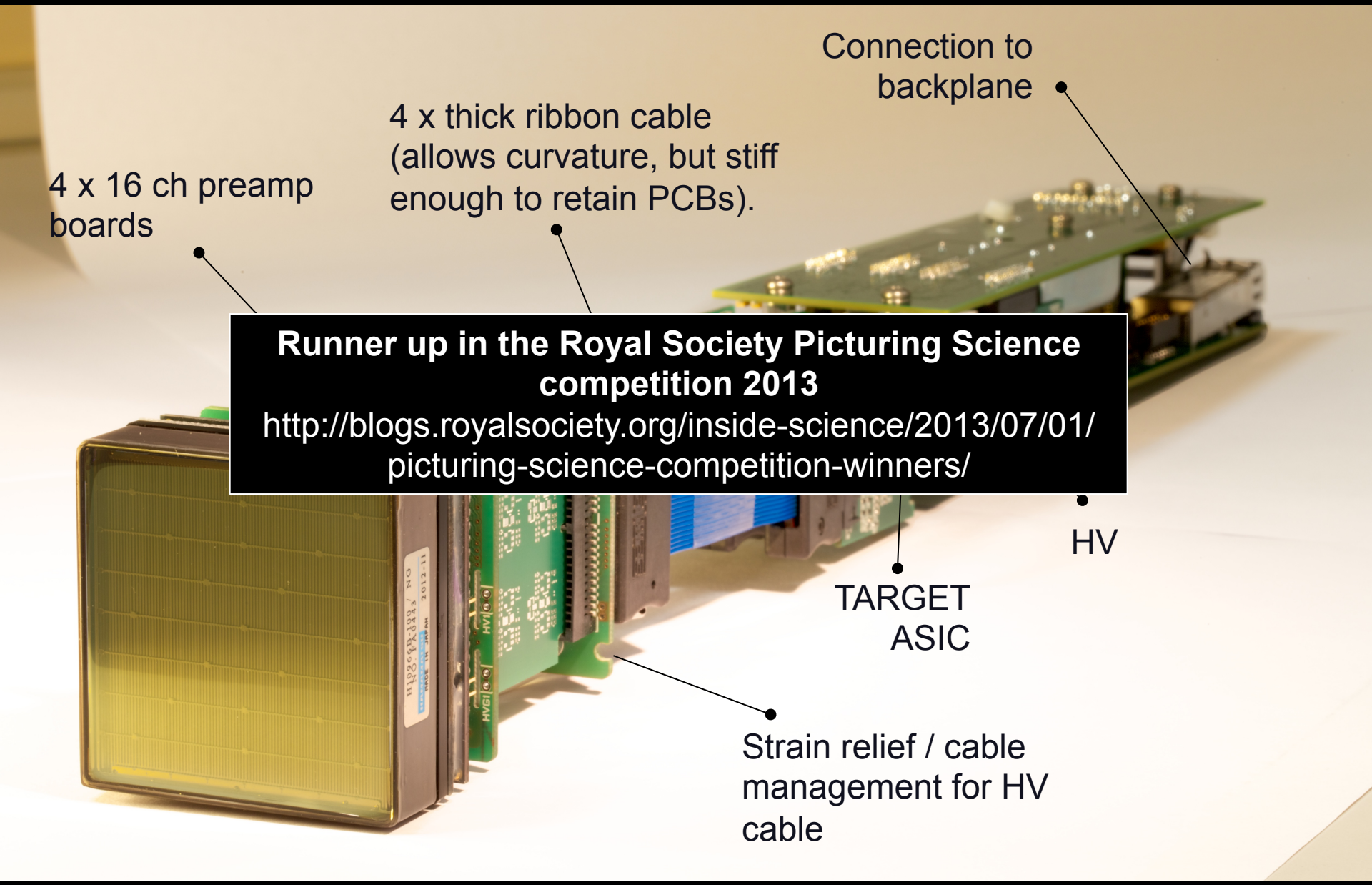
TARGET ASIC
Strain relief / cable management for HV cable

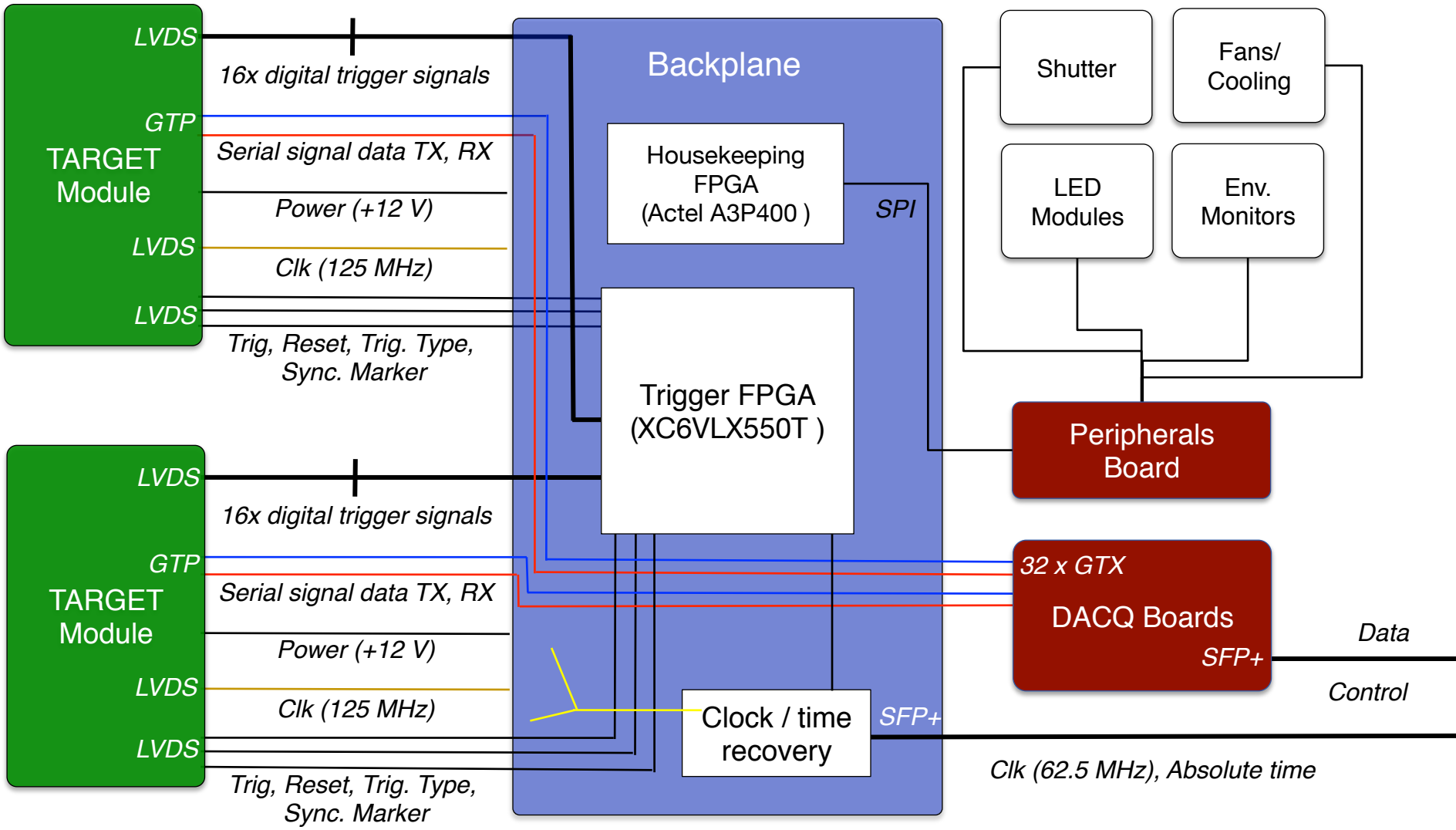
CHEC Module



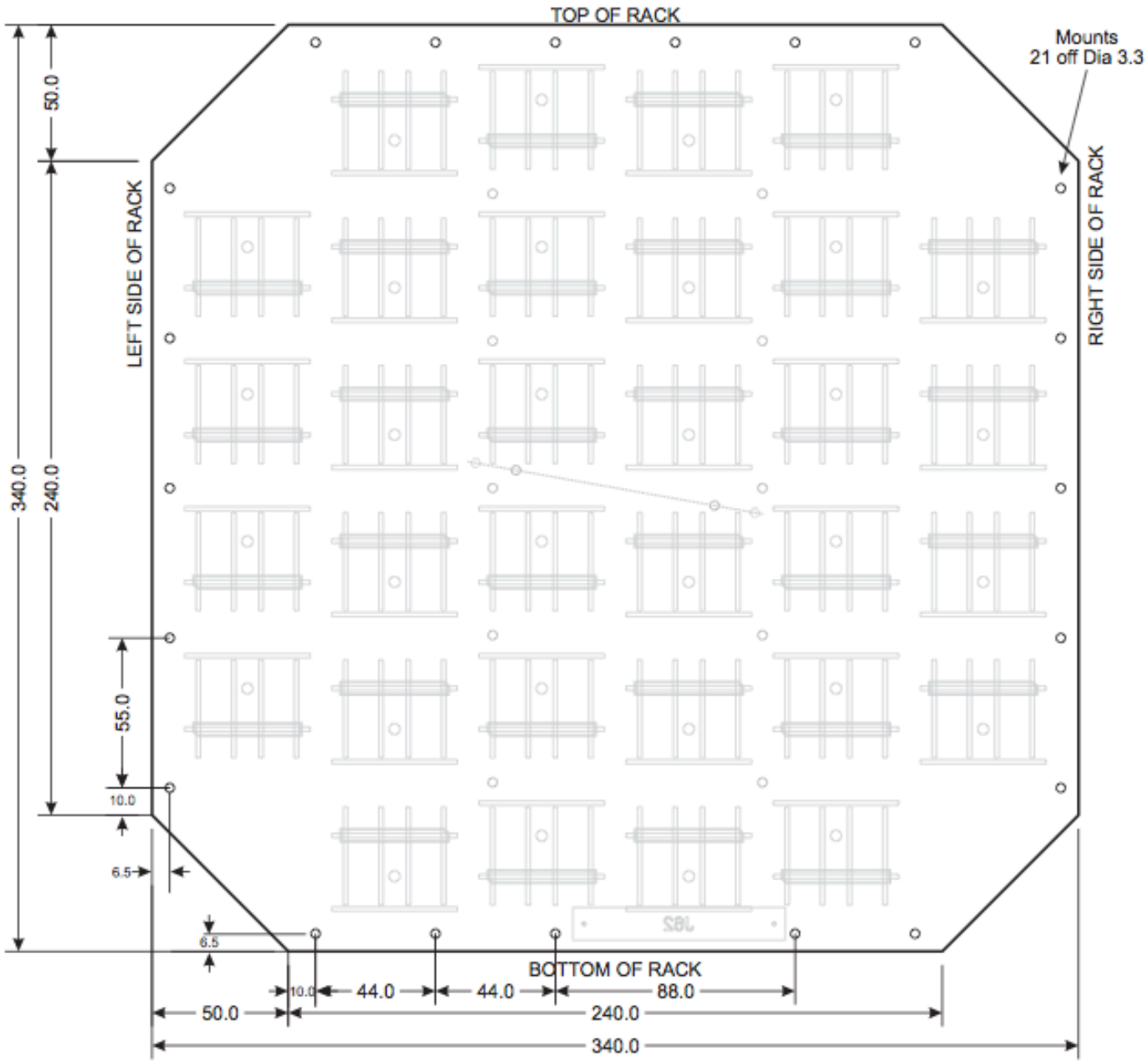
Runner up in the Royal Society Picturing Science competition 2013
http://blogs.royalsociety.org/inside-science/2013/07/01/picturing-science-competition-winners/

CHEC

back-end electronics

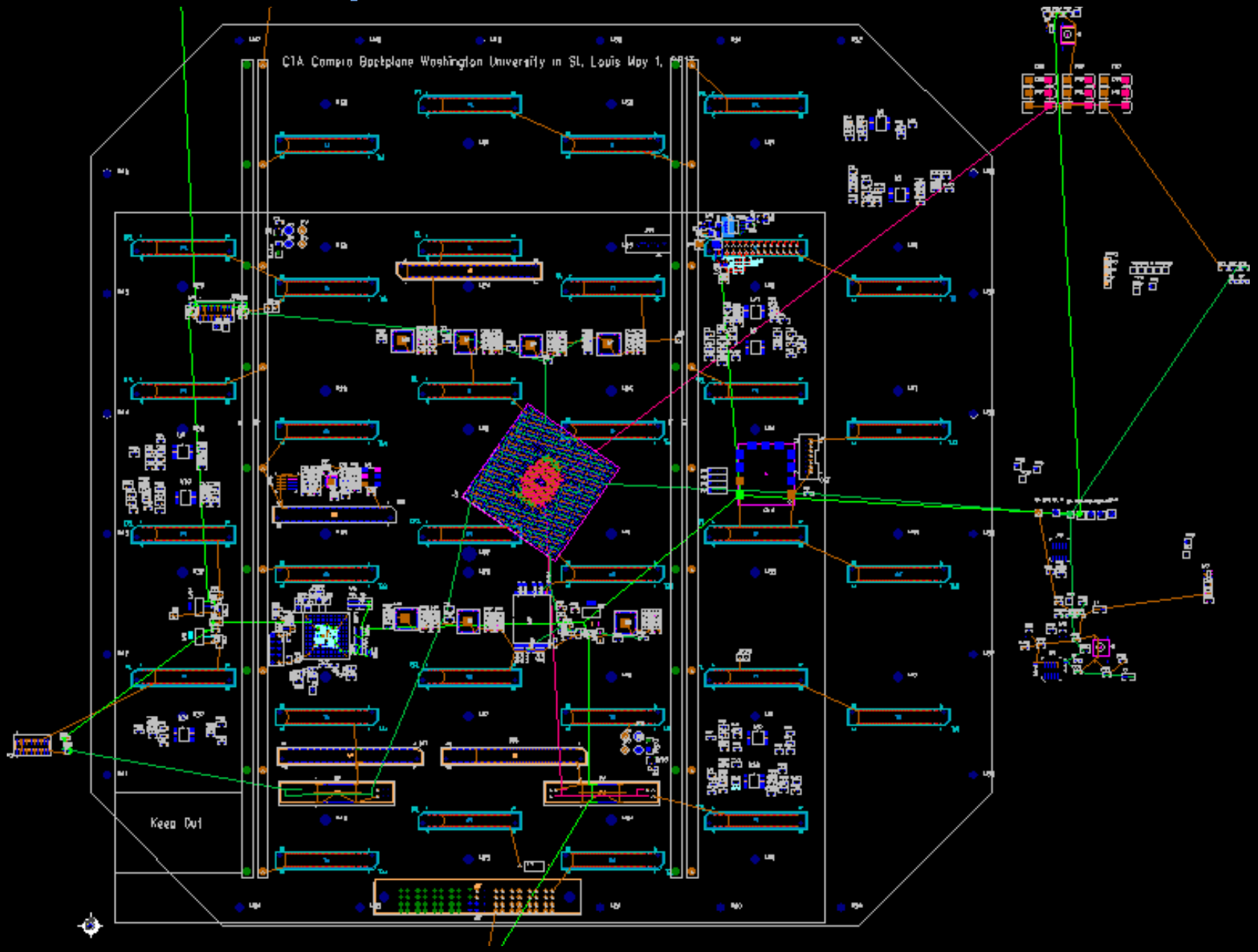


CHEC Backplane

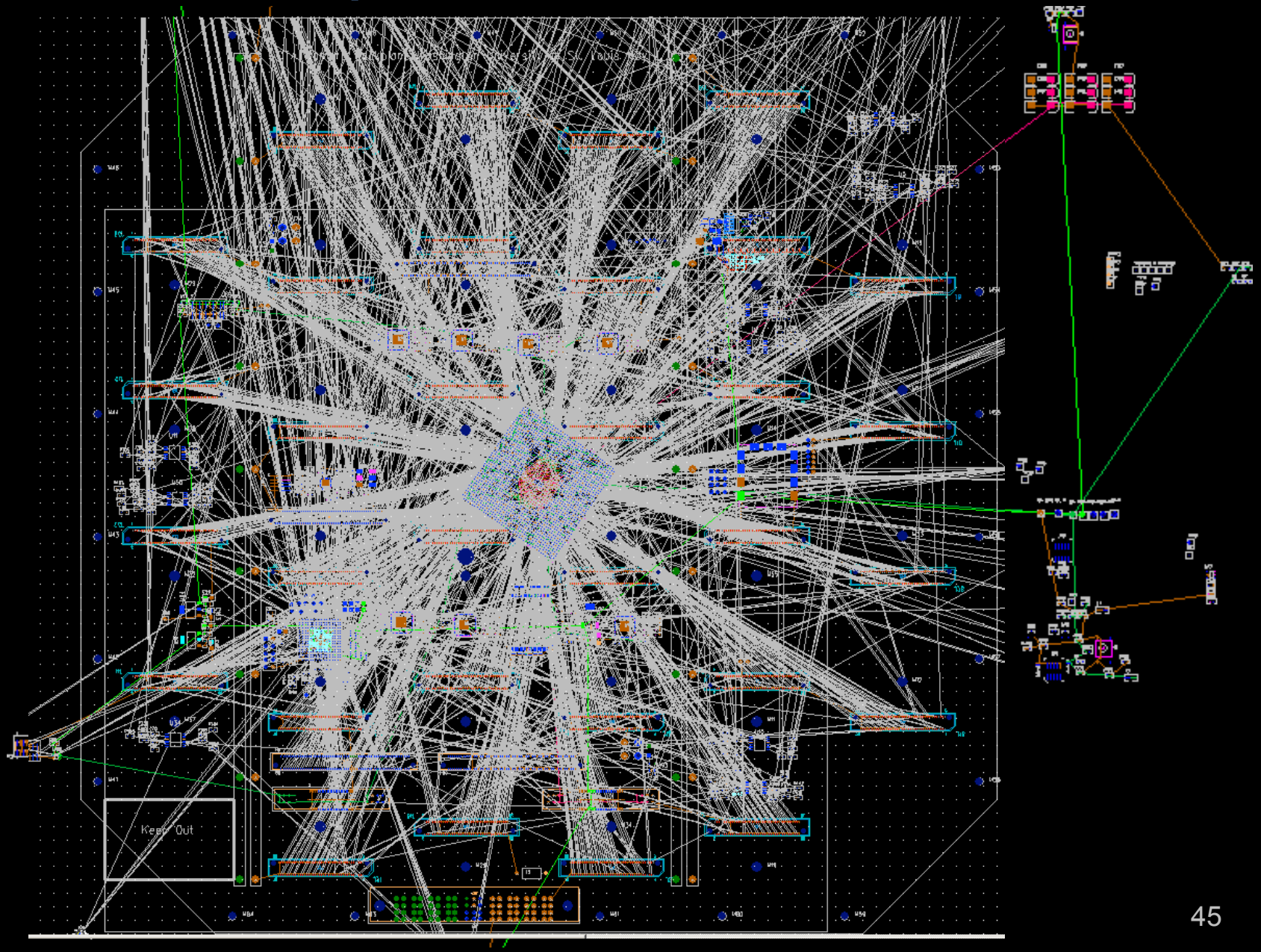


CHEC Backplane

University of Leicester



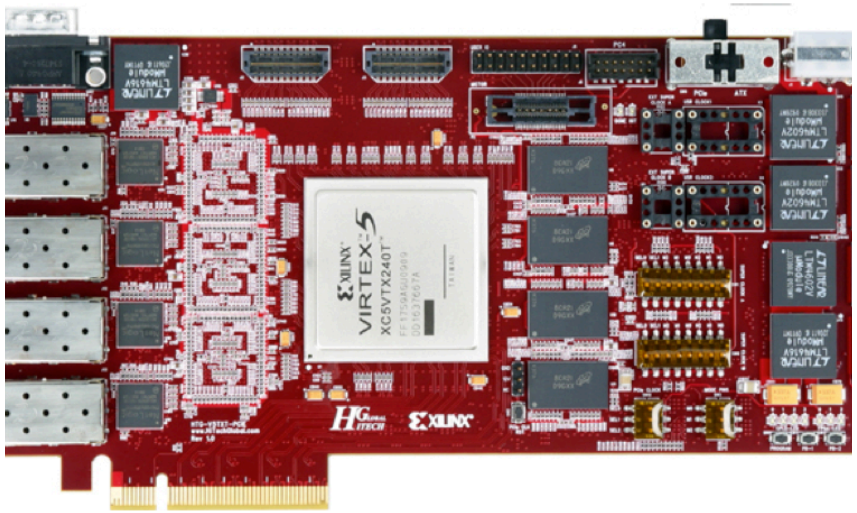
CHEC Backplane

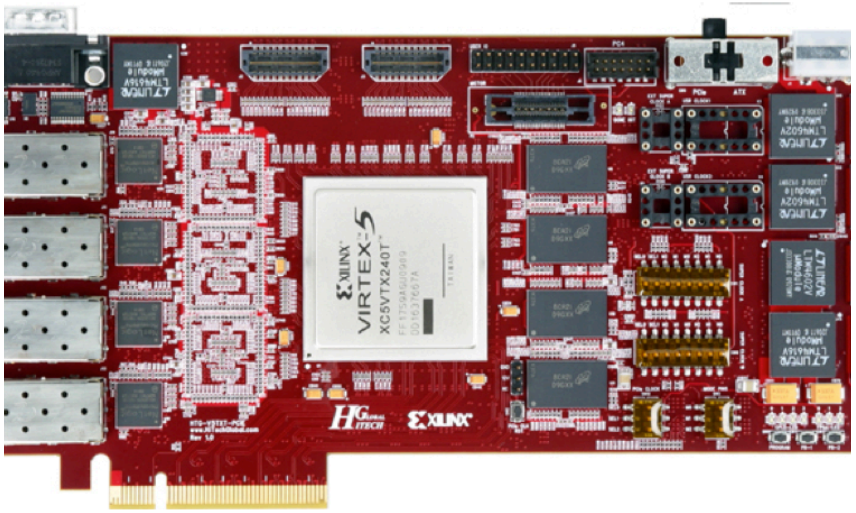


CHEC

DACQ boards

- Baseline plan:
  - Commercial boards
  - HTG-V5TXT-PCIE
  - Virtex-5 XC5VTX240T, access to 20 GTX transceivers on each board
- Long-term plan:
  - University of Amsterdam
  - SST-specific board

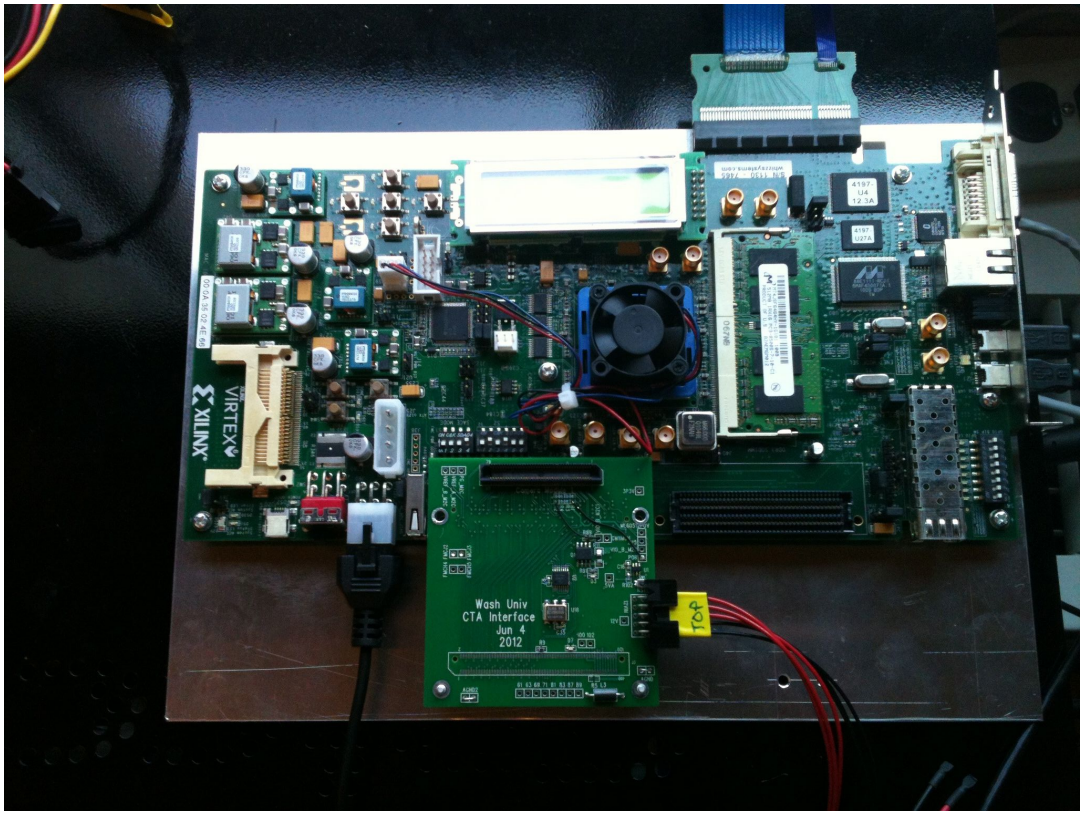




CHEC

back-end electronics demonstrator

- Demo backplane: Xilinx ML605_EvaluationKit
  - Accepts single Target Module
  - Allows data-transmission protocol to be developed
    - PGP
    - Aurora
    - UDP?
  - Trigger logic and time stamping tests



CHEC Calibration

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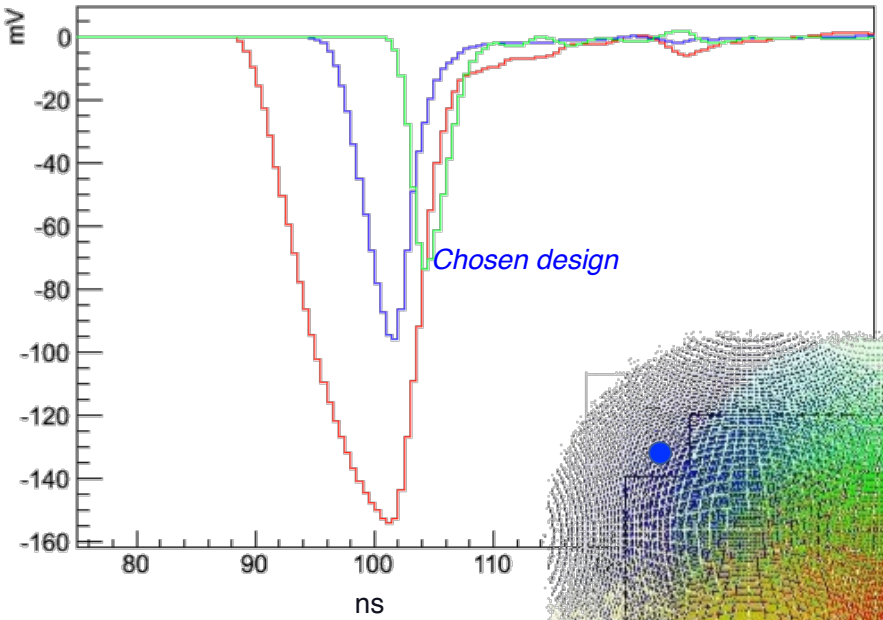
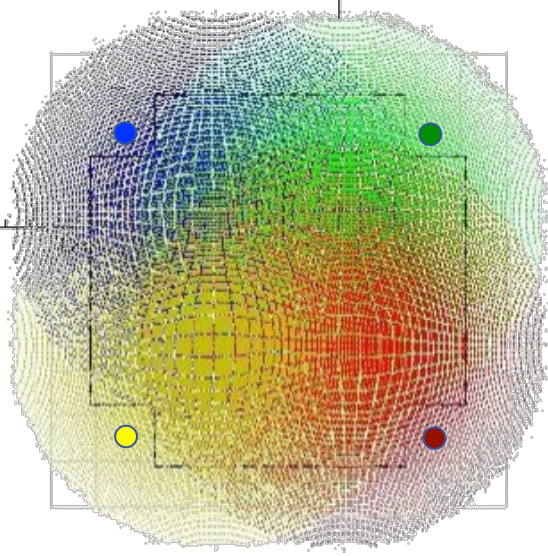
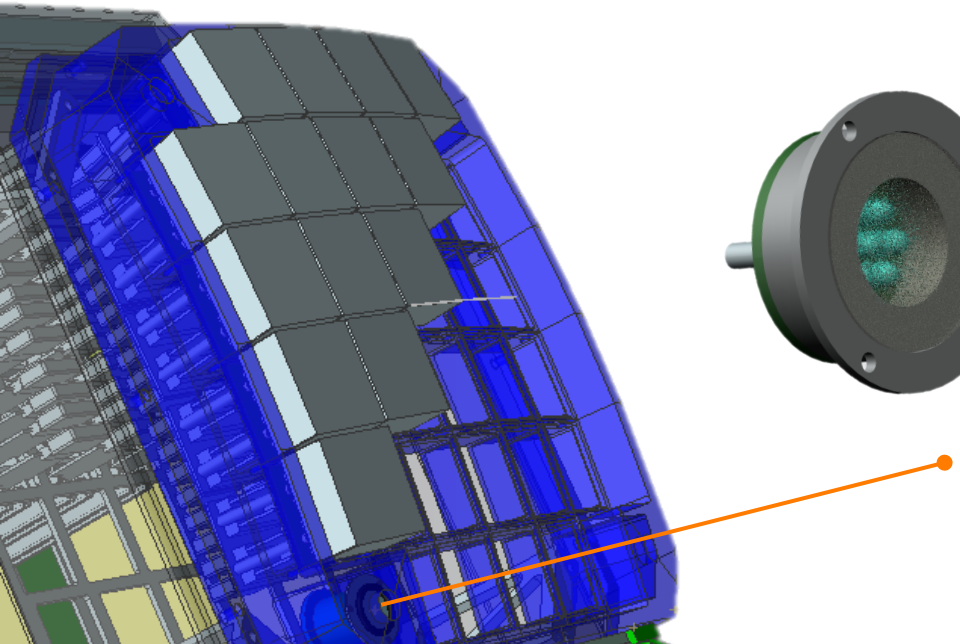
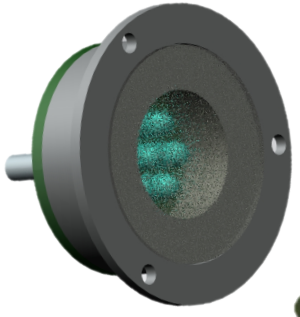
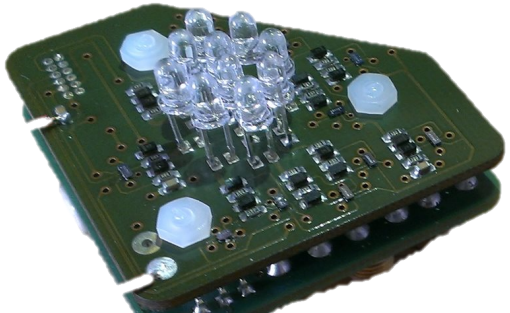
- Indirect (via 2M) off-axis illumination:
  - LED Modules in each corner of the camera
  - 4 ns FWHM pulses
  - Multiple LEDs cover the required dynamic range (0.1-1000 pe)





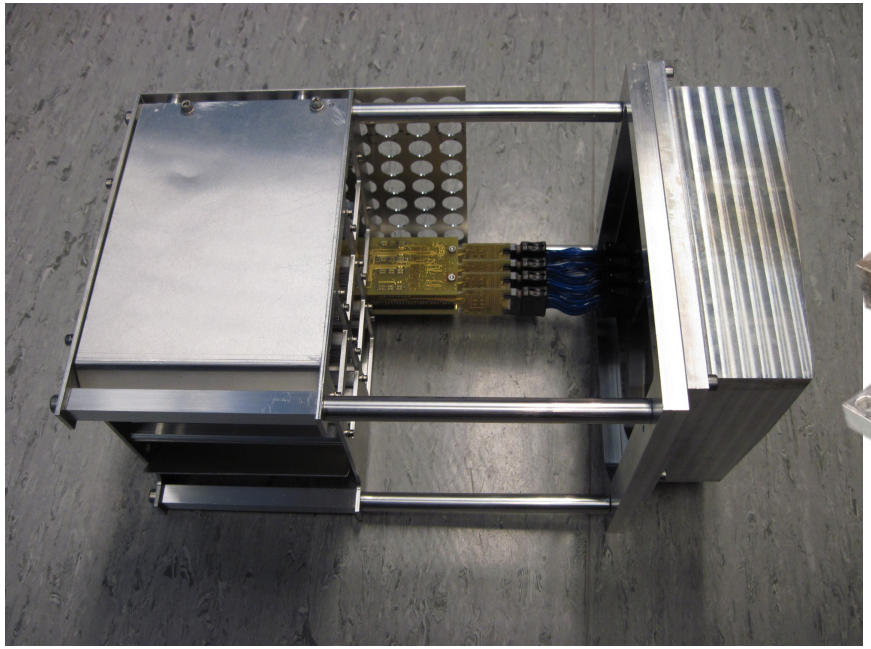


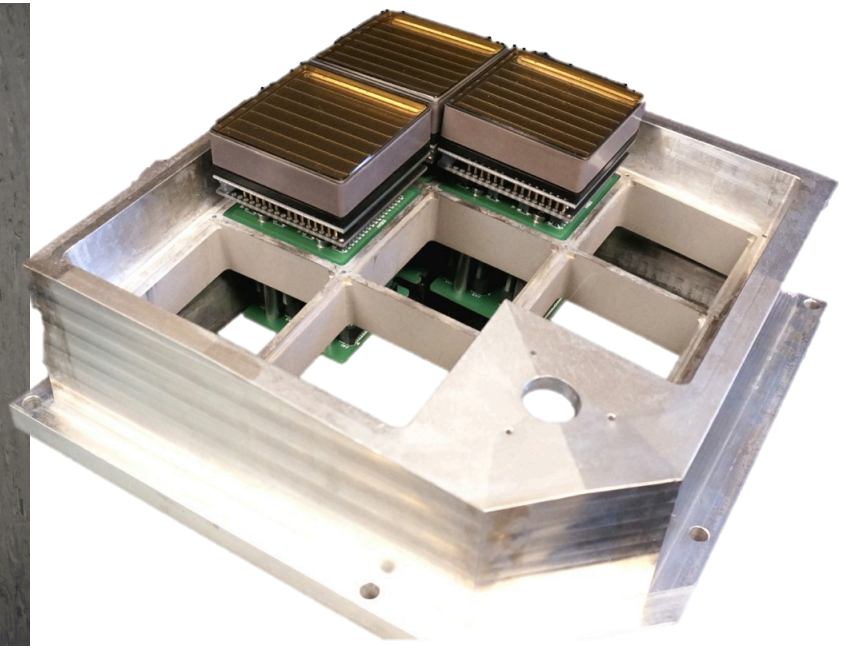


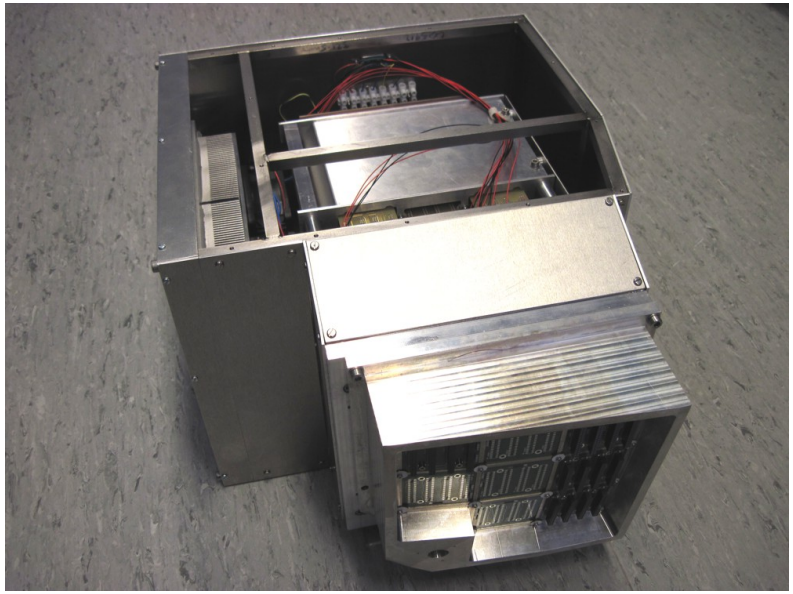


CHEC ¼ Demonstrator

University of Leicester



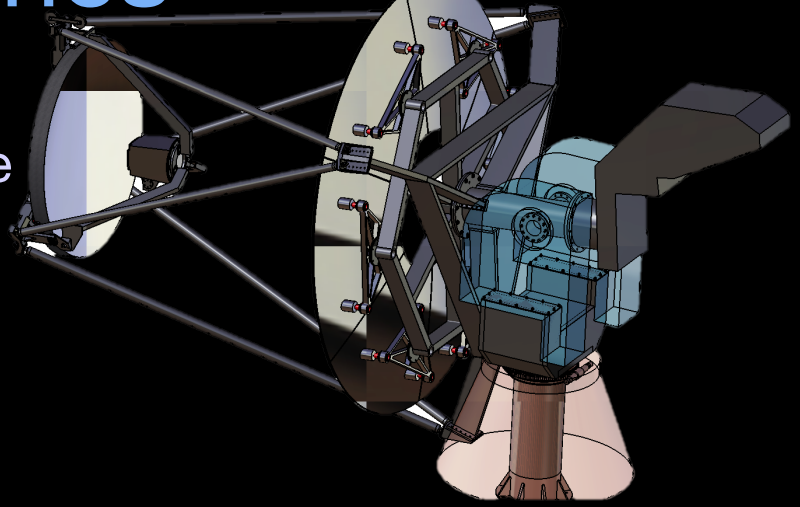


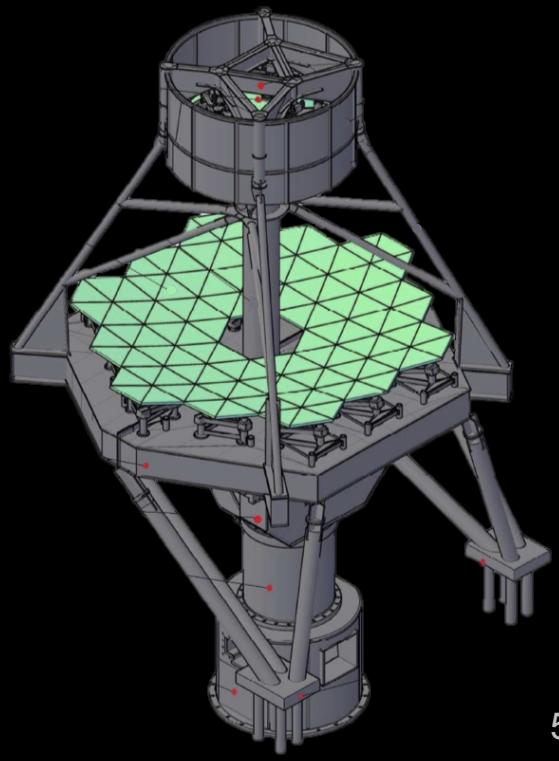


Dual Mirror Test Benches

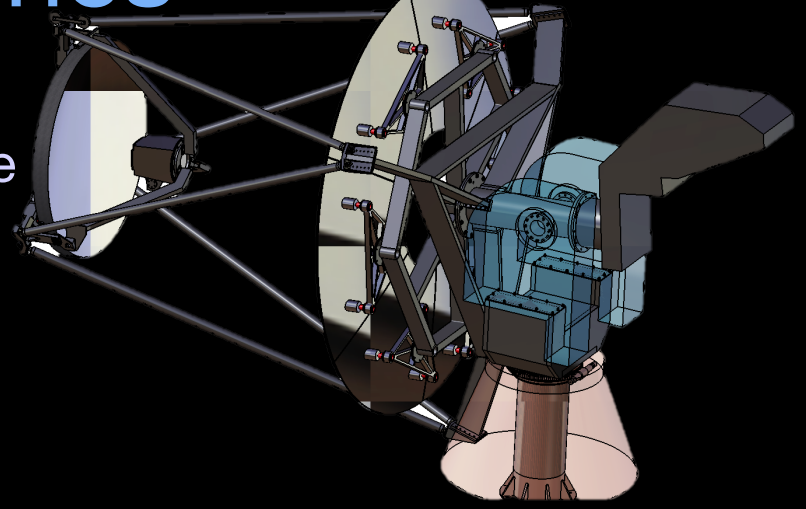
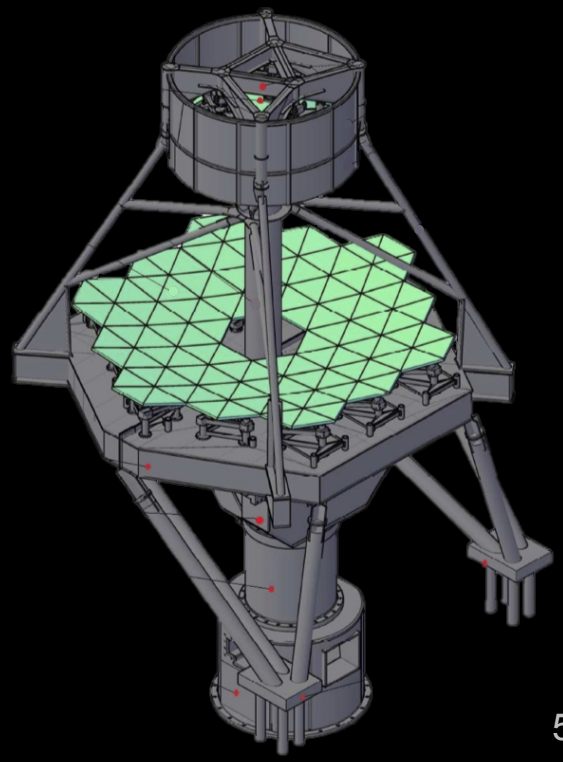
University of Leicester

- GATE
  - French development of UK structure design + mirror development
- ASTRI
  - INAF €8M project for SST
    - Structure, Mirrors and Camera
  - Prototype at Etna Observatory - 2014





Dual Mirror Test Benches

University of Leicester

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    - Structure, Mirrors and Camera
  - Prototype at Etna Observatory - 2014
- CTA Seed Array
  - ~6 SST-2M telescopes
  - Converged designs for telescope structures and cameras
  - The first CTA science from 2016!