Test Automation of 3D Integrated Systems

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Mentor Graphics Corporation
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Agenda

- Basic semiconductor test concepts
  - Scan test
  - Design-for-Test (DFT)
  - Built-In Self-Test (BIST)

- 3D-IC Testing
  - New challenges
  - Known-Good-Die (KGD)
  - Test access for stacked die
  - Testing die within 3D stack
  - Testing TSV connections between stacked die
Semiconductor Test – In a Nutshell

- Process to ensure fabricated IC works correctly
  - Tester applies stimulus to input and examines output data

- Test automation: input patterns and expected output data generated automatically
  - Need to maximize defect detection and minimize patterns
Field Returns vs Test Cost Correlation

All Test Technologies provide a trade-off between quality and cost

Key is to achieve the steepest possible curve

Field Returns (DPM)

Test Cost
Design-For-Test (DFT)

- Circuit modification and/or additions to make IC easier to test
  - Scan for ATPG
  - Built-In Self-Test (BIST): all testing done on chip

Reduced test time and hence cost
Scan Design

- **Internal scan** is a structured DFT technique that
  - Replaces sequential storage elements with scan cells
  - Stitches scan cells into a serial scan register (scan chain)
  - Makes sequential circuitry appear combinational

- **Structural test technique**
  - Directly tests circuit structure rather than higher-level function
  - Easier to automate
  - Enables standardized defect coverage metrics
Mux DFF Scan Cell

- Multiplexer selects data input:
  - D in normal mode
  - Scan_in (SI) scan mode

- Scan_enable (SE) selects mode of operation

- Increased propagation delay

- Adds 5-15% area overhead

- Standard approach today

Original Flip-Flop

\[ \begin{array}{c}
\text{D} \\
\text{CLK} \\
\end{array} \quad \begin{array}{c}
\text{Q} \\
\end{array} \]

Replaced by MUX-D Scan Cell

\[ \begin{array}{ccc}
\text{D} & \text{SI} & \text{SE} \\
\text{CLK} & \text{N}_2 & \text{MUX 1} \\
\end{array} \quad \begin{array}{c}
\text{DFF 1} \\
\text{DFF} \\
\text{scan\_out} \\
\end{array} \]
Scan Chains

- **Scan_Enable (SE):**
  - When active allows scan data to enter the registers.

- **Scan input port (SI):**
  - Data is loaded into scan cells.

- **Scan output port (SO):**
  - Data is read by shifting data out.
Typical ATPG Flow

ATPG: Automatic Test Pattern Generation
Stuck-At Fault Model

- Fault models are logic targets for defects.
- A fault is detected:
  - When a difference is observed between a “good” and “faulty” circuit.
- Most common fault model:
  - Most defects are detected with the stuck-at fault model.
  - A terminal of a gate is permanently stuck-at 0 or 1.
  - Also detects other defects:
    - Opens
    - Shorts
    - Bridging faults
    - Others...

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Good</th>
<th>A s.a.0</th>
<th>A s.a.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
Fault Model Progression

Schematic

Static Timing Analysis

Calibre®

Stuck-At Fault Model

Transition Fault Model

Bridging Fault Model

Small Delay Fault Model

User Defined Fault Model

Eldo®

Cell Layout

Cell-aware ATPG library characterization

ATPG Fault Simulation

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Boundary Scan – IEEE 1149.1 Standard

Scan cells placed on I/O support both external test of interconnect as well as internal test of die
Embedded Test IP - BIST

Megabits worth of high performance memories

Tens of millions of logic gates running at many different asynchronous frequencies

Dozens of multi-gigahertz Serdes I/O
Embedded IP Architecture

- At-speed embedded test, diagnostics and repair for memories
- At-speed embedded test and diagnostics for logic
- Hierarchical Access
- High precision embedded test and measurement of Serdes I/O
- IEEE 1149.1 standard test interface
Memory BIST – Basic Architecture

Tessent MemoryBIST Controller

- FSM
- SIGNAL GEN
- COMP

BIST_ON

FUNC ADDR

CTRL

SRAM

ADDRESS

DATA IN

DATA OUT

BIST DONE

BIST_GO

MEM_STAT

COMP

Memory Interface
Logic Test Solutions

Test Data

100100101
010101011
010011110

Result Data

100100101
010101011
010011110

Compressed Test Data

100100
010101

Compacted Test Data

010101
111011

Compressed Result Data

010101
111011

Decompressor

Compactor

Scan Chains

Scan Chains

ATPG

TESTKOMPRESS
ATPG Compression Technology

- Use logic to convert compressed tester stimulus to many short internal chains
- Cycles/time to load each pattern dramatically reduced
- 100X time & data compression enables higher test quality
- Patented X-masking ensures no loss in test coverage
Logic Test Solutions

Scan Chains

Test Data: 100100101 010101011 010011110

Result Data: 100100101 010101011 010011110

Compressed Test Data: 100100 010101

Compressed Result Data: 010101 111011

Decompressor

Compact

Signature Calculator

Random Pattern Generator

Pass/Fail

Start
Logic BIST Overview

- On-chip random pattern generator (PRPG) creates test patterns on the fly
- On-chip signature calculator (MISR) accumulates all response data into single pass/fail signature
- Uses same scan architecture as ATPG
- Eliminates the need for stored patterns
  - Not limited by tester memory or clock speed
- Perfect for test reuse and in-system test applications
  - Addresses mil-aero, medical and automotive POR test requirements
Logic BIST – Basic Architecture

Control unit sequences all activity

Pseudo-Random Pattern Generator

All flops placed into large number of relatively short scan chains

Multiple Input Signature Register compresses responses into a signature
Logic BIST – Test Sequence

1. PRPG SEED 1

2. LogicBIST control & timing

3. MISR SEED 1

1. PRPG

2. Scan chain

3. Scan chain

4. Scan chain

5. Scan chain

10,000 loads, applications & unloads

SIG: 10,000
3D-IC TEST
3D IC Test Challenges

- Known good die (KGD) requirement
- Known good interposer requirement
- Partial stack testing
- Memory to logic TSV testing
- Logic to logic TSV testing
- Die test in package
ENSURING
KNOWN GOOD DIE
Wafer vs Package Test – Before 3D

Only small percentage of packaged parts thrown away
Wafer vs Package Test – With 3D

Potentially larger percentage of more expensive packaged parts thrown away.
Stacking Approaches

**Wafer-to-wafer (W2W) Bonding**
- Works only with homogeneous die
- Very difficult to control individual stack yield

**Die-to-wafer (D2W) Bonding**
- Necessary for heterogeneous stacked die
- Stack yield controlled with KGD and partial stack testing
Known Good Die Requirement

Die Defect Coverage
\[ DC_D \]

Final Package Yield
\[ \Pi DC_{D_i} \]

For 10 Die Stack:

<table>
<thead>
<tr>
<th>DC_D</th>
<th>( \Pi DC_{D_i} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>90%</td>
<td>35%</td>
</tr>
<tr>
<td>95%</td>
<td>60%</td>
</tr>
<tr>
<td>99%</td>
<td>90%</td>
</tr>
<tr>
<td>99.9%</td>
<td>99%</td>
</tr>
</tbody>
</table>

Bare die
Low Cost

3D Stack
High Cost

Still 10 times more wasted packages and test time
Known Good Die Requirement

Need comprehensive wafer test coverage

High coverage of multiple fault models
- Stuck-at, TDF, N-Detect, Cell-Aware, ...

Contactless performance test
- Leakage, delay testing, ...

Contactless parameter measurement
- Jitter, sampling instant, BER, ...

At least basic coverage of common functions
- PLLs, ADC/DAC, filters, ...
High Logic Defect Coverage
Transistor Level (Cell-Aware) ATPG

Methodology for improving detection of defects internal to standard cells
— Layout defects mapped to transistor faults
— Spice simulation maps fault effects to UDFM model
  – UDFM is generalized truth-table based fault representation
— ATPG engine enhanced to target UDFM-based faults
Cell-Aware ATPG  
*Silicon Results - 32nm experiment*

The methodology has demonstrated an ability to target otherwise uncovered and hard-to-get-to defect sites

<table>
<thead>
<tr>
<th>Pattern Type</th>
<th>#fails</th>
<th>DPM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell-aware slow speed</td>
<td>98</td>
<td>218</td>
</tr>
<tr>
<td>Cell-aware at-speed</td>
<td>268</td>
<td>597</td>
</tr>
</tbody>
</table>

Results from 400k tested ICs

*Data source: AMD presentation at Mentor’s ITC Theater 2011*
KGD IO Test Requirements

Regular IO
- Structural, performance and leakage test of drivers and receivers

SerDes IO
- Accurate measurement of performance parameters (Jitter, duty cycle, slew rate, etc)

Pre-Bond TSV
- Structural and performance test of partial logic
Contactless Test of Regular IO
Boundary Scan Based Solutions

- Test for structural I/O defects using wrap test approach
  - Standard Bidi Bscan cell used to drive and capture data

- Measure/test IIL, IIH, and inter-pin leakage without contacting bond pads on any tester
  - IIH test procedure
    - Drive pads to logic 1
    - Disable drivers – leakage current affects $V_{PAD}$
    - Capture pad logic values precise time later

![Diagram of Bidi Bscan cell and bond pad]](image-url)
Contactless Test of Regular IO

- Propagation delay measurement using Bscan
- BIST provides high-speed Bscan control signals
- Delay-difference measurement eliminates signal propagation variations and noise
- Rise and fall delay measurement with resolution adjustable from nanoseconds to picoseconds
Contactless Test of SerDes IO
SerDes BIST

- Accurate picosecond measurements of critical parameters
  - Jitter (Random, Total)
  - Jitter Tolerance
  - Rise/fall time, Slew rate

- RTL-based, vendor independent BIST

- No changes to physical IP under test
Contactless Test of SerDes IO
SerDes BIST

Undersampling-Based Approach

- Samples continuously, but only analyzes transitions
- Measures jitter and phase delays relative to median edge positions
- On-chip capture of histogram or RMS value of HF or LF jitter
Contactless Test of Pre-Bond TSVs

- All techniques described for regular IOs can be applied to pre-bond TSVs
  - Boundary Scan based solutions
  - IO BIST

- Extra load may be problematic due to lack of IO driver
  - Fuse can be used to eliminate load after test
TEST ACCESS FOR STACKED DIE
Generic 3D Package Components

- DRAM Die
- Wide I/O TSV Bus
- Multiple SoCs (with DFT)
- TSV Interconnect
- I/O to outside
Test Access Within Stack

- Dedicated TSVs used for test signals between die
- Control hardware needed to route test data up and down stack
- Standard architecture necessary to support heterogeneous die from multiple vendors.
  — IEEE P1838 under development
Mentor 3D Test Access

- Uses cascaded TAPs
  - Each TAP can be instructed to enable the next higher TAP
- Default is bottom TAP only in path
- Standard structure for die independent of position
- Die can work directly if packaged as a stand-alone device
TESTING DIE WITHIN 3D STACK
Die Test In-Package

- BIST best suited for re-test of die within stack
  - ATPG patterns can also be used
- Dies can be tested in parallel to minimize test time
- Screens for any new defects due to the packaging process
In-Package ATPG Application

- Options
  - Die-level ATPG patterns generated at package level
    - Full package netlist is used
    - Non-targeted die are grayboxed
  - Die-level ATPG patterns retargeted from wafer level
    - Patterns resequenced in accordance to active bypass stages
STACKED MEMORY TEST
Stacked Memory Test
BIST Approach

- External Memory BIST added to logic die
  - Provides full-speed testing of memory die and bus
  - Bus-only test algorithms can optionally be used
- Post-silicon programmability supports changes in memory die
Stacked Memory Test
BIST Approach

- All BIST transactions performed through functional PHY interface
  - Interface handles all signal synchronization
  - Interface also handles mux/demuxing for DDRs

- BIST supports all forms of DRAM access
  - Bursting, Refresh, etc

- BIST highly programmable
  - Address range and read/write operations for supporting different memories
  - Algorithms for different quality and test cost needs
    E.g. Interconnect only coverage

- Supports bussed memories
Wide IO DRAM Example

Each channel accessed separately

Channel

0 1 2 3

Rank

0 1 2 3

Stacked chip 1
Stacked chip 2 (optional)
Stacked chip 3 (optional)
Stacked chip 4 (optional)

Base chip
Wide IO DRAM Example Implementation
4 shared buses, 4 DRAMs behind each shared bus, 128-bit bus

Each Rank corresponds to a BIST step

Output data 128 bits/shared bus
Input data 128 bits/shared bus
Address and control separate for each shared bus

Shared bus modules (4 instances)
Stacked Memory Test
Boundary Scan Approach

- Interconnect test performed using boundary scan
- JEDEC WideIO standard defines bscan chain for DRAM

Advantages
- Does not require functional DRAM core for test and diagnosis

Disadvantages
- Low speed test might not be sufficient to detect/diagnose parasitic effects
- Does not support memory re-test
STACKED LOGIC TEST
Logic Die to Logic Die Interconnect Test
Various Approaches

- Traditional Boundary scan
  - Boundary scan cell placed at each die TSV and IO
  - Interconnect test patterns produced to find shorts or opens
  - Test operation based on standard boundary scan board test approach
  - Limitation: does not support at-speed test of TSV connections

- Pulse-Vanishing

- Hierarchical ATPG Approach
Pulse-Vanishing Approach
Targeted Faults in an Interposer

(1) **Parametric Open Fault** in an interposer wire
(2) **Parametric Bridging Fault** between two interposer wires

Micro-bump

Die #1

Die #2

Die #3

Die #4

Interposer

C4 bumps for connecting to package substrate
Boundary-Scan Based Architecture

The proposed test methods can be built on top of the IEEE-1149.1

Diagram:
- Die 1 (Master)
- Die 2 (Slave)
- Interposer Wires
- PV Test Wrapper
- BIST controller
- Tester
- {TCLK, Start_BIST}
- {TCLK, TRST, TMS}
- {TDI, TDO}
- Driver and Receiver symbols

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Concept of Pulse-Vanishing Test

A two-pulse signal (shared by all IWs)

Target clock cycle time (e.g., 1ns)

Local controller

Driver

Interposer Wire (IW) under test

Receiver

TM

0

1

D

Q

FF

R

1ns

('0' initially)

A

B

WO

('1' initially)

('0' initially)

Threshold

Functional input

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When There is a **Delay Fault**…

A two-pulse signal (shared by all IWs)
Logic-to-Logic TSV Interconnect Test
Hierarchical ATPG Approach

- Approach based on TSVs between scan-isolated cores
- Hierarchical ATPG tests signals between cores
- Cores on neighboring die conceptually the same
Logic TSV Test Pattern Generation

- TSV test patterns applied using scan chains in two or more die
- ATPG engine generates patterns using full package netlist
  - Non-targeted die and/or cores are grayboxed
- Only ATPG is supported
  - BIST and Compression can not easily be extended across multiple die
  - Less critical as TSV test set should be relatively small
Summary

- 3D-ICs introduce new test challenges and requirements

- Critical test solution components include
  - Known-Good-die test
  - Standardized TSV-based test access to die in stack
  - Programmable BIST for stacked memory die
  - Scan based testing of logic-to-logic TSV connections