University of Twente

InGrid: the integration of a grid onto a pixel anode by means of Wafer Post Processing technology

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Victor M. Blanco Carballo

University of Twente
The Netherlands

Overview

- Our wafer post processing requirements
- Concept and materials requirements
- Fabrication process
- Advanced processing
- Conclusions

Wafer post processing

- Use microelectronics to add functionalities
- Chip still functional after process

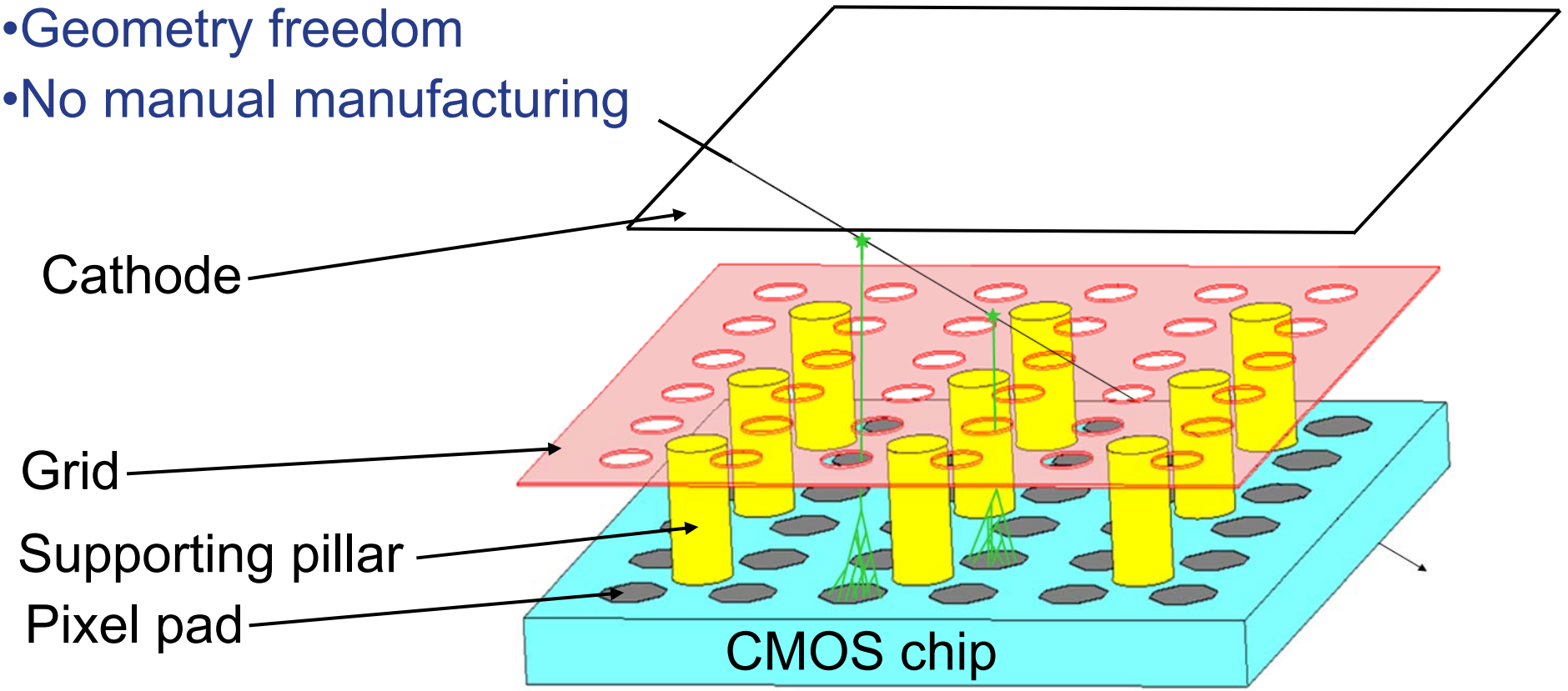
  -Temperature budget

  -Plasma damage

  -Stress
- Wafer level and chip level post-processing
- Suitable for Medipix, Timepix, Gosssipo, PSI-46…(general purpose process)

Integrated Micromegas

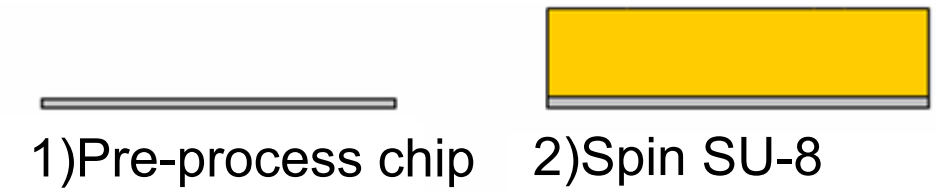
- Use the chip as electronics
- Perfect alignment holes to pixels
- No dead areas
- Geometry freedom
- No manual manufacturing



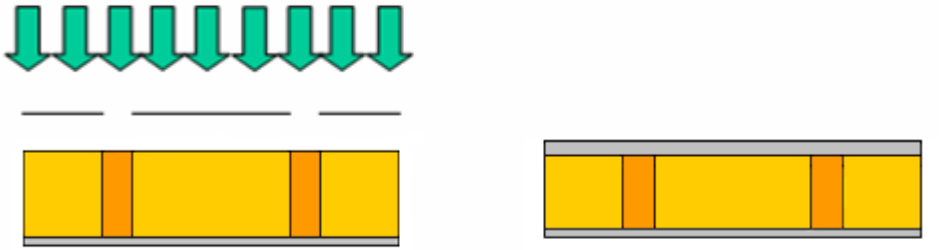
Materials for the structures

- SU-8 negative photoresist for insulating pillars
  - Easy to define structures by lithography
  - Low temperature process (below 95 °C)
  - Suitable thickness range (2µm to 1mm)
  - Insulating as Kapton foil (3MV/cm)
  - Some radiation hardness data available
- Aluminum for conductive grid
  - Commonly used in microelectronics
  - Easy to deposit
  - Easy to pattern
  - Low residual stress

InGrid: Integrated Grid

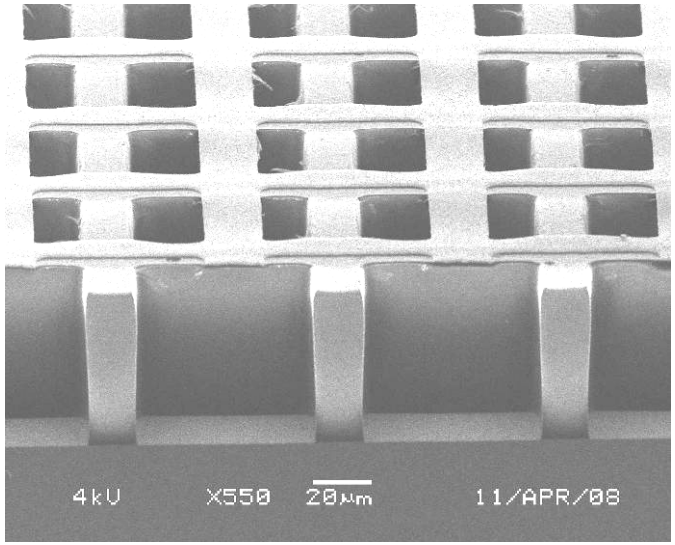


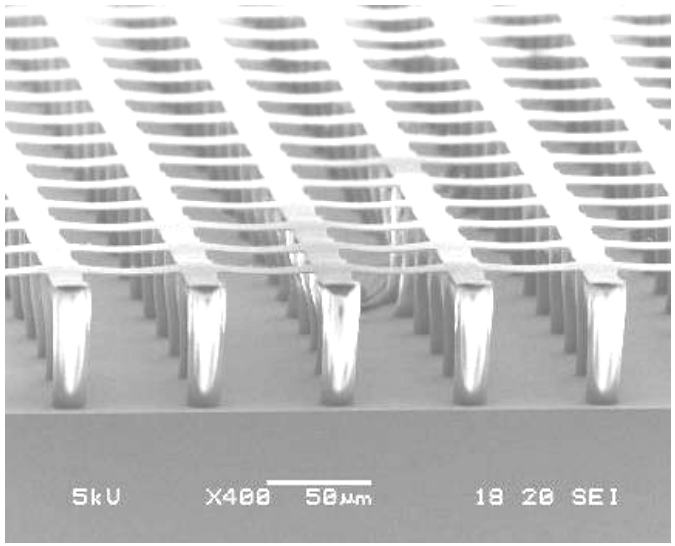
1)Pre-process chip 2)Spin SU-8



3)UV exposure 4)Deposit metal

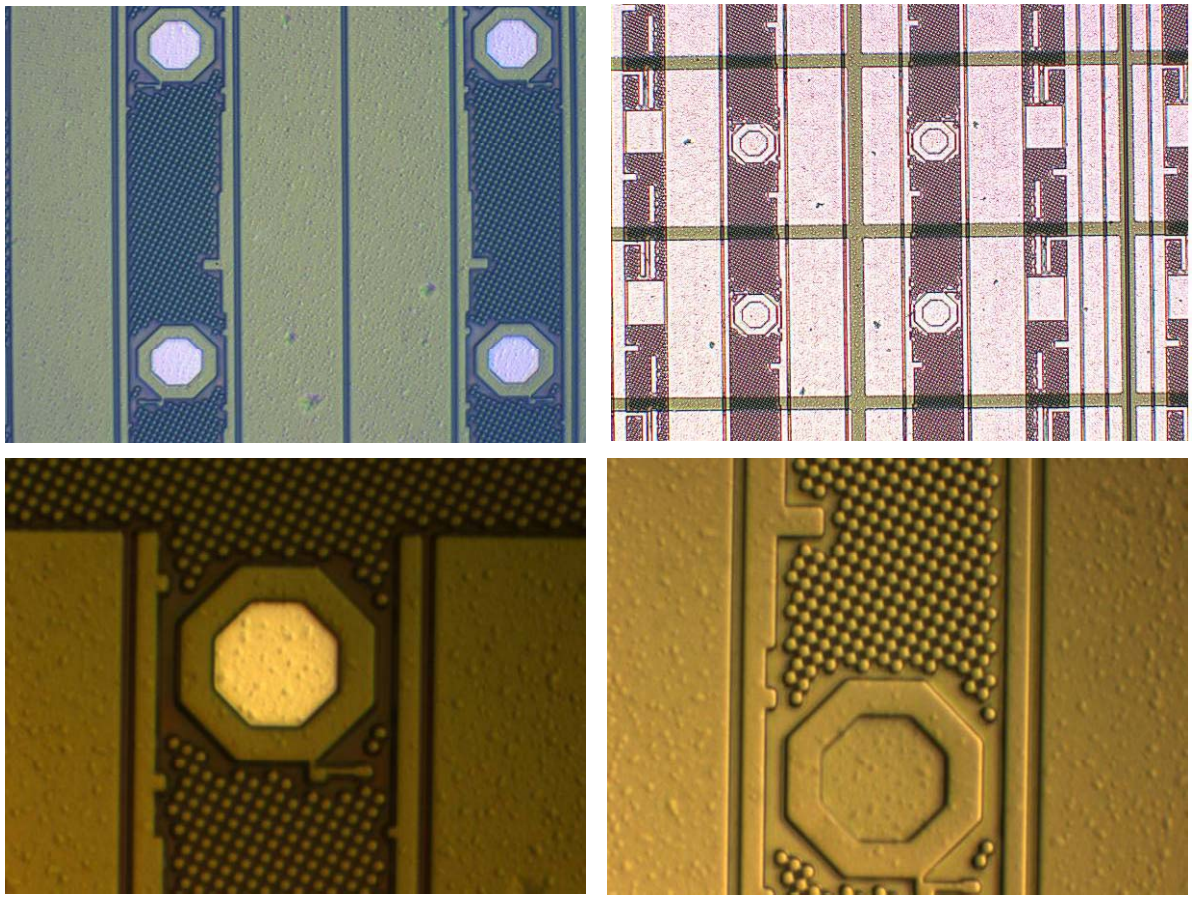
5)Pattern metal 6)Develop resist





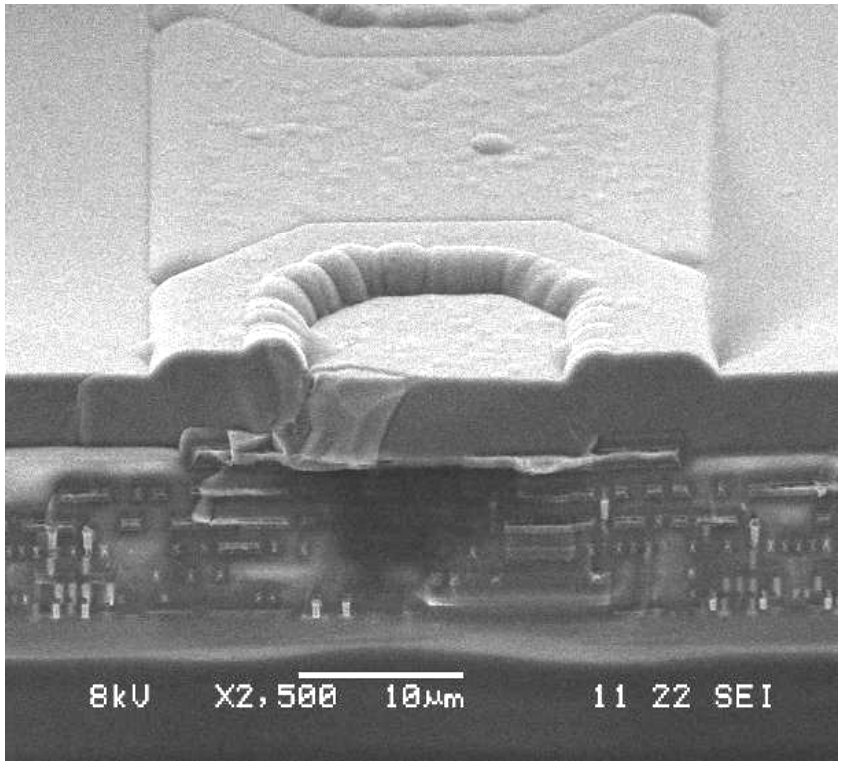
1) Pixel enlargement

- Increase sensitive area for better charge collection
- Pixel enlargement done by lift-off

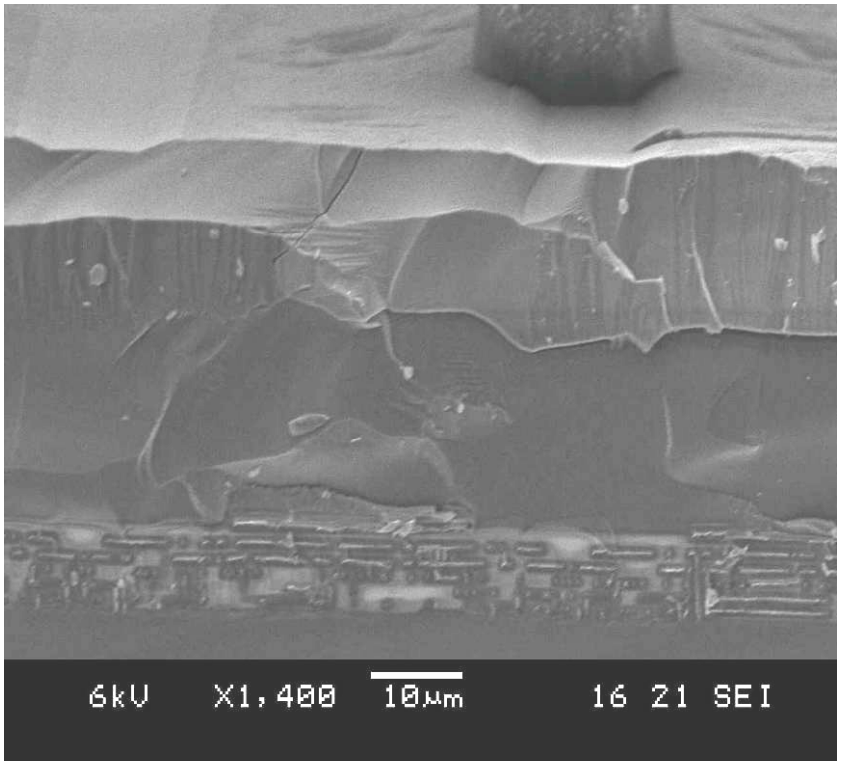


2) a-Si deposition (Neuchatel)

3µm a-Si



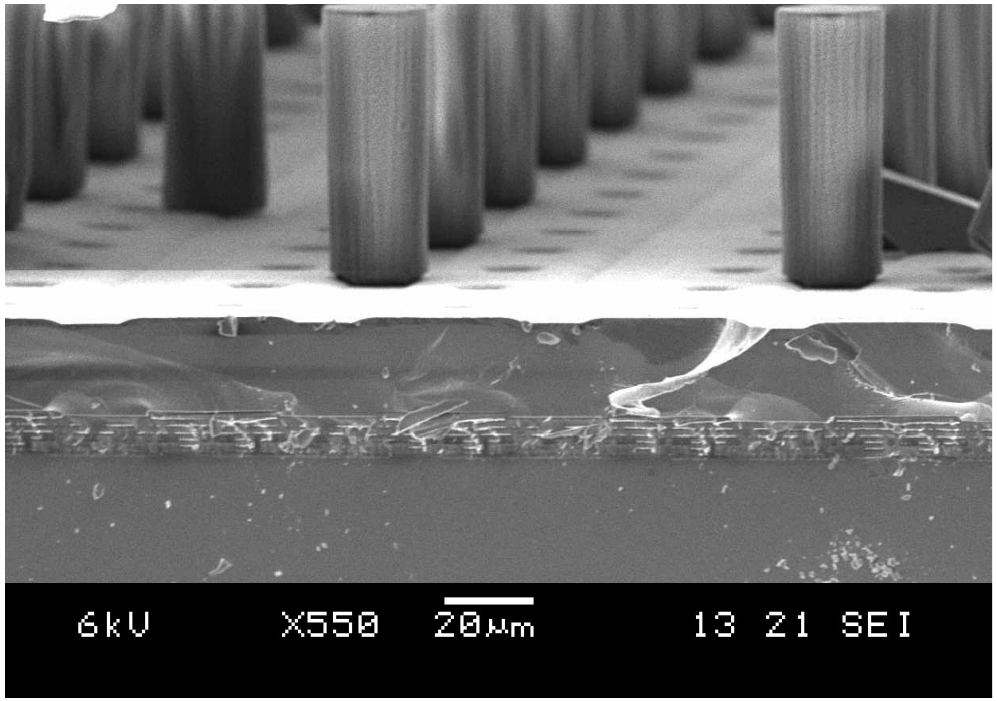
30µm a-Si

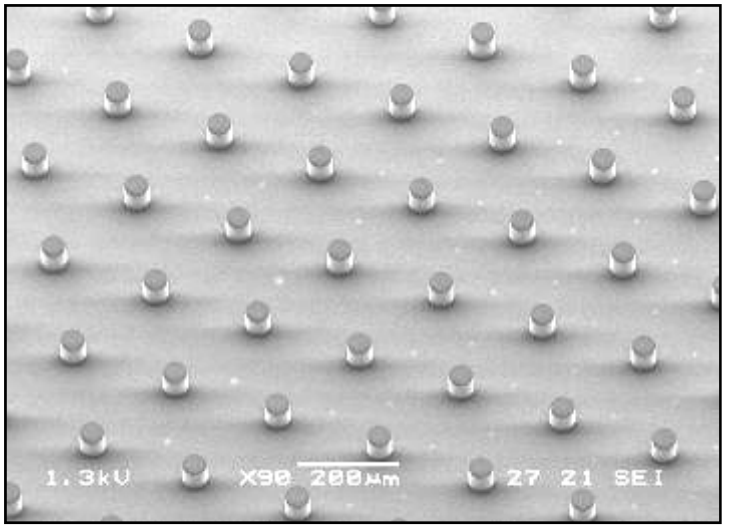


•For later steps a-Si topography seems not to limit lithography performance

3) SU-8 supporting structures

- Pillars tipically ~50µm tall and 30µm diameter
- Sparsed according to the pitch of the chip



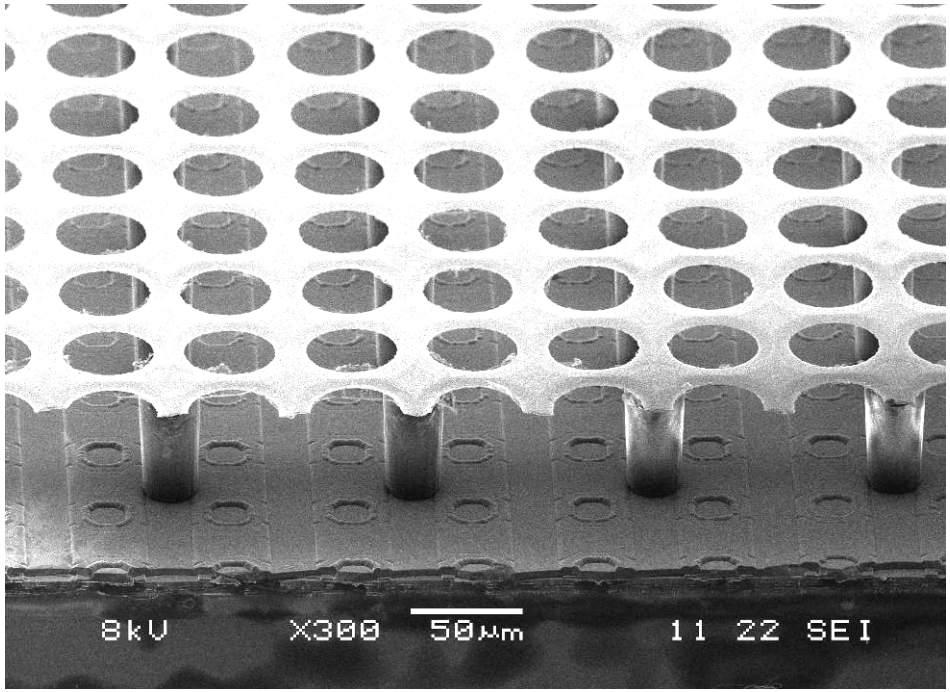


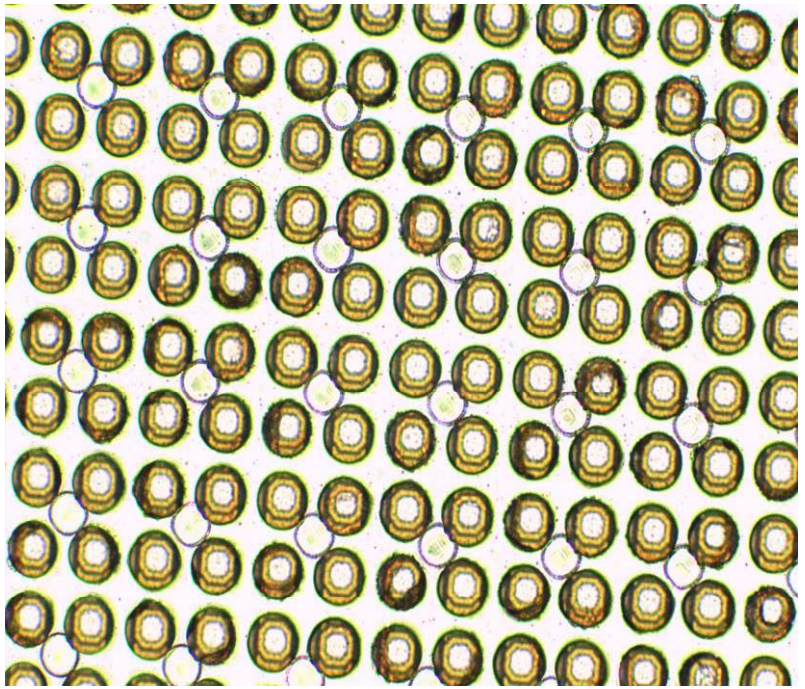
4)The integrated device

-Chip+a-Si+grid supported by insullating pillars

-Pillars in the middle of four pixels

-Perfect alignment hole to pixel

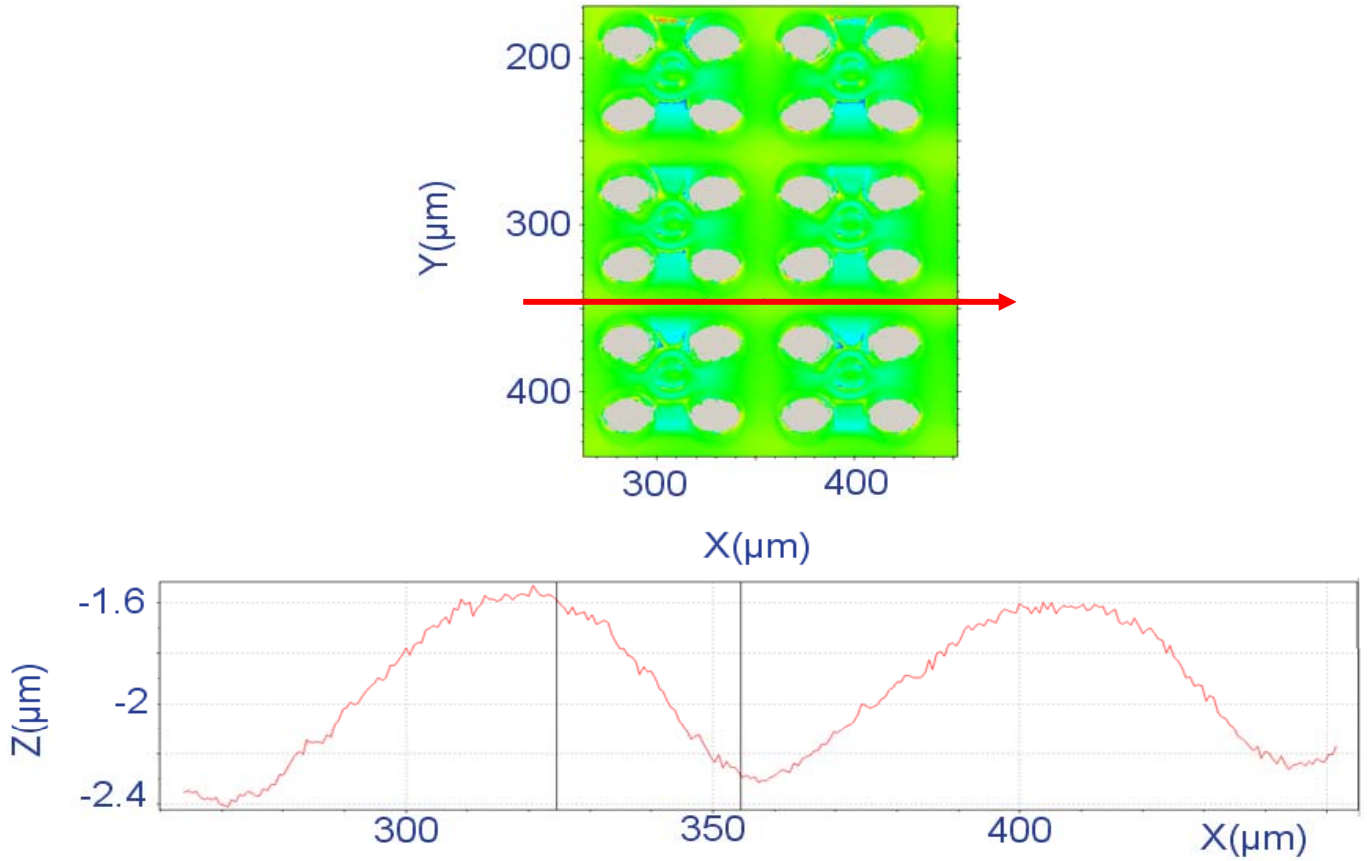




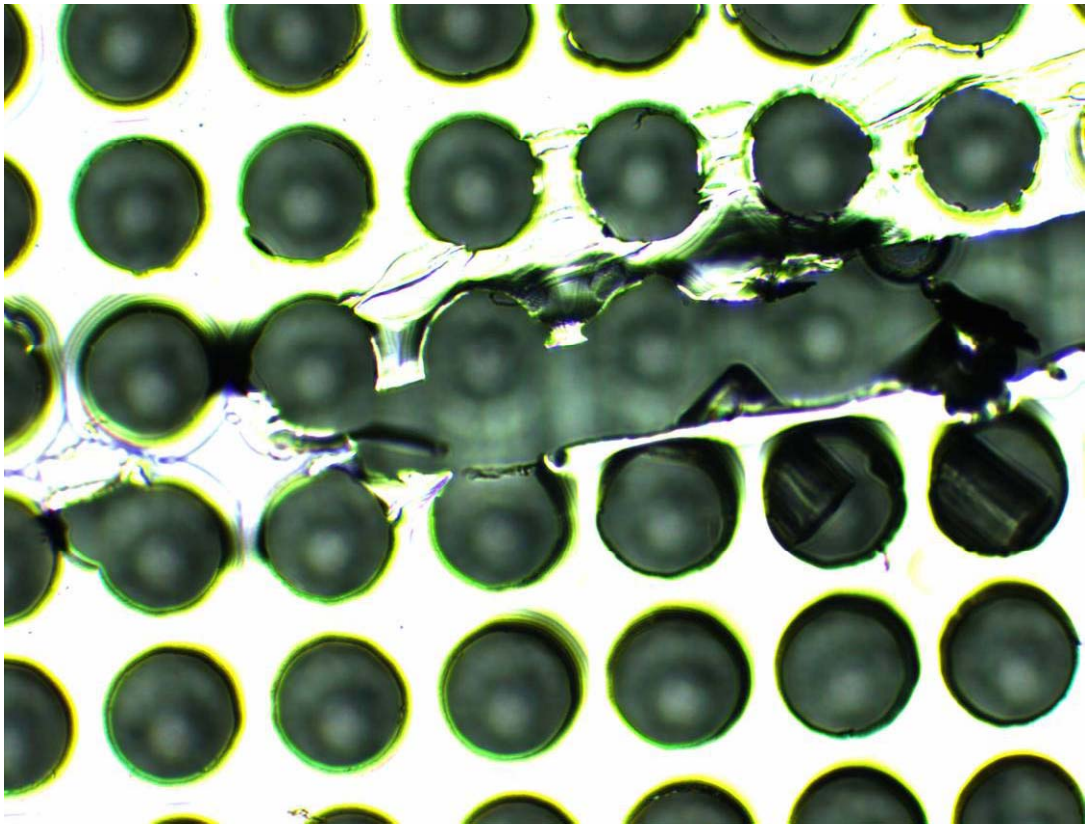
Grid profile

~1μm variation in grid roughness

Low gain fluctuations due to mechanical imperfections



And the system is robust



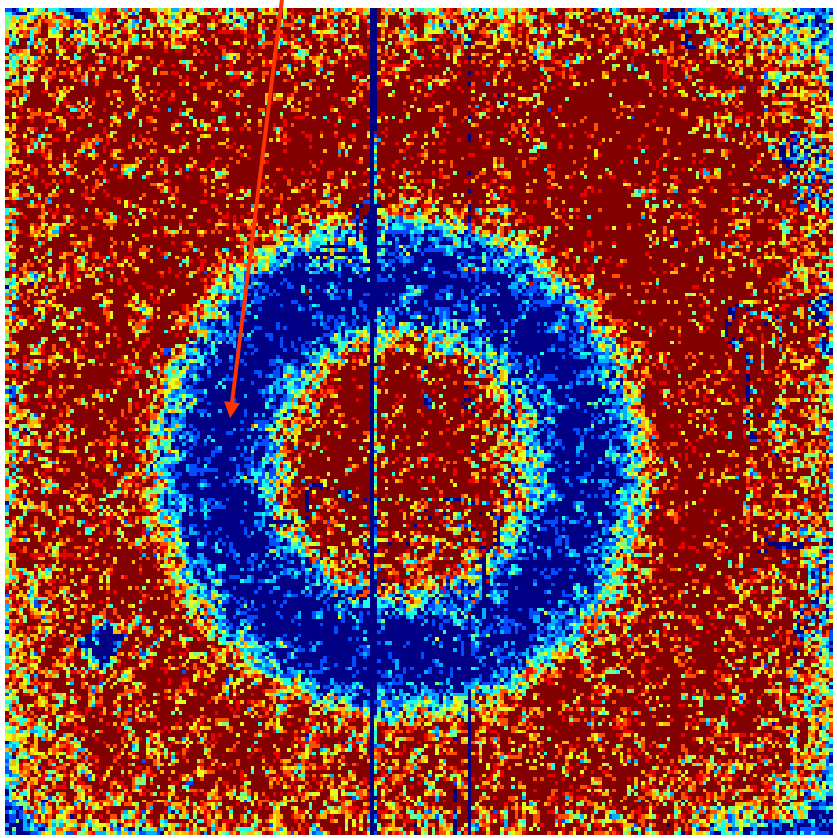
- A scratch occurred during fabrication but system works

-Several months working in Helium/Isobutane

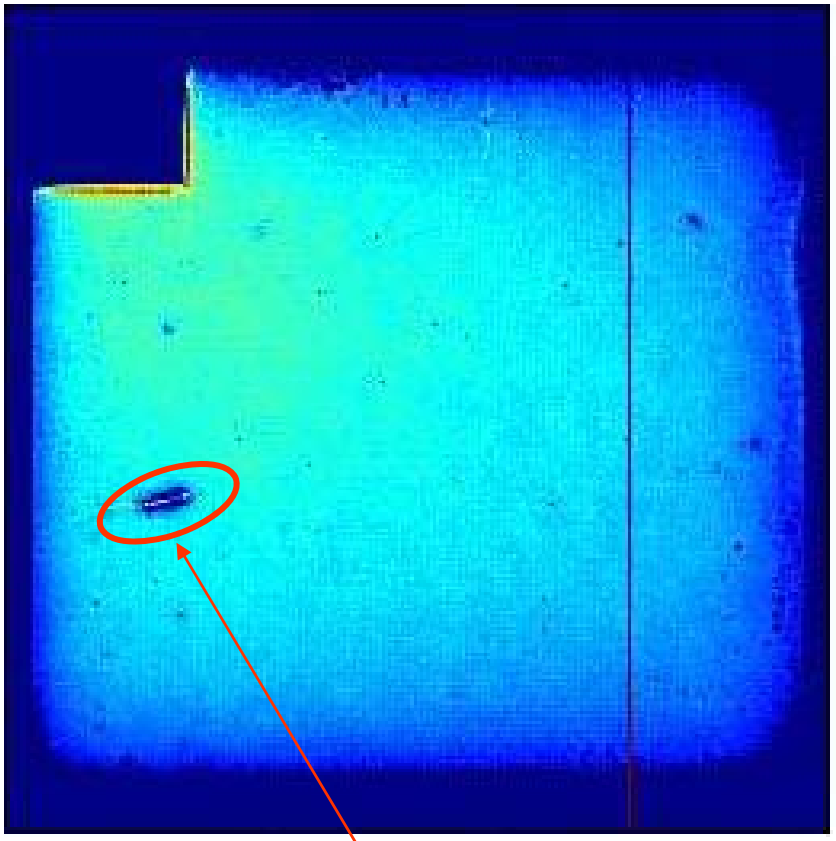
-Several months working in Argon/Isobutane

An homogeneous response

Nut image after ^{55}Fe irradiation

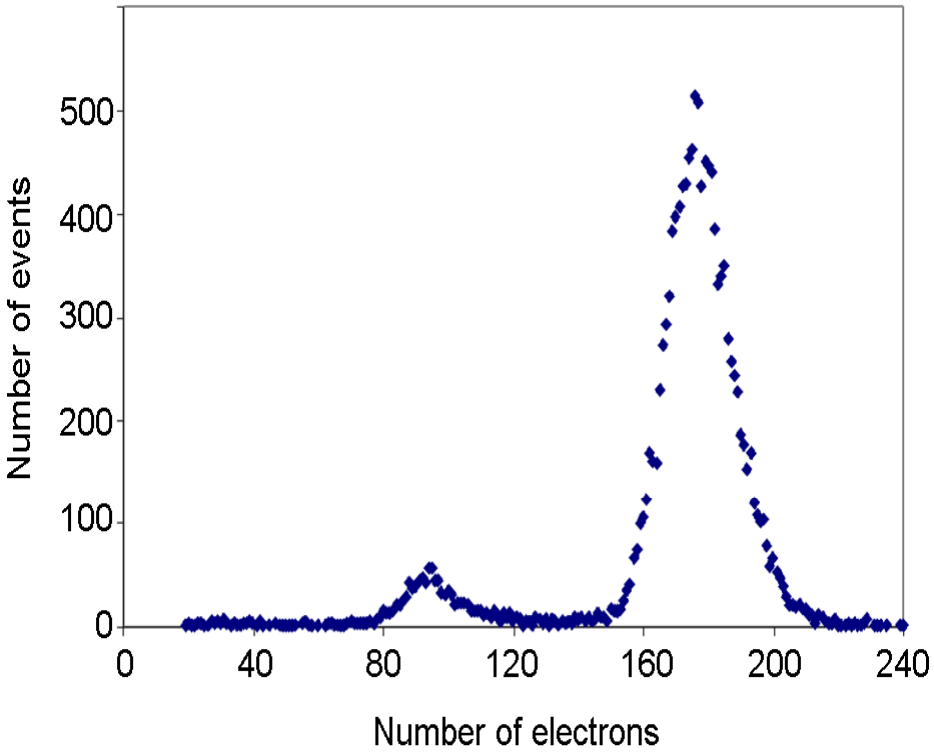


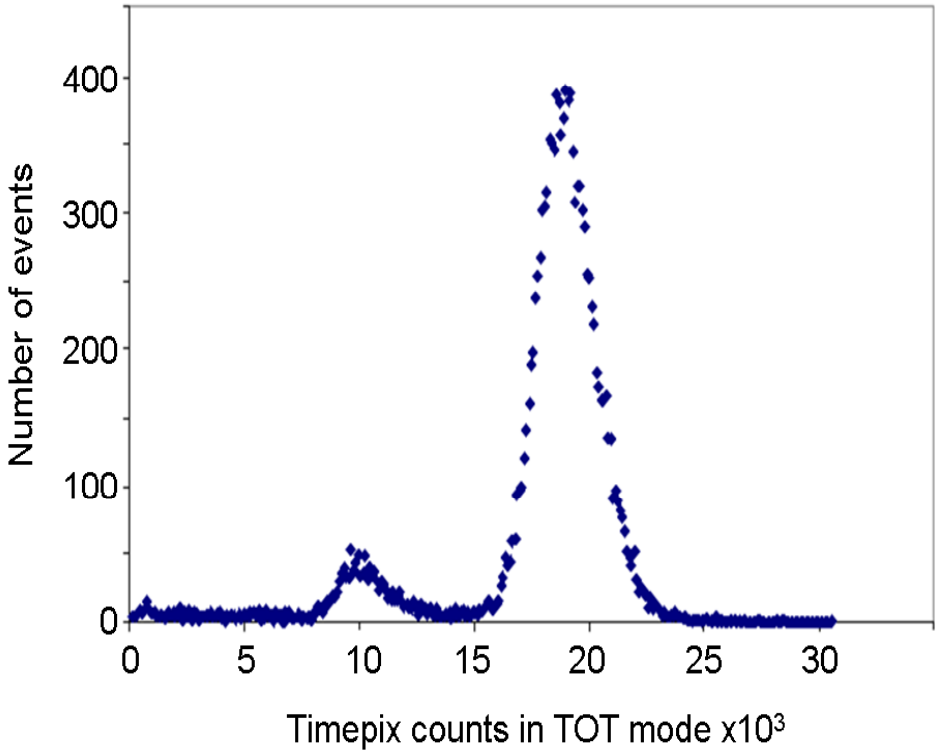
No Moire effect



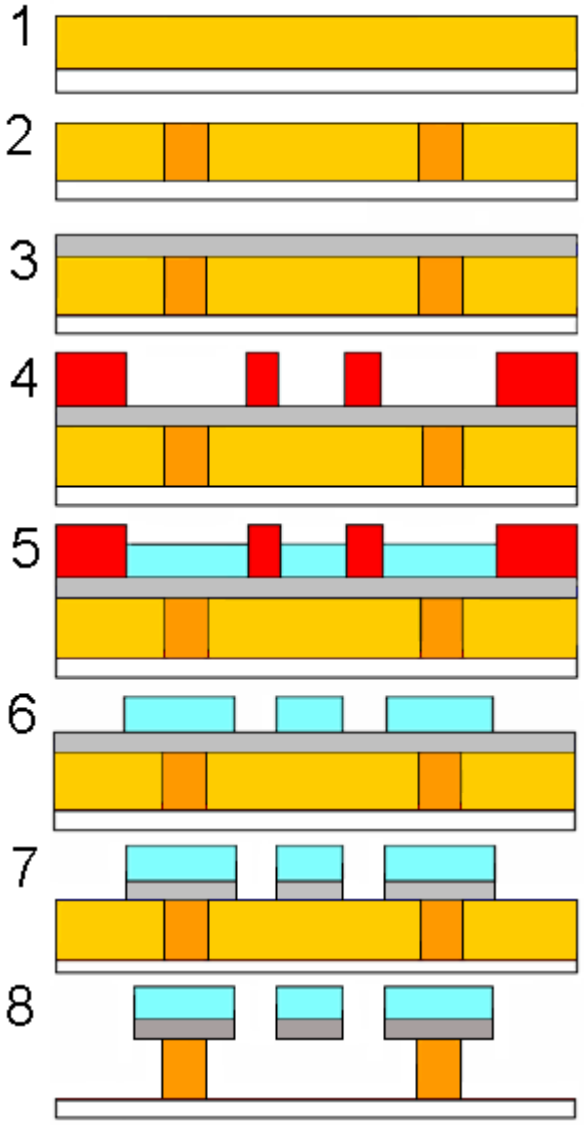
Single electron counting possible

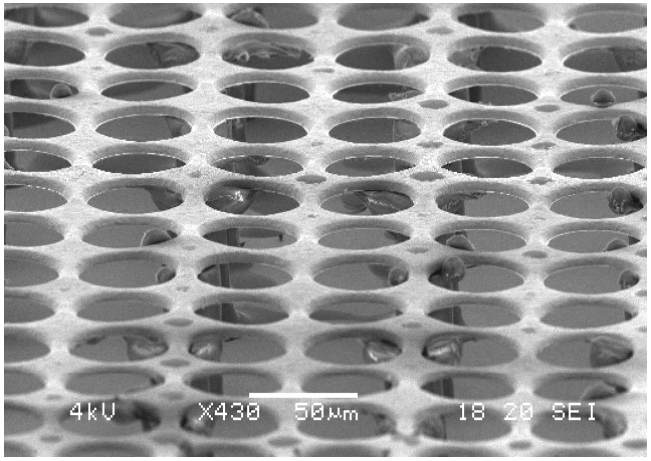
- Charge spread over chip area
- ^{55}Fe spectrum reconstructed from single electron counting and TOT mode

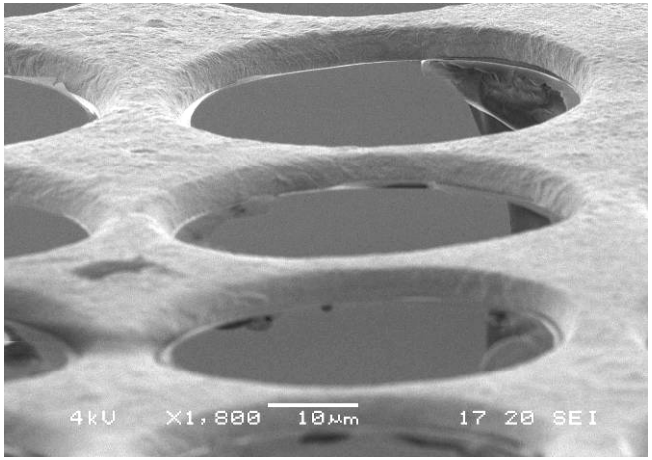




Electroplated grid



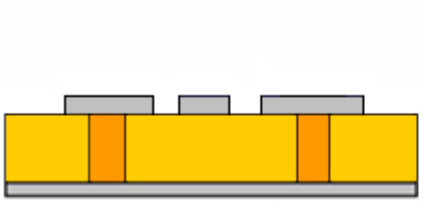




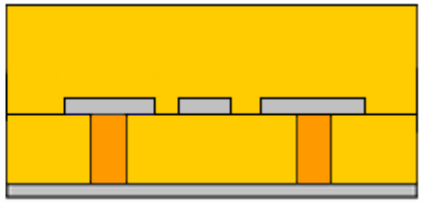
- Thicker and more robust grid possible
- Copper instead of aluminum
- Other materials possible by plating

CMOS chip	Seed metal layer
Unexposed SU-8	Molding resist
Exposed SU-8	Plated metal

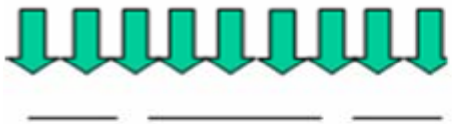
TwinGrid

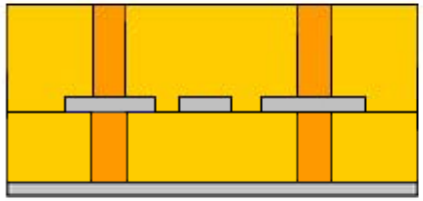


1)First InGrid

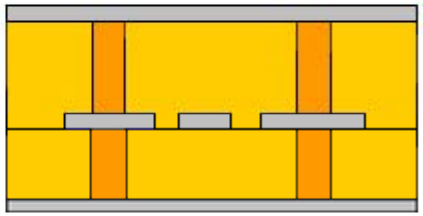


2)Deposit resist

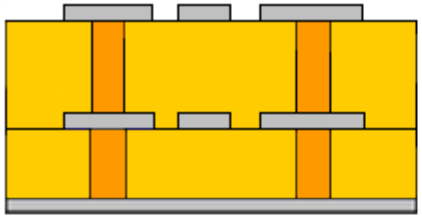




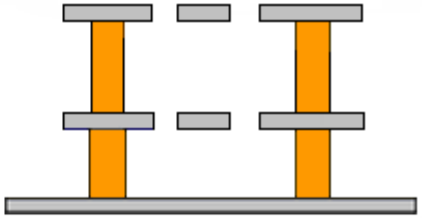
3)UV exposure



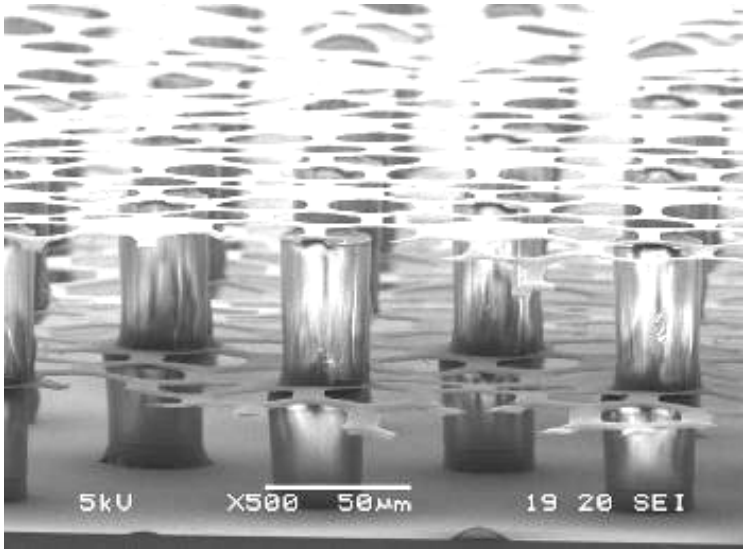
4)Deposit metal

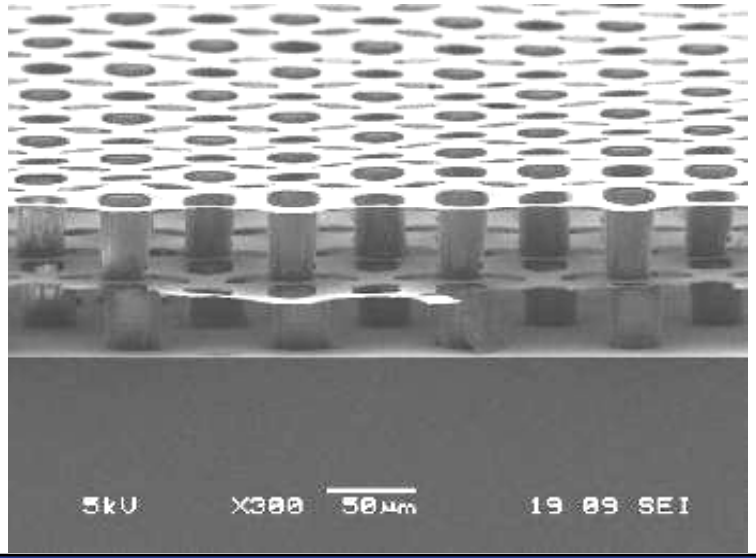


5)Pattern metal



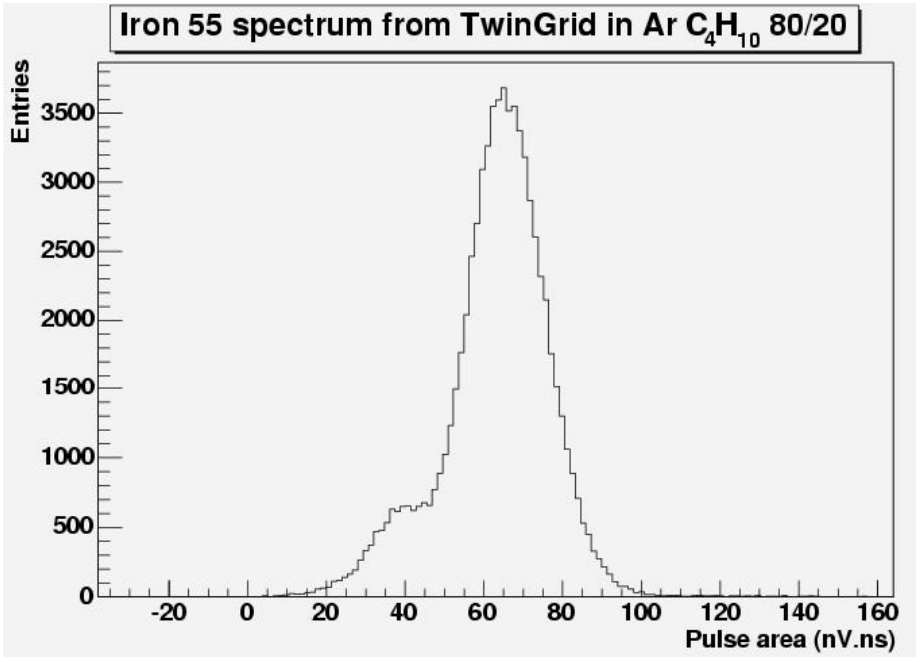
6)Develop structure

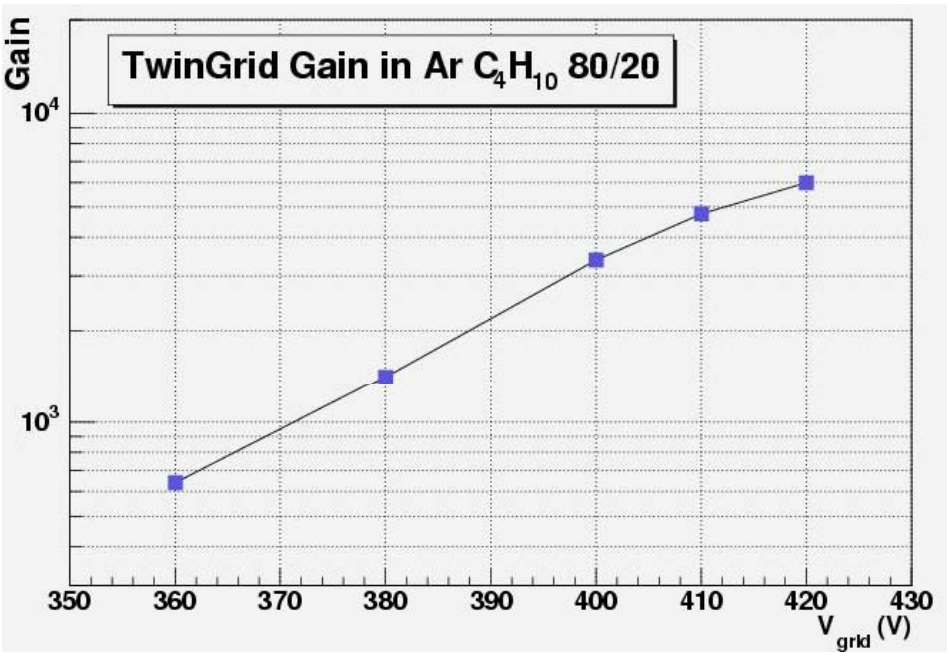




And it works

- Voltage on top grid, middle grid floating
- Next step integrate on a chip with voltage on both electrodes

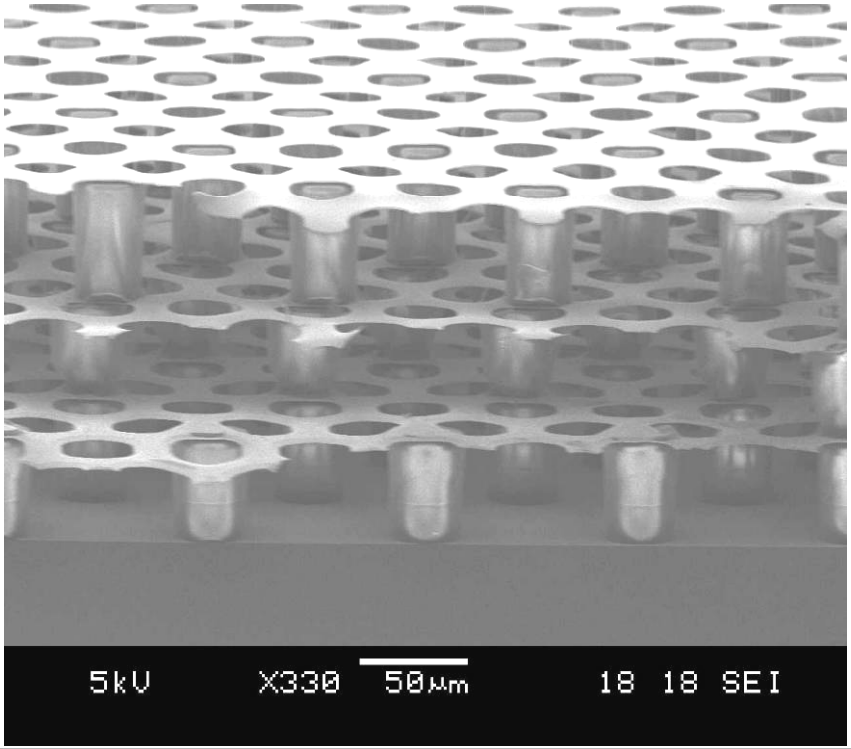


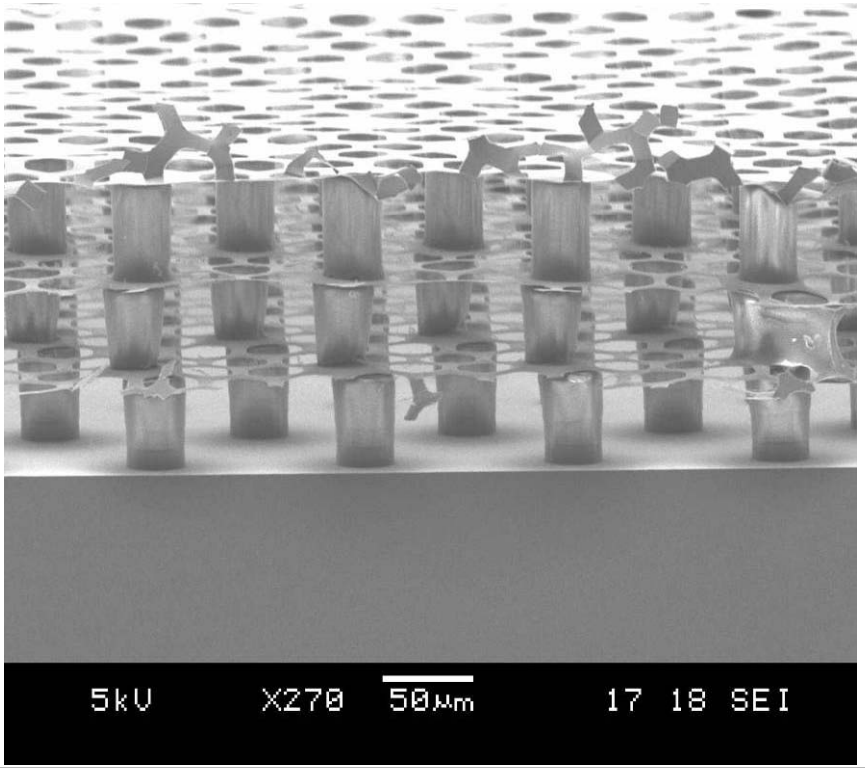


Triple grid

- Follow same fabrication scheme
- Lower electric field facing the chip in Twingrid and triple grid

  -reduce spark risk? reduce a-Si thickness needed?
- Intentionally misaligned grids can reduce ion-back flow?





Conclusions

- Medipix/Timepix/Gossipo+a-Si+InGrid working
- Wafer and chip level processing possible
- Lot of freedom in the fabrication process
- GEM-like structures seem feasible

Special thanks to you and

- SC group (Tom, Arjen, Bijoy, Jurriaan, Joost, Jiwu,Sander,Cora)
- Mesa+ lab (Dominique, Hans)
- NIKHEF(Max,Martin,Yevgen,Jan,Joop,Harry, Fred)
- Philips (Eugene)
- NXP (Rob)
- STW

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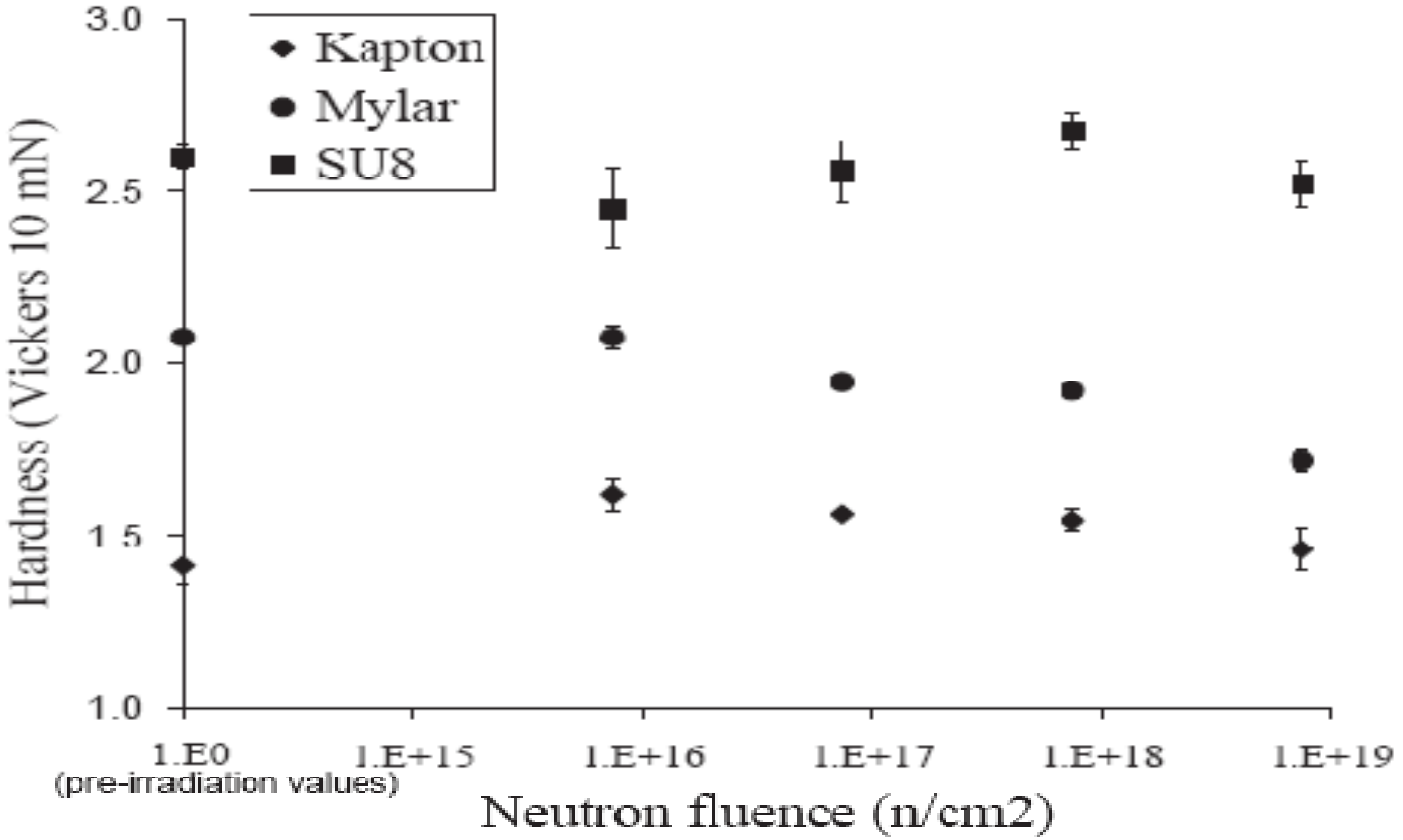
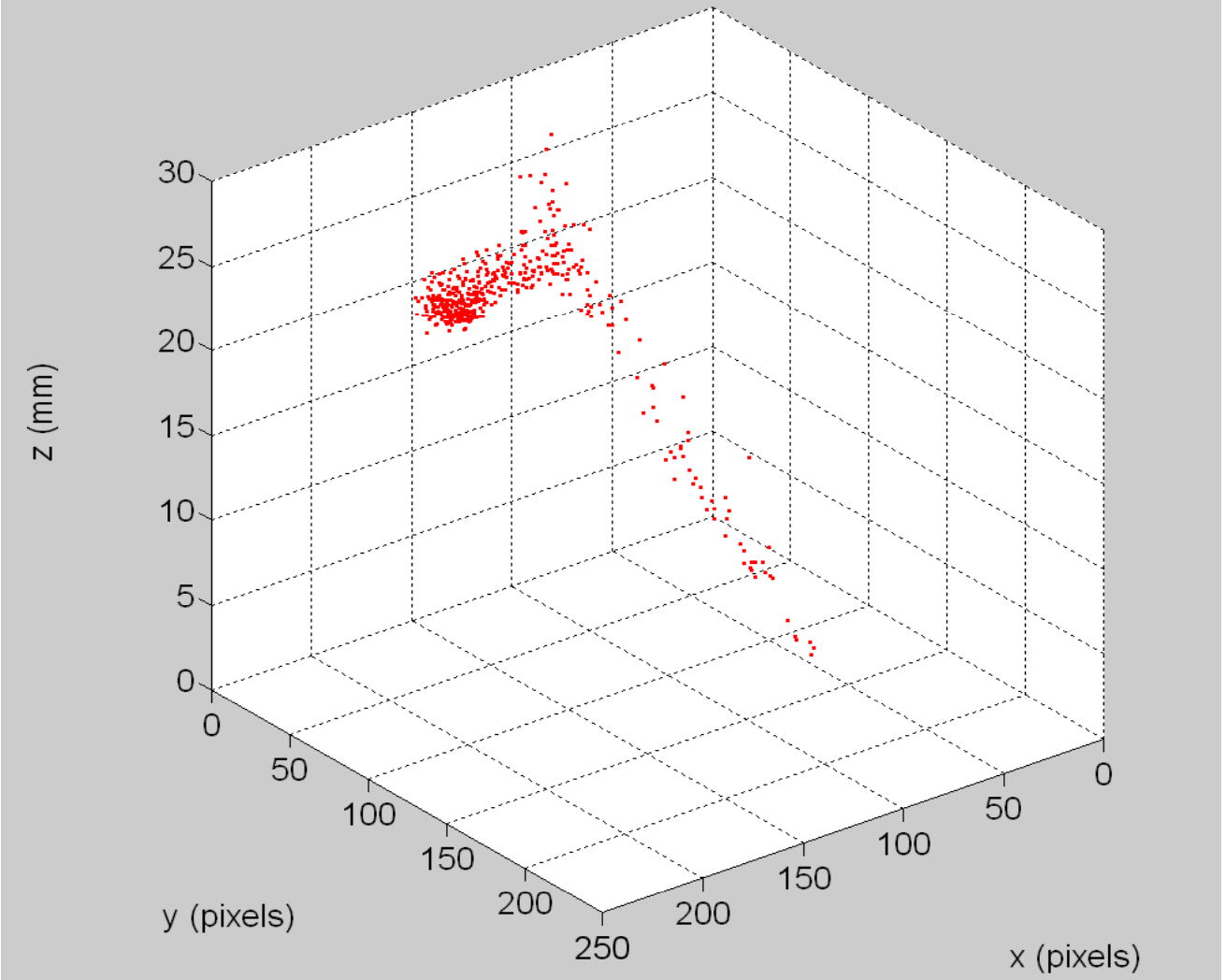
SU-8 radiation hardness

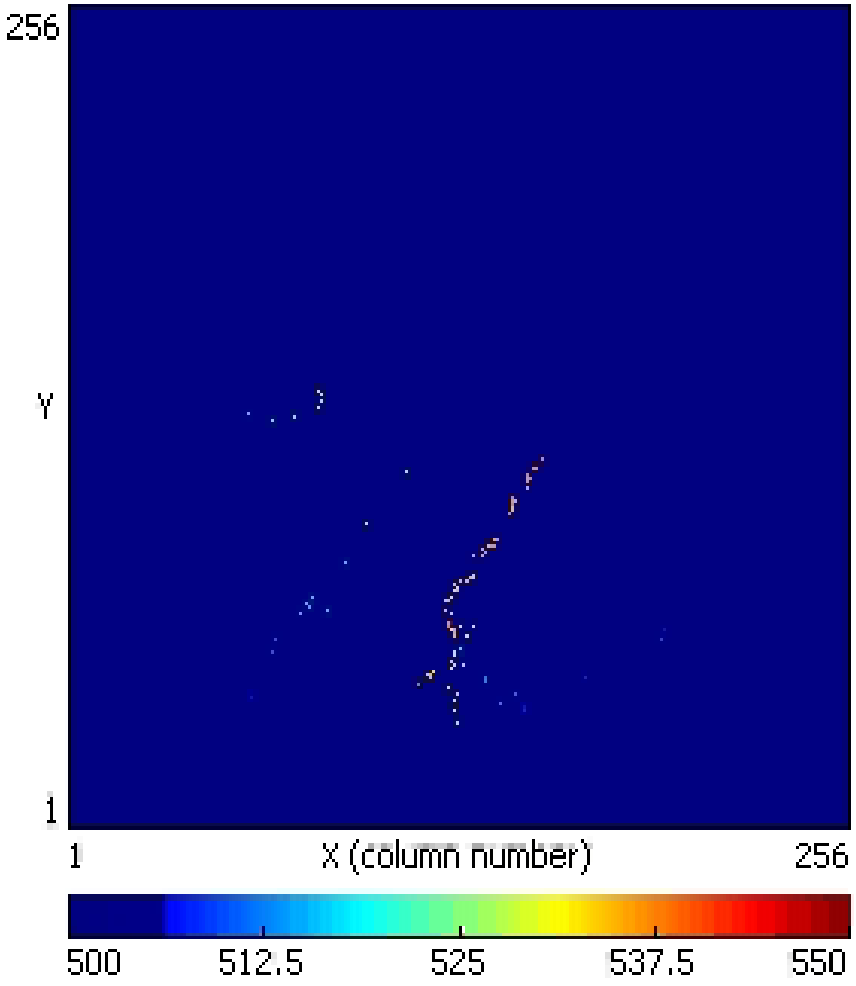


Mylar fluence of 7.5 10^{18} n cm2 ~ dose 10^{6}–10^{7} Gy

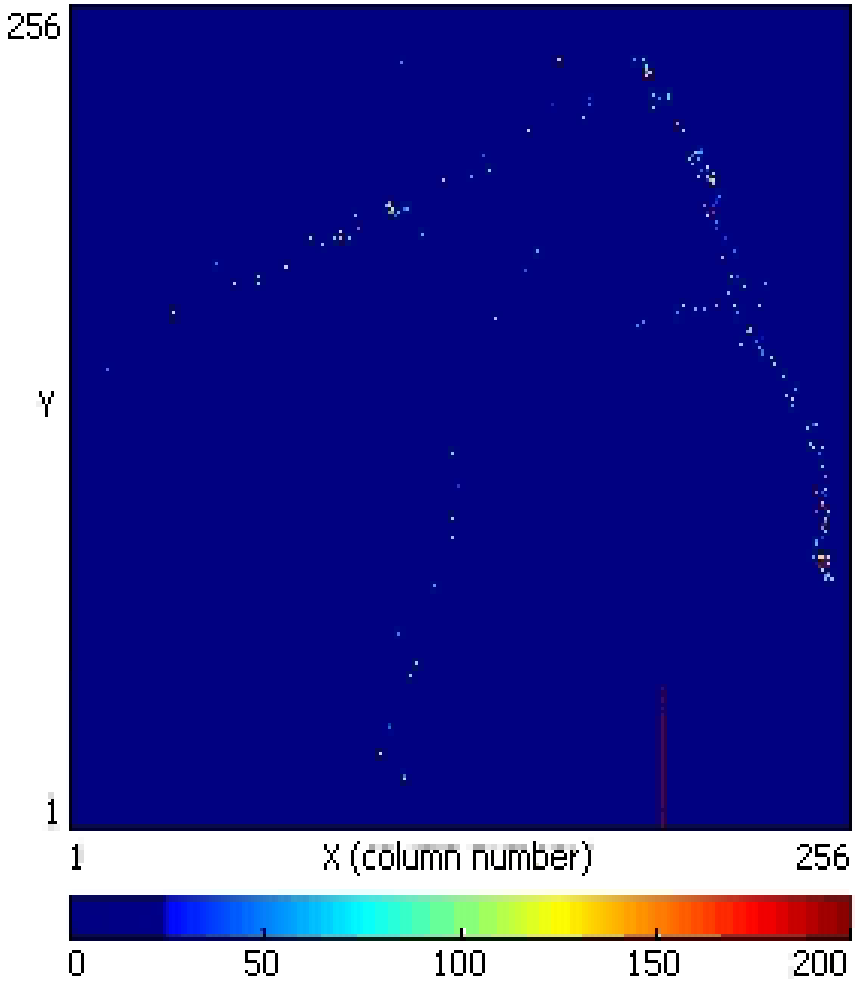
And they look great in 3D



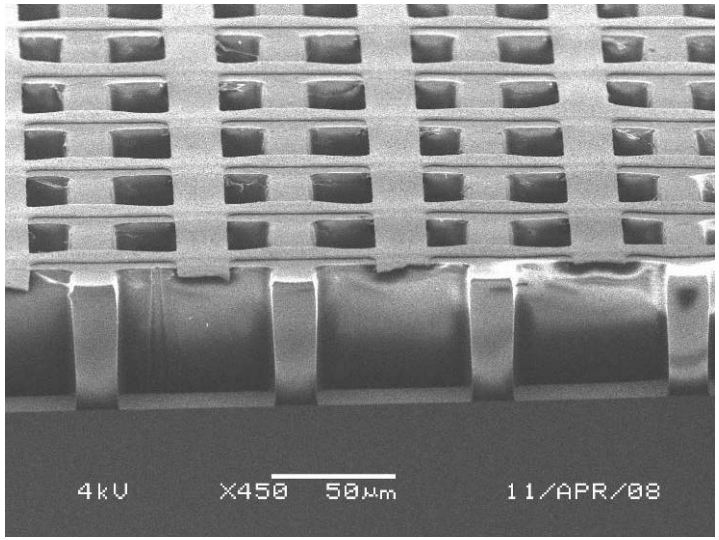
2D tracks projections

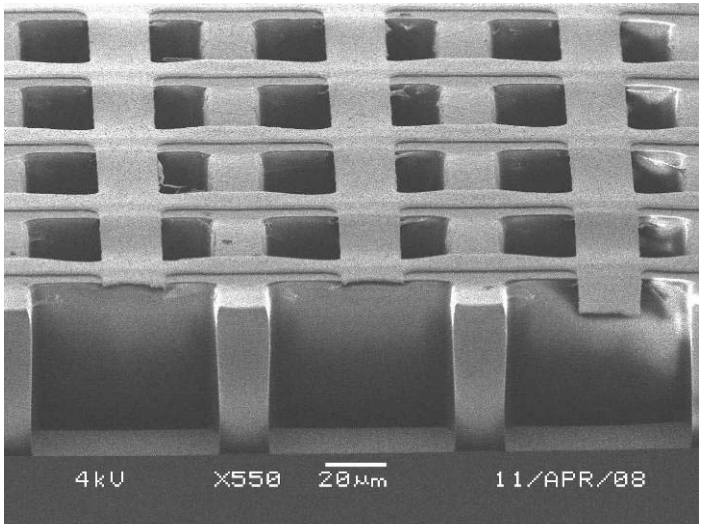


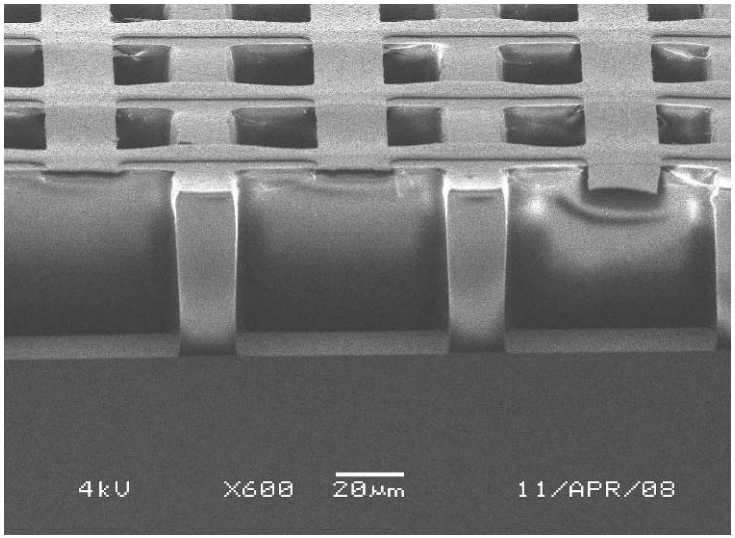
Cosmic rays



Strontium


4kV X450 50µm 11/APR/08


4kV X550 20µm 11/APR/08


4kV X600 20µm 11/APR/08