FNAL 65nm test structures
TZ65 chip

Fermilab
CMS pixels project
March, 2013

U.S. DEPARTMENT OF ENERGY
Fermilab

65nm test structures (TZ65 chip)

- Submission in March 2013 (MOSIS run 03/25/2013)
- $2 \times 6 mm^2$,divided in two parts
- Cost $83k (*expensive*)
- TSMC 65nm, 1P9M, 2MT 900Å, 14500Å AP, No RV
- Design: Farah Fahim and Alpana Shenai
- Open for sharing with institutions interested in: technology, hot carrier degradation and irradiation tests

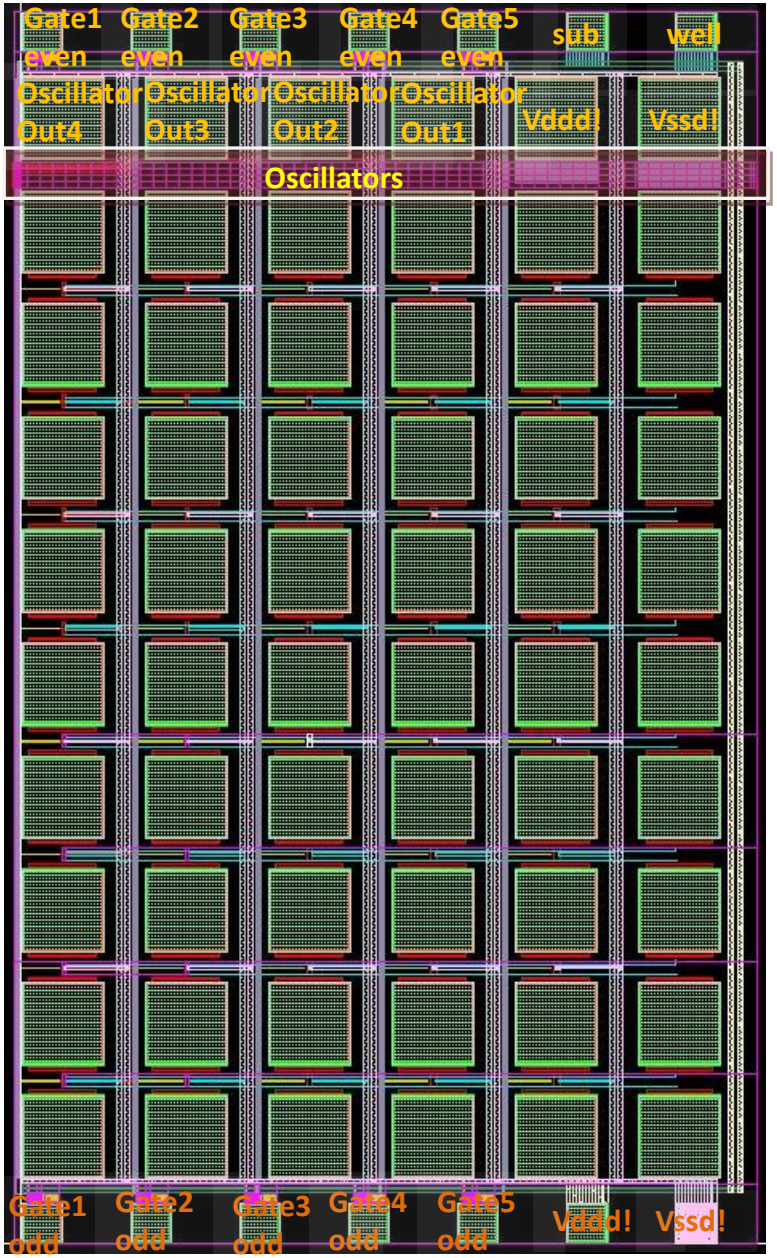
General comments

- Submissions in 65nm every 2 weeks via MOSIS
- Very efficient and professional technical support for TSMC 65nm provided by MOSIS, many questions generated
- Troubles with understanding of DFM rules, verification: DRC and LVS run very slowly, upgrade of tools required, e.g. parasitics extraction

65nm ½chip1

Table of transistor sizes

PMOS	500n/100n M=1	500n/60n M=1	25u/200n M=5	25u/100n M=5	25u/60n M=5
NMOS	500n/100n M=1	500n/60n M=1	25u/200n M=5	25u/100n M=5	25u/60n M=5
PMOS	1u/100n M=1	1u/60n M=1	5u/200n M=1	5u/100n M=1	5u/60n M=1
NMOS	1u/100n M=1	1u/60n M=1	5u/200n M=1	5u/100n M=1	5u/60n M=1
PMOS	500n/200n M=1	500n/200n M=1	2.5u/200n M=1	2.5u/100n M=1	2.5u/60n M=1
NMOS	500n/200n M=1	500n/200n M=1	2.5u/200n M=1	2.5u/100n M=1	2.5u/60n M=1
PMOS	1u/200n M=1	1u/200n M=1	10u/200n M=2	10u/100n M=2	10u/60n M=2
NMOS	1u/200n M=1	1u/200n M=1	10u/200n M=2	10u/100n M=2	10u/60n M=2



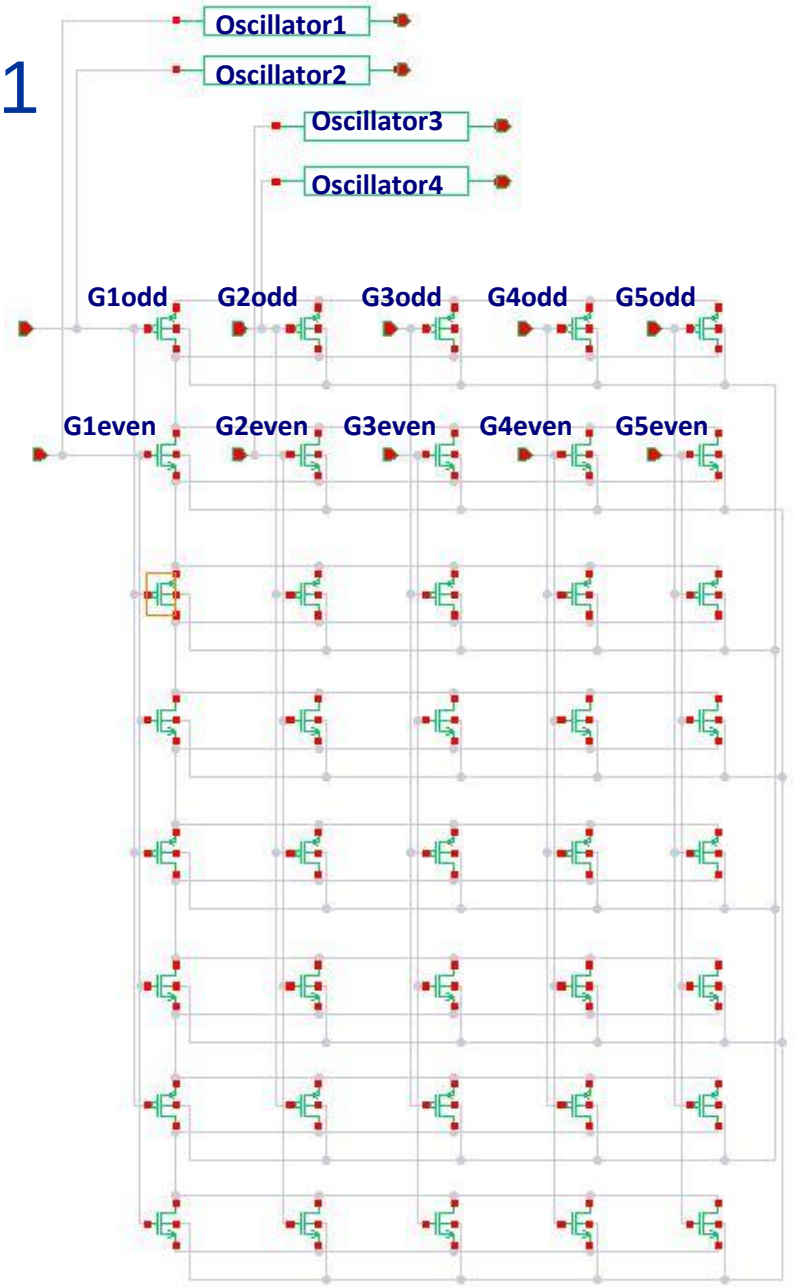
4 ring oscillators

With 923 inverting stages each with the following inverter sizes

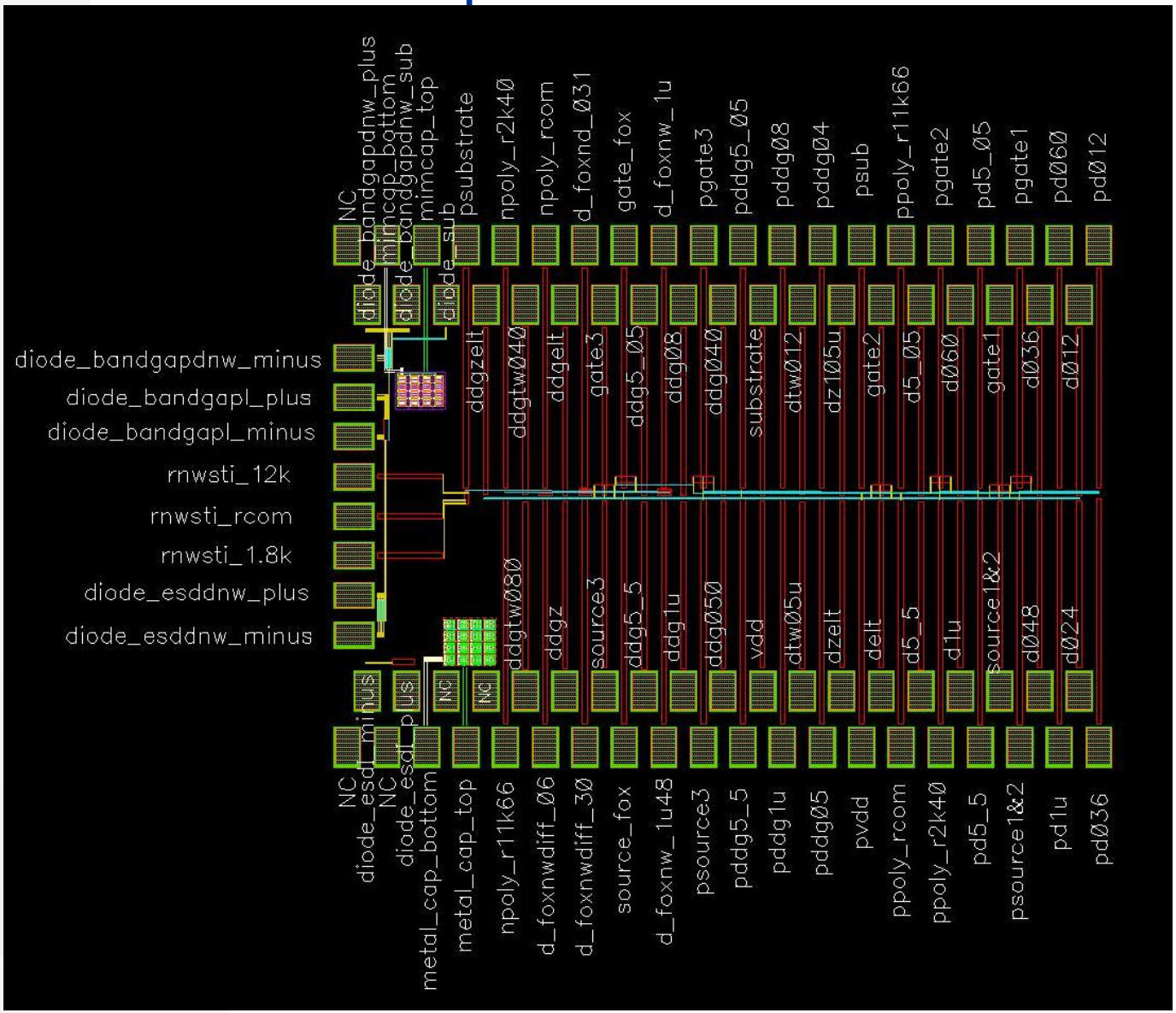
- PMOS 2u/60n; NMOS 1u/60n
- PMOS 2u/130n; NMOS 1u/130n
- PMOS 2u/200n; NMOS 1u/200n
- PMOS 2u/300n; NMOS 1u/300n

65nm ½chip1

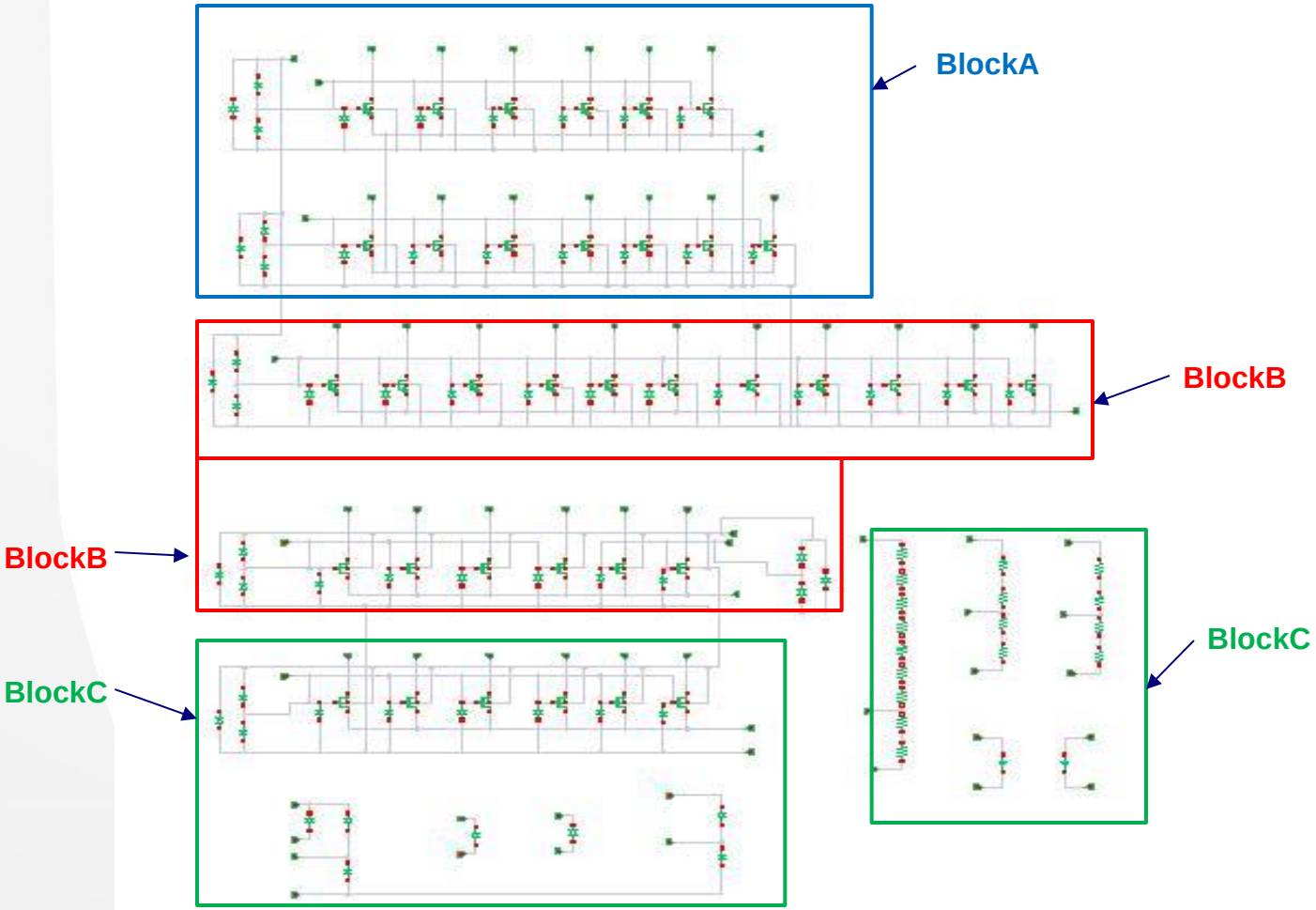
schematics



65nm ½chip2

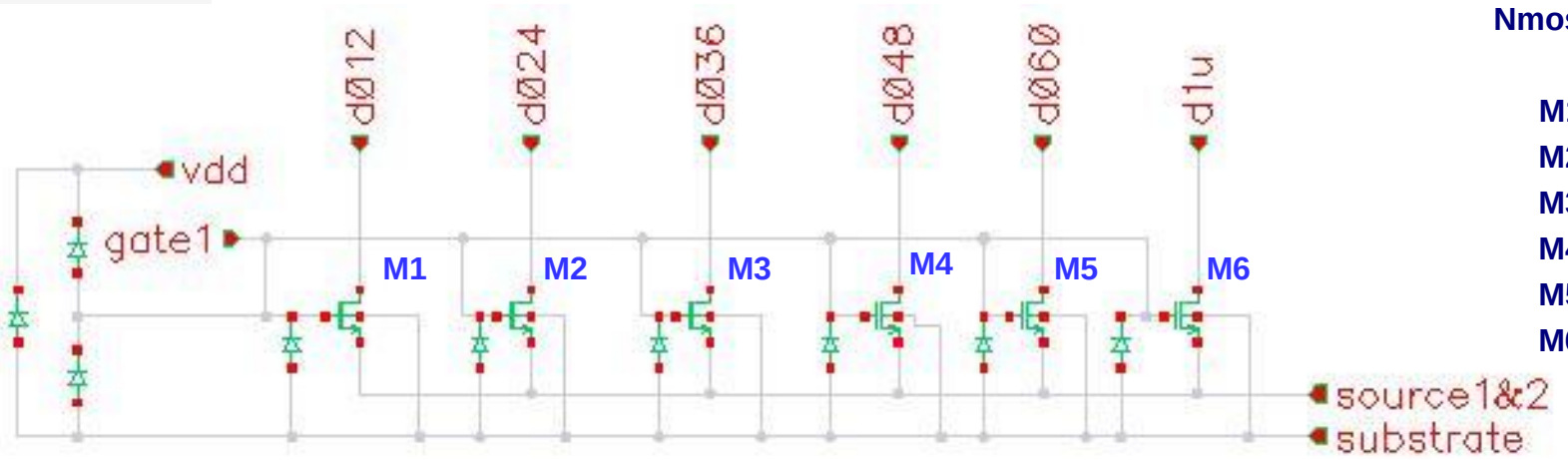

diode_bandgapdnw_minus
diode_bandgapl_plus
diode_bandgapl_minus
rnwsti_12k
rnwsti_rcom
rnwsti_1.8k
diode_esddnw_plus
diode_esddnw_minus
NC
diode_bandgapdnw_plus
mimcap_bottom
diode_bandgapdnw_sub
mimcap_top
diode_sub
psubstrate
npoly_r2k40
npoly_rcom
d_foxnd_031
gate_fox
d_foxnw_1u
pgate3
pddg5_05
pddg08
pddg04
psub
ppoly_r11k66
pgate2
pd5_05
pgate1
pd060
pd012
ddgzelt
ddgtw040
ddgelt
gate3
ddg5_05
ddg08
ddg040
substrate
dtw012
dz105u
gate2
d5_05
d060
gate1
d036
d012
ddgtw080
ddgz
source3
ddg5_5
ddg1u
ddg050
vdd
dtw05u
dzelt
delt
d5_5
d1u
source1&2
d048
d024
NC
diode_esdl_minus
NC
diode_esdl_plus
metal_cap_bottom
metal_cap_top
npoly_r11k66
d_foxnwdiff_06
d_foxnwdiff_30
source_fox
d_foxnw_1u48
psource3
pddg5_5
pddg1u
pddg05
pvdd
ppoly_rcom
ppoly_r2k40
pd5_5
psource1&2
pd1u
pd036

65nm ½chip2



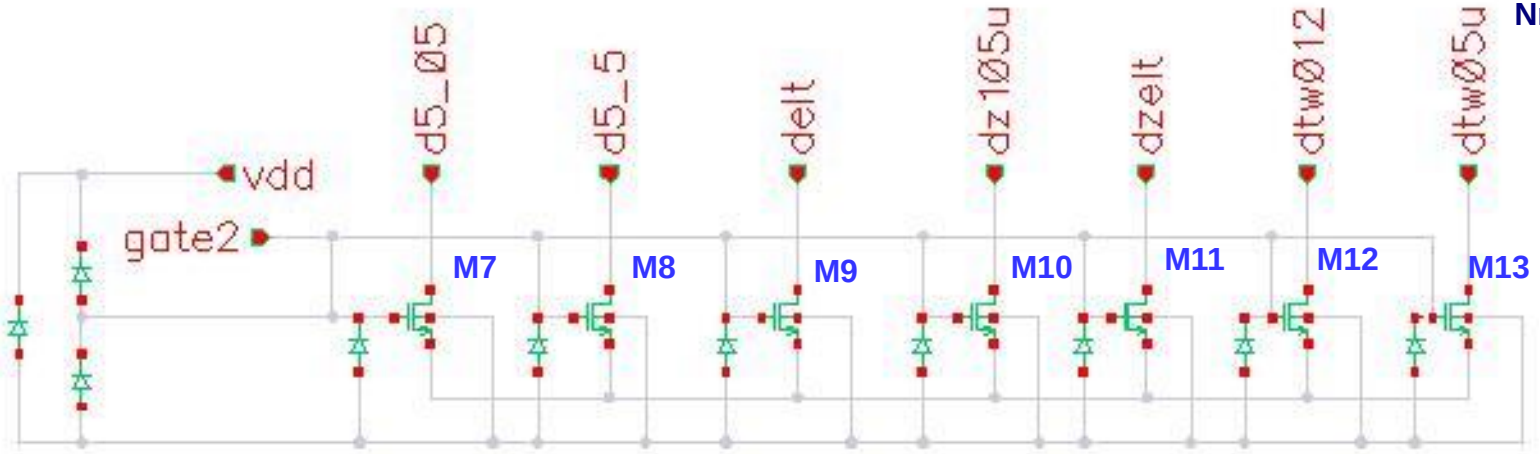
65nm ½chip2

details of BlockA schematics



Nmos Transistors (nch)

M1:	.12/.06
M2:	.24/.06
M3:	.36/.06
M4:	.48/.06
M5:	.6/.06
M6:	1/.06

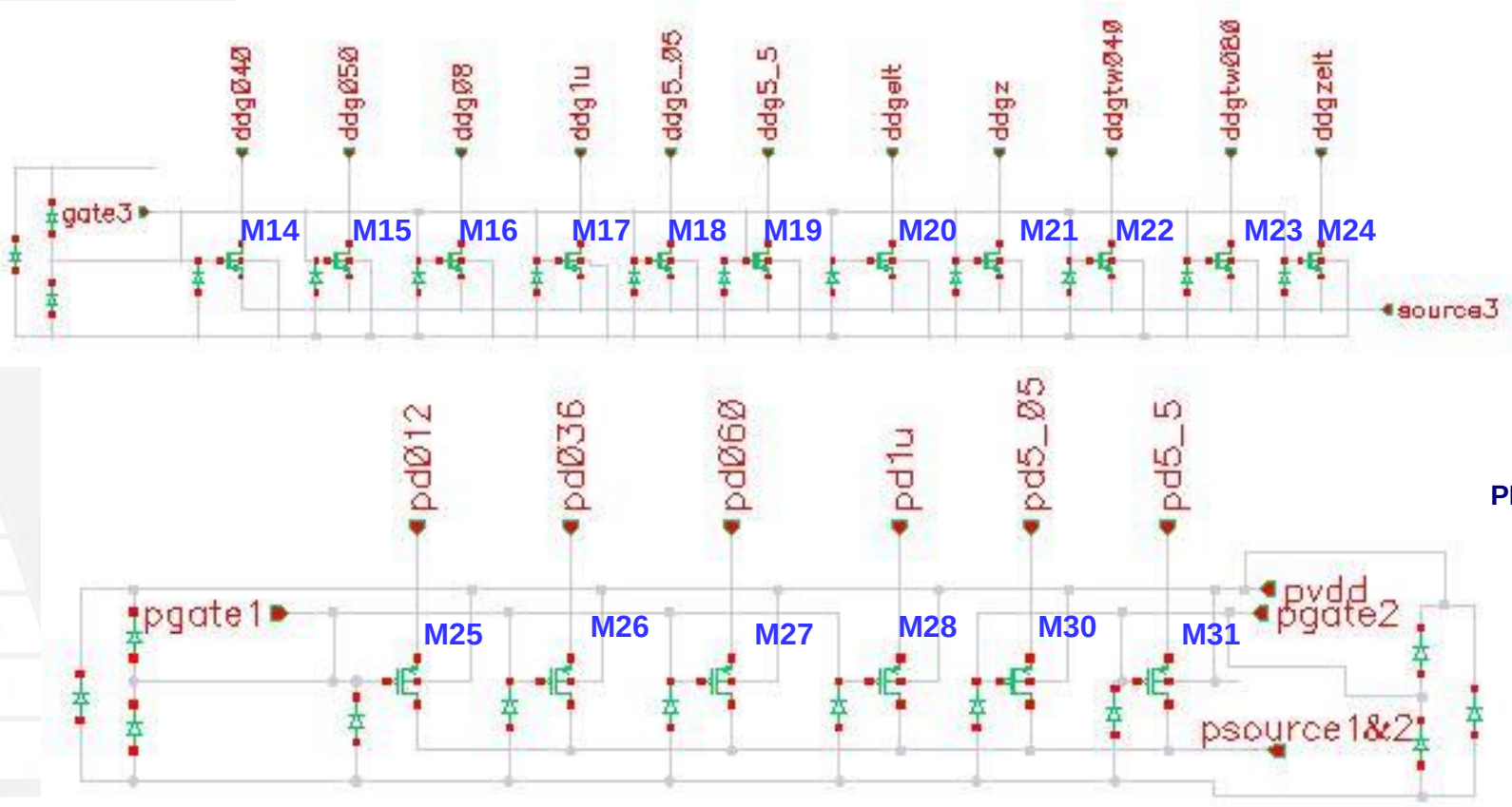


Nmos Transistors (nch)

M7:	5/.5
M8:	5/5
M9:	2.05/.06
M10:	1.5/.3
M11:	2.24/.3
M12:	.12/.06
M13:	5/.06

65nm ½chip2

details of BlockB schematics



NMOS Transistors (nch_25)

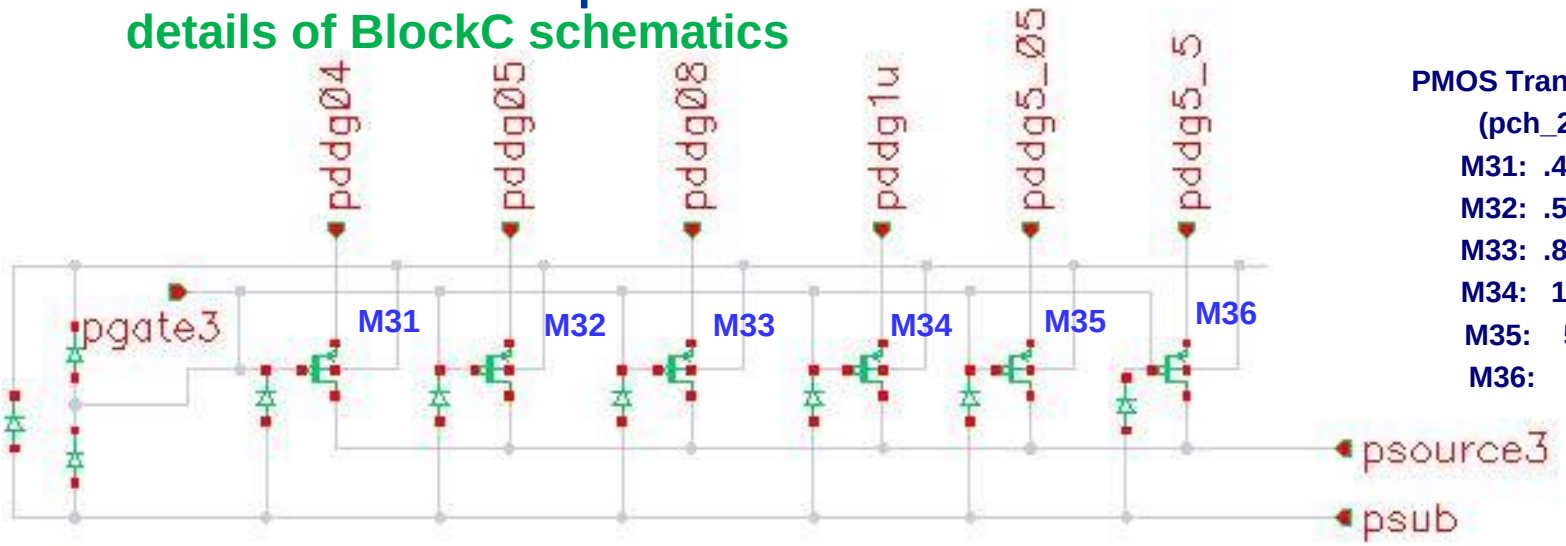
M14:	.4/.28
M15:	.5/.28
M16:	.8/.28
M17:	1/.28
M18:	5/.5
M19:	5/5
M20:	2.22/.28
M21:	3.38/1.2
M22:	.4/.28
M23:	.8/.28
M24:	3.45/1.2

PMOS transistors (pch)

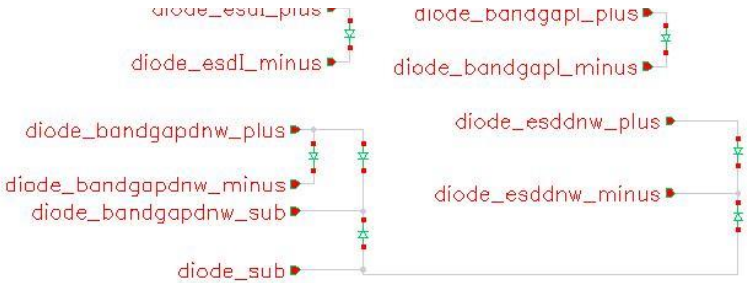
M25:	.12/.06
M26:	.36/.06
M27:	.60/.06
M28:	1/.06
M29:	5/.5
M30:	10/10
M31:	5/5

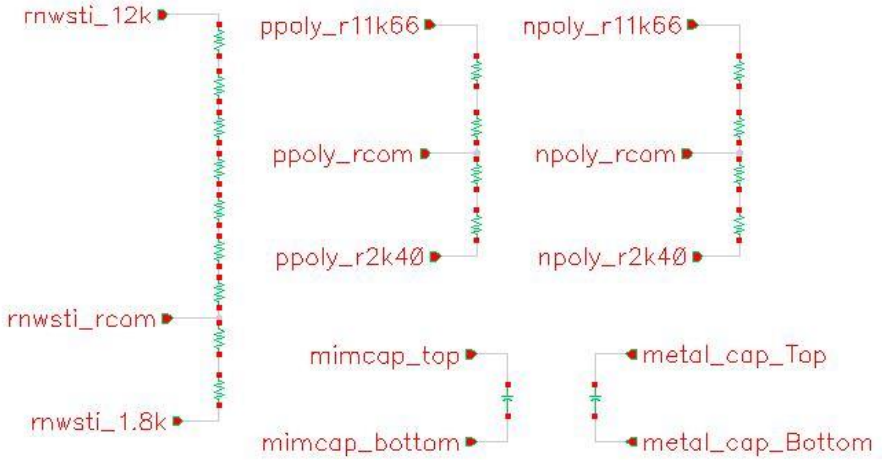
65nm ½chip2

details of BlockC schematics



PMOS Transistors
(pch_25)
M31: .4/.28
M32: .5/.28
M33: .8/.28
M34: 1/.28
M35: 5/.5
M36: 5/5



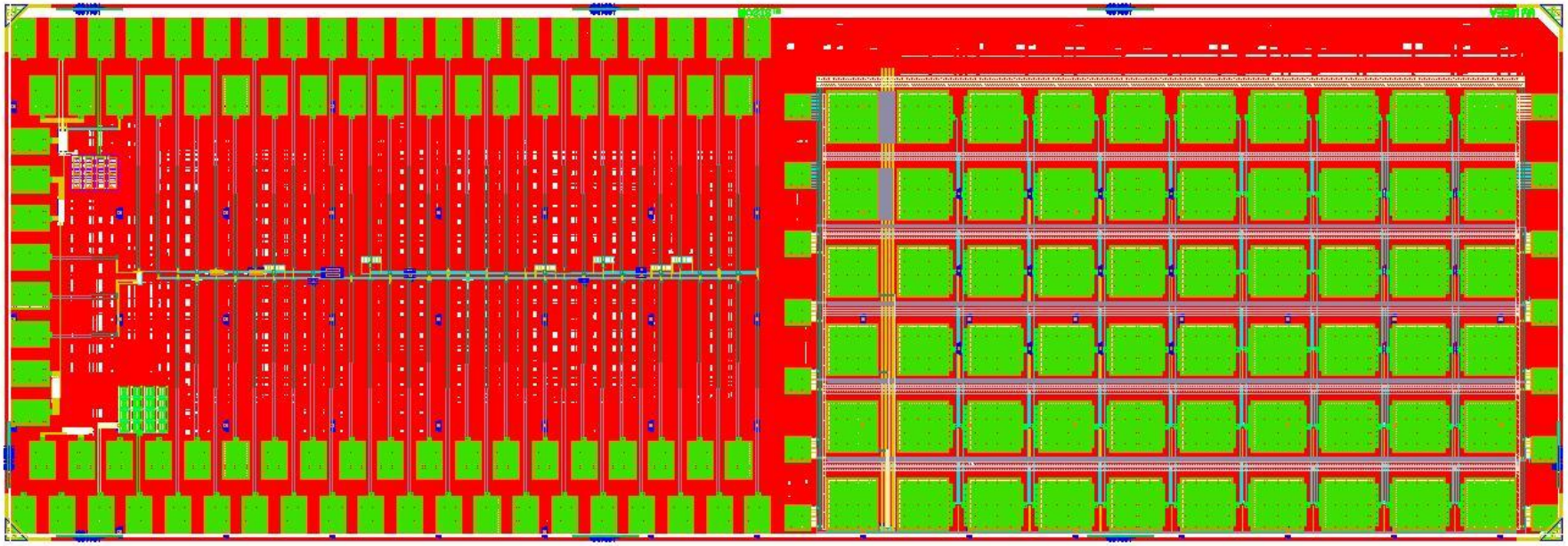


65nm ½chip2

Summary with size and number of Pads

Device	Size	Pad count	Numbers
Gate Oxide Devices for 1.2V			
NMOS W array, L=0.06	W=0.12, .24, .36, .48, .6, 1	8 (s, g, 6xd)	M1,M2,M3,M4,M5,M6
NMOS L array, W=5	L=.5, 5	3 (g, 2xd)	M7,M8
NMOS edgeless (ELT)	W=2.05, L=0.06	1 (d)	M9
NMOS ZVt	W=1.5, L=0.3	1 (d)	M10
NMOS ZVt edgeless (ELT)	W=2.24, L=0.3	1 (d)	M11
NMOS triple well array, L=0.06	W=0.12, .5	2 (2xd)	M12,M13
PMOS W array, L=0.05	W=0.12, .36, .6, 1	6 (s, g, 4xd)	M25,M26,M27,M28
PMOS L array, W=5	L= .5, 5	3 (g, 2xd)	M29,M30
		25	
Gate Oxide Devices for 2.5V			
NMOS W array, L=0.28	W=0.4, 0.5, 0.8, 1	6 (s, g, 4xd)	M14, M15,M16,M17
NMOS L array, W=5	L=.5, 5	2 (2xd)	M18,M19
NMOS edgeless (ELT)	W=2.22, L=0.28	1 (d)	M20
NMOS ZVt	W=2.94, L=1.2	1 (d)	M21
NMOS ZVt edgeless (ELT)	W=3.38, L=1.2	1 (d)	M24
NMOS triple well array, L=0.28	W=0.4, .8	2 (2xd)	M23,M24
PMOS W array, L=0.28	W=0.4, 0.5, 0.8, 1	6 (s, g, 4xd)	M25,M26,M27,M28
PMOS L array, W=5	L=.5, 5	2 (2xd)	M29,M30
		21	
Resistors			
rnpoly , rppoly, & rnwsti	(R=11.52 kΩ, 1.6 kΩ, 12.67 kΩ & ,3.6 kΩ)	9	
		9	
FOXFETs			
Nwell/Nwell foxfet array, W=100	L=1.0, 1.48	3	
N+diff/N+diff foxfet, W=100	L=0.2, 0.4	2	
N+diff/Nwell foxfet array, W=100	L=0.2	2	
		7	
Diodes			
ESDI, ESDII(DNW), BandgapI, & BandgapII(DNW)	Area = 1096 µm2	9	
		9	
Capacitors			
Mimcap, & metal to metal cap	0pf, 10pf	**4**	
Power			
Vdd, Gnd	3,5	**5**	
Pad Total		**80**	

Submitted layout



Fermilab