CMS phase 2 pixel news & ATLAS-CMS RD collaboration (Electronics)

Jorgen Christiansen, CERN PH-ESE

News

- EPIX ITN proposal did not get requested EU funding
  - CERN based proposals did very bad this time.
  - I better not comment on the reviewer comments
  - We “lost” funding for ~8 PHD students for ATLAS/CMS phase 2 pixels.
- New collaborators/ contributers
  - Bari: We will visit Bari in ~2weeks time
  - Bergamo: Shows first signs of interest (superB cancelled)
  - Desy ?.
  - PSI ? (obviously 200% busy with Phase1)
  - Other ?
- 65nm tech.
  - TSMC – IMEC formally chosen for CERN frame contract (5 year contract)
  - Development of design kit/flow already started
    - Subcontracted to Cadence – Similar to 130nm design kit
    - First version to be tested by CERN before summer
  - Fine details of contract & NDA in negotiation.
  - Extended radiation tests in the planning
    - Modifications to CERN X-ray machine enables to get to ~1Grad in a ~week
    - E.g. new ~1Grad results from CPPM in the pipeline.
    - Pixel phase 2 RD collaboration
  - Rad tolerant IP’s to be subcontracted (by CERN to IP companies):
    - SRAM generator
    - Slow ADC
    - CMOS IO pads (with core transistors because of radiation tolerance)
    - PLL
    - Bandgap
    - These may not be compliant with 1GRad/10^{16} neu/cm^2 ! (others: ~100Mrad)

CMS – ATLAS RD collaboration

- Formal CMS support from tracker.
  - Focussed on Phase 2.
- ATLAS: Formal support coming, Informal support clearly there.
- First draft version of RD collaboration document end this week.
  - ~20 pages
  - 6 ATLAS institutes, 6 CMS institutes, 1 CLIC (CERN)
  - 100% hybrid pixel chips in 65nm
  - Institute board
  - Spokesperson(s)
  - Work packages with coordinators
- Discussion meeting ~end next week
  - Document
  - Work packages
  - Collaborators from each institute
  - Etc.
- Final version ~June 1st.
- LHCC presentation June 12/13
- First IB meeting during/after summer
  - Spokespersons, work package coordinators, “detailed” work program
  - MOU:
    - Conditions for sharing (known to be non trivial)
    - Common fund ? (no)
    - Etc.
- Next (first formal) RD collaboration workshop this autumn

Work packages (preliminary)

WP1	65nm technology and radiation hardness
Coordinated Test and qualification for 1Grad TID and 10^{16} neu/cm^2 Extensive radiation tests and report. Transistor simulation model after radiation Expertise on radiation effects in 65nm Other ?	
WP2	Design methodology for large scale mixed signal Pixel ASIC
Integration of analog in large digital design Design and verification methodology for very large chips. Design methodology for low power design/synthesis. Clock distribution and optimization. Other ?	
WP3	Pixel architecture optimization and simulation/verification platform
System Verilog simulation and Verification framework Optimization of global architecture/pixel regions/pixel cells	
WP4	Readout and Control interface
Definition and standardization of readout and control interfaces (e.g use of LPGBT) Definition of control and monitoring functions Implementation of readout and control interfaces in EOC. Include safety system and features for this ? (independent projects ?) Other ?.	
WP5	Analog pixel front-end with charge digitization? (make part of building blocks WP ?)
Define detailed requirements to analog front-end and digitization Evaluate different approaches Make analog front-end block(s) available to collaboration	

WPs (cont.)

WP6	**65nm radiation hard building blocks**
Definition of required building blocks: PLL, references , , Distribute design work Coordinate implementation and test/verification work Make cells available to collaboration	
WP7	Power distribution/conversion/conditioning? (part of building blocks WP ?)
Define and evaluate different power approaches: DC/DC & serial power Coordinate implementation and test/verification of power blocks Make power blocks available to collaboration Other ?	
WP8	Pixel system/chip specification and requirements? (General RD collaboration ?)
Define general requirements to pixel system/ASIC. Other ?.	
WP9	Trigger contribution and impact on system/ASIC ? (global RD collaboration ? or part of architecture optimization WP ?)
Evaluate of pixel contributing to trigger (Physics) Evaluate consequences for pixel system/chip architecture and implementation Define clear requirements to pixel chip Perform detailed simulations (together with WP3)	
WP10	Prototypes coordination and verification ?
Coordination of common MPW submissions Coordination of test an verification of test chips/circuits Coordination of test reports on test chips Other ?	
WPX	Other ?
?	