Possible contribution of Pisa on pixel electronics R&D

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VLSI Competences @ INFN and University of Pisa

- **Design of radiation tolerant digital & mixed mode Integrated Circuits for HEP experiments (IBM 250nm, IBM 130nm, UMC/TSMC 65nm)**
  - **SRAM, ADC (CMS DCU), TX and RX Interfaces to serial links (FF-LYNX) => Magazzu, Saponara, Fanucci**
  - **Front-End (Atlas FE-I4) ASICs => Beccherle**
  - **Associative Memory (Last on Atlas FTK) => Morsani, Beccherle**
  - **Time-to-Digital-Converter in 65 nm UMC for nuclear imaging detectors => Saponara, Fanucci**

Areas of interest

- **High level and VHDL modeling of data processing and data transmission modules (ISE)**
- **FPGA based emulators and test benches**
  - **Validation of protocols**
  - **Test bench for chips using emulators**
- **Digital modules implementing programmable clustering algorithms and data readout**
- **Radiation tolerant IP cores**
  - **TX and RX interfaces to high speed serial links**
  - **Clock Data Recovery modules**
  - **FIFO buffers**
  - **…**
- **Expect one (or more) students to join**

Integrated Simulation Environment (ISE)

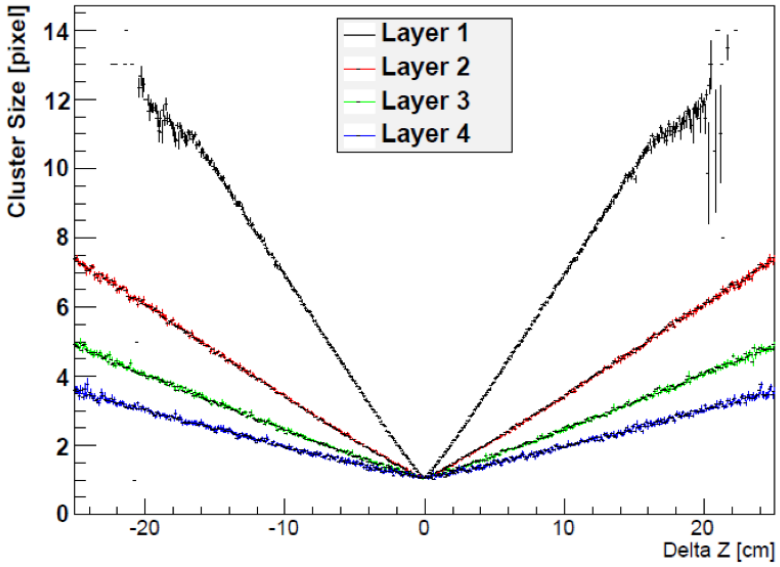
- Input data from physics simulations (GEANT4) performed in the LHC upgrade scenarios
- System-C/HDL models of the components of the TTC/DAQ systems
- Definition of the system requirements (e.g. data rates) and Figures Of Merit (data losses)
- Validation and performance evaluation of algorithms (e.g.: clustering) and readout architectures (e.g.: readout protocols)

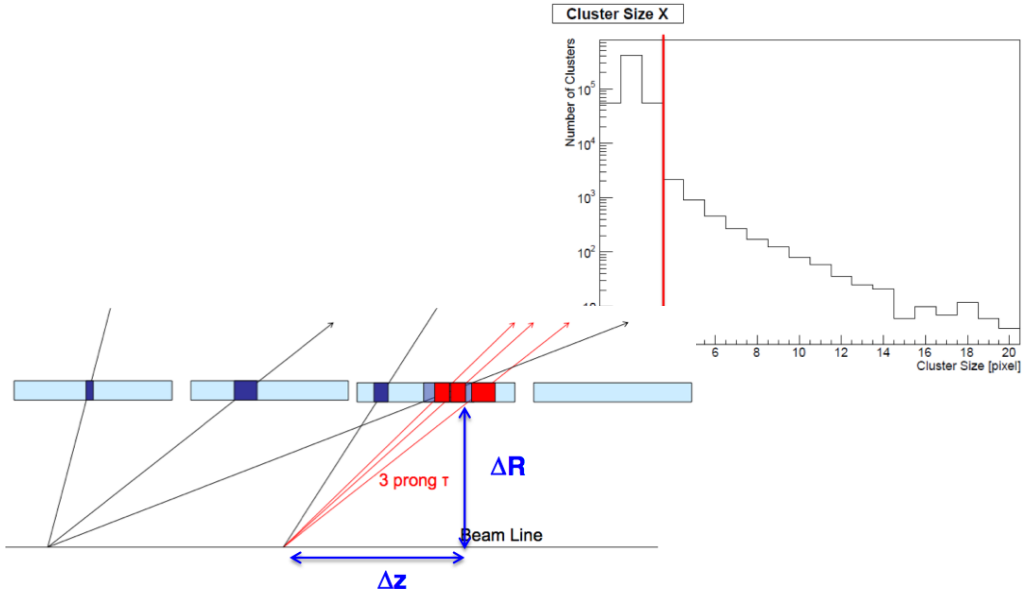
High Speed Serial Links

- **FF-LYNX => Flexible serial protocol for the integrated distribution of the TTC signals and the data readout**
- **TX and RX interfaces to optical and electrical serial links available as IP-cores for FPGA and ASIC (130nm) developments**
  - **Interfaces implementing the FF-LYNX protocol (“double-wire” – 160/320/640 Mbps)**
  - **Interfaces implementing the 8b/10b protocol with Clock & Data Recovery (“single-wire” – 1.2 Gbps in post-layout simulations)**

Physics Simulation

- **Actively working with some (physics) PhD students in studying use cases where pixels could be used in L1-trigger.**
  - **(see https://indico.cern.ch/getFile.py/access?contribId=3&resId=0&materialId=slides&confId=250641 and https://indico.cern.ch/getFile.py/access?contribId=9&sessionId=0&resId=0&materialId=slides&confId=235529)**





Δz = cluster_barycenter - τ_z_production_Vertex