65nm activities in Turin (short status report)

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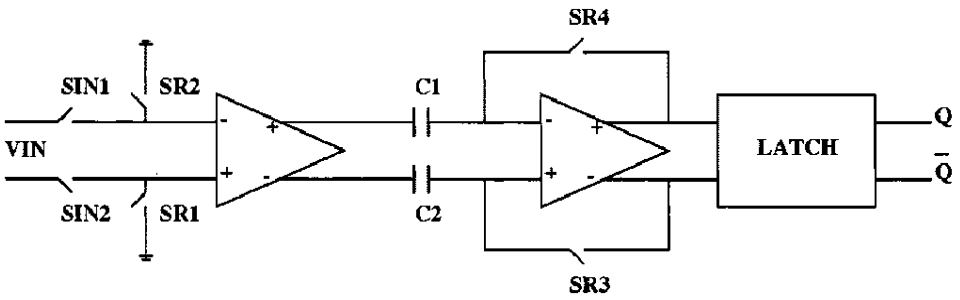
Design guidelines

- we want to design and test a complete front-end analog chain in 65 nm
- try to explore ***innovative options***
  - fast and low threshold ***synchronous*** comparator (discrete time)
  - zero suppressed charge encoding using SAR-ADC
- make a comparison with more 'standard' approaches
  - asynchronous comparator (continuous time)
  - Time over Threshold (ToT) technique
- ***area***
  - most recent CMS Phase-2 pixel size guess: **25 µm x 100 µm**
  - assume **25 µm x 50 µm** for the analog part
- ***power consumption***
  - ***realistic constraints*** for the total analog power consumption becomes essential to ***fix DC bias currents***
  - assume a total power consumption per unit area < 0.4 W/cm^2
  - < 10 µW /pixel (50% analog + 50% digital... is this realistic?)
  - ***< 5 µW /pixel*** for the analog part → ***~ 4 µA total bias current (static current) !***
  - ~1 µA per branch work fine (OK with ***weak*** and ***moderate inversion*** operating transistors)
  - the power contribution from a 5-bit SAR-ADC per pixel should not be a problem if a ***zero suppression scheme*** is adopted (= decide and digitize → ~1 conversion cycle every 10 µs, 100 kHz)
- our goal: plan a submission before the end of 2013

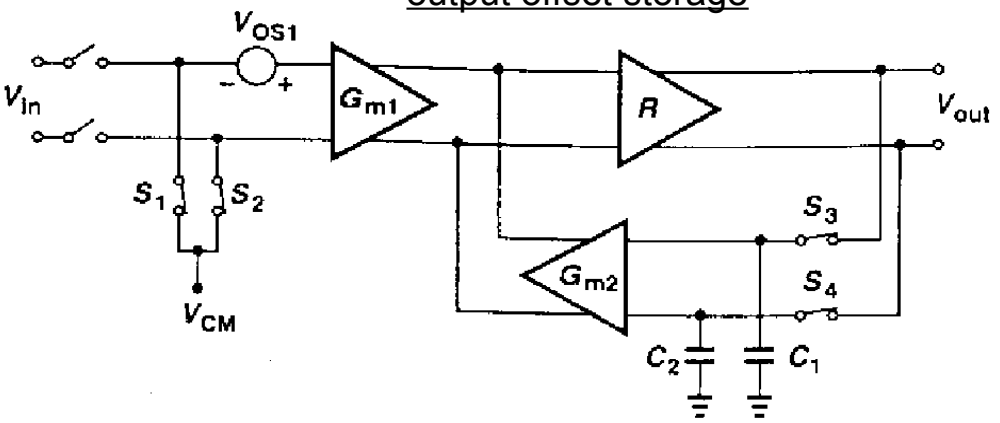
Comparator designs

- we want to explore ***two different comparator designs***
  - continuous time approach
  - discrete time (track-and-latch) @ 40 MHz clock (BX) → now optimizing the previous design
- both designs would employ ***self offset compensation techniques*** (autozeroing)
  - usage of input + output offset storage [1,2]
  - local trimming with DACs is no more required → no more configuration registers and SEU protections
  - we are considering to do the offset compensation for each bunch crossing
- try to exploit ***all transistor options*** available with the 65 nm PDK (high Vt, low Vt transistors etc.)

input + output offset storage



output offset storage

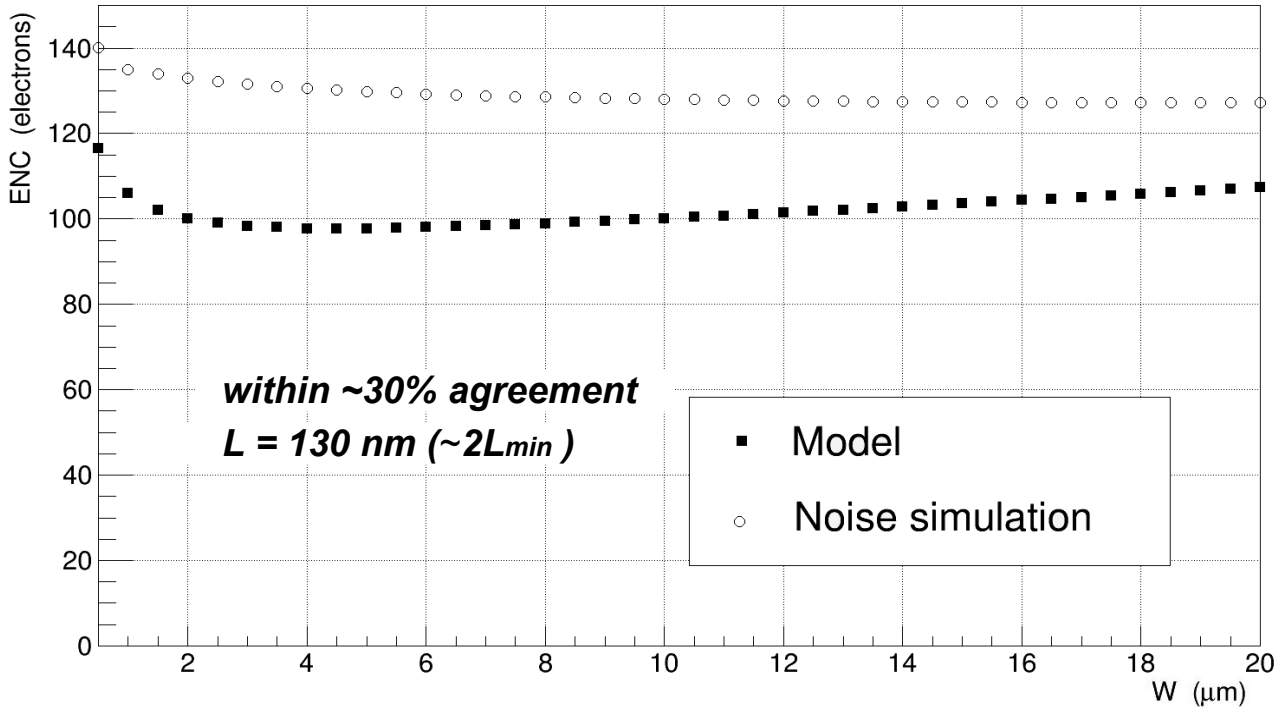


[1] F. Brianti, A. Manstretta, G. Torelli, *High Speed Autozeroed CMOS Comparator for Multistep A/D Conversion*

[2] A. Rivetti, G. Anelli, G. Mazza and F. Rotondo, *A Low-Power 10-bit ADC in a 0.25-μm CMOS: Design Considerations and Test Results*

Very front-end preliminary studies

- preliminary studies on the very front-end stage are required to get a realistic estimation of the ***total RMS noise*** fed to the comparator
- getting started exercises with the ***very front-end input stage*** (E.Monteil – master thesis)
  - deep n-well nmos input device + cascode stage + ideal CR-RC2 shaper (12.5 ns peaking time)
  - optionally *gm* enhancement using current splitting techniques
  - systematic studies on *ENC* by varying the input device aspect ratio (100 fF input capacitance)
  - compare simulation results with standard theoretical predictions [1,2]



[1] C.C. Enz F. Krummenacher and E.A. Vittoz, *An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications*

[2] P.O'Connor, G. De Geronimo , *Prospects for Charge Sensitive Amplifiers in Scaled CMOS*

Next steps

- **continue on comparator architectures studies and optimizations**
- **exploring options for the very front-end stage**
- **getting ready as soon as possible with a complete schematic design (comparator + ADC)**
- **then move to layout**