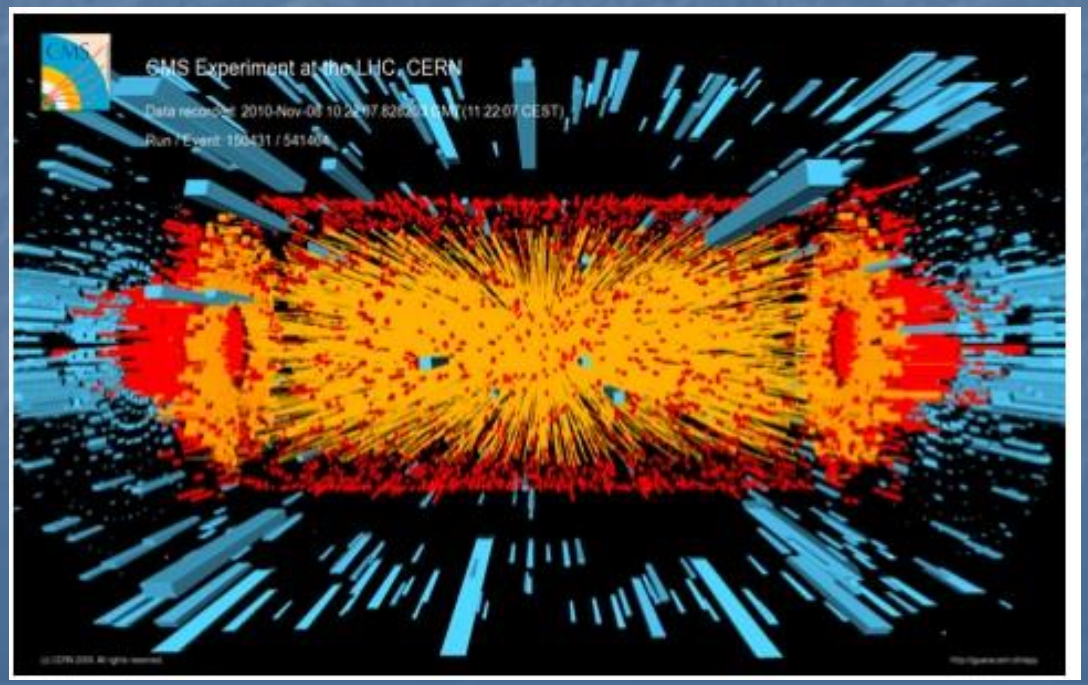
Electronics for HL-LHC trackers

NB: Only considering silicon trackers

Jorgen Christiansen CERN/PH-ESE

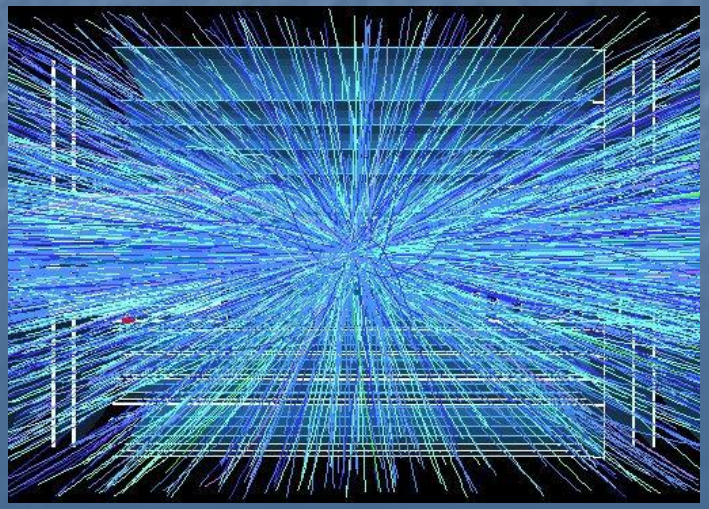
Acknowledgements to all my tracker colleagues from near and far



Typical HL-LHC event x 40MHz

Tracker electronics challenges

- Highest particle rates of all sub-detectors in HEP experiments
  - **Extremely high hit rates: Up to 1-2GHz/cm^2**
  - **Extremely high radiation: Up to 1Grad, 10^{16} Neu$_{eq}$/cm^2**
  - Enormous amounts of data to read out
- High spatial resolution and track separation: ~10-100um
  - Extremely high channel density
  - **Extremely high integration of electronics**
- Large hermetic detectors
  - Pixels: 0.1–10m^2 , 0.1 - **25 Billion channels**
  - Strips: ~**200m^2** , ~100 Million channels
  - Must be affordable for large surfaces
- Must not disturb traversing particles
  - Low mass
  - Thin detectors –> Small signals –> Low noise
  - **Lowest possible power - cooling**
- High magnetic field: 1 – 4 T
  - No Ferromagnetic inductors
  - Non magnetic materials
- Limited (no) access as in centre of experiments
  - Highly reliably and long lived (10 years)
- Increased trigger rate and latency
  - Local storage requirements and high rate readout
- Participation in first level trigger(s) (new)

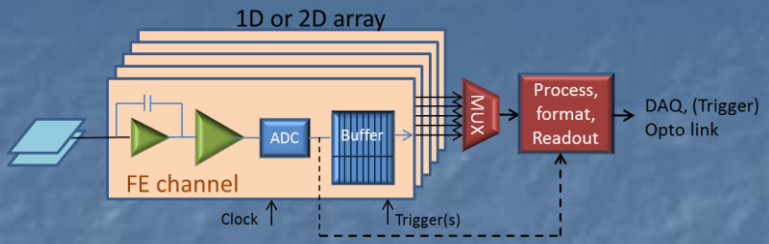


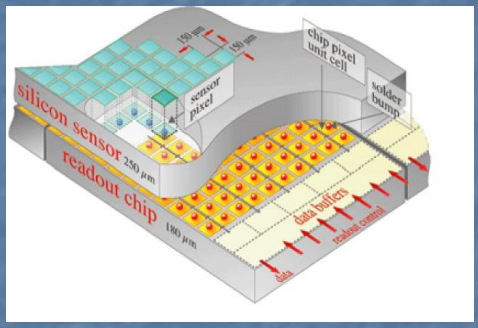
On-detector electronics 100% custom made with highly specialized complex ASICs that must work reliably in unprecedented hostile radiation environments for many years.

Ever increasing fusion (merging/integration) of sensor and its electronics.

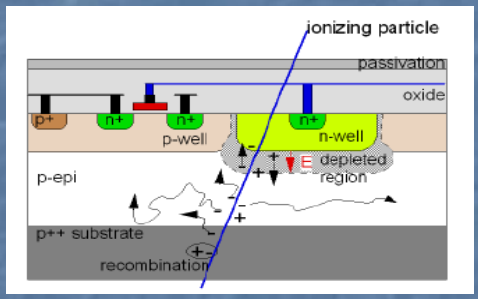
Tracker electronics

- Typical tracker front-end channel chain
  - **Front-end ASIC**
    - Low noise pre-amp + shaper
    - Digitization
      - Binary: Discriminator
      - Charge digitization (4-8bit): ADC or TOT
    - Synchronization to correct bunch clock
    - (send data to trigger system)
    - Buffering during trigger latency
    - Extraction of triggered events
    - Data merging/formatting/compression
  - **Readout/control via optical link**
  - **DAQ interface and trigger**
  - **Power distribution system**
- Strips
  - Linear array of channels (128 – 256 per FE chip)
- Hybrid pixels
  - 2D array of channels (~100k per FE chip
- MAPS: Monolithic Active Pixel System
  - 2D array of detector and channels (~100K per FE chip)

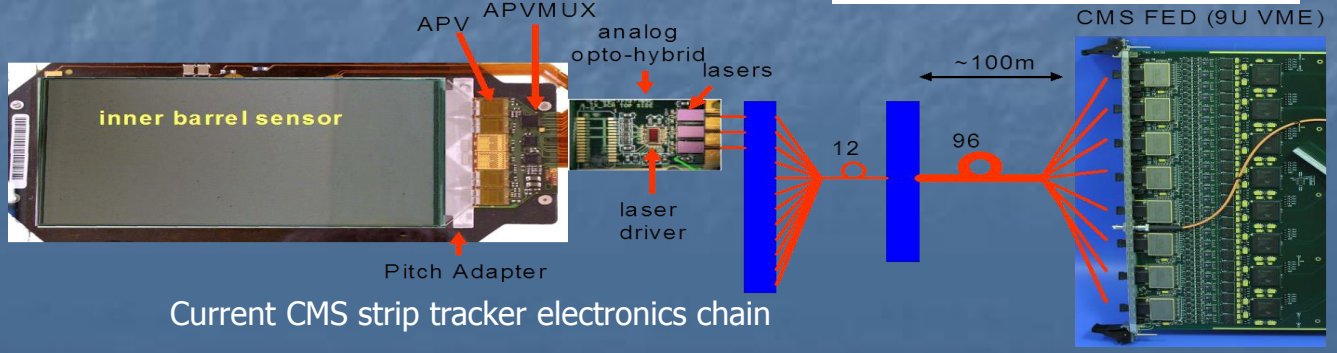




Hybrid pixel



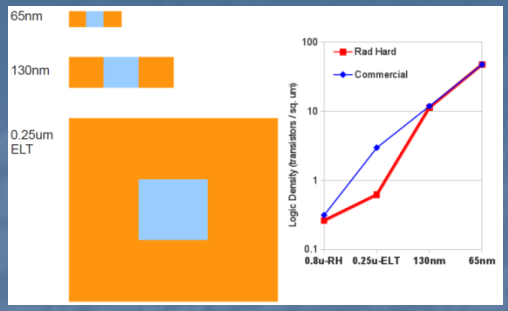
MAPS



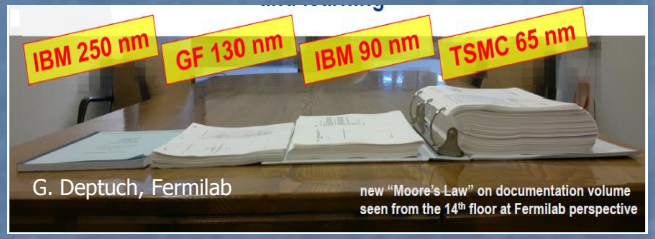
Current CMS strip tracker electronics chain

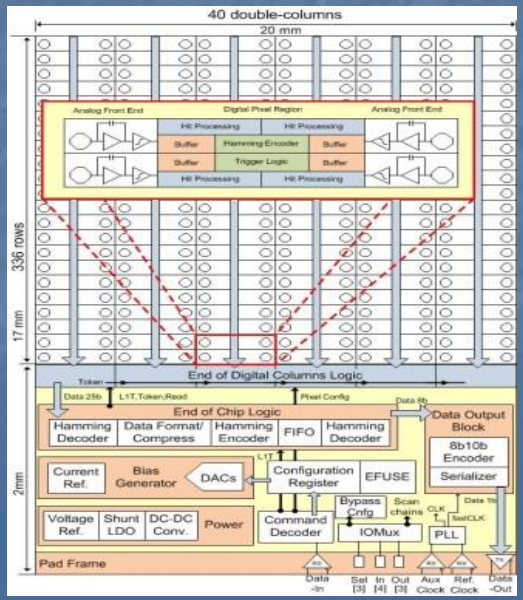
Tracker ASICs

- The use of appropriate ASIC technologies is critical
  - Radiation tolerance, Density, Mixed signal (analog/digital)
- Assured access and support is critical
- Long term availability
  - LS2 (ALICE/LHCb) : Designs on-going – Production 2014-2015
  - LS3 (ATLAS/CMS): R&D started – Production 2016-2020
- Assemble appropriate design teams (technology, analog, digital, tools, radiation, links, tracker systems, etc.) for large complex ASICs across participating partners.
  - Next generation (pixel) ASICs have more channels and complexity than complete HEP experiment a few decades ago.
    - **We are approaching the 1Billion transistor ASICs**
  - **Technologies are increasingly complicated to use.**
  - **The HEP ASIC design community is largely distributed with only few major design centres.**
  - Collaborative examples: FEI4 (ATLAS IBL), ABCN (ATLAS Strip), RD53 (ATLAS/CMS pixels)
- The R&D phase for next generation tracker ICs is long and costly: Manpower, expertise, tools, submissions, test facilities, radiation qualification, test beams, etc.
  - **Significant R&D manpower/resources are needed early in the project (where funding is often scarce)**
  - Do we have time and resources to consider the use of more advanced technologies (<65nm) ?.
  - Production is cheap and fast.

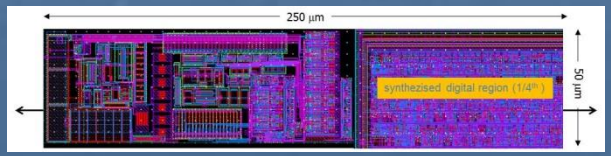


Effective density for radiation applications
M. Garcia-Sciveres, LBNL





FEI4 pixel chip for ATLAS IBL



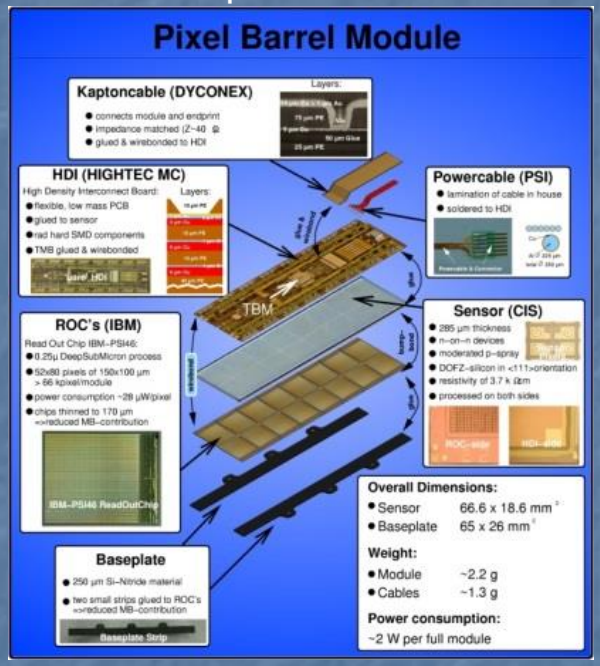
ASIC technologies for trackers

	350nm (HV)	250nm	180nm (imager)	130nm	65nm
ATLAS pixel IBL (LS1)				Pixel chip	
CMS pixel (LS1-LS2)	DC/DC	Pixel chip			
Alice ITS (LS2)	(DC/DC)		MAPS	GBT link	
LHCb Vertex & UT (LS2)	(DC/DC)		LS 2 upgrades	Pixel chip + Strip chip + GBT link	
ATLAS strips	(DC/DC)			Strip chip	Link
CMS TT	DC/DC		LS3 strips	Strip chip	Pixel chip Link
ATLAS/CMS pixel RD53	DC/DC			LS3 pixels and links	Pixel chips Links

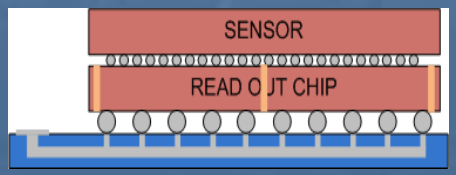
Interconnect and packaging

- Increased channel densities makes High Density Interconnect (HDI) technologies increasingly critical
  - Connection between sensor and front-end chip
  - Assembly of FE chips on module
- Wire bonding on large scale on large modules
  - ATLAS Strip module/stave, CMS TT strip modules, LHCb
  - Industrial standard but not necessarily for the module sizes used in HEP
  - HEP community has several centres with wire bonding capability/experience
- Bump bonding
  - Coarse bump bonding: Industry standard for flip-chip
    - CMS TT pixel modules, ALICE pixel staves
  - Very fine pitch bump bonding: Not (yet) industrial standard
    - LHCb/ATLAS/CMS hybrid pixels: Sensor to FE chip
    - Special contracts with specialized companies/R&D centres and/or In house HEP
- Through Silicon Via (TSV) and coarse bump bonding
    - Difficult access: R&D level within silicon industry, Our volume is small
    - Option for CMS TT pixel module and ATLAS/CMS pixels
- Interconnect is one of the main production cost drivers for large trackers
  - **Expensive in both R&D and production phase**
- Getting access to modern interconnect technologies from the micro electronics industry is difficult
  - **Packaging and interconnect industry is highly volume (and cost) oriented**
    - Small "one off" client with difficult requirements and long project schedules
    - No "Europractice & MPW" in interconnects and packaging
  - **We (HEP) will need to have centre(s) of excellence in this domain and community/frame/R&D contracts with a few industrial partners**

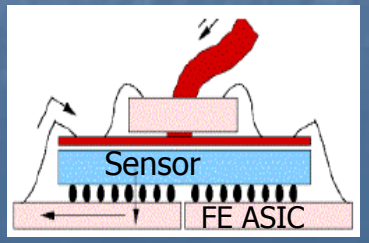
CMS pixel module



Use of TSV

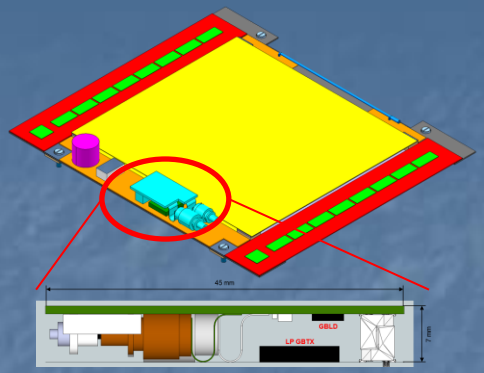


Combined bump bonding and wire bonding

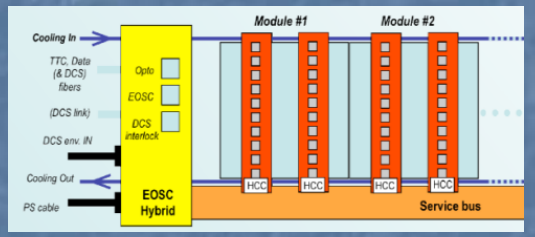


Data/optical links

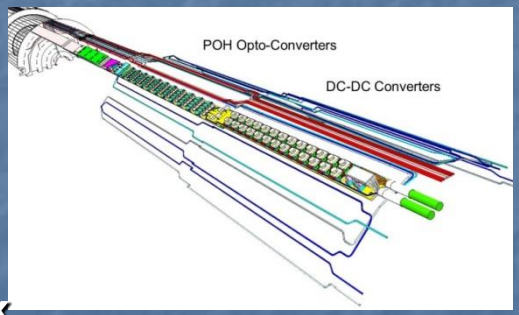
- Tracker Requirements:
  - **High radiation tolerance**: 1Mrad (ALICE ITS) – 1Grad (ATLAS/CMS pixels)
  - **One link does all**: readout, clock, trigger, trigger data, control/monitoring
    - Very high SEU immunity
    - (Safety/protection system assumed separate)
  - **Increased data rates**: Hit rates (~10) x Trigger rates (~10) = **~100x !**
  - **Low mass, low power, small form factor, reliable, long-lived, etc**.
- Use of standardized (very) rad hard links (where ever possible)
  - **Common development: Flexibility and support for specific tracker needs**
- LS2: ~5(3.2)Gbits/s GBT link in 130nm: Under final testing
  - LHCb vertex: Outside vacuum, Modest radiation
  - ALICE ITS: Connection to MAPS, very small space, Modest radiation
- LS3: Low power GBT ~10Gbits/s in 65nm: To be defined & designed
  - ATLAS & CMS "strip": < 100Mrad
    - **Optical link within tracker volume**
    - Collect data from multiple sources (FE chip or modules) and control "fanout".
      - CMS TT: **1 link per module**
      - ATLAS strip: **1 link per tracker stave**
  - CMS/ATLAS pixels: ~1Grad
    - Optical link can most likely not survive radiation environment: Opto , High speed
      - **Opto link located few (2-10) meters from pixel modules**
      - **High speed and low power electrical links critical to get data out of pixel volume**
    - Links per module: 2 – ¼ (depending on location/layer)
- **Tracker upgrades relies critically on APPROPRIATE optical link**
  - Radiation tolerance, link speed, Low power, front-end chip interface
  - Significant efforts will be required to define, develop, test and qualify, support next generation link (LPGBT) appropriate for LS3 tracker upgrades



CMS TT with opto link per module



ATLAS strip with opto link per stave

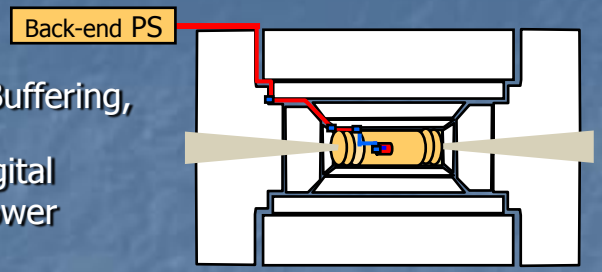


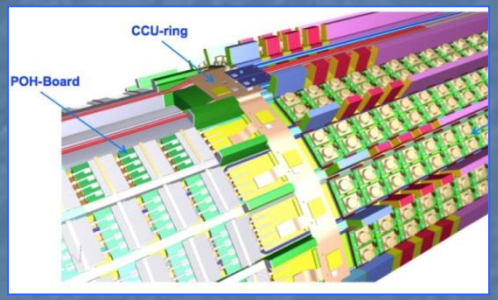
Pixel with displaced optical link and DC/DC (CMS phase 1 pixel)

Power-cooling-integration

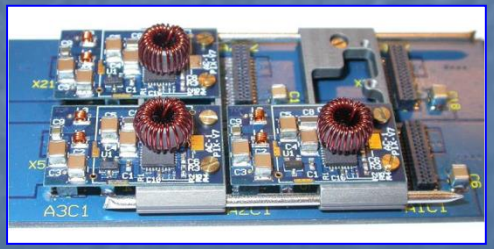
- Power optimized electronics critical for trackers
  - Low power technology: Deep submicron ASICs
  - Architecture optimization: Segmentation, ADC/binary, Triggering, Buffering, Readout bandwidth, etc.
  - Circuit optimization: Low power low noise analogue, Low power digital

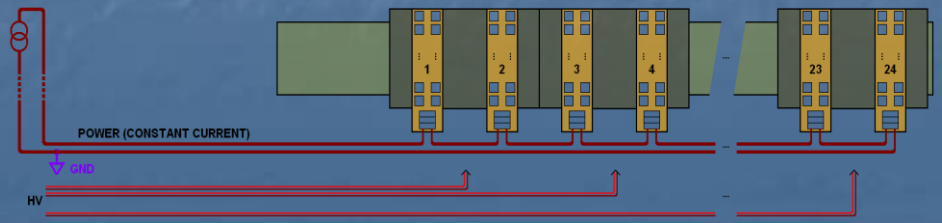
  Significantly increased performance requirements do not favour low power
- Power densities and cooling
  - Hybrid pixels: 0.5 – 1.5W/cm^2 (Extremely high rates)
    - Uniform high power density over full "small" detector –> CO2 cooling
  - Strips: ~0.05W/cm^2 (High rates)
    - Localized heat sources distributed over large detector -> CO2 cooling
  - MAPS (ALICE ITS): ~0.05W/cm^2 (modest rates but high event multiplicity)
    - Uniform low power density -> Low material cooling systems under investigation
- Low voltage power distribution critical for trackers.
  - Low power -> Low voltage ASICs ~1V -> High currents -> High cable losses
  - Highly power optimized digital designs have high power transients
  - Associated power control/monitoring and safety systems
- Active power distribution required within detectors
  - **Power conversion in very high radiation and magnetic fields**
    - **DC/DC conversion (common development)**
    - **Serial powering (project specific)**
  - Optimization of power conversion on module versus cable losses
- Hard to define/guess power/cooling needs early in project phase





DC/DC for CMS pixel phase1

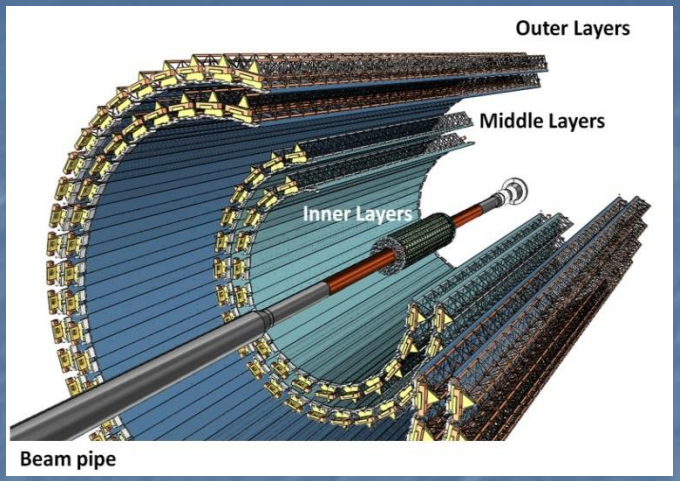


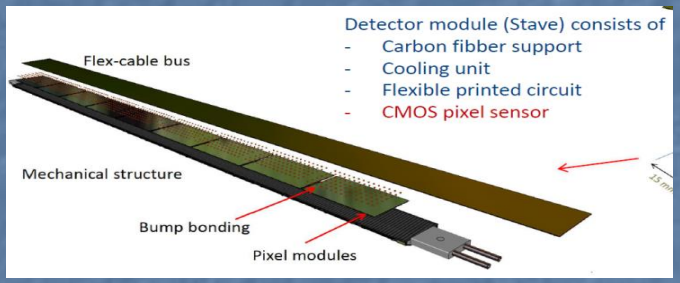


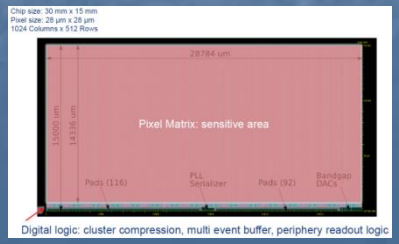
Serial powering as proposed for ATLAS strips

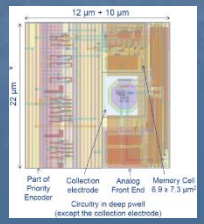
Alice inner tracker upgrade

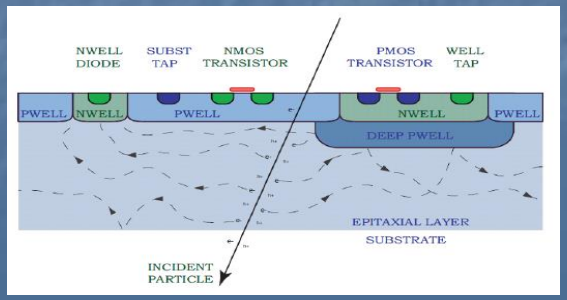
- **Novel MAPS** based tracker system for LS2
  - Replaces 3 tracking detectors: Pixel, Strips, Silicon drift
  - High track multiplicity of 115/cm^2 per event at 50KHz interaction rate : 5MHz/cm^2 (inner layer)
- Detector – Front-end - Interconnect
  - 22 x 22 um^2 MAPS: Binary
  - 10 m^2, 25k 15x30mm^2 Pixel chips, **25G pixels**
  - **Modest radiation**: < 1Mrad , < 10^{13} 1Mev n_{eq}/cm^2
    - **Enables use of MAPS**
  - **180nm CMOS imager sensor technology**
  - **Status: Design and testing on-going**
- Module/stave Interconnect:
  - **Bump bonding of thinned chips** (50um)
- Readout:
  - Event trigger (50KHz): **<1Gbits/s per pixel chip**
  - Electrical links to intermediate patch panel
- Power:
  - **Aims at very low power consumption**: ~50mW/cm^2
  - DC/DC ?







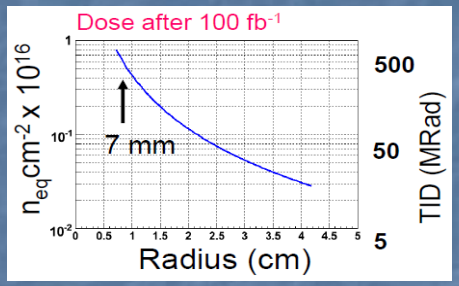


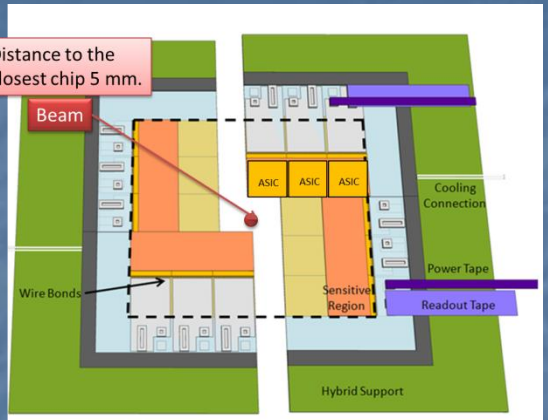


LHCb Vertex pixel

- Detector:
  - 55 x 55um^2 hybrid pixel
  - 0.14 m^2 , 26 stations, 600 Pixel chips
  - **In vacuum 5mm from beam**
  - Open detector (access)
  - **Radiation**: <400 Mrad
    - **Highly non uniform**
    - Factor 40 across module.
      Factor 7 across pixel chip.
  - Installation: LS2

Non uniform radiation





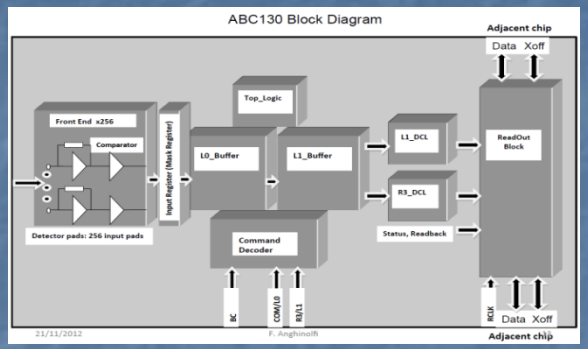
Vertex pixel station

- Front-end: Binary/(TOT)
  - **130nm pixel chip based on Medi/Time-pix3 chips**.
  - **Trigger less: Very high readout rates, no latency buffering**
  - **Status: Design on-going**
- Interconnect:
  - Sensor: Fine pitch bump bonding
  - Module: Wire-bonding
- Readout:
  - Trigger less: **Up to 20Gbits/s per pixel chip**
  - Electrical links out of vacuum to optical links
- Power:
  - DC/DC outside vacuum tank
  - CO2 cooling with small tubes or micro channels
- Off-detector: Standardized LHCb readout board ATCA40

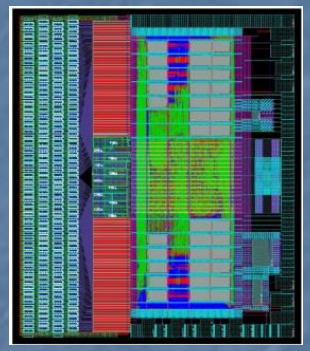
LHCb readout board: ATCA40, CPPM

ATLAS strip detector

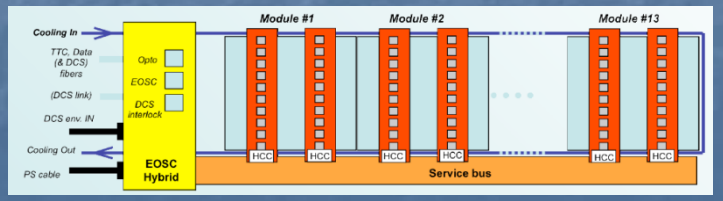
- Detector
  - Inner: Short strips, Outer: Long strips
  - **200 m²** (Replace current SCT and TRT)
  - 300k FE chips, 75M channels
  - Radiation: <25Mrad
- Front-end: Binary
  - 130nm 256 channel chip for both short and long strips
  - **Two level trigger with Region Of Interest (ROI) readout**
    - L0: 500kHz , 6us, 10% ROI
    - L1: 200KHz, 20us (max 256 events)
  - Status:
    - Initial 250nm version made and extensively tested on strip modules
    - **130nm version just submitted: Collaboration between 7 institutes**
- Interconnect:
  - Wire bonding: Sensor to FE chip and Front-end chip to hybrid
  - **Status: Short stave prototypes tested in test beams with 250nm chip**
- Readout
  - **1 (2) LPGBT link at end of stave**
  - 320Mbits/s electrical links from module to end of stave
  - Module controller merging data (design on-going)
  - 160Mbits/s electrical links on module
- **Power: Two approaches being evaluated**
  - A. Serial power at module level
  - B. DC/DC converter per module

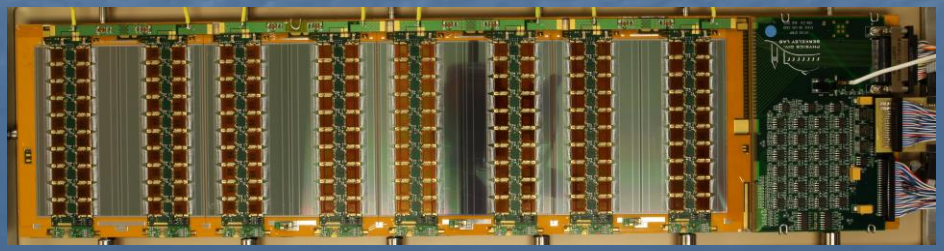


130nm FE chip



Stave concept

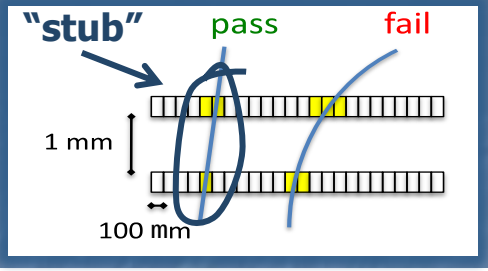


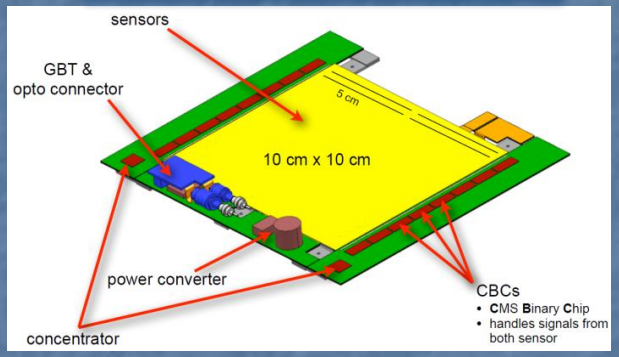


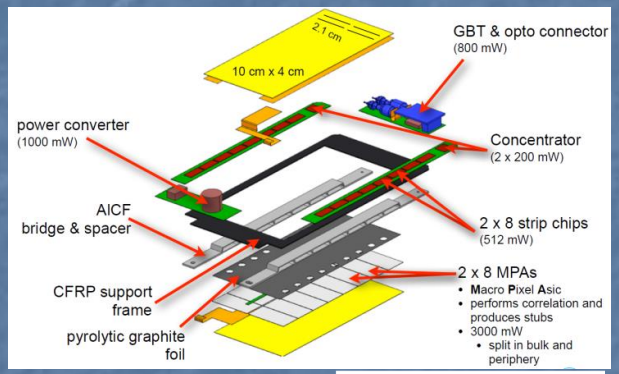
Short Stave prototype with 250nm FE chip

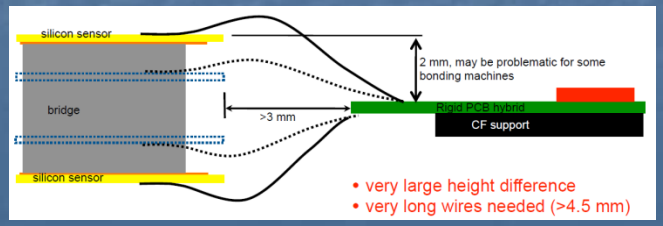
CMS track trigger

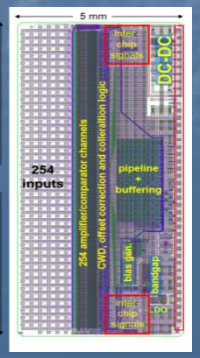
- Tracking and **track trigger function** (high Pt candidates)
- Detector
  - **Outer 2S** : Double layer strips with Phi coordinate and Pt cut
  - **Inner PS**: Strips + pixels for Phi and Z coordinate and Pt cut
  - **200 m²**
  - Radiation: <100Mrad
- Front-end: Binary
  - 2S: **130nm 256 channel strip FE chip (CBC) and module controller**
    - **2nd version of CBC under test on double strip module**
    - Module controller chip architecture definition and design on-going.
  - PS: **FE pixel chip in 65nm**
    - Architecture defined and design on-going
- Interconnect:
  - Wire bonding strips to hybrid
  - Bump bonding FE chip to hybrid
  - Bump bonding pixel sensor to pixel chip
  - **Option of Through Silicon Via (TSV) for pixel modules**
- Readout
  - **1 link (10G) per module**
    (high Pt trigger data plus 1MHz trigger)
- Power: **Independent DC/DC per module**

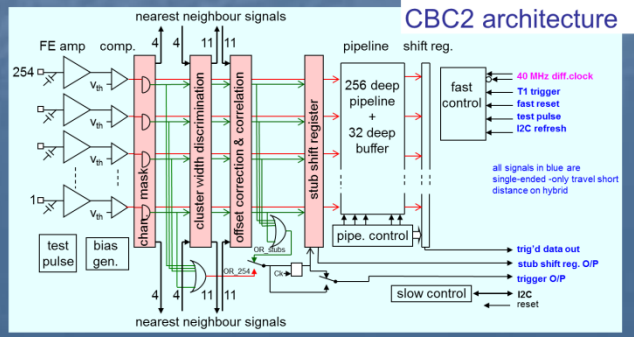






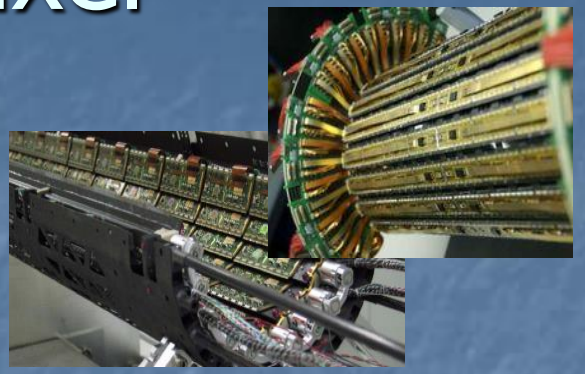




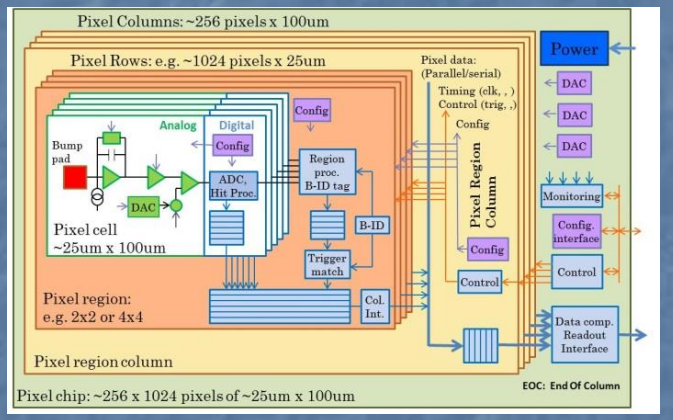


ATLAS and CMS pixel

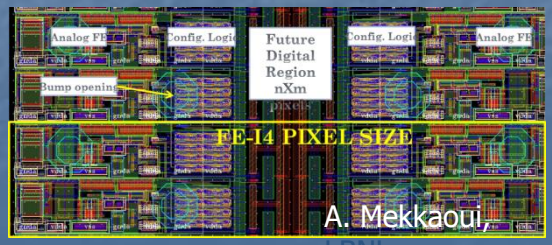
- Hybrid pixel detectors
  - **Extreme radiation levels: 1Grad, 10^{16} neu/cm^2**
    - **Parts of detector may need replacement after few years**
  - **Extreme rates: 1-2GHz/cm^2**
  - **Small pixels**: Double track resolution, Spatial resolution
    - Pixel size will probably be determined by front-end ASIC: ~25 x 100 um^2
    - Extensive processing/storage needed within pixel array
- Pixel chip
  - Extreme radiation hardness, mixed signal, Very high density
  - **Large chip ~2 x ~2 cm^2** to efficiently build pixel detector modules
  - **~1Billion transistors**, 100x more storage than in previous generation
  - **65nm technology: Radiation hardness to be confirmed**
    - Initial test chips: Radiation test structures, Small ATLAS & LCD pixel arrays
  - **RD53 collaboration**: Technology, circuits, architecture, tools, qualification
    - **Common platform** to make pixel chips for the two experiments + LCD
    - **100 collaborators** and more coming
- Interconnect
  - Fine pitch bump bonding: To be developed, verified and cost optimized
  - Wire-bonding for module assembly
    - Option of TSV to bring IO and power to back side of pixel chip
- Readout
  - **100x readout rate: ~10Gbits/s link required per pixel chip (inner)**
  - **Opto parts can most likely not survive within pixel volume:**
  - **Low power, low mass cable, high speed electrical links to intermediate opto link**
- Power distribution
  - **High power density and hostile radiation environment makes serial powering the most realistic option**
    - Requires R&D and qualification
    - Option: Combination with DC/DC (e.g. **on-chip switched capacitor**)



Current ATLAS and CMS pixels



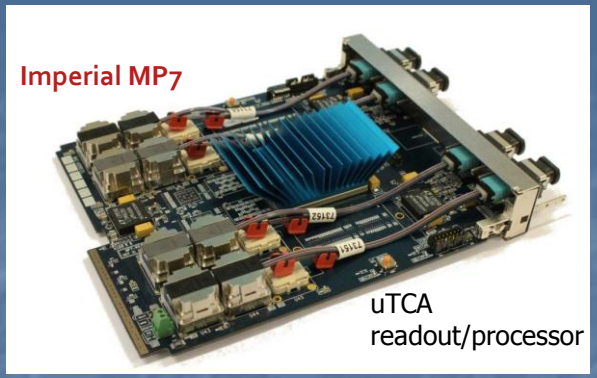
Generic phase 2 pixel chip architecture

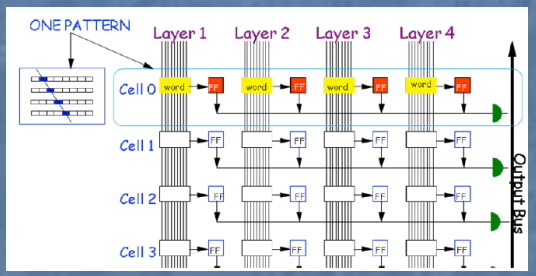


ATLAS pixel prototype in 65nm

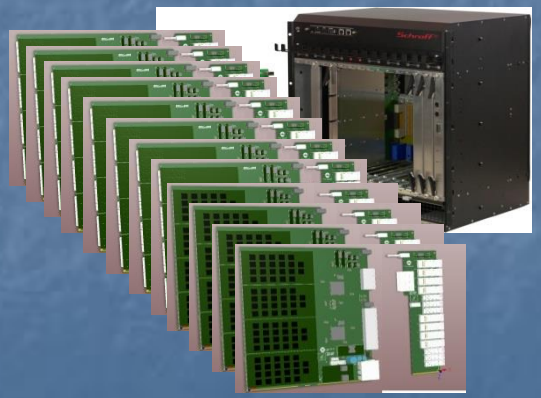
Off-detector

- HV and LV power supplies: Parts in caverns
  - Power supplies (Radiation tolerant) to be developed with industrial partners when possible
    - Only few companies have expertise on rad tol power supplies (at affordable cost)
  - Configuration depends on power distribution scheme
- DAQ (and control) interface: In counting house
  - Many (10-100) optical front-end links:
    - Transceivers for rad hard optical front-end links
  - High end FPGA's for link interface and processing.
  - Standardized interface to DAQ/control system (e.g. GBE)
- Fast track trigger
  - CMS: L0 trigger at 40MHz within 10us
  - ATLAS: L1 trigger at 500KHz within 20 us.
  - Complex pattern recognition/matching over very large channel counts with short latency and no dead time (clock/event pipelined).
    - Highly challenging connectivity and processing problem
      A. Massive use of custom made associative memories. High end ASIC technology (65nm and below), no radiation
      B. FPGAs, Graphics processors, ?





Associative memories for pattern matching



Fast track trigger crated based on massive use of custom made associative memories

System integration and design

- The design and construction of tracker (electronics) is a complex interplay with very challenging requirements and requires delicate optimization of multiple technologies, architectures and detailed design choices.
  - The design of the ASICs is on the critical schedule path but this work must be done in close synergy with all the system aspects: Physics, Tracking, Triggering, Layout/mechanics, Cooling, Powering, Readout, etc.
  - Extensive test and qualification (e.g. radiation) must be performed before electronics can be considered ready for production.
  - System production/assembly/test long and delicate as the final system is the first full "prototype" that must work reliably for 10 years without repair in extremely hostile radiation environment.

Relative challenges

Detector	Surface	Hit rates/ radiation	Channel Density	Trigger latency	Trigger rates	New features	Readout rates	Material
CMS/ ATLAS pixels	**~2 x** 4–8m^2	**10 x 1GHz/cm^2 1Grad 1 10^{16} neu**	**4 - 8 x** ~25-50 x 100-150um^2	**8 x** 10 - 20us **80x storage**	**~10 x** 1MHz(CMS) 500KHz (ATLAS)		**~100x 2Gbits/ s*cm^2**	~1 x
CMS TT Strips + Pixels	~1 x **200m^2**	10 x 100Mrad	2x strips 100xPix.	8 x 10us (20us)	10 x 1MHz	**Track trigger**	~100x	<~1 x
ATLAS strips	**~4 x 200m^2**	10 x 25Mrad	4 x	4 x L0 6us, L1 20us.	2 (5) x L0: 500KHz L1: 200KHz	**Two level buffer with ROI**	~10x	<~1 x
LHCb Vertex	1 x 0.1 m^2	4 x **400Mrad non uni.**	1000x 55x55um^2 Strips to pixels		**40 x 40MHz**	**Trigger less**	~100 x **10Gbits/ s*cm^2**	~1 x
ALICE MAPS	**10m^2**	5MHz/cm^2 1Mrad	**22x22 um^2**		50KHz	**MAPS**	0.2Gbits/ s*cm^2	**~1/3**

Summary/conclusions

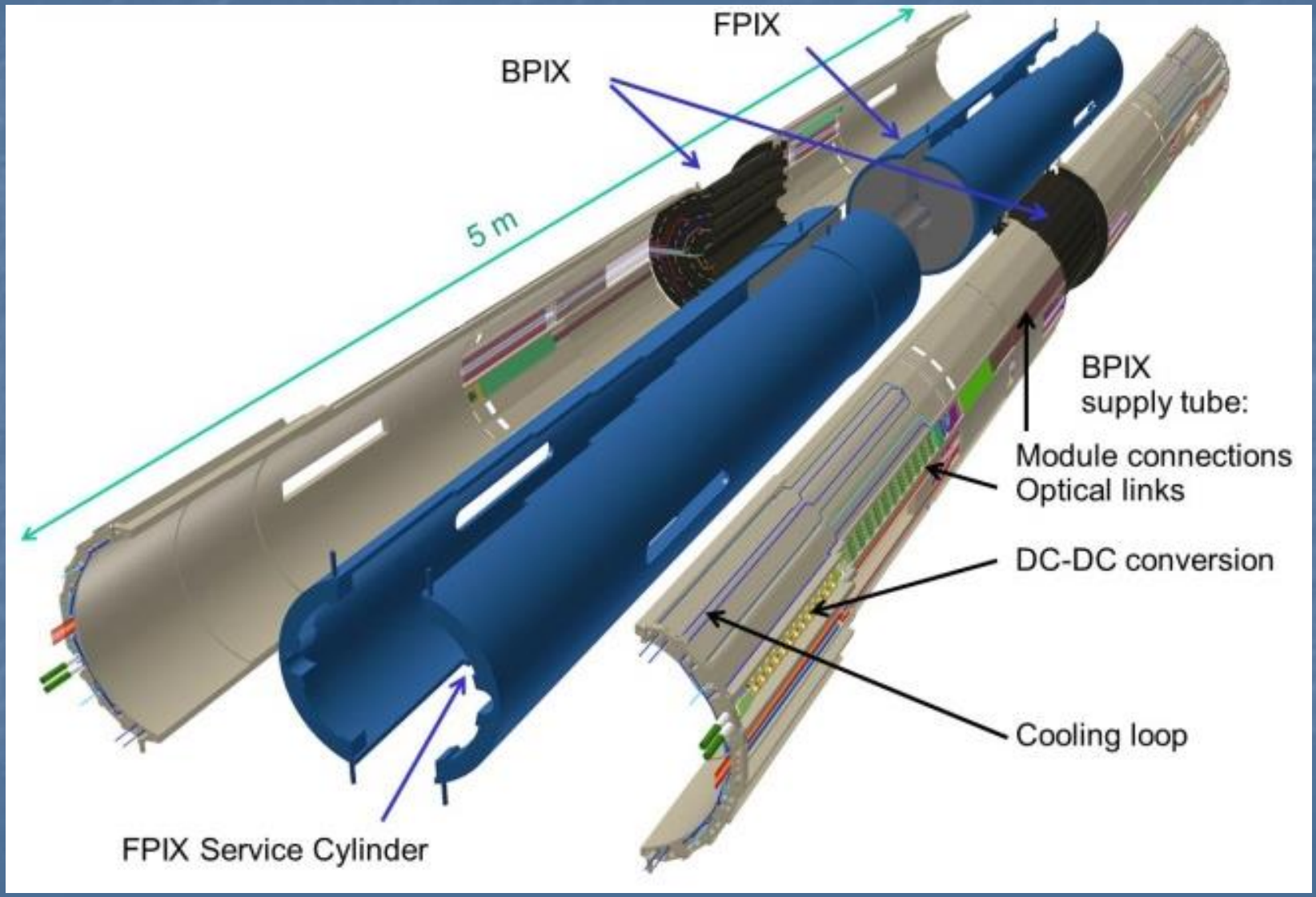
- The development of tracker electronics with unprecedented performance requirements for the HL-LHC requires delicate and complex optimization across many technologies and disciplines and the electronics is one of the major ingredients.
- The LHC experiments have conceived viable and highly optimized tracker system upgrades for the extremely challenging HL-LHC conditions
  - Significant electronics engineering resources will be required to develop, verify and build these trackers
  - A lot has been learned from the current very well working trackers
- Large, complex, low power, radiation hard, mixed signal ASICs are critical
  - Resources for their development are needed early in the project phase.
  - Manpower must be appropriately organized and trained
    - Collaborative efforts across multiple institutes and when possible across experiments.
  - Centralized technology access, support, tools, radiation qualification, etc. critical to enable small design teams across many institutes to develop such IC's
- Common and appropriate (e.g. rad hard) building blocks critical:
  - Low power 5 & 10Gbits/s optical links appropriate for use in trackers
  - Power conversion,
- Access to high density packaging and interconnect technologies required for the integration of tracker systems and their production (cost)
  - Industrial partners
- Fast and complex off detector electronics critical for track triggers.

Backup slides

What has not been mentioned

- 3D ICs:
  - Not to confuse with 3D transistors, 3D and 2 ½D packaging, 3D sensor
  - Can potentially offer very integrated solutions
  - Problems of availability, maturity, yield and access
  - Not currently part of baseline solutions
- Options of using <65nm
  - Could bring significant advantages for pixels systems
  - Radiation tolerance ?
  - Track triggers with associative memories (no radiation)
  - Does time and funding allow this ?
- Use and integration of Micro channel cooling.
- Safety systems (normally independent from front-end system)
- TPC of ALICE (tracking)
- LHCb fiber tracker and upstream silicon strip tracker

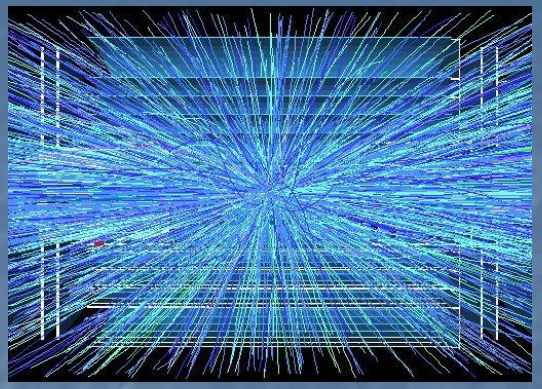
Pixel services

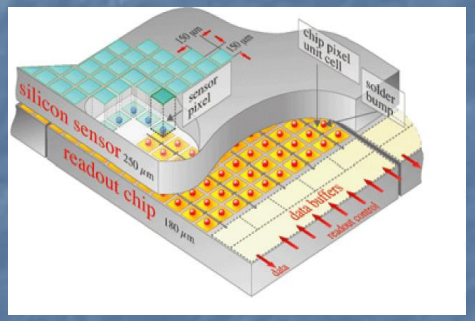


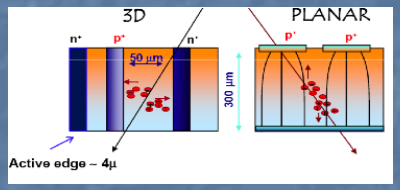
Phase 2 pixel challenges

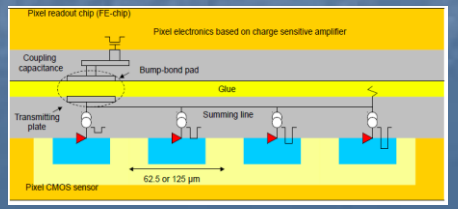
- ATLAS and CMS phase 2 pixel upgrades very challenging
  - Very high particle rates: 500MHz/cm^2
    - Hit rates: 1-2 GHz/cm^2 (factor 16 higher than current pixel detectors)
  - Smaller pixels: ¼ - ½ (25 – 50 um x 100um)
    - Increased resolution
    - Improved two track separation (jets)
  - Participation in first/second level trigger ?
    A. 40MHz extracted clusters (outer layers) ?
    B. Region of interest readout for second level trigger ?
  - Increased readout rates: 100kHz -> 1MHz
  - Low mass -> Low power

  Very similar requirements (and uncertainties) for ATLAS & CMS
- Unprecedented hostile radiation: 1Grad, 10^{16} Neu/cm^2
  - Hybrid pixel detector with separate readout chip and sensor.
  - Phase2 pixel will get in 1 year what we now get in 10 years
- Pixel sensor(s) not yet determined
  - Planar, 3D, Diamond, HV CMOS, , ,
  - Possibility of using different sensors in different layers
  - Final sensor decision may come relatively late.
- Very complex, high rate and radiation hard pixel readout chips required









ATLAS HVCMOS program

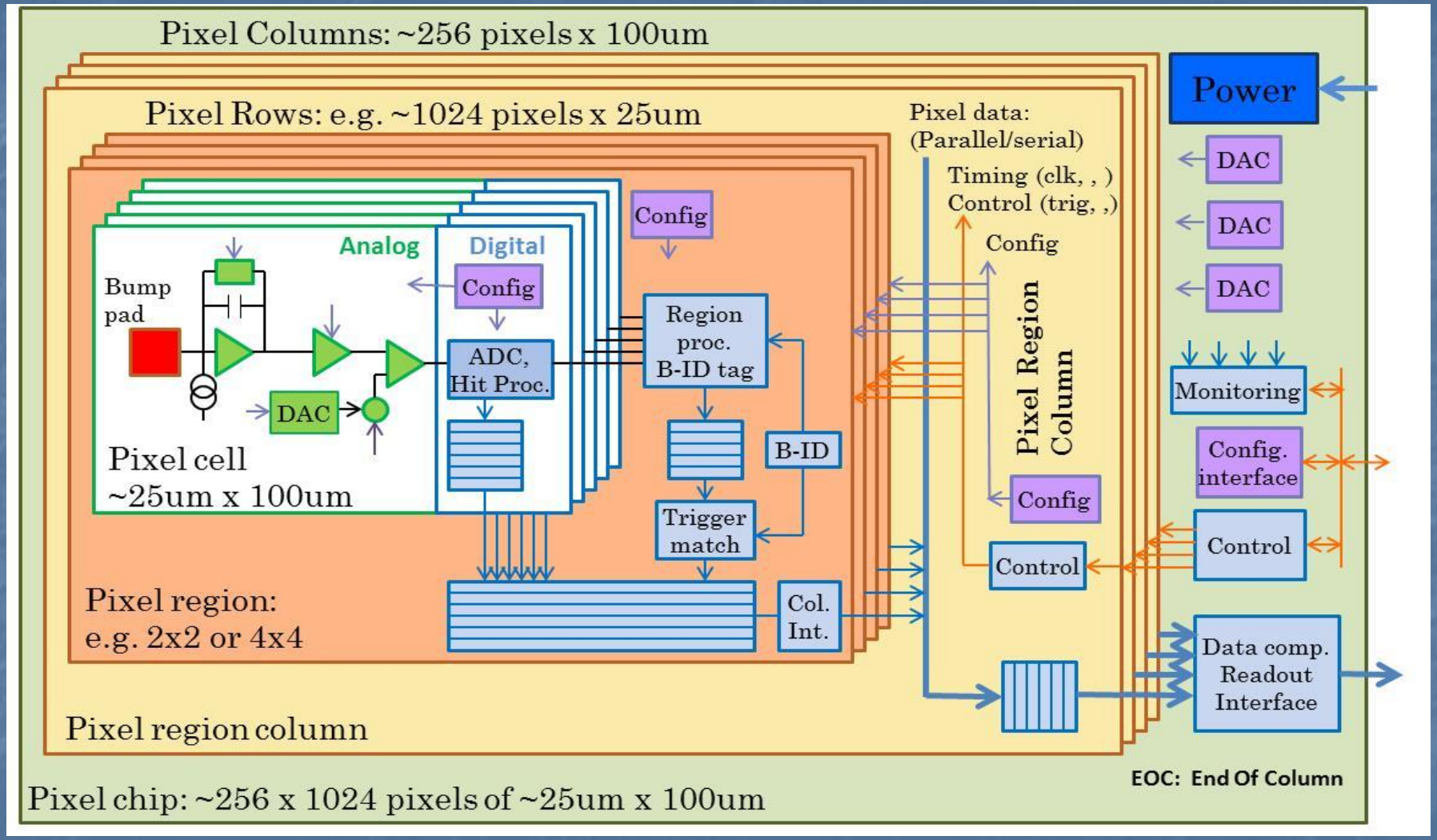
Pixel chip

- Pixel readout chips critical for schedule to be ready for phase 2 upgrades
  - Technology: Radiation qualification
  - Building blocks: Design, prototyping and test
  - Architecture definition/optimization/verification
  - Chip prototyping, iterations, test, qualification and production
  - System integration
    - System integration tests and test-beams
  - Production and final system integration, test and commissioning
- Phase 2 pixel chip very challenging
  - Radiation
  - Reliability: Several storage nodes will have SEUs every second per chip.
  - High rates
  - Mixed signal with very tight integration of analog and digital
  - Complex: ~256k channel DAQ system on a single chip
  - Large chip: ~2cm x 2cm, ½ - 1 Billion transistors.
  - Very low power: Low power design and on chip power conversion
- Both experiments have evolved to have similar pixel chip architectures and plans to use same technology for its implementation.
- Experienced chip designers for complex ICs in modern technologies that most work in a extremely harsh radiation environment is a scarce and distributed "resource" in HEP.

Pixel chip generations

Generation	Current FEI3, PSI46	Phase 1 FEI4, PSI46DIG	Phase 2
Pixel size	100x150um^2 (CMS) 50x400um^2 (ATLAS)	100x150um^2 (CMS) 50x250um^2 (ATLAS)	25x100um^2 ?
Sensor	2D, ~300um	2D+3D (ATLAS) 2D (CMS)	2D, 3D, Diamond, MAPS ?
Chip size	7.5x10.5mm^2 (ATLAS) 8x10mm^2 (CMS)	20x20mm^2 (ATLAS) 8x10mm^2 (CMS)	**> 20 x 20mm^2**
Transistors	1.3M (CMS) 3.5M (ATLAS)	87M (ATLAS)	**~1G**
Hit rate	**100MHz/cm^2**	**400MHz/cm^2**	**1-2 GHz/cm^2**
Hit memory per chip	0.1Mb	1Mb	~16Mb
Trigger rate	100kHz	100KHz	200kHz - **1MHz**
Trigger latency	2.5us (ATLAS) 3.2us (CMS)	2.5us (ATLAS) 3.2us (CMS)	6 - 20us
Readout rate	40Mb/s	320Mb/s	**1-3Gb/s**
Radiation	**100Mrad**	**200Mrad**	**1Grad**
Technology	250nm	130nm (ATLAS) 250 nm (CMS)	**65nm**
Architecture	Digital (ATLAS) Analog (CMS)	Digital (ATLAS) Analog (CMS)	Digital
Buffer location	EOC	Pixel (ATLAS) EOC (CMS)	Pixel
Power	~1/4 W/cm^2	~1/4 W/cm^2	**~1/4 W/cm^2**

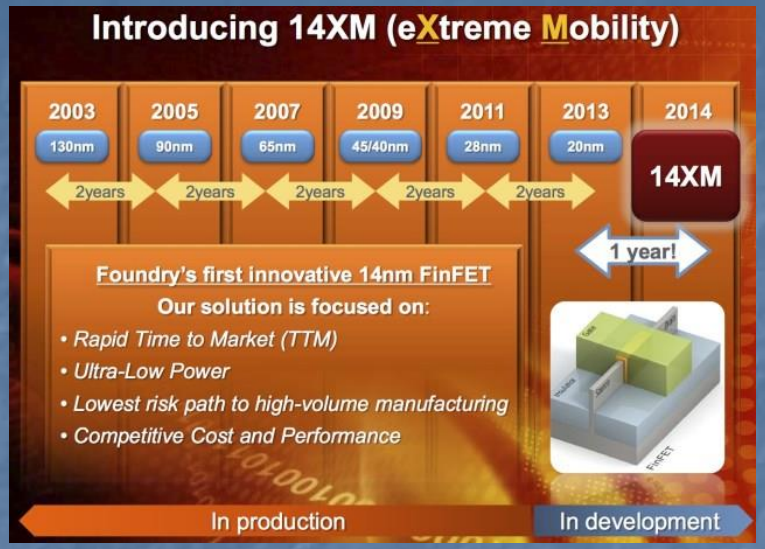
3rd generation pixel architecture

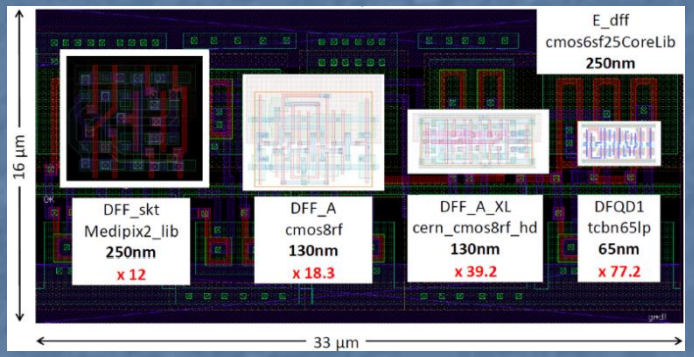


- 95% digital (as FEI4)
- Charge digitization
- ~256k pixel channels per chip
- Pixel regions with buffering
- Data compression in End Of Column

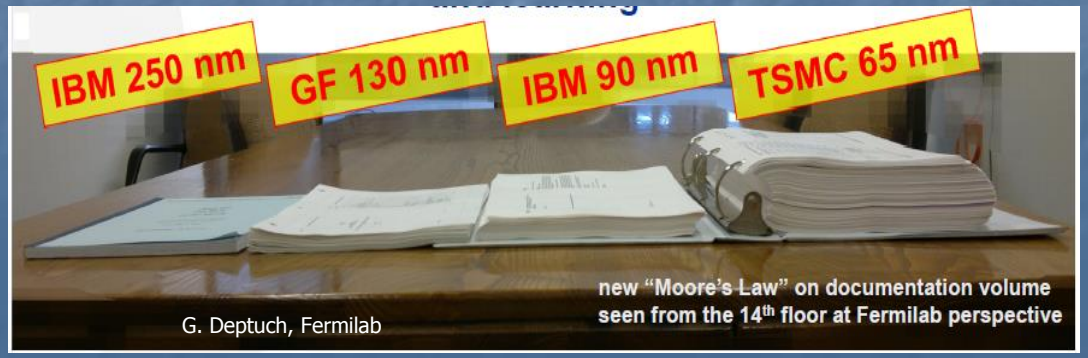
Why 65nm Technology

- Mature technology:
  - Available since ~2007
- High density and low power
- Long term availability
  - Strong technology node used extensively for industrial/automotive
- Access
  - CERN frame-contract with TSMC and IMEC
    - Design tool set
    - Shared MPW runs
    - Libraries
    - Design exchange within HEP community
- Affordable (MPW from foundry and Europractice, ~1M NRE for full final chips)
- Significantly increased density, speed, , , and complexity !





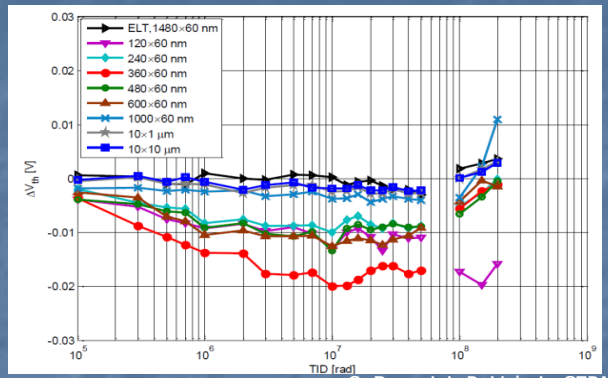
X. Llopart CERN



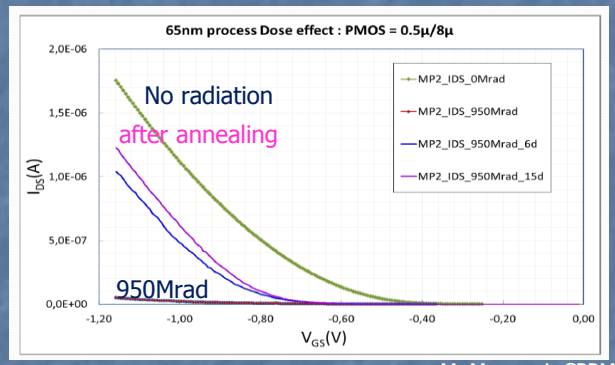
G. Deptuch, Fermilab

65nm Technology

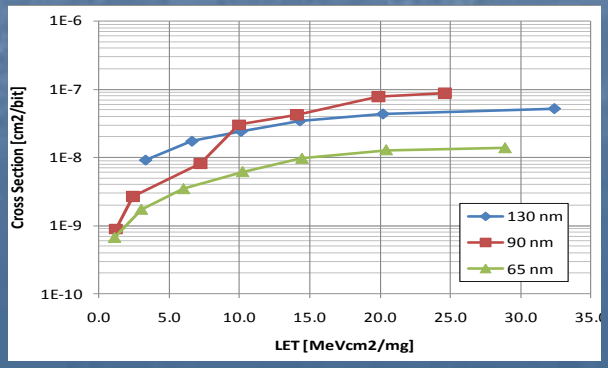
- Radiation hardness
  - Uses thin gate oxide
    - Radiation induced trapped charges removed by tunneling
    - More modern technologies use thick High K gate "oxide" with reduced tunneling/leakage.
  - Verified for up to 200Mrad
  - To be confirmed for 1Grad
    - PMOS transistor drive degradation, Annealing ?
    - If significant degradation then other technologies must be evaluated and/or a replacement strategy must be used for inner pixel layers
  - CMOS normally not affect by NIEL
    - To be confirmed for 10^{16} Neu/cm^2
    - Certain circuits using "parasitic" bipolars to be redesigned ?
  - SEU tolerance to be build in (as in 130 and 250nm)
    - SEU cross-section reduced with size of storage element, but we will put a lot more per chip
  - All circuits must be designed for radiation environment (e.g. Modified RAM)



S. Bonacini, P. Valerio CERN



M. Menouni, CPPM



ATLAS – CMS RD collaboration

- Similar/identical requirements, same technology choice and limited availability of rad hard IC design experts in HEP makes this ideal for a close CMS – ATLAS RD collaboration
  - Even if we do not make a common pixel chip
- Initial 2day workshop between communities confirmed this.
  - Workshop: http://indico.cern.ch/conferenceDisplay.py?confId=208595
- Forming a RD collaboration has attracted additional groups and collaborators
  - Synergy with CLIC pixel (and others): Technology, Rad tol, Tools, etc.
- Institutes: 17
  - ATLAS: CERN, Bonn, CPPM, LBNL, LPNHE Paris, NIKHEF, New Mexico, RAL, UC Santa Cruz.
  - CMS: Bari, Bergamo-Pavia, CERN, Fermilab, Padova, Perugia, Pisa, PSI, RAL, Torino.
- Collaborators: 99, ~50% chip designers
- Collaboration organized by Institute Board (IB) with technical work done in specialized Working Groups (WG)
- Initial work program covers ~3 years to make foundation for final pixel chips
  - Will be extended if appropriate:
    A. Common design ?,
    B. Support to experiment specific designs

Working groups

WG	Domain
WG1	Radiation test/qualification
Coordinate test and qualification of 65nm for 1Grad TID and10^{16} neu/cm^2 Radiation tests and reports. Transistor simulation models after radiation degradation Expertise on radiation effects in 65nm	
WG2	Top level
Design Methodology/tools for large complex pixel chip Integration of analog in large digital design Design and verification methodology for very large chips. Design methodology for low power design/synthesis. Clock distribution and optimization.	
WG3	Simulation/verification framework
System Verilog simulation and Verification framework Optimization of global architecture/pixel regions/pixel cells	
WG4	I/O + (Standard cell)
Development of rad hard IO cells (and standard cells if required) Standardized interfaces: Control, Readout, etc.	
WG5	Analog design / analog front-end
Define detailed requirements to analog front-end and digitization Evaluate different analog design approaches for very high radiation environment. Develop analog front-ends	
WG6	IP blocks
Definition of required building blocks: RAM, PLL, references , ADC, DAC, power conversion, LDO, , Distribute design work among institutes Implementation, test, verification, documentation	