# IC Design and Technologies for HL-LHC

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# Outline

- Background and motivation
- Technical roadmap
- Requirements
- Organizational issues
- Summary

# Background

- Modern HEP experiments depend on IC technology as much as they depend on powerful new accelerators.

- There is no distinction any more between detector and electronics, they are inseparable parts of the same instrument.

- COTS ICs are not sufficient because of unique radiation and functionality requirements.

- It is the functionality built into ICs that can add new "capabilities" to the detectors.
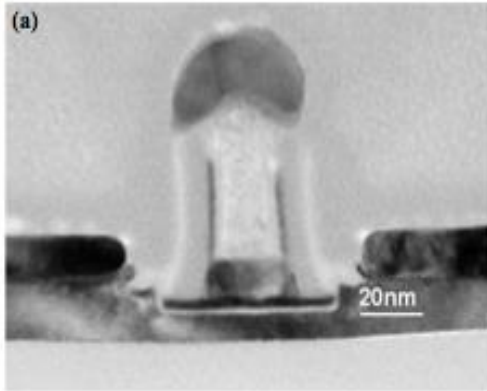
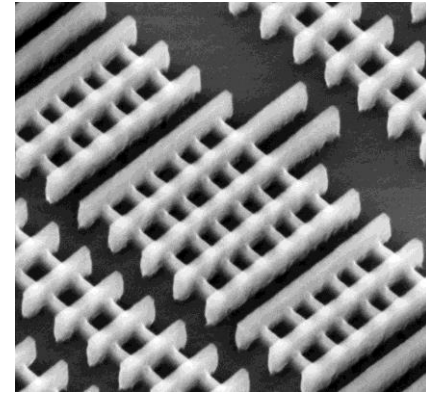# State of the art 2013: 16 nm FINFET
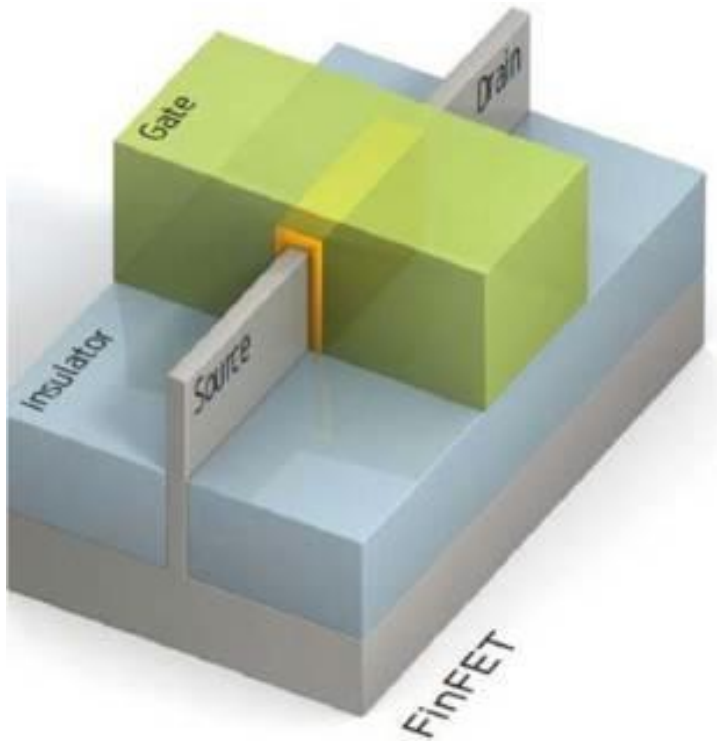
16 nm
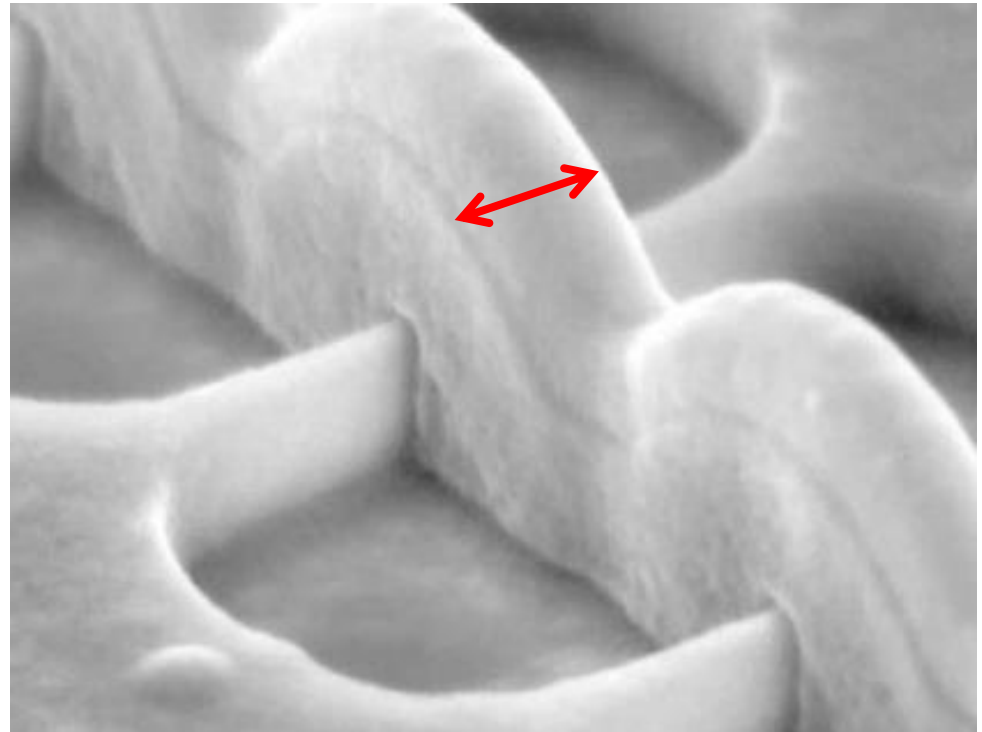


Source: TSMC

# Some advanced devices

Various sources



20 nm FDSOI from ST



22 nm TriGate from Intel
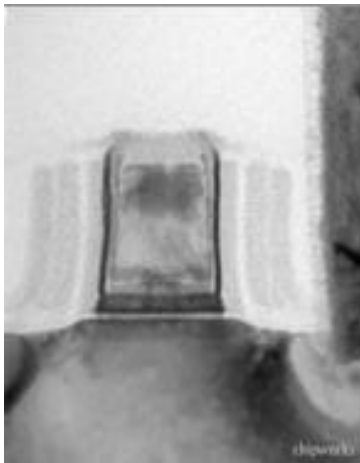


28 nm planar from TSMC
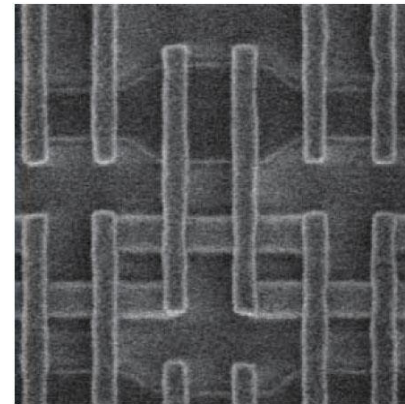


32 nm SOI from IBM

# Technologies used in ISSCC[$] papers



Trends 2007/2013

*Percentage of papers* vs *Technology*

Legend: 2007, 2008, 2009, 2010, 2011, 2012, 2013

X-axis: > 0.8, 0.5, 0.35, 0.25, 0.18, 0.13, 90, 65, 45-38, 32-28, 24-22, 20-18, BCD, Tri-Gate

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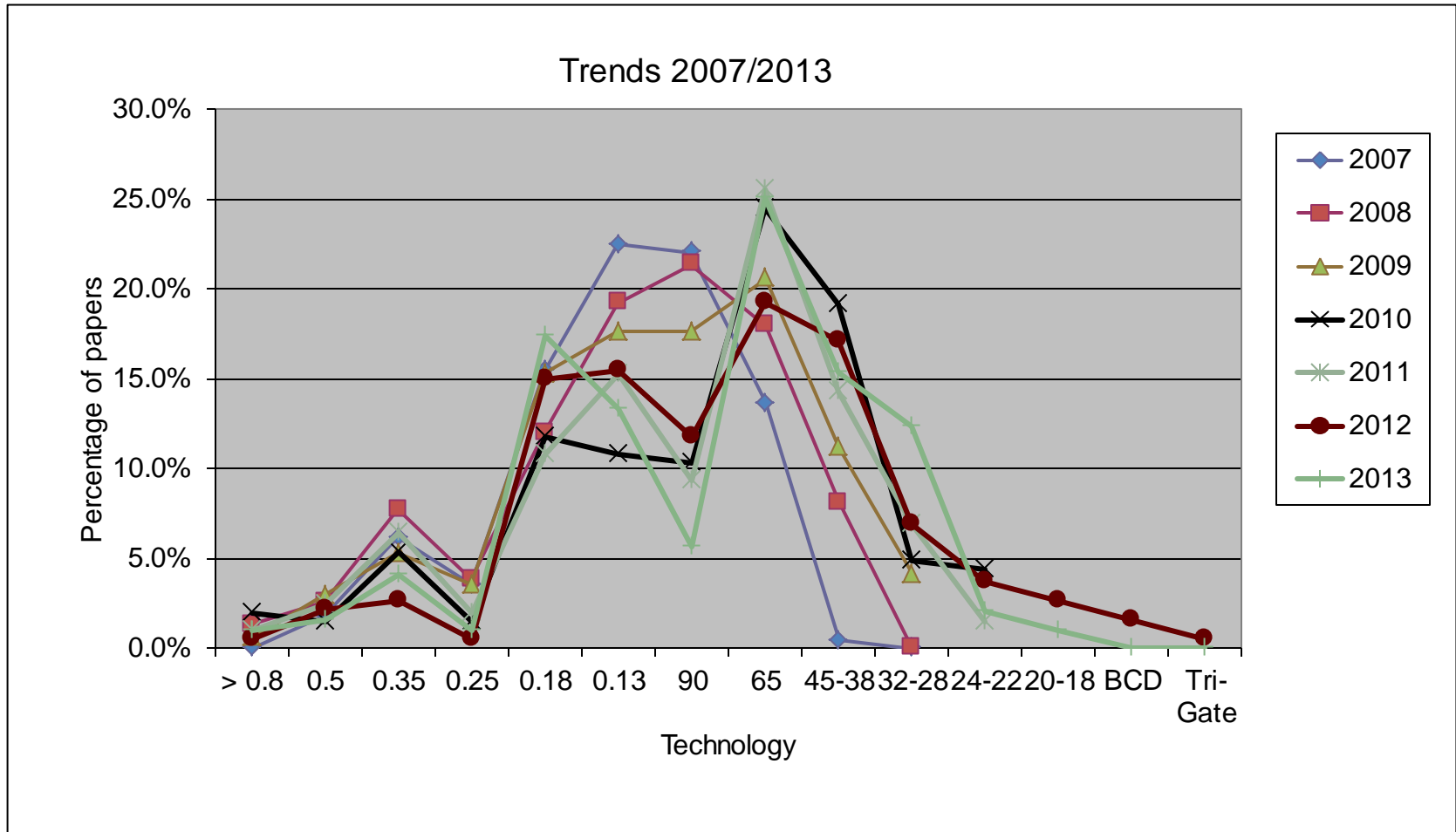
[$] ISSCC: International Solid State Circuits Conference

# Installed Capacity by Technology

Source: TSMC
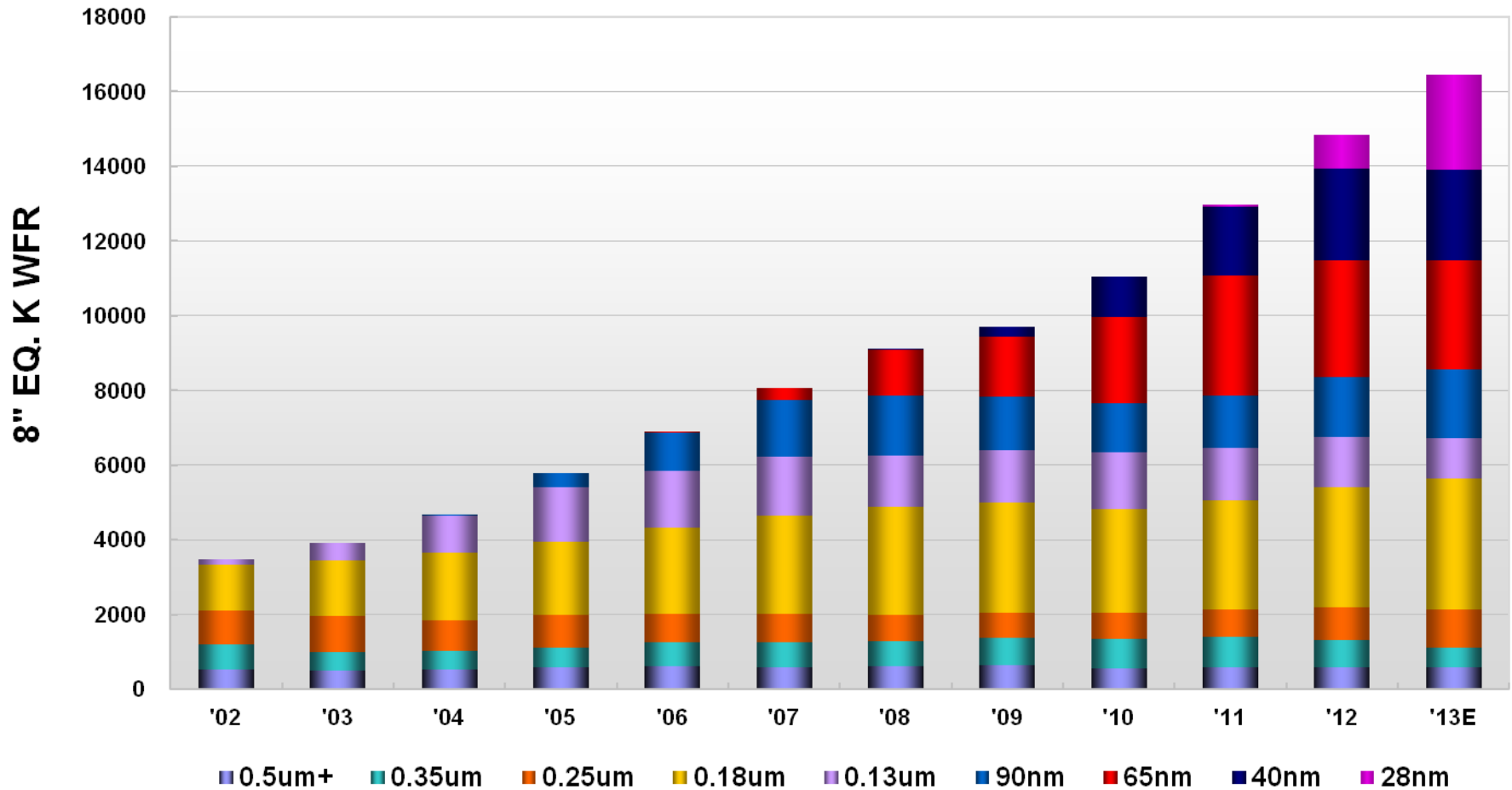
# Expected Requirements: CMOS

| | .35 um Power | 250 nm | 180 nm | 130 nm | 65 nm | < 65 nm |
|---|---|---|---|---|---|---|
| Pixels (Hybrids) | | | | ✓ | ✓ | ✓ |
| Pixels (Monolithic) | | | ✓ | ✓ | ✓ | |
| Si Trackers | | | | ✓ | ✓ | |
| Calorimeters | | ✓ | | ✓ | | |
| TPC | | | | ✓ | ✓ | |
| MPGD | | | | ✓ | | |
| Links (Electrical and Optical) | | | | ✓ | ✓ | ✓ |
| Embedded Power | ✓ | | ✓ | | | |

# Interconnects

- New High-Density-Interconnect technologies are required:
  - To manufacture large area, fully sensitive detectors
  - To allow new functionalities to be implemented: mainly stacks of sensor-analog-digital chips with lower dead-material budgets
  - For reducing assembly costs of detectors (today's this is the dominating cost)

# HDI Example: TSV



Vias

NiAu finishing

Copper and organic passivation

27
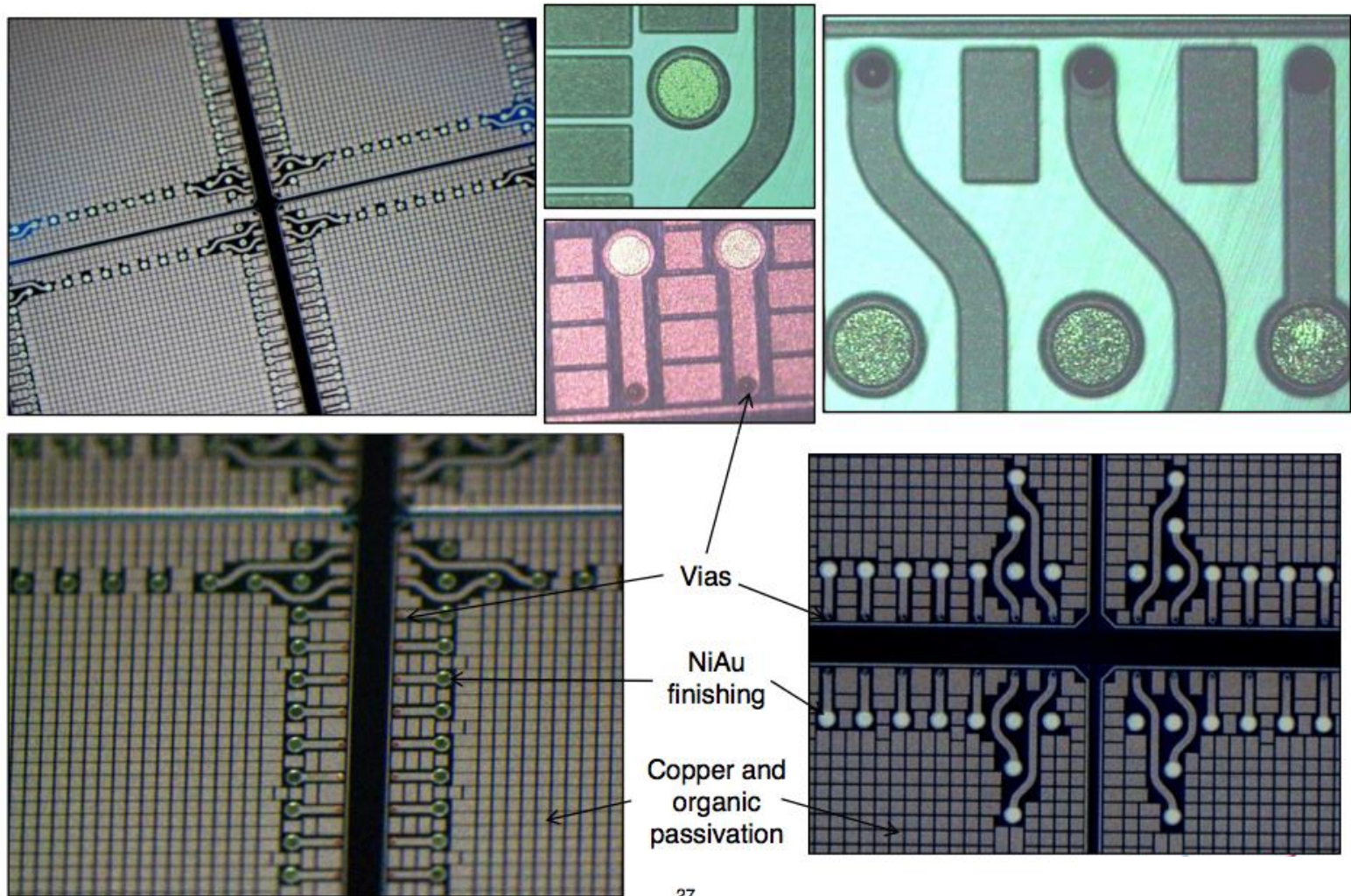
# Requirements: High Density Interconnect

| | Low Density Bump Bonding | High Density Bump Bonding (< 100 um) | LD TSV | HD TSV (< 25 um) |
|---|---|---|---|---|
| Pixels | ✓ | ✓ | ✓ | ✓ |
| Si Tracker | ✓ | | ✓ | |
| Calorimeters | ✓ | | | |
| Links | ✓ | | ✓ | |
| TPC | ✓ | | ✓ | |
| MPGD | ✓ | | ✓ | |
| Powering | ✓ | | ✓ | |

TSV: Through-Silicon-Via

# Organizational issues

- There is a large discrepancy between industrial and HEP projects cycles:

| | Product Design Cycle | Technology Cycle |
|---|---|---|
| Industry | 6-9 m | < 2 y |
| HEP | > 3 y | > 5 y |

- Large and complex SoC design require large and hierarchical engineering design teams
  - Productivity of teams is a non-linear function of their size
- Many IP blocks can be purchased from external suppliers
  - ADC macros, PLLs, SRAMs, IO libraries etc.
- "Routine tasks" can also be purchased
  - Chips assembly, P&R services etc.
- Pure R&D is necessary only in relatively few domains
  - Under the excuse of "too expensive", HEP rarely uses external design services and duplicates efforts often

# Examples of complexities accompanying technology scaling

- Technical:
  - with shrinking the following issues become progressively more important:
    - matching, planarity, proximity effects, short channel effects, wide channel effects, NBTI, hot-electron, number of model parameters, on-chip signal coupling, lower intrinsic transistor gain, number of technology options, lower supply voltage, higher gate leakage, atomic variability, line-edge-roughness…
- Thickness of technology design manual:
  - 250 nm:     ~ 200 pages
  - 130 nm:     ~ 500 pages
  - 65 nm:       > 1500 pages

# Costs/Performance[$]

| Generation [nm] | Cost / mask set | Cost / 8" wafer | Cost Proto/mm2 | Density gates/[unit A] | Design Complexity | Power per gate |
|---|---|---|---|---|---|---|
| 250 | 1.0 | 1.0 | 1.0 | 1 | 1 | 1.00 |
| 130 | 2.9 | 0.9 | 6.0 | 5 | 3-5 | 0.36 |
| 65 | 5.3 | 1.1 | 10.8 | 27 | 10-25 | 0.18 |
| 28 | 15.0 | 2.4 | 36.3 | 50 | 25-125 | 0.09 |

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[$] Normalized to 250nm generation

# μTechnologies in HEP

- New technologies open up many new possibilities for creative physicists/engineers
  - There is no doubt that commercial microelectronics technologies available today are well ahead of most requirements foreseen for the HL-LHC generation
- New technologies can only be exploited if:
  - The design groups organizations are matched to the challenges and risks accompanying these technologies
    - Minimum group sizes to be increased
    - Project and personnel continuity to be preserved
    - Duplications to be avoided
  - The HEP community manages to keep a "privileged" (i.e. non strictly $ based) access to advanced foundries

# Summary

- Advanced IC technologies are available to satisfy HL-LHC needs
  - NRE Costs are high but not out of reach with respect to the size of the HL-LHC upgrade projects
  - Radiation robustness to be validated and monitored
  - HDI: TSVs may or may not become available for "small" customers
- To use these technologies successfully and efficiently, substantial engineering investments are necessary
  - Adapt and evolve our design teams to the structure needed to manage these complex technologies
  - Keep resources matched to the ambitions
  - Strengthen collaborative support and shared services inside community