

# Power Distribution

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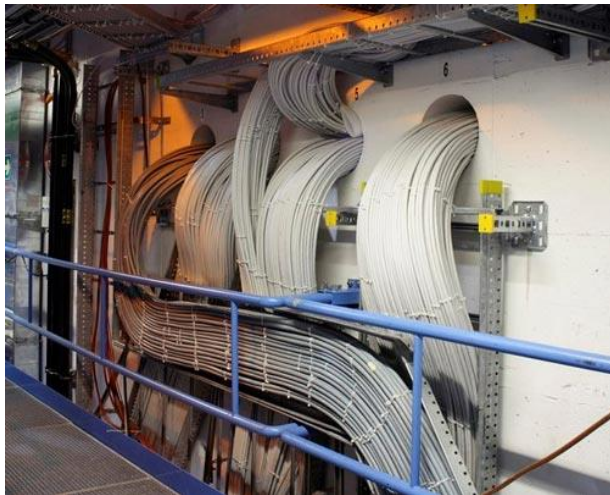
STFC Rutherford Appleton Laboratory

ECFA HL-LHC Workshop, Aix-les-Bains, 1-3 October 2013

# Outline

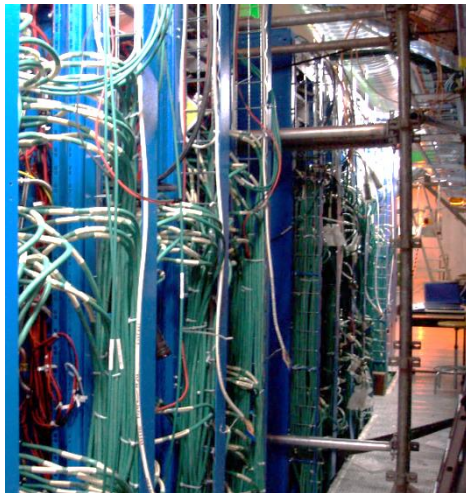
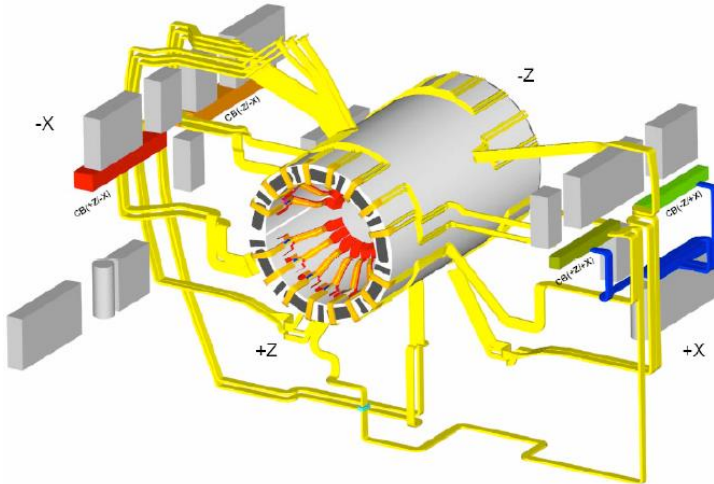
- Power Distribution at LHC
- Serial Powering
- DC-DC Point of Load Converters
  - Buck Converter
  - Switched Capacitor
- Other common interests
  - HV Multiplexing
  - Bulk Supplies
- Conclusions

# Example: ATLAS SCT (Silicon Strips)



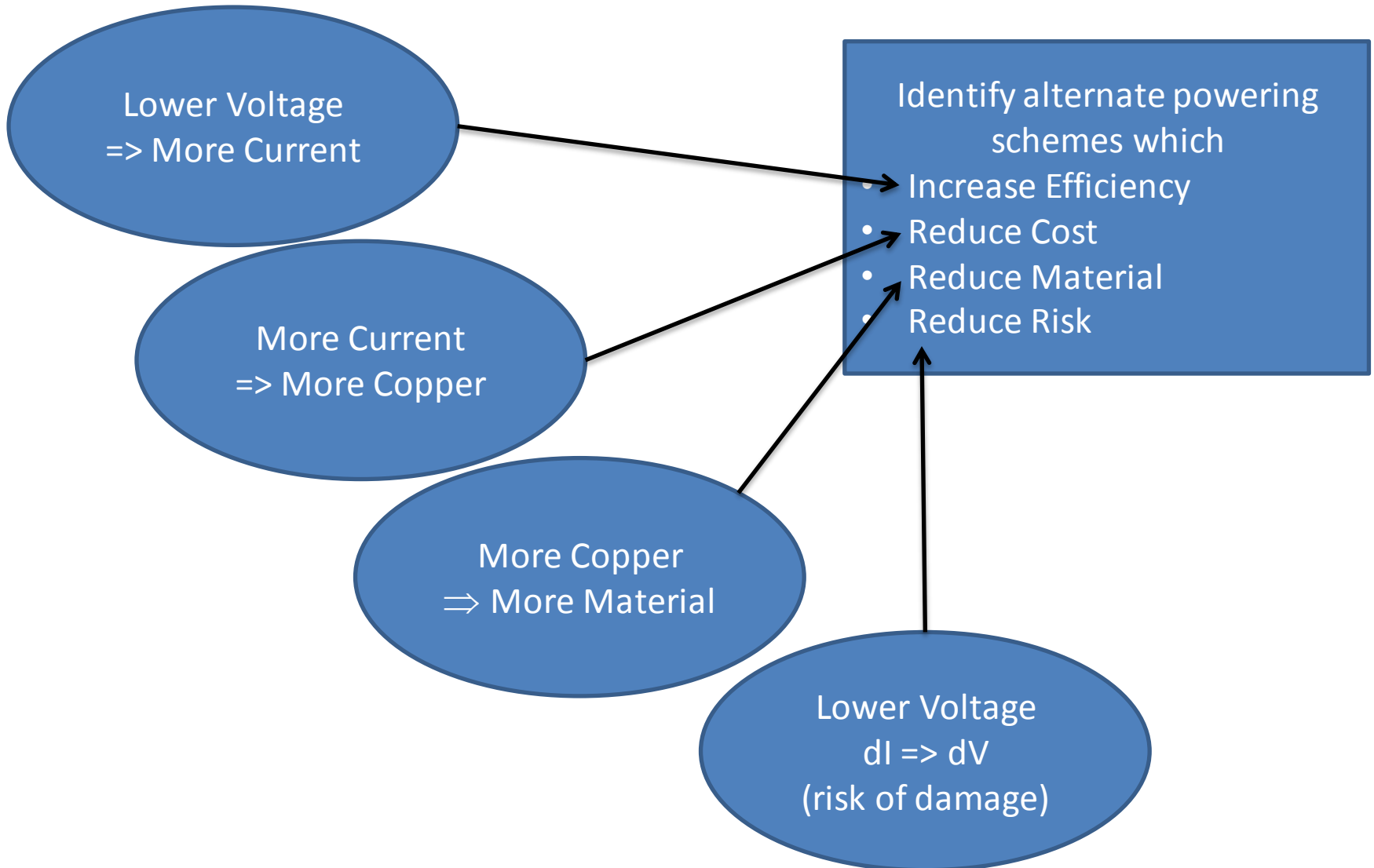
- 4088 Detector Modules
- **Independent Powering**
  - 4088 cable chains
  - 22 PS racks *in service caverns*
  - 4 crates / rack
  - (up to) 48 LV and 48 HV channels / crate
- Longest cable run
  - ~130m copper cable (3 gauges)
  - ~2m copper/kapton (endcap) or aluminium/kapton (barrel) power tapes
  - Voltage limiter in line to block spikes due to sudden drops in load
- Typical overall efficiency ~40%

# Example: CMS Silicon Strip Tracker

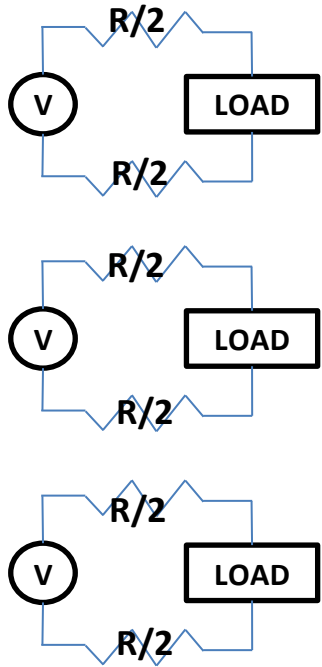


- 15000 Detector Modules
- **Parallel Powering**
  - 1944 “detector power groups”
  - 29 racks in **main cavern**
  - (up to) 6 crates per rack
  - CAEN EASY system for “hostile environments”
    - Magnetic field tolerant
    - Radiation tolerant
- Typical cable run
  - 40m copper + 6m aluminium
- Typical overall efficiency ~40%

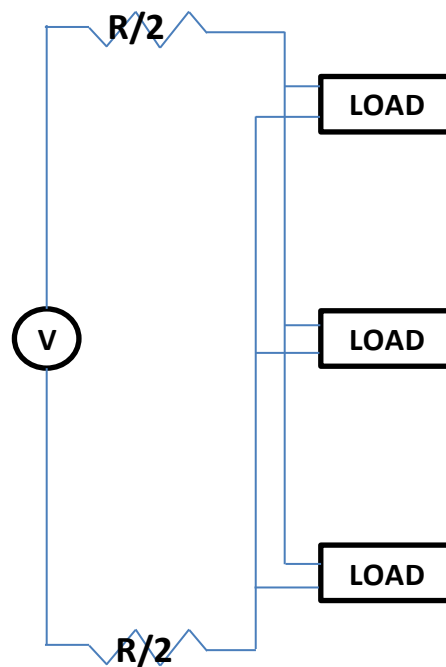
# Motivations for Change



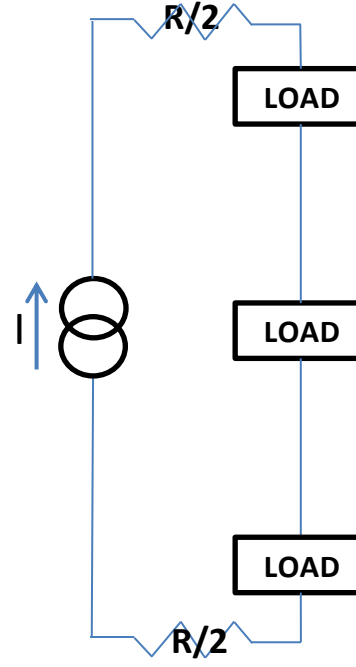
# Powering Schemes and Cables



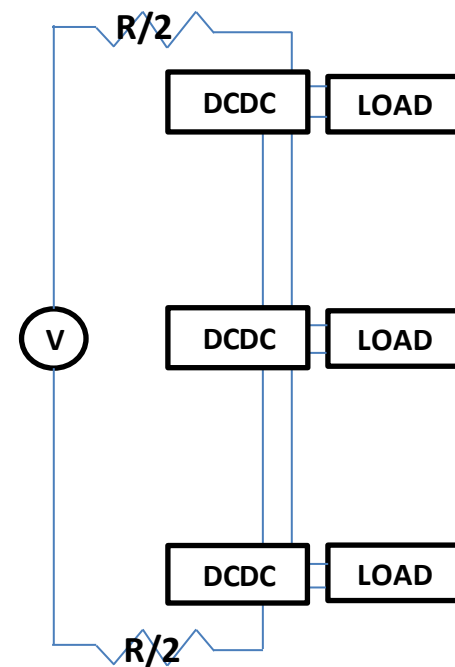
Independent Powering



Parallel Powering



Serial Powering



DC-DC Powering

Losses in off-detector cabling of total resistance  $R$  for  $n$  loads drawing current  $I$ :

$$P = nI^2R$$

$$P = n^2I^2R$$

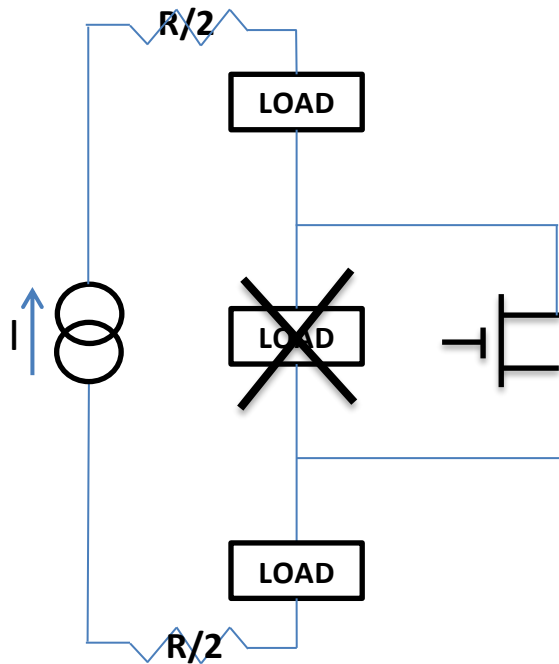
$$P = I^2R$$

$$P = n^2I^2R / r^2$$

where ratio  $r = V_{in}/V_{out}$

Serial Powering and DC-DC Point of Load conversion offer more efficient cable usage than Independent or Parallel Powering. *Total system efficiency will be lower as this depends upon the efficiencies of bulk supplies, DC-DC converters shunts which are neglected here.*

# Serial Powering



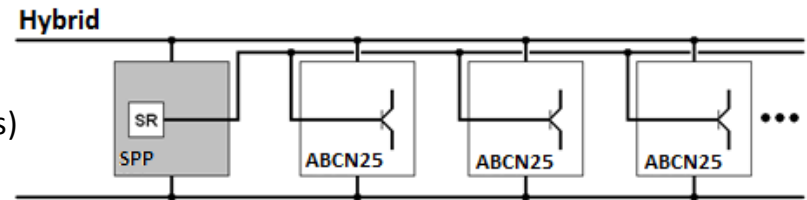
- Elements of a serially powered system
  - Current Source
  - Shunt regulator / transistor
  - AC or opto-coupling of control signals
  - Protection circuit & Bypass shunt
    - Shunt current past faulty device in response to over-voltage condition or under DCS control
- Current must be sufficient to cover the peak demand of the biggest load in the chain
  - Best suited to chains of identical devices
  - Not ideally suited to disk geometries (but possible)
- Intrinsically low mass, needs little if any extra space
  - Can be useful for tracking detectors, especially pixels (where power density highest and space most limited)



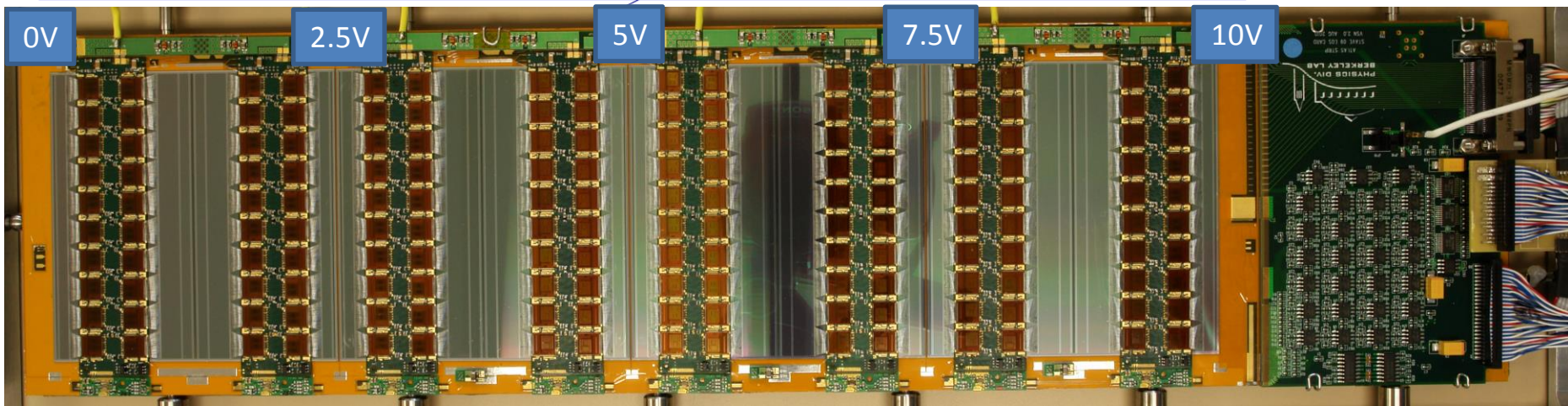
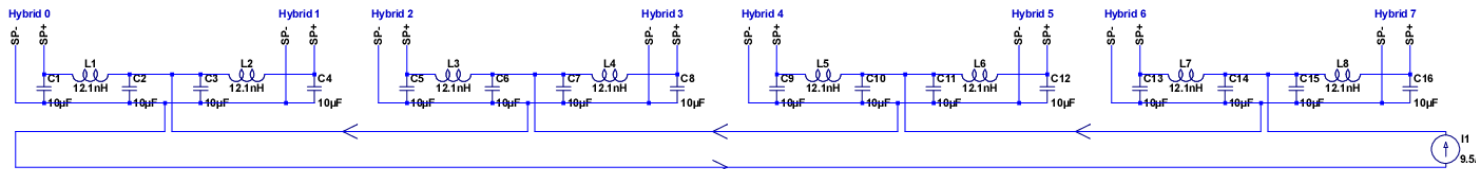
# Example: ATLAS Strip Stave (SP)

Further Example in Backup

- Distributed SP Architecture
  - Shunt transistors within ABCN25 FE ASIC, 20 per hybrid
  - One control block per hybrid (SPP chip or commercial parts)
- Three short (8 hybrid) prototypes built
  - Some with protection circuitry (SPP chip or commercial parts)
  - Good results in “Chain of Modules” Configuration
- Longer (24 hybrid) prototype to follow in the coming months
  - With integrated protection from SPP chip

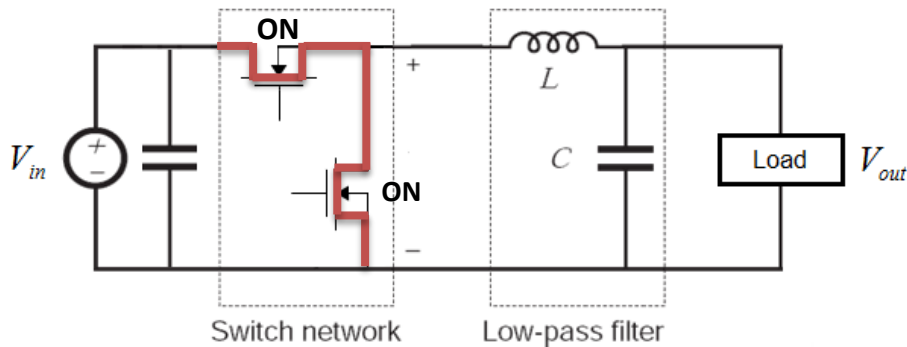


Distributed SP Architecture (within the hybrid)

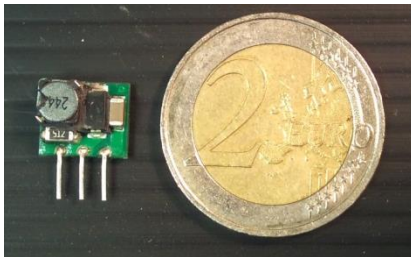




# DC-DC Synchronous Buck Converter



Output voltage is regulated by adjustment of the duty cycle of the two switch transistors

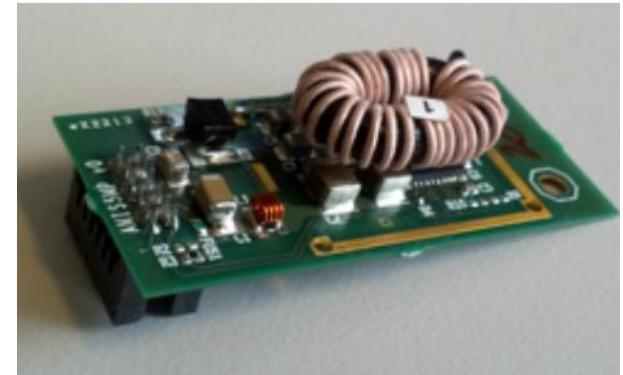


Typical Commercial Buck Converter:  
Input 24V, Output 5V 1A, 90% efficiency

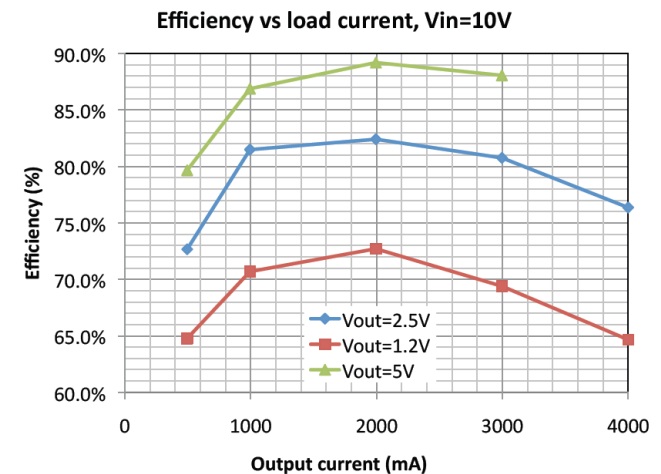
- Why not COTS?
  - readily available
  - cheap & efficient
  - small and reliable
- BUT
  - ferrite-cored inductors
    - may not be used in magnetic fields
  - not radiation hard
    - May not be used in HL-LHC environment
- We need custom converters
  - air-cored inductors
  - radiation hardened ASIC
  - *for tracker applications: low mass design*

# Buck Converters for HL-LHC Phase 1

- FEAST, a production ready converter ASIC for **Phase 1 upgrades**, is now under test at CERN
  - Follows on from AMIS5 prototype in same, commercial 0.35um technology
- FEAST DC-DC converter Module
  - 127um thick tinned copper shield (not shown)
  - Custom 430nH oval air-cored inductor
  - Vin 5V (6V for AMIS5) to 12V (min Vin = Vout+2V)
  - Vout 1.2V to 5V, 4A max
  - EMC compliant with conductive noise requirements of CISPR11 Class B
  - TID above 200Mrad, displacement damage up to  $7e14$  1MeV neutrons/cm<sup>2</sup>
  - Magnetic field tolerance > 40,000 Gauss
- Sample converters with AMIS5 available now
  - Includes module to generate -V from +V
- Converters with FEAST available 2014
  - 10,000 units to be made



AMIS5MP: 3.7cm x 1.7cm

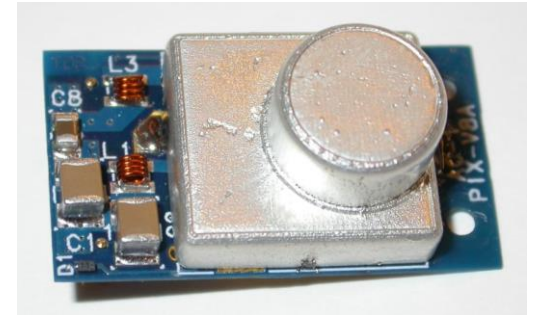


FEAST: Preliminary Efficiency Data @ 1.8MHz

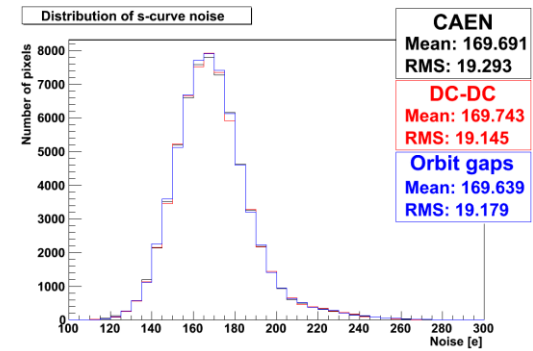
# Example: CMS Pixel Upgrade

- For installation in 2016-17 Extended Technical Stop
  - x1.9 increase in channel count
    - x1.9 increase in power consumption
  - Must use existing cable plant
- Use DC-DC converters with AMIS5 / FEAST
  - Smaller, round 450nH air-cored inductor
  - Converters located 2.2m away from modules
  - 13 converter pairs (analogue, digital) per bus board
    - Each converter pair serves 1 - 4 pixel modules
  - $I_{out} < 3A$  per converter
- No noise increase due to use of DC-DC converters

Further Example in Backup



AC\_PIX\_V8 A: 2.8cm x 1.6cm; ~ 2.0g



Prototype bus board with 24 DC-DC converters



# Summary of R&D leading to FEAST

- Five ASIC technologies were studied in pursuit of a process with “high voltage” capability able to survive multi-Mrad irradiation.
  - First ASIC (AMIS2) made in in 0.35um technology then moved to a more advanced 0.25um technology which looked very promising.
- Made 2 iterations of the design in that technology (IHP1 and IHP2)
  - Had to discontinue the technology because of latch-up problems and SEB sensitivity after the manufacturer changed the design of the power transistors.
- Revert to 0.35um technology
  - Make 3 other iterations (AMIS4, AMIS5 and FEAST)
- The present technology is available through Europractice
  - Affordable, but turnaround time up to 6 months
  - Extends development time
- Effort
  - Integrated effort since project start (April 2008): ~20 FTE
  - Peak effort: ~5FTE
- Other Costs
  - ASIC submissions, custom components, irradiations, PCBs
  - CHF ~150k per annum

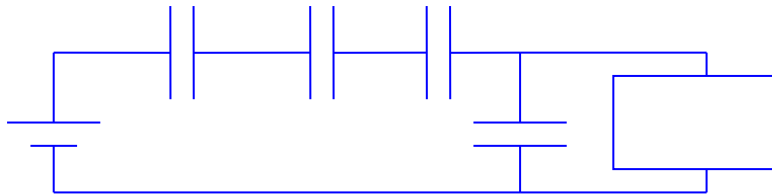
# Buck Converters for HL-LHC Phase 2

- Much of the groundwork has been done
  - Design Team familiar with required disciplines: EMC, magnetics, DCDC layout techniques, power ASIC design
  - Community has learnt how to use DCDC within detector systems
- Requirements for phase 2 can be met
  - Exploring two candidate technologies
  - Exploration of converter size and mass reduction presented at TWEPP 2011
- Next Steps
  - Evaluate performance of low mass converters using FEAST
  - Further ASIC iterations to optimise radiation tolerance
    - Stability of bandgap reference voltage
    - Studies of Single Event Effects (SEE)
- Effort and costs
  - Should be similar if we continue to develop the present architecture
- More exotic designs are of course possible
  - For example: multi-phase for higher power; GaN for higher input voltage;
  - If such designs are necessary to meet experimental requirements, effort and costs will rise accordingly

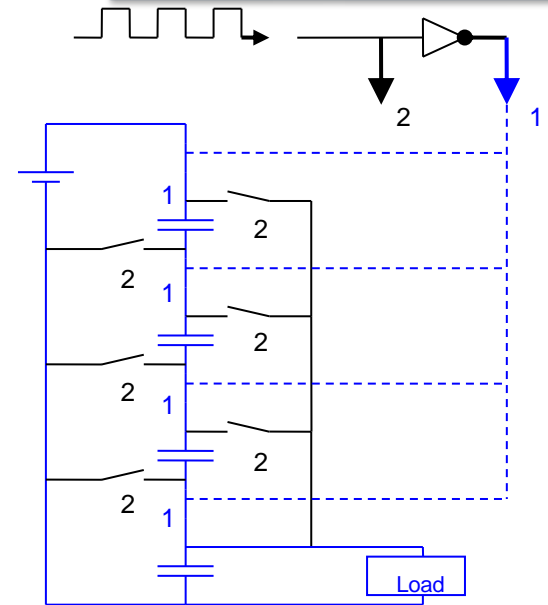
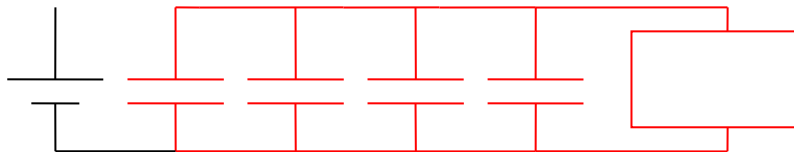
# DC-DC with Switched Capacitors

Further Detail in Backup

Phase 1 – Charge in series



Phase 2 – Discharge in parallel



No inductors – can be implemented on our FE hybrids – even completely in the FE ASICs

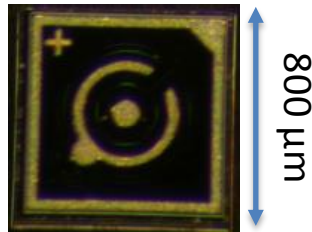
- Much industrial R&D focussed in this area
- A high efficiency alternative to on-chip LDOs
- May be used as part of a DC-DC or SP powering scheme
- Concept successfully demonstrated with ATLAS FE-I4A ASIC (**see backup**)
- Optimum performance requires access to technologies with integrated capacitors



# Other areas of Common Interest

## Sensor Bias Multiplexing

- Bias cables of course have mass
  - Can be a concern in tracking applications
- Could parallel power n sensors
  - May lose all of them if one fails as a short
- Propose use of rad-hard HV switches
  - To be able to disconnect any failed sensors
- Present phase: Device Identification
  - Study of commercial HV transistors
    - GaN, Silicon, Silicon Carbide
    - before and after irradiation



300V Silicon JFET

## Bulk Supplies

- Needed irrespective of powering scheme choice
  - Current sources for SP
  - Voltage sources for DC-DC
- For use in experimental caverns, must be suited to “hostile environments”
  - Magnetic Field
  - Radiation
- **Must** be done with commercial partners
  - careful not to leave this too late!

# Conclusions

- Two main power strategies being explored for HL-LHC
  - Serial Powering
    - circuit blocks built, small scale system tests give encouraging results
  - DC-DC Buck converters
    - demonstrated to meet the requirements of Phase 1 Upgrades
- In addition
  - Switched capacitor DC-DC conversion is a viable, high efficiency alternative to on-chip LDO regulators
- Necessary to continue work on all of the above
  - “One size does not fit all”
- Continued support is needed to deliver suitable parts *in time to build* Phase 2 Upgrades
  - Bulk supplies
  - Evaluation of larger Serially Powered systems
  - Low mass DC-DC Buck Converters *with increased radiation tolerance*
  - Identification of “HV” switch transistors for sensor bias applications

# Backup

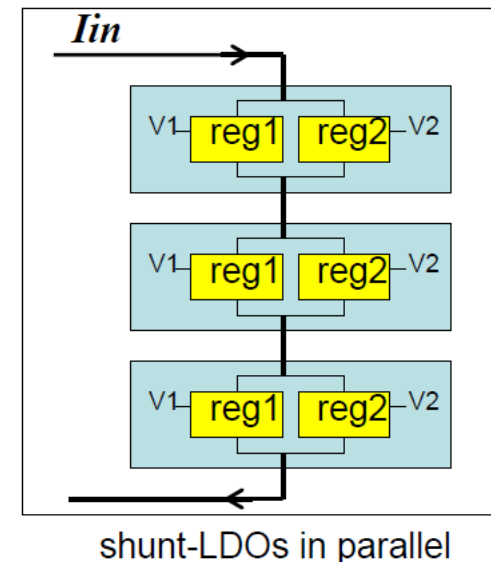
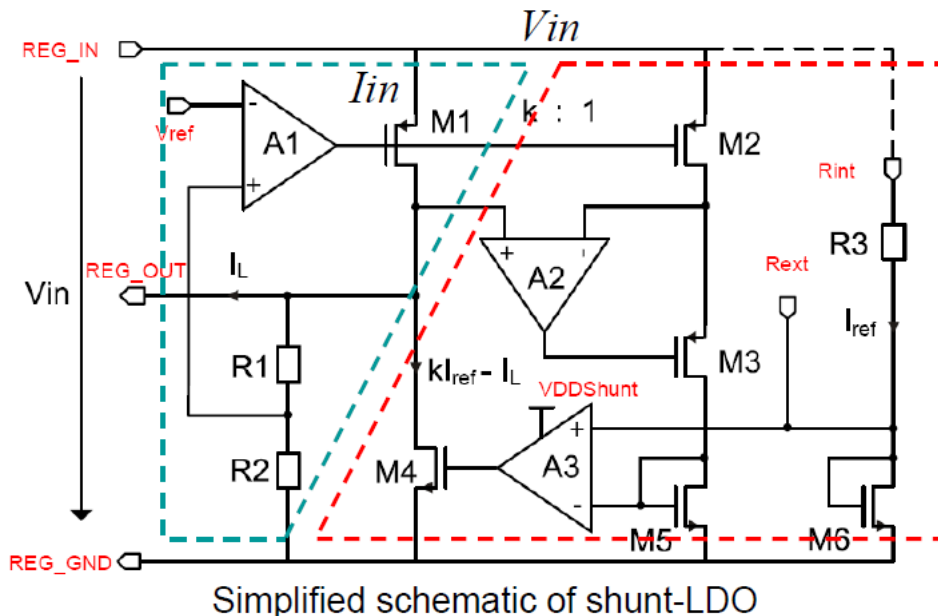
# Abstract

Compared to their LHC counterparts, the HL-LHC detectors require significantly increased channel count and rate capability in order to meet physics needs. Low power design techniques and deep-submicron technologies (130 or 65 nm CMOS) will enable upgraded performance to be delivered at power levels comparable to the present detectors, however as the improved efficiency of such technologies comes largely as a result of lower power supply voltages the current drawn by the front-end electronics is actually increased. In the case of individual or parallel powering, the losses in off-detector cabling quickly become unacceptable. It is clear that new power distribution strategies are required.

Two alternate powering schemes are being studied for HL-LHC detectors: DC-DC Conversion and Serial Powering. Radiation hard DC-DC converters with air-core inductors have been designed to meet the needs of Phase 1 upgrades, and the circuit blocks needed to operate a chain of serially connected detector modules have been prototyped. Both schemes have been shown to perform well in small-scale system tests. In addition, switched capacitor DC-DC converters have been demonstrated to be a viable, high efficiency alternative to on-chip linear regulators. The status of this work shall be shown and the merits and drawbacks of each scheme outlined. The directions of future development will be described, as required to deliver reliable, low-mass powering solutions for Phase 2 upgrades on an appropriate timescale.

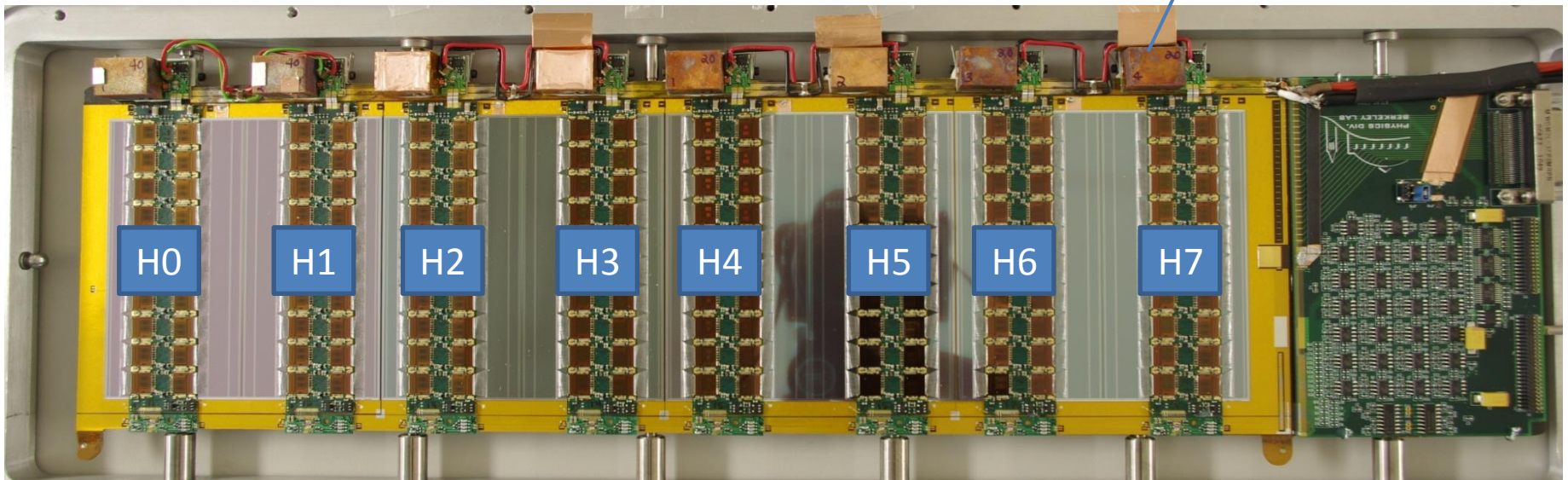
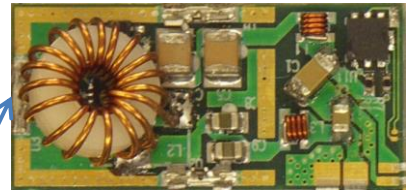
# Example: ATLAS Pixel Shunt-LDO

- Combined Shunt and LDO (ShuLDO) in FE-I4
  - The **left** part is a standard LDO
  - The **right** part is the shunt circuit
- Benefit wrt standard shunt regulators
  - Shunt-LDO regulators generating **different output voltages** can be placed in parallel without any problem regarding mismatch and shunt current distribution



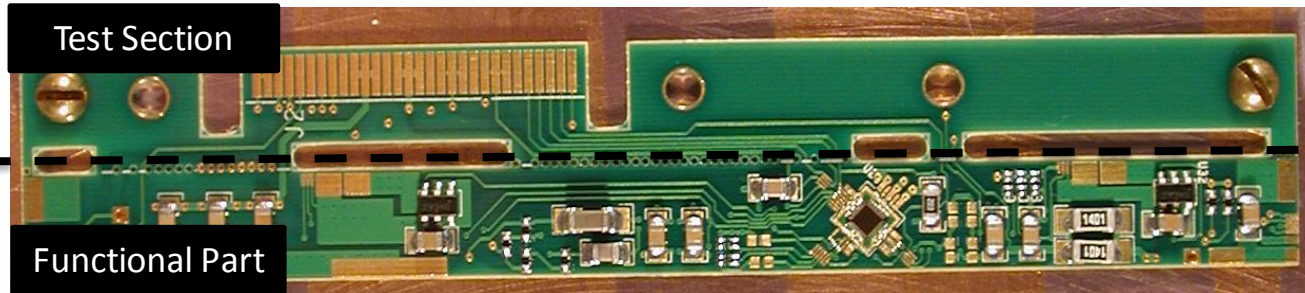
# Example: ATLAS Strip Stave (DC-DC)

- STV-10 Buck Converters from CERN group used *on stave*
  - Based on commercial chip due to high current requirement
  - Low mass shield (plated plastic)
- Three short (8 hybrid) prototypes built
  - All with good results, even with converters adjacent to the front end
- Longer (24 hybrid) prototype under construction

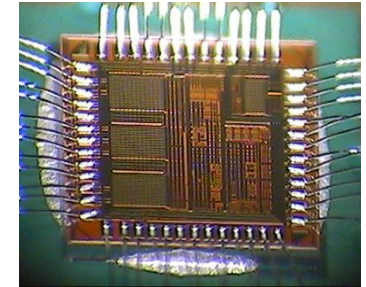




# Example: Serial Power and Protection (SPP) Chip

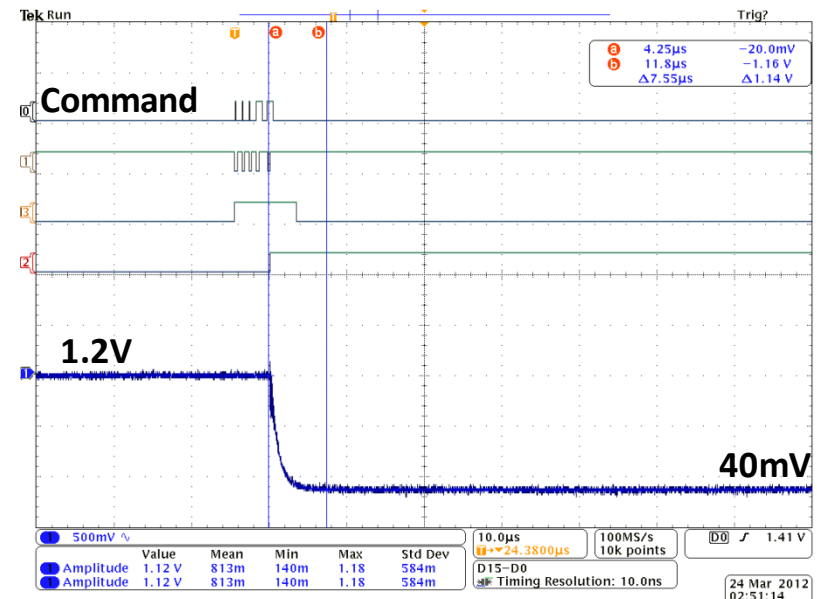


**SPP PCB for ATLAS Strip Stave Tests**



**SPP Chip**

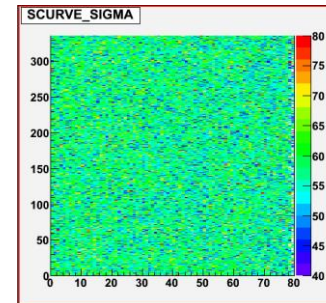
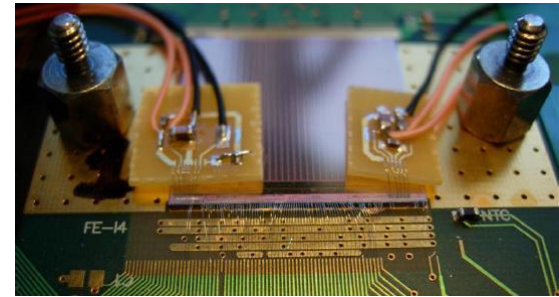
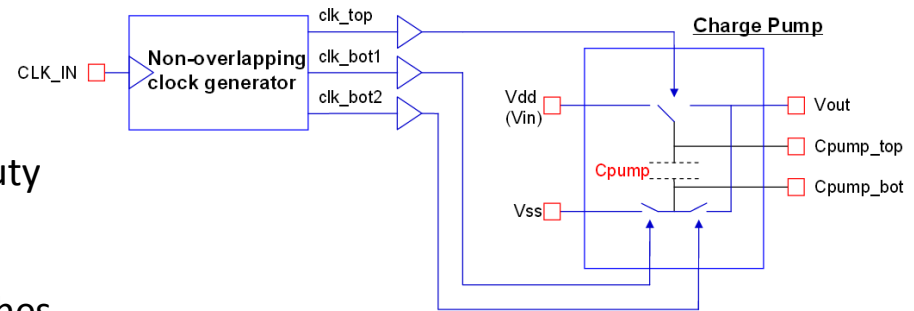
- SPP ASIC Provides
  - Shunt Regulation
  - Over Voltage Protection
  - Bypass under DCS control
    - using internal and/or external transistors
- PCB Shown provides diagnostics
  - Including external transistors to shunt 10A
  - Component count for phase 2 design much smaller: just SPP, the FE chips and a couple of passives
- Radiation Tolerance
  - Gamma tested to 30MRad
  - Protons to follow



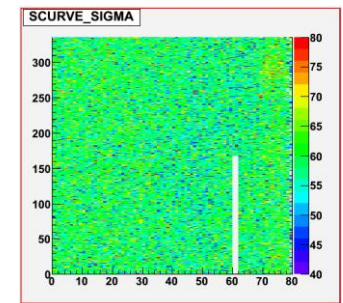
**Activation of Bypass Mode**

# Example: Switched Capacitor DC-DC circuit in ATLAS Pixel FE-I4A

- Non-overlapping Clock Generator
  - generates 3 internal clocks from CLK\_IN
  - same frequency but different phase & duty
- Charge Pump
  - consists of 4 transistors working as switches
  - manipulates pump capacitor under control of clocks
- External Pump Capacitor
  - Must be close to ASIC for good results
  - No significant impact upon noise performance when Cpump on top of FE-I4A
    - Missing pixels unstable, not related to DC-DC
- Demonstrates Technique is Viable
  - Best results would require access to ASIC technologies with embedded capacitors



Normal Power

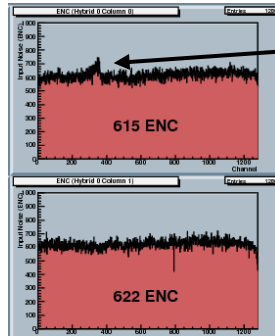


DC-DC Power

# Example: ATLAS Strip Stave Integrated Module Concept

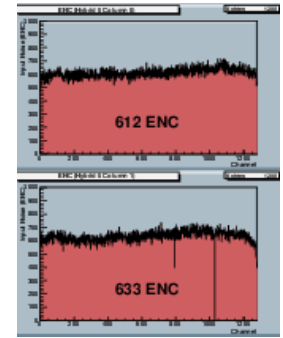
Q) What happens if we stick a (shielded) DC-DC Buck Converter on a Silicon Strip Sensor?

Right way up



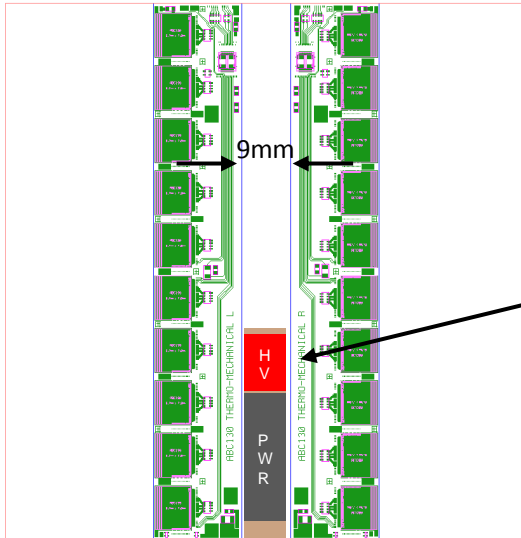
Noise bump correlates with gap in EMI Shield: we expect to be able to resolve this.

Wrong way up



No evidence of converter seen

This promising result leads to the following Integrated Module Concept for the new 130nm chipset:



- HV and powering moved to a carrier located between hybrids
  - Can be DC-DC or SP
  - Existing STV10 converter 38mm x 13mm, will need a smaller equivalent
    - Aggressive, but looks possible
- Power/HV circuitry placement driven by DC-DC requirements
  - I/P and O/P to converter placed close together (min loop area)
  - Results in best converter performance w.r.t. noise
- Results in a highly integrated module
  - All module electrical circuitry contained within area of sensor
  - Benefits in reduced stave width – less material