Modular Electronics

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Outline

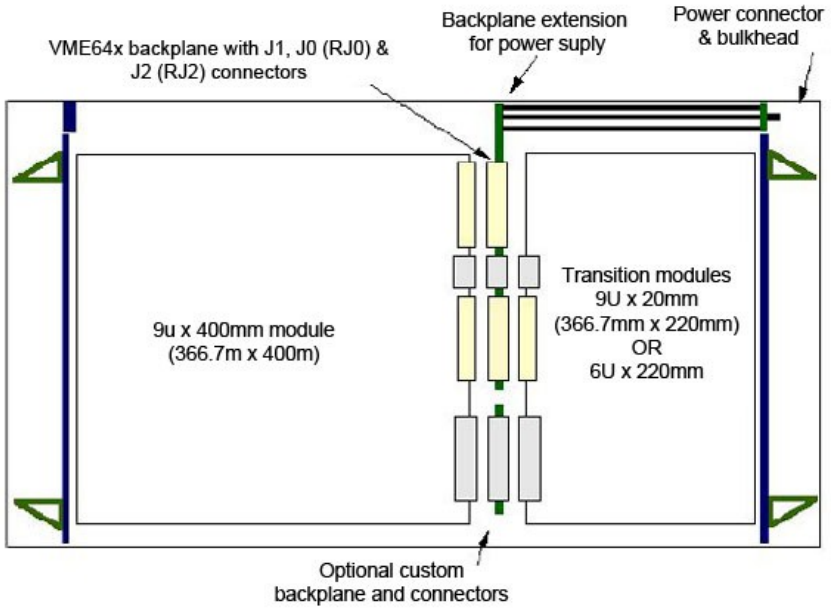
- Current modular electronics and reasons for change
  - VME in LHC
  - Limitations and reasons for change
  - Industry trends
  - Crate evolution
- Towards a new modular electronics standard
  - Foreseen DAQ and trigger scheme
  - Replacement candidates
  - Reasons to choose xTCA
  - Risks
- Roadmaps
  - Validation route and schedule
  - Possible roadmaps

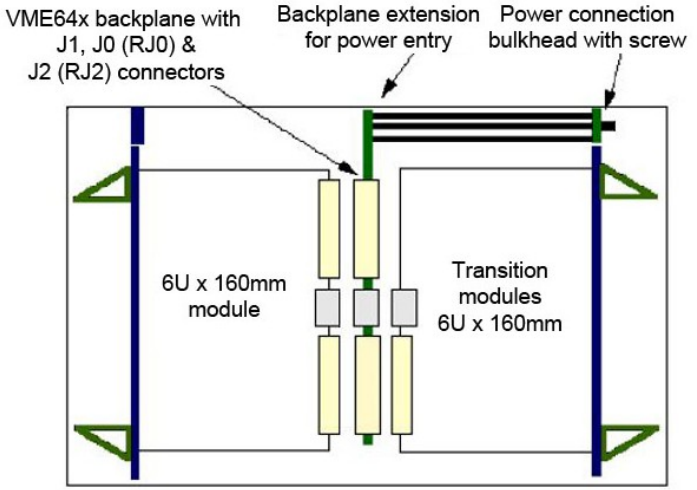
VME in LHC

Largely proven system

- First designs in the 80's
- Comfortable form factors
- Robust mechanics
- Support by CERN pool
- Hundreds of crates in LHC

ALICE	69 crates
ATLAS	219 crates
CMS	194 crates
LHCb	146 crates
Total	***628 crates***





Limitations and reasons for change

HL-LHC life duration: 2022 – 2035

- Will VME still exist ?

Current crates reliability ?

- Will they survive another 25 years ?

Already poorly adapted to major technology changes of the last decade

- ***Power consumption of new components***
  - Power dissipation per 9U VME slot ~ 137 W ~ 9 W/dm^2
  - Power density for current electronics ~ 40-70 W/dm^2 and more
    - More current needed, higher voltages at crate level to limit losses
- ***Cooling***
  - VME not dimensionned to cool down present standards
- ***Most data transfers are now serial and point to point***
  - VME speed limited by multidrop parallel bus

Industry trends

Everything goes serial

- PCI → PCI Express
- ATA → Serial ATA
- SCSI → Serial Attached SCSI
- VME → VPS (VITA41)
  → VXS (VITA46)

Busses

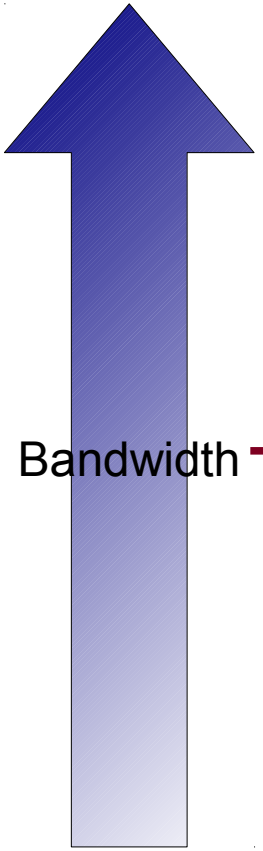
- FPGAs now embed tens of serial links
- Memories with serial interface soon to be available

Chips

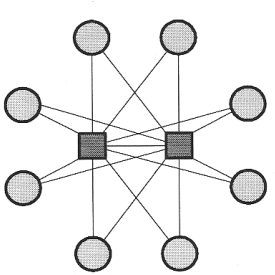
Advantages

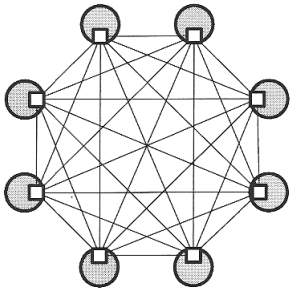
- No issue with skew
- Negligible crosstalk
- Higher speeds

Crates and backplanes evolution



Standard	Bandwidth in Mbytes/s
ATCA 40Gb	1 820 000
ATCA 10Gb	455 000
VPX (VITA46)	112 500
VXS (VITA 41)	20 000
SHB Express	17 500
Compact PCIe/PSB	5 000
PCI 64 x 33 Mbits/s	533
VME 320	320
VME64x	160
PCI 32 x 32 Mbits/s	133
VME64	80
VME32	40
VME16	20

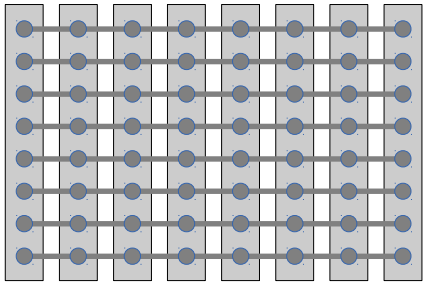




Serial differential star/mesh topologies

Technology break

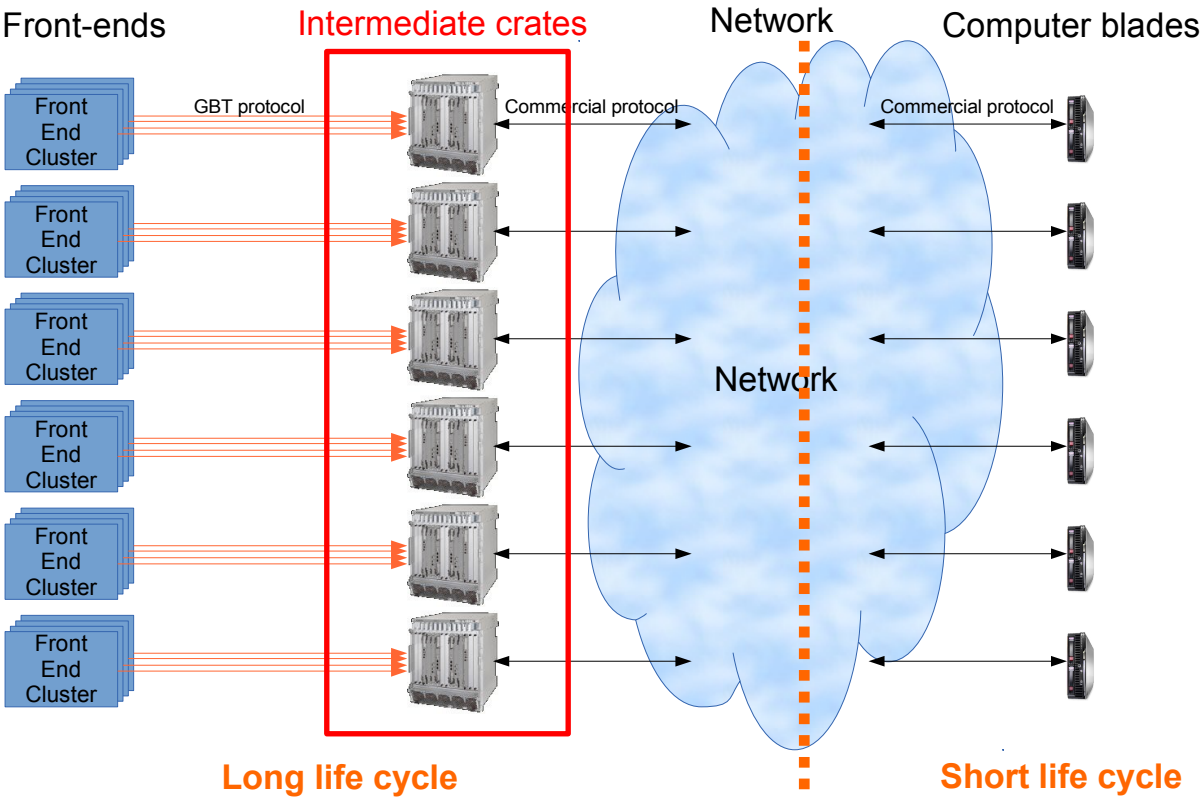
Parallel multidrop busses



Foreseen DAQ or Trigger scheme

Similar to current scheme

- Intermediate crates for Back-End side
- Allows easy change of farm PCs
- Good decoupling between two worlds



More powerful crate required for HL needs: which one ?

Few replacement standards

xTCA (ATCA, µTCA)

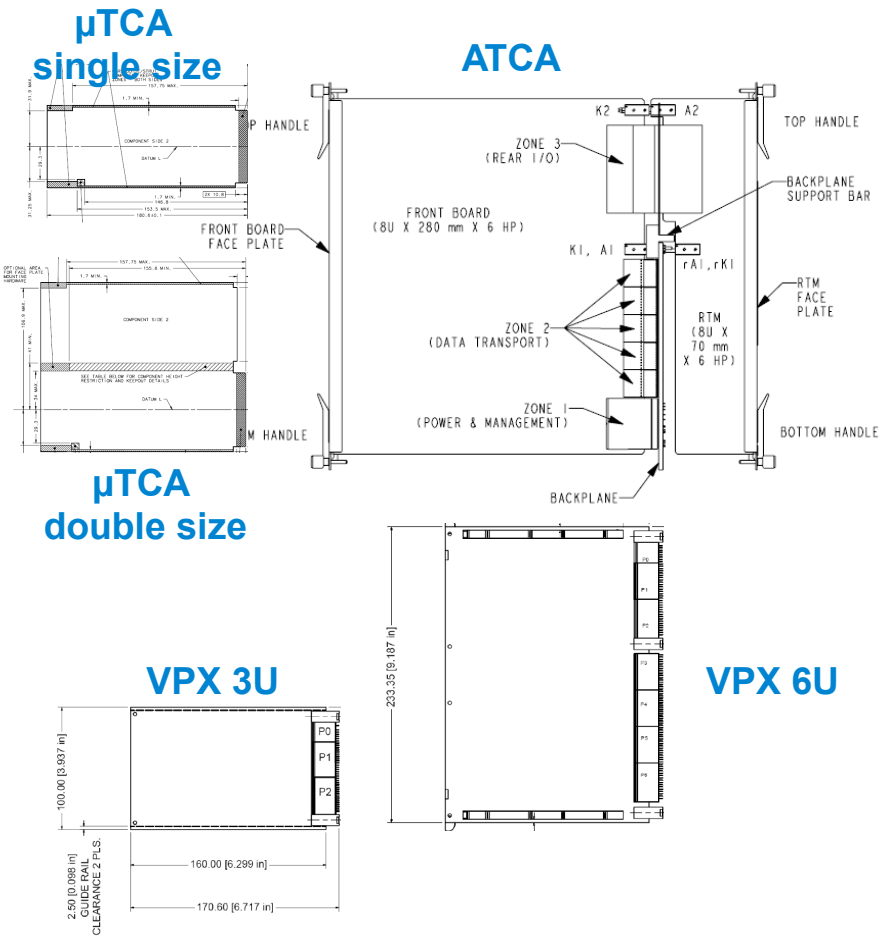
- « Totally new » standard (appeared in 2001 yet …)
- Many form factors, standard connectivity (dual star or full-mesh), ptotocole agnostic
- Standard mezzanines (AMC), RTM

VXS and VPX natural successors of VME

- Appeared in 2006
- Catch-up of xTCA :
  - Integrate some interesting features of xTCA

SHB Express:

- PCIe busses on a backplane
- Very small form factor

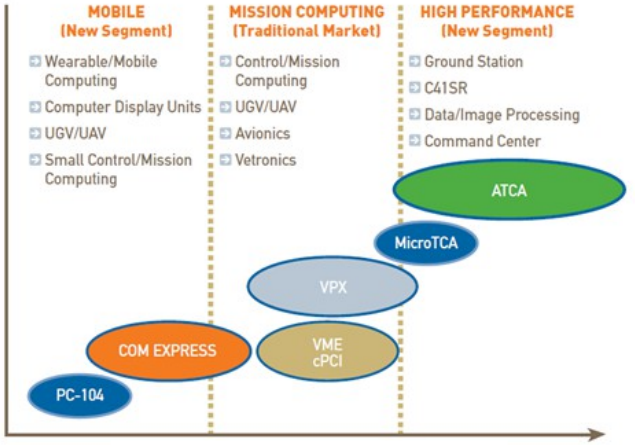


XTCA, VPX and SHB Express boards relative sizes

Reasons to choose xTCA

Reusability of existing VME designs

- None for SHB express and xTCA but ...
- Weak with VXS : new backplane needed, existing boards have no serial connections with new ones
- Extremely weak with VPX : different connectors, requires design of a hybrid backplane
- Both VXS and VPX : Need to redimension power supplies and cooling system
  - Marginal reuse



Performance comparison
(source Radisys)

Performance

- Better bandwidth for xTCA
- Better allowance for power consumption for ATCA

Standard	Power consumption per slot
VPX 3U	75W
VPX 6U	150 W
µTCA	50 to 80 W
ATCA 10G	200W
ATCA 40G	400W

Maximum power consumption

Other reasons

Cost

- VPX mainly driven by the military domain
  - Expensive solutions

Physics profiles

- xTCA for Physics committee created in 2010
  - Focus on precise time distribution and low noise analog interfaces

Many developments for High Energy Physics

- ATCA: ITER, LHCb, ATLAS, ILC, JET …
- µTCA: CMS, XFEL, LCLS

- VXS: LLC injectors
- VPX, SHB: none identified

Compact µTCA crate

Flexibility

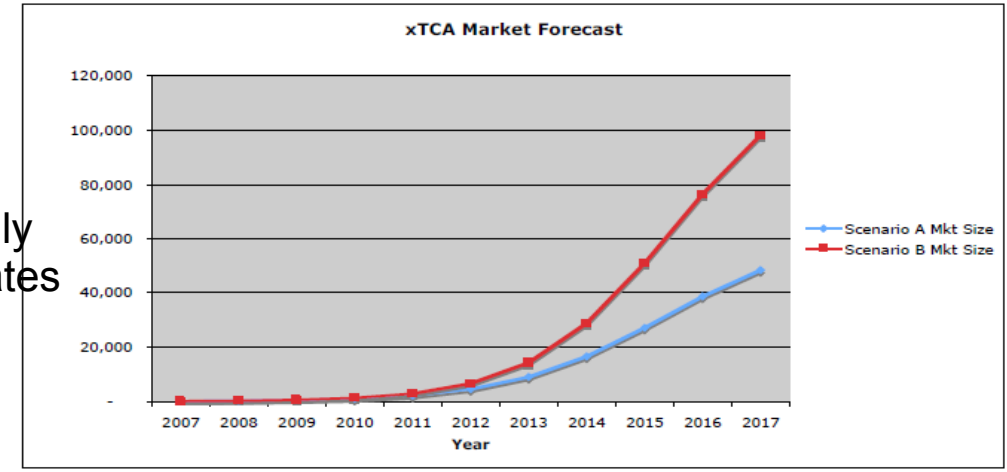
ATCA crate

Risks

What if xTCA does not become a long term standard ?

- Risks limited for systems where all hardware is **home designed**
  - The case of many « VME-like » systems today
  - Few dependance on third party electronics

- Large installed basis for **third party based ones**
  - Already exists since 12 years
  - Very well implanted in telecom, medical imagery, avionics and military domains
  - Industrials already support specially designed « xTCA for physics » crates



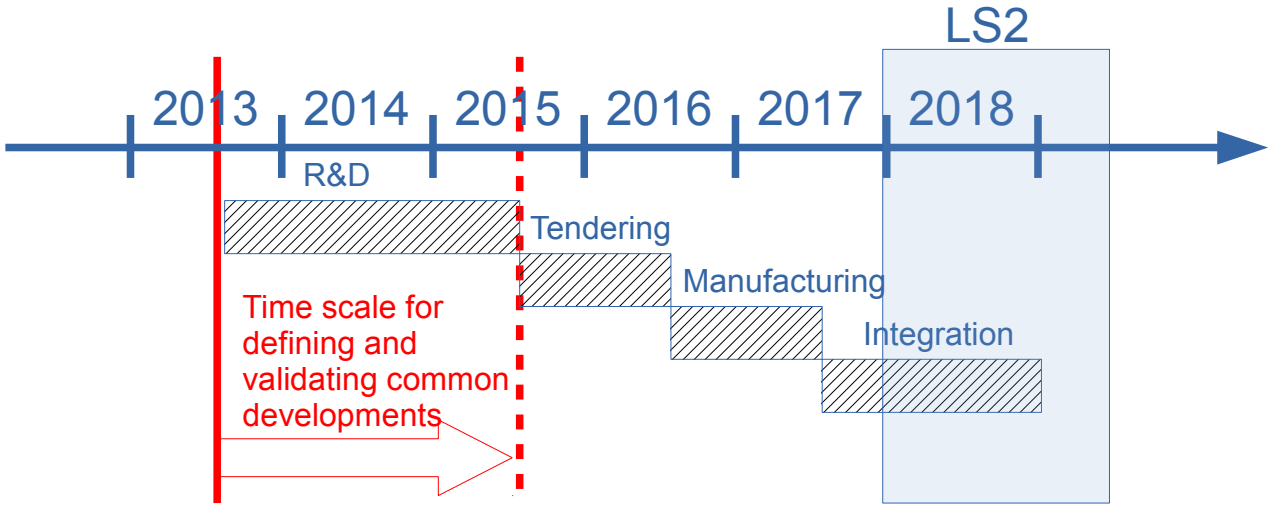
XTCA market forecast in M$
Source Signallake

Validation route and schedule

HL planned in 2022, but …

… LHCb and some subdetectors from ATLAS, CMS or ALICE plan to replace back-end electronics during LS2 in 2018

- ***Missing the LS2 window could lead to divergence of developments***



- ***Time scale is short !***
  - Approximately two years available for defining and validating a first common approach
  - Can rely on experience of early users

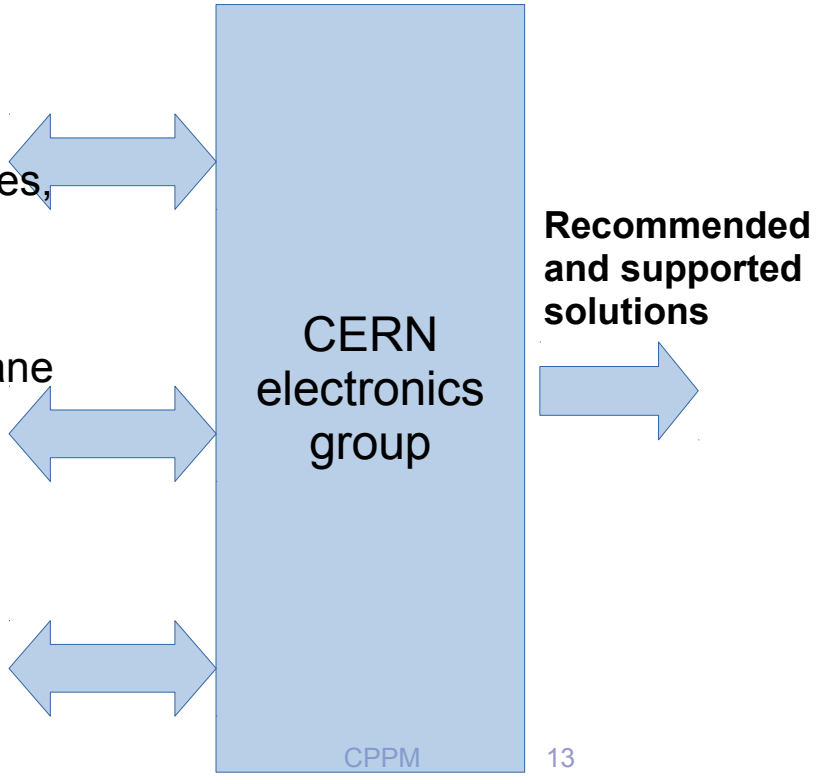
Possible roadmap:
Define common crate(s) and developments

xTCA has a steep learning curve

Counterpart of an exhaustively defined standard : mechanics, topologies, supervision, communication profiles, signal integrity

- 24 documents, several hundreds of pages each

- ***Sharing common developments is a key point to accelerate fast adoption and decrease costs***
  - First attempt made by ATLAS and LHCb:
    - Common ATCA crate and cooling,
    - Common IPMI scheme and ancillary modules,
  - Common crate definition made by CMS
    - Common µTCA crate with standard backplane
    - Customized µTCA backplane for trigger applications
    - Common supervision software
  - CERN xTCA evaluation project
    - Test interoperability issues



Possible roadmap:
Defining physics profiles

Current standard does not include specific features required by physics applications

- Ex:
  Precise time distribution
  Analog and digital electronics in a same crate

- ***xTCA for Physics PICMG sub-committee created in 2010 focussed on such topics***

- ***xTCA Interest Group created at CERN in 2011 where designers can share problems and solutions***
  - Already helped a lot sharing developments
  - But could be more pro-active in defining «LHC profiles »:

    Ex:
    - Define *specific purpose data paths* in ATCA mesh backplane interconnections (Clocks, data results, synchronizations, etc …)
    - Reduce the number of mechanical form factors
    - Reduce the number of communication standards between boards
    - Impose minimum set of signals to manage

Add new specific functionalities

Limit number of functionalities (interoperability)

Required skills and equipments

Several man years required to develop xTCA compliant solutions

Signal integrity issues

Routing signals at 10 Gbits/s on a backplane far from easy

- ***Needs electromagnetic simulation softwares (2D/3D), trained people and quite expensive measurement equipments***
  - Serial data analyzers,
  - Time domain reflectometers

Complex communication standards between boards or systems

PCIe, RapidIO, Gbit Ethernet, XAUI, Infiniband, Fibre channel, 10GBASE-KX4, 10GBASE-KR, …

- ***Buy IPs (Intellectual Properties: Reusable logic blocks)***

  Should be collectively bought: expensive licence fees
  - Not exactly plug and play
  - Several thousands of pages of documentation each
- ***Manpower to develop and maintain reference designs on how to use these IPs***

Conclusion

xTCA and its sub-standards: credible candidate as successor of VME

Tight roadmap to define and test common platforms, solutions and equipments

But raising the competence of developers community will take time
→ manpower and tools needed right now to develop common solutions and support them

Many coordinating actions already started, but lots to be done

xTCA IG could play a major role

Spare slides

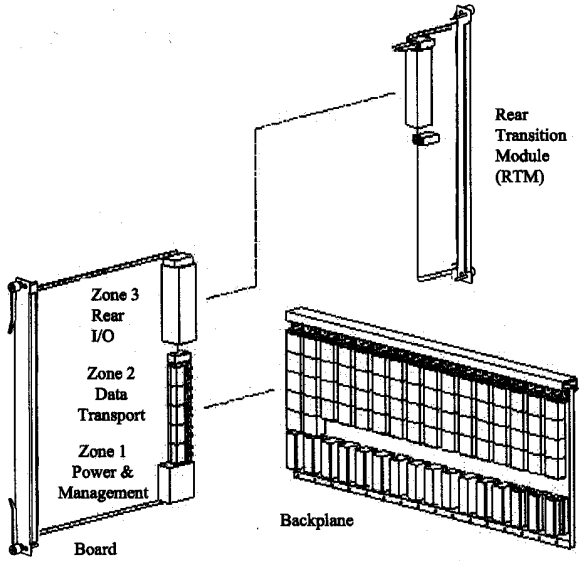
xTCA

- ***ATCA***
  - 2 type of cards : hub and node
  - Single form factor : 8U x 280 x 30.48 mm
  - Standard topologies : dual star, dual-dual star, full-mesh
- ***AMC***
  - Standardized mezzanine for ATCA boards
  - 6 form factors : compact, mid and full size, single and double width
- ***µTCA***
  - Uses **AMC boards in a backplane** for small or medium system
  - 6 form factors
  - Dual star topology
- ***Health monitoring system:***
  - IPMI from Intel

XTCA standards

Item ID.	Title
AMC.0 R2.0	*Advanced Mezzanine Card Base Specification*
AMC.1 R2.0	*PCIExpress™ on AdvancedMC™*
AMC.2 R1.0	*Ethernet Advanced Mezzanine Card Specification*
AMC.3 R1.0	*Advanced Mezzanine Card Specification for Storage*
AMC.4 R1.0	*Serial RapidIO on AdvancedMC™ Specification*
IRTM.0 R1.1	*AdvancedTCA® Intelligent Rear Transition Module Base Specification*
PICMG 3.0 R3.0	*AdvancedTCA® Base Specification*
PICMG 3.1 R2.0	*Ethernet/Fibre Channel for AdvancedTCA® Systems*
PICMG 3.2 R1.0	*InfiniBand™ for AdvancedTCA® Systems*
PICMG 3.3 R1.0	*StarFabric/Advanced Switching for AdvancedTCA® Systems*
PICMG 3.4 R1.0	*PCIExpress™/Advanced Switching for AdvancedTCA® Systems*
PICMG 3.5 R1.0	*Serial RapidIO™ for AdvancedTCA® Systems*
PICMG 3.7	*AdvancedTCA Extension*
PICMG 3.8 R1.0	*AdvancedTCA Rear Transition Module Zone 3A Specification*
PICMG COM.0 R2.1	*Com Express® Module Base Specification*
CDG	*COM Express Carrier Design guide*
PICMG HPM.1 R1.0	*Hardware Platform Management IPM Controller Firmware Upgrade Specification*
PICMG HPM.2 R1.0	*LAN-Attached IPM Controller Specification*
PICMG HPM.3 R1.0	*DHCP – Assigned Platform Management Parameters Specification*
PICMG MicroTCA.0 R1.0	*Micro Telecommunications Computing Architecture Base Specification*
PICMG MicroTCA.1 R1.0	*Air Cooled Rugged MicroTCA® Specification*
PICMG MicroTCA.2 R1.0	*Hybrid Air/Conduction Cooled MicroTCA® Specification*
PICMG MicroTCA.3 R1.0	*Hardened Conduction Cooled MicroTCA® Specification*
PICMG MicroTCA.4 R1.0	*MicroTCA Enhancements for Rear I/O and Precision Timing Specification*
phyTCA	*xTCA for Physics*
Total	*24 documents*

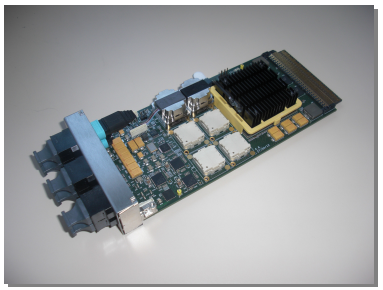
ATCA and µTCA objects



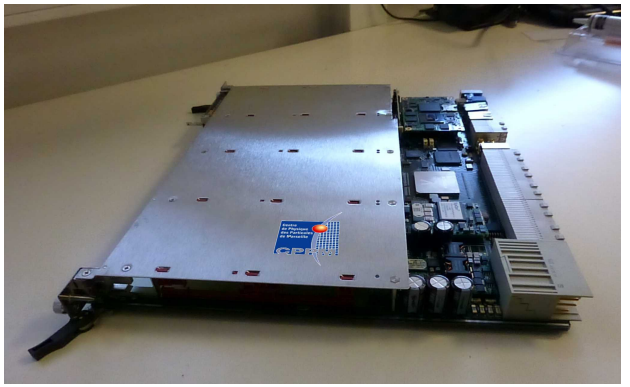
Compact µTCA crate

Scalability

ATCA crate



AMC board

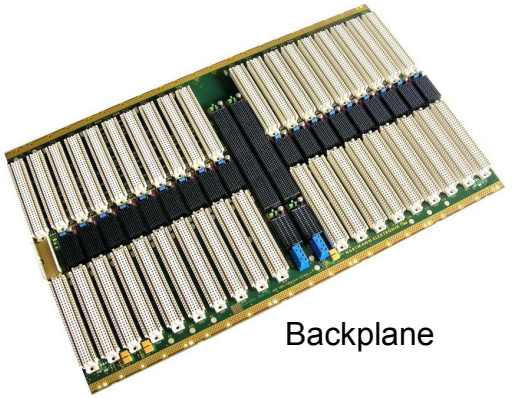


ATCA board with 4 AMC mezzanines

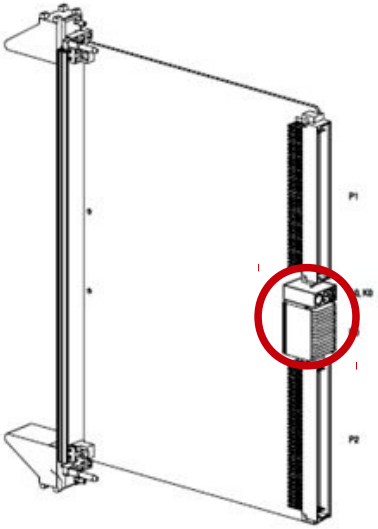
VXS

	Basic module
VITA 41.0	VXS Base Standard - ANSI ratified
VITA 41.1	InfiniBand Protocol on VXS
VITA 41.2	Serial RapidIO Protocol on VXS
VITA 41.3	VXS Ethernet 1000 Mbit/s Baseband IEEE 802.3 Protocol Layer Standard
VITA 41.4	VXS 4X PCI Express® Protocol Layer Standard
VITA 41.10	Live Insertion System Requirements for VITA 41 Boards
VITA 41.11	VXS Rear Transition Module Standard

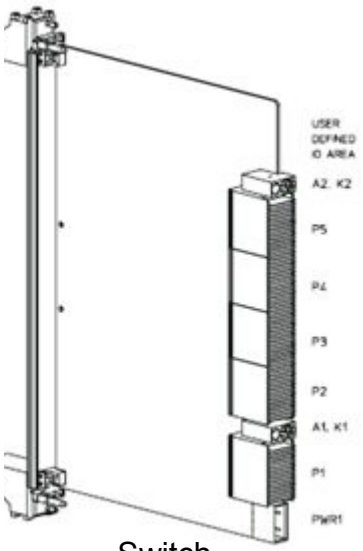
- 2 type of cards : payload and switch
- Single form factor : 6U x 160 x 20.32 mm
- Payload boards connected to switch board in a dual star topology
- Same connectors as VME for payload boards:
  - Addition of a new connector for serial transfers



Backplane



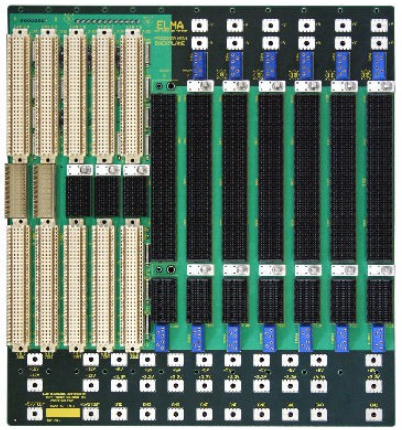
Payload



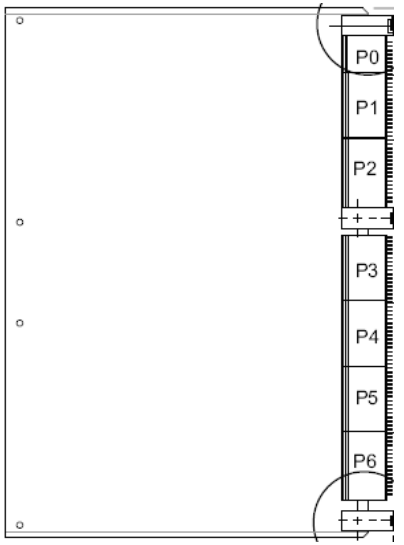
Switch

VPX

- Single type of board configurable as payload or switch
- 2 form factors : 2U x 160 x 20.32 mm and 6U x 160 x 20.32 mm
- Completely new connector type
  - No compatibility with existing hardware except with hybrid backplane
- 14 standard backplane topologies



VPX backplane



VPX board

VPX standards

Standard Name	Description
ANSI/VITA 46.0-2007	VPX Base electrical and mechanical specification
ANSI/VITA 48.0-2010	VPX REDI Cooling specifications.
ANSI/VITA 65.0-2010	OPEN VPX. Organizes the versatile VPX system into a series of industry compatible backplane, module, and chassis profiles.

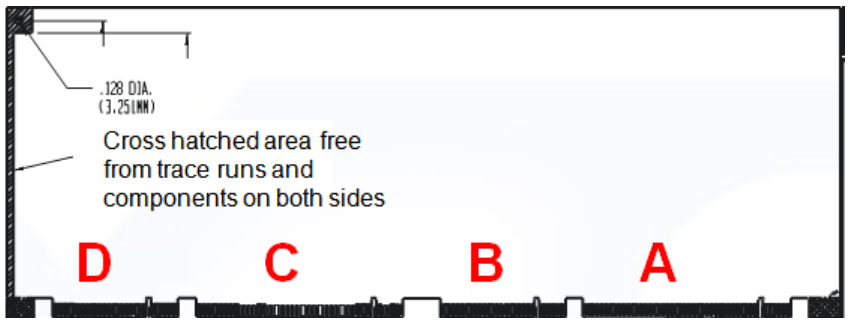
Dot Standard	Status[1]	Description
46.1	Approved	VMEBus Signals (Hybrid) on VPX Fabric Connector
46.3	Trial Draft[2]	Serial RapidI/O™ on VPX Fabric Connector
46.4	Trial Draft[2]	PCI Express on VPX Fabric Connector
46.6	Trial Draft[2]	Gigabit Ethernet External Control Plane on VPX
46.7	Trial Draft[2]	Ethernet on VPX Fabric Connector
46.9	Draft	PMC/XMC Rear I/O Backplane Routing
46.10	Approved	Rear Transition Modules
46.11	Draft	System Management Signals

Cooling Method	Pitch	Description
Air	0.80"	Standard VITA 46 compliant board. Supports Front I/O. Fits in all VPX chassis.
Conduction Cooled	0.85"	Top Conduction Cooling plate added to VITA 46. Only supports Rear I/O. Fits in most chassis.
Conduction Cooled-REDI	1.00"	REDI Conduction Cooled with level 2 maintenance support. This type of module has cover plates on both sides with no exposed components for ESD protection. Rear I/O only. Fits only in VITA 48.2 compliant chassis.

VPX topologies (VITA65)

SHB Express (PICMG1.3)

- System Host Board for PCI Express
- Two form factors 13.33 x 4.98 mm and 6.6 x 4.98 mm
- System consists of one SHB Express board and several PCIe, PCI-X or PCI cards :
  - Connectors A and B provide 20 PCI Express lanes, which can be configured as x16, x8, x4 or x1 links.
  - Connector C provides additional interfaces for 2 serial ATA/150 interfaces, 2 Gigabit Ethernet interfaces, up to 4 USB 2.0 interfaces and connections to IPMI sensors
  - Connector D provides PCI or PCI-X (32-bit/66 MHz) connections
- No standard backplane : user defined
  - Active backplane : can contain a PCIe switch or bridge
- No standard mechanics



SHB Express (PICMG1.3)

- Example of backplanes